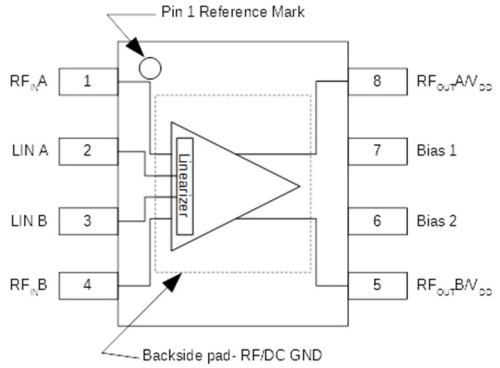
TAT7467E1F

CATV 75 Ω pHEMT Dual RF Amplifier

Product Description

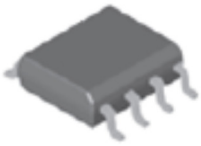
The TAT7467E1F is a 75 Ω, fully integrated, single-die differential RF Amplifier covering medium power applications in the CATV band. The TAT7467E1F includes on-chip linearization to improve 3rd order distortion performance while maintaining low power consumption on a +5 V supply. It is fabricated using 6 inch GaAs pHEMT technology to optimize performance and cost.

Functional Block Diagram



Pin Configuration

Pin No.	Label
1	RF_{IN} A
2	LIN A
3	LIN B
4	RF_{IN} B
5	$RF_{OUT}B$ / V_{DD}
6	Bias 2
7	Bias 1
8	$RF_{OUT}A$ / V_{DD}
Backside Pad	RF/DC GND



SOIC-8 Package

Product Features

- 50–1218 MHz Bandwidth
- 75 Ω Impedance
- pHEMT Device Technology
- Meets DOCSIS 3.1 Output Requirements
- +5 V Supply Voltage
- 380 mA Current Consumption
- On-chip Linearization
- SOIC-8 package

Applications

- Replacement for +5 V SOIC-8 Amplifiers
- Edge QAM Output Stage
- MDU Output
- Distribution Amplifiers
- Transmitter Driver Amplifier

Ordering Information

Part No.	Description
TAT7467E1F	75 Ω Dual pHEMT Amplifier
TAT7467E1F–EB	Amplifier Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	+10 V
Storage Temperature	–60 to +150 °C
Operating Temperature	–40 to +85 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD}		+5.0		V
I_{DD} (Total EVB current)		380		mA
Tj for >10^6 hours MTTF			+145	°C

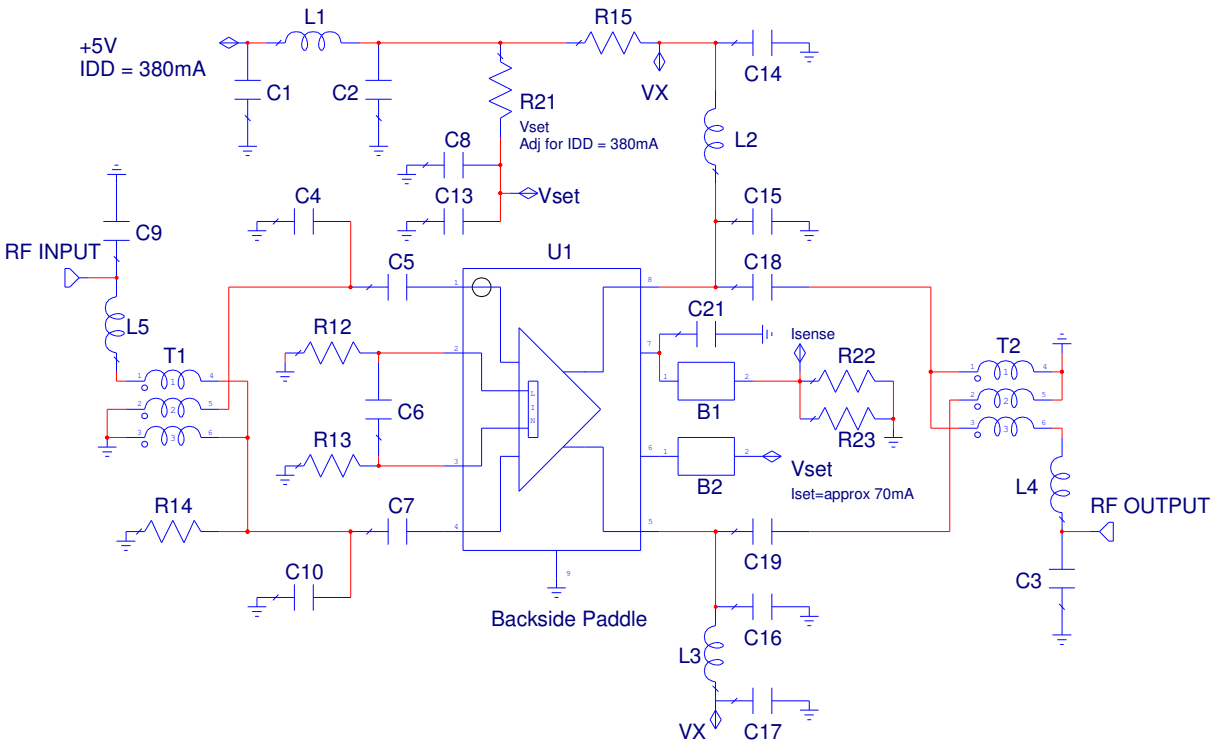
Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		1218	MHz
Gain			18		dB
Gain Flatness	Peak deviation from straight line across full band.		±0.75		dB
Noise Figure			4.7		dB
Input Return Loss			15		dB
Output Return Loss			16		dB
EQAM Output Out-of-band Spurious and Noise for single channel on a single port	V_{OUT} = 62 dBmV / ch adjacent, See Notes 2, 3, and 4			–62	dBc
P1dB			+25		dBm
OIP3	P_{OUT}=+12 dBm / tone, Δf=10 MHz		+43		dBm
Equivalent Harmonics	See Note 5			-63	dBc
V_{DD}			+5		V
I_{DD} (Total current of Test Circuit)	See Note 7		380		mA
Bias 2 (Vset range to adjust I_{DD})		4		5	V
Thermal Resistance θ_{jc} (jct. to case)			14.5		°C/W

Notes:
1. Test conditions unless otherwise noted: 75 Ω impedance, V_{DD} = +5 V, I_{DD} = 380 mA fixed by Vset [7] from +4 V to +4.7 V, T_A = +25 °C
2. Production tested at 66 MHz, 330 MHz, and 990 MHz.
3. Adjacent channel 1 (750 kHz from channel block edge to 6 MHz from channel block edge).
4. Adjacent channel 2 (6 MHz from channel block edge to 12 MHz from channel block edge).
5. Spurious and noise levels in channels coinciding with 2nd harmonic or 3rd harmonic.
6. Recommended application circuit uses active bias described on page 6.
7. Test Circuit, page 3, can be used for evaluation with some variation in I_{DD} when Vset is a fixed voltage between +4 to +4.7 V adjusted by R21. Variation to I_{DD} may change some performance parameters.

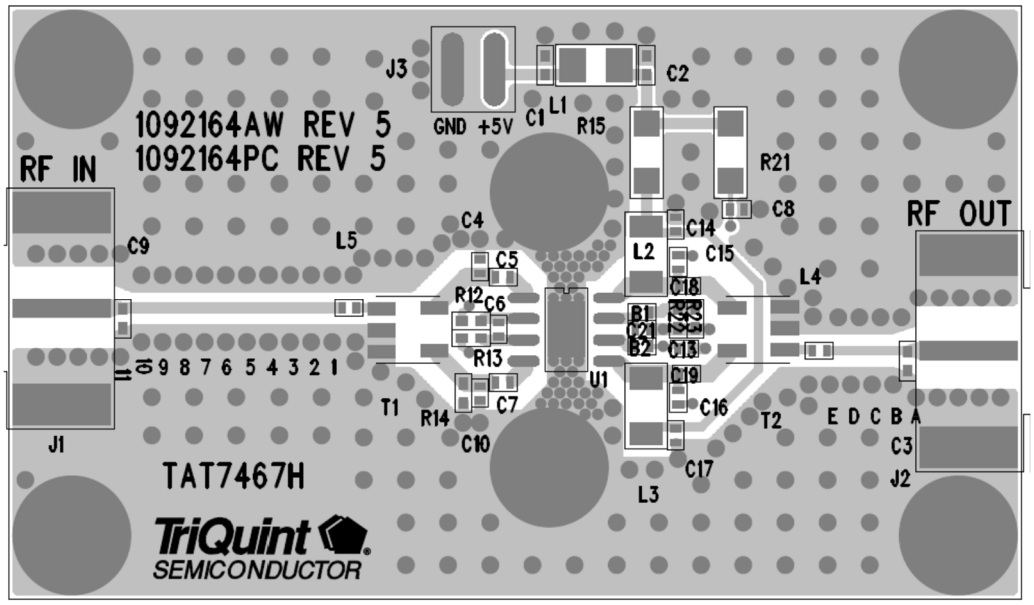
TAT7467E1F–EB Evaluation Board (Test Circuit)



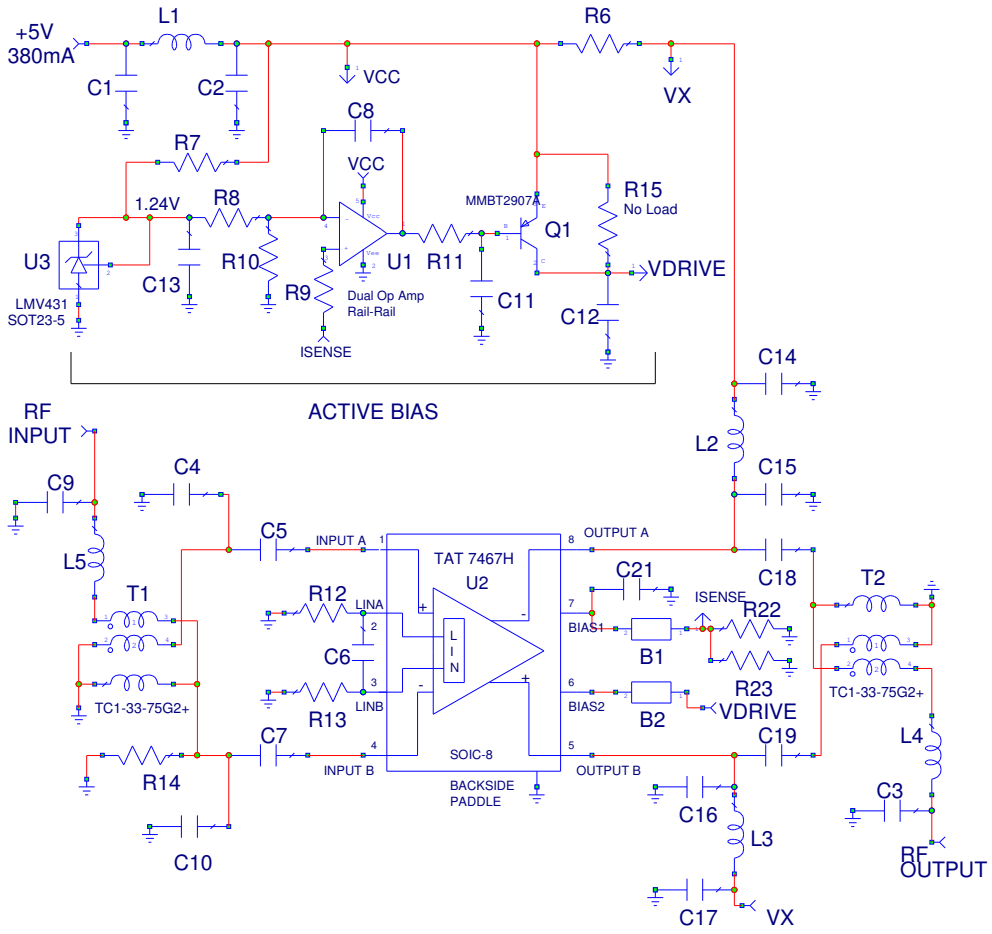
Bill of Material–TAT7467E1F

Reference Designator	Description	Manufacturer	Part Number
PAD	Sil Pad for Heatsink	various	
BLOCK	HEATSINK		
U1	TAT7467E1F	Qorvo	
PCB	TAT7467E1F Application Board		
C1, C2	CAP, 0402, 0.1uF, 10%, 10V	Panasonic Corp of North America	ECJ-0EB1A104K
C18, C19	CAP, 0402, 270 pF, 10%, 50V	Panasonic Corp of North America	ECJ-0EB1H271K
C5, C6, C7, C13, C14, C17	CAP, 0402, 0.01uF, 10%, 16V, XR7	Panasonic Corp of North America	ECJ-0EB1C103K
C3, C4, C10, C15, C16	CAP, 0402, 0.5pF +/-0.25pF, 50V	Murata	GRM1555C1HR50CZ01D
R12, R13	RES, 0402, 1.21K Ω, 1%, 1/16W	Panasonic Corp of North America	ERJ-2RKF1211X
R22, R23	RES, 0402, 1.5 Ω, 1%, 1/16W	Yaego	RC0402FR-071R5L
R14	RES, 0402, 750 Ω, 1%, 1/16W	VISHAY-DALE	CRCW0402750RFKED
R15	RES, 1206, 1 Ω, 5%	Panasonic Corp of North America	ERJ-8GEYJ1R0V
R21	RES, 1206, 12 Ω, 5%, 1/4W	Panasonic Corp of North America	ERJ-8GEYJ120V
L4	IND, 0402, 5.6nH, 5%, W/W	Coilcraft, Inc.	0402CS-5N6XJLW
L5	IND, 0402, 2.7nH, 5%, W/W	Coilcraft, Inc.	0402CS-2N7XJLW
L1	IND, 1008, 0.9uH, 10%, 1.3A, Ferrite	Coilcraft, Inc.	1008AF-901XKL
L2, L3	IND, 1206, 500nH, 10%, 260mA, Ferrite	Murata	LQH31HNR50K03
B1, B2	Bead, Chip Ferrite, 0402, 600 Ω, 300mA	Murata	BLM15AG601SN1D
T1, T2	XFMR, SMT, 75 Ω, CD542, 1:1	Mini-Circuits	TC1-33-75G2+
J3	Header Pin, 2 POS, 0.1”, RA, SMT	Molex	022-28-8021
J1, J2	Conn, 75 Ω, Edge Launch F	Lighthorse Technologies	LTI-FSF55MGT-P-10A-X7
S1, S2, S3, S4, S5, S6	Screw, 4-40, ¼”, Phillips, Pan HD, SEMS	McMaster-Carr Supply Company	90403A106
C8, C9, C21	Not Populated Item		Dummy Part

TAT7467E1F–EB Evaluation Board



Application Circuit with Active Bias

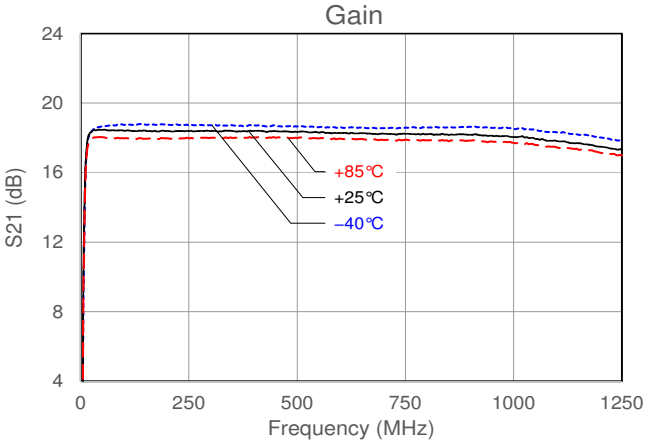


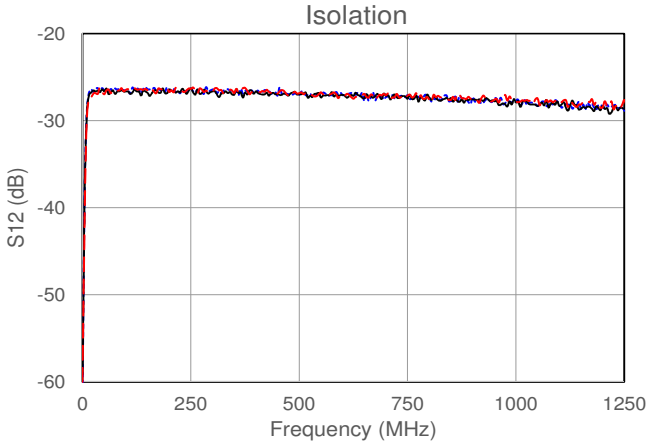
Notes:
1. EVB Nominal I_{DD} current is 380 mA

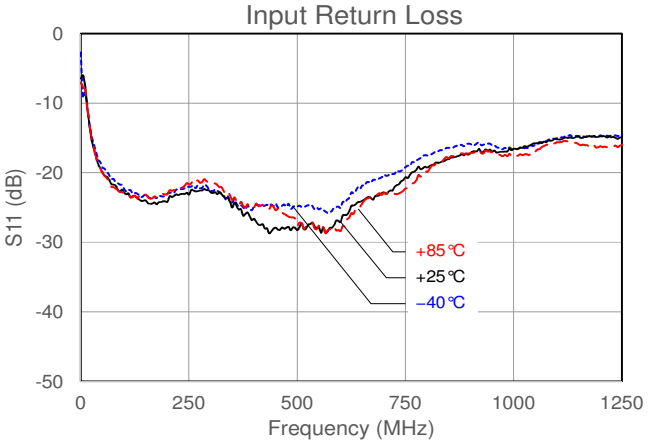
Bill of Material: Active Bias Section

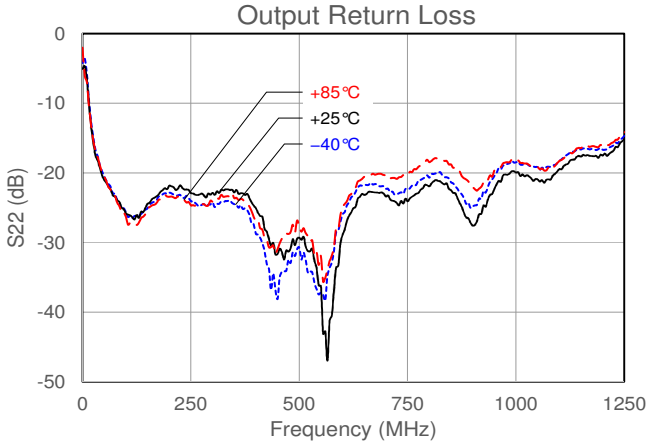
Reference Designator	Description	Manufacturer	Part Number
U1	Rail-Rail Op-Amp	On Semi	LM7301
U3	Adjustable shunt voltage regulator	TI	LM431
Q1	General purpose transistor (pnp)	Various	
C1, C2, C8	CAP, 0402, 0.1uF, 16V, 10%	Various	
C11, C12, C13, C14, C15	CAP, 0402, 10.01uF, 6V, 10%	Various	
R6	RES, thick film, 1206, 1 Ω, 5%	Various	
R7, R8, R9	RES, thick film, 0402, 10.0k Ω, 1/16 W, 1%	Various	
R10	RES, thick film, 0402, 5.6k Ω, 1/16 W, 1%	Various	
R11	RES, thick film, 0402, 100 Ω, 5%	Various	
R15	No Load		
L1	IND, High Current, 1008, 0.9uH, 10%	Coilcraft	1008AF-901XKL

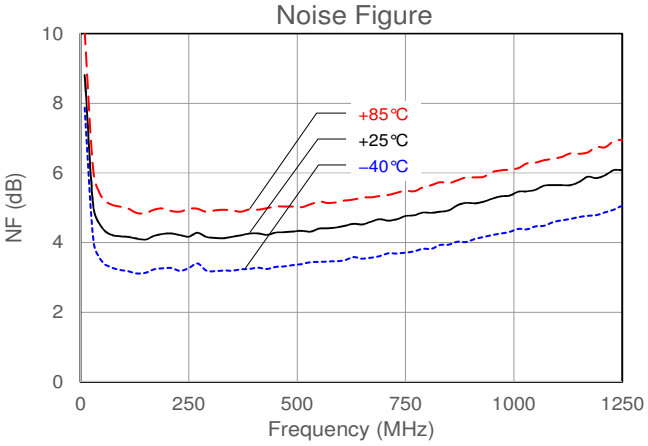
Performance Plots

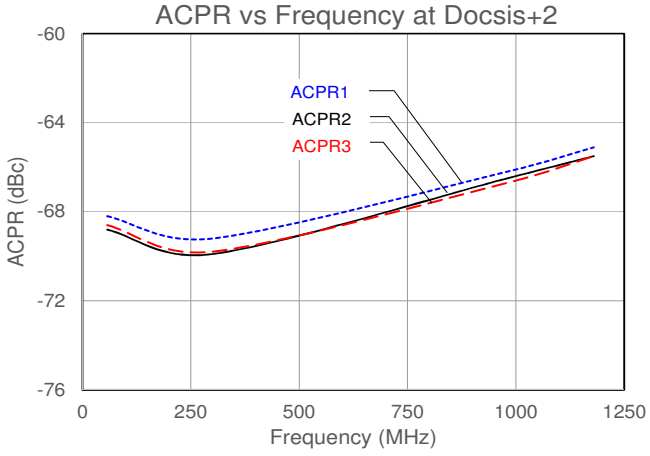








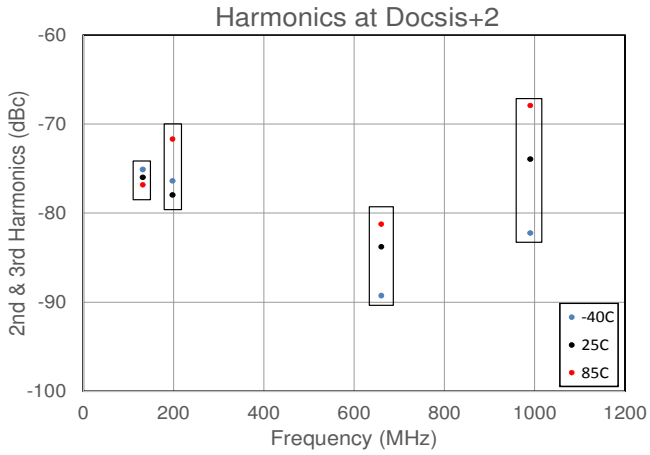


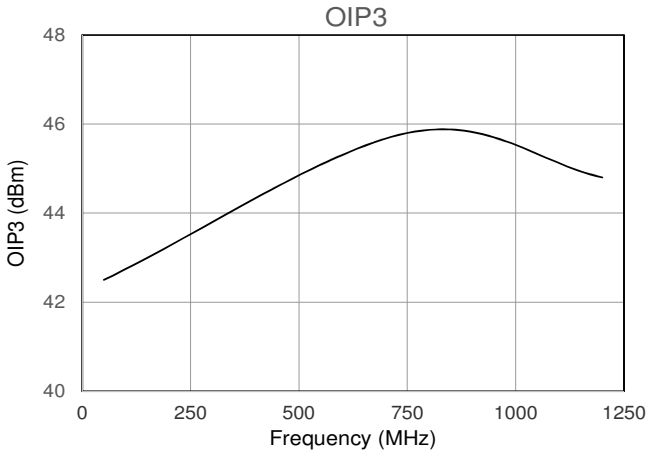


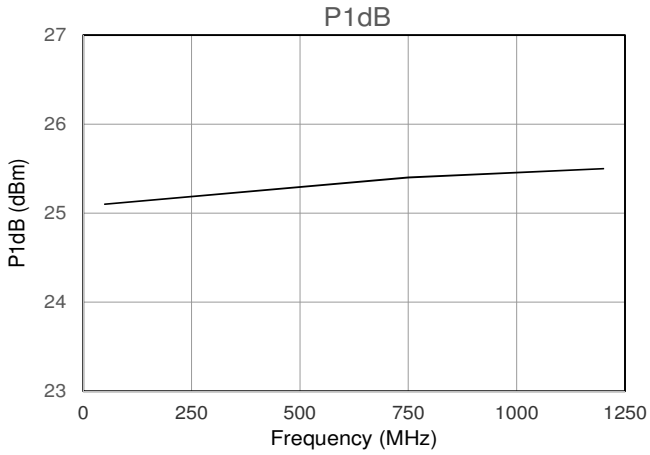
Notes:

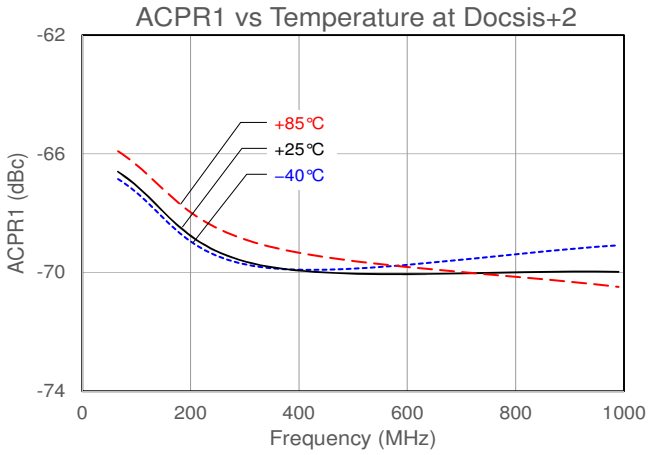
1. V_{DD} = +5 V, I_{DD}= 380 mA, T_A= +25°C

Typical Performance Plots (cont.)





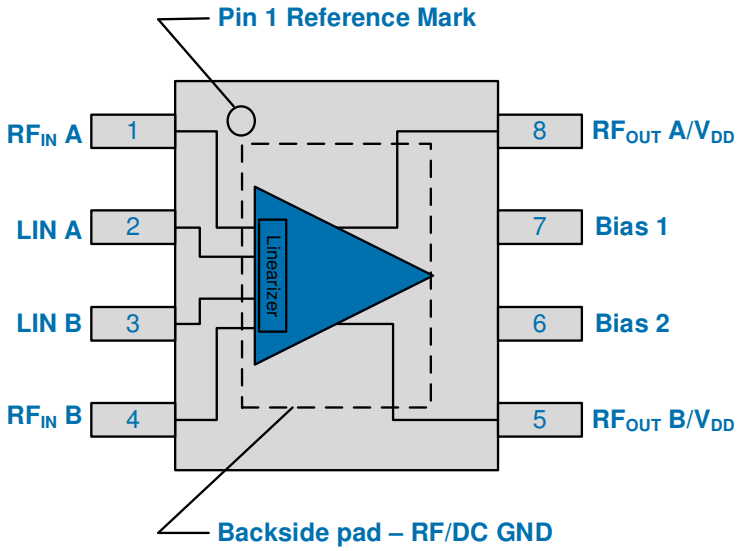




Notes:

1. V_{DD} = +5 V, I_{DD}= 380 mA, T_A= +25° C

Pin Configuration and Description



Pin No.	Label	Description
1	$RF_{IN}A$	RF Input A. DC blocking capacitor required.
2	LIN A	Linearizer A. Recommend using 1.21K resistors to ground for optimal on-chip linearizer current setting.
3	LIN B	Linearizer B. Recommend using 1.21K resistors to ground for optimal on-chip linearizer current setting.
4	$RF_{IN}B$	RF Input B. DC blocking capacitor required.
5	$RF_{OUT}B$ / V_{DD}	RF Output B. DC blocking capacitor required.
6	Bias 2	I_{DD} adjust. Set for 380mA, approx. Pin 6 draws approx. 70mA
7	Bias 1	Output stage common source node. Current sense line for active bias.
8	$RF_{OUT}A$ / V_{DD}	RF Output A. DC blocking capacitor required.
Backside Pad	RF/DC GND	Ground Slug

Detailed Device Description

The TAT7467E1F is a flexible +5 V differential amplifier for medium power CATV applications. The amplifier of the TAT7467E1F was specifically designed to work with on-chip linearization to provide 3rd order distortion improvement over a wide range of RF power levels and across the full CATV bandwidth. Operation of the linearizer will not affect overall gain by more than 0.7 dB.

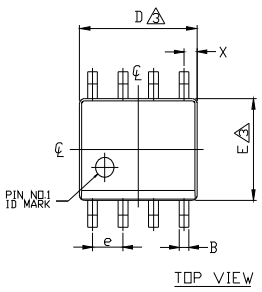
For any amplifier bias current, output 3rd order distortion may be improved by adjusting a small bias current of the on-chip linearization circuit. The Application Schematic shows resistors setting the linearizer currents. Alternate linearizer drive circuitry is possible; consult Qorvo for discussion.

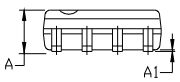
Bias current may be adjusted with changes to external components making the TAT7467E1F ideal for both input and output gain stages in an EdgeQAM amplifier line-up. For output stage applications, bias currents of between 300 mA to 400 mA are recommended. For input stage applications, bias currents of 230 mA to 280 mA are recommended. Active bias circuits, like the one shown on page 6 of this datasheet, may be used to achieve greater control over the bias current.

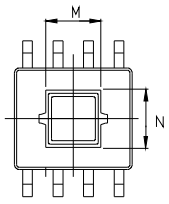
The TAT7467E1F is built using a single die, which significantly improves its resulting circuit balance and corresponding 2nd order distortion performance. For best 2nd order performance, an input balun using a 3rd wire construction may be used to improve the input phase balance going into the TAT7467E1F.

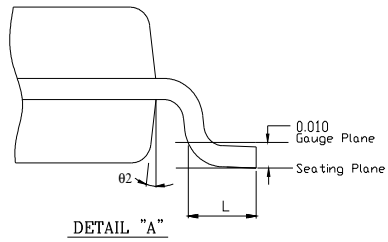
The TAT7467E1F is packaged in an industry standard SOIC-8 package with a large exposed paddle to enable good heat flow to a backside heatsink. At the maximum recommended bias current of 400 mA the power consumption will be 2 W. The TAT7467E1F is fabricated using a mature pHEMT process that has demonstrated outstanding reliability performance on other Qorvo products. Please use contact information section to consult Qorvo for further information.

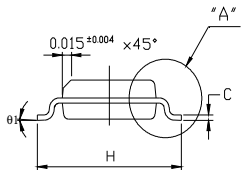
Package Marking and Dimensions







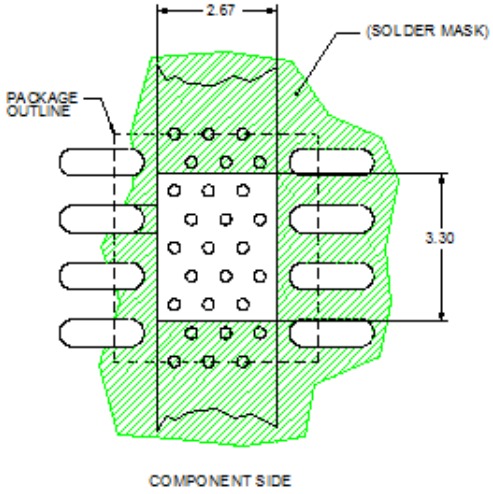


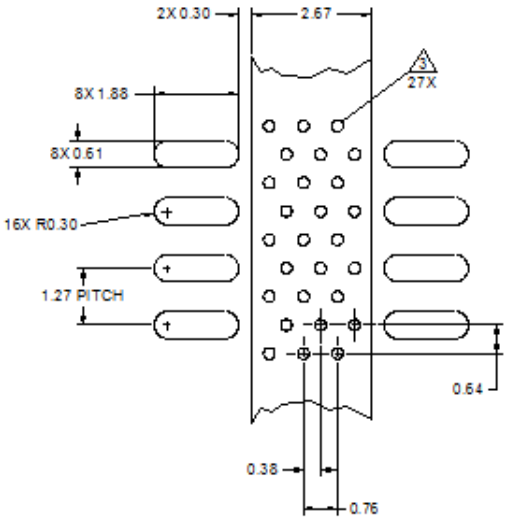


SYMBOL	8 SOIC	
	MIN	MAX
A	0.054	0.068
A1	0.001	0.004
B	0.014	0.019
D	0.189	0.197
E	0.150	0.157
H	0.228	0.244
M	0.072	0.097
N	0.067	0.092
e	0.050 BSC	
C	0.0070	0.0010
L	0.016	0.050
X	0.0215 REF	
θ1	0°	8°
θ2	7° BSC	

NOTE :
1. All dimension are in inch
2. Top package surface to be NiPdAu plating
3. Bottom package surface to be NiPdAu plating
4. Dimension are exclusive of mold flash and gate burr
5. Foot length measurement is based on the gauge plane method

PCB Mounting Pattern





Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.010").
5. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA /JEDEC JS-001-2012
ESD – Charged Device Model (HBM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.

Contact plating: Ni, Pd, & Au

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: 1-844-890-8163

Web: www.qorvo.com

Email: customer.support@qorvo.com

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Revision History

Rev.	Date	ECN# (Hillsboro Only)	Description of Change	WEBMASTER POSTING INSTRUCTIONS TO PUBLIC WEBSITE		
				Email* Info Link Only	1st page only	Full Data Sheet
				Answer YES in one column only OR NO** all 3 columns		
A	12-11-14	90048	Original Documentation (A.Sardar)	No	No	Yes
B	02-02-15	90832	Added active bias circuit and associated BOM, added Pin Configuration section, updated functional block diagram. (A. Sardar, C. Blum)	No	No	Yes
C	02-23-15	91275	Declare test condition to I_{DD}=380mA for Electrical specs, limit Vset control range from 4 to 6V for Idd to a 4 to 4.7V (5V max) to be compatible with 5V active bias application circuit, referenced test circuit on page 3 to Electrical specs. Added test conditions to all performance plots, declared them as typical. Updated package marking & dimensions per OUT.308, added PCB mounting pattern (T. Cummings)	No	No	Yes
D	10-08-15	96531	Updated data sheet to dual branding. Update package dimensions and marking. Corrected pin description table. Pin 1 mislabeled. Added C21 to EVB BOM. Corrected Functional Block Diagram. Pin 1 mislabeled. Corrected typos.	No	No	Yes
E	06-05-17	17-16773	Updated to Qorvo format. Updated EVB BOM. (D.Fun)	No	No	Yes

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