Dual SilentMOS Smart Power Stage in 5mm × 8mm LQFN

FEATURES

- 70A Peak Output Current per Channel
- SilentMOS™ Smart Power Stage
  - Utilizes Low EMI/EMC Silent Switcher®2 Architecture
  - Ultra-low SW-Voltage Overshoot
  - Frequency Up to 2MHz
- V_{IN} Up to 14V
- Up to 94% Efficiency at 1MHz with 1.8V_{OUT}
- Integrated Boost Diodes and Capacitors
- Accurate Switch Current Monitoring
- Power MOSFET Overcurrent Protection
- Input Overvoltage and Bias Undervoltage Protection
- Thermal Monitor with Overtemperature Flag
- 3.3V/5V Compatible Tri-State PWM Input
- 5mm × 8mm LQFN Package

APPLICATIONS

- High Current Servers and Workstations
- Networking/Telecom Microprocessor Supplies
- Small Form-Factor POL Converter

DESCRIPTION

The LTC®7050 dual monolithic power stage fully integrates high speed drivers with low resistance half-bridge power switches plus comprehensive monitoring and protection circuitry in an electrically and thermally optimized package. With a suitable high frequency controller, this power stage forms a compact, high current voltage regulator system with state-of-the-art efficiency and transient response.

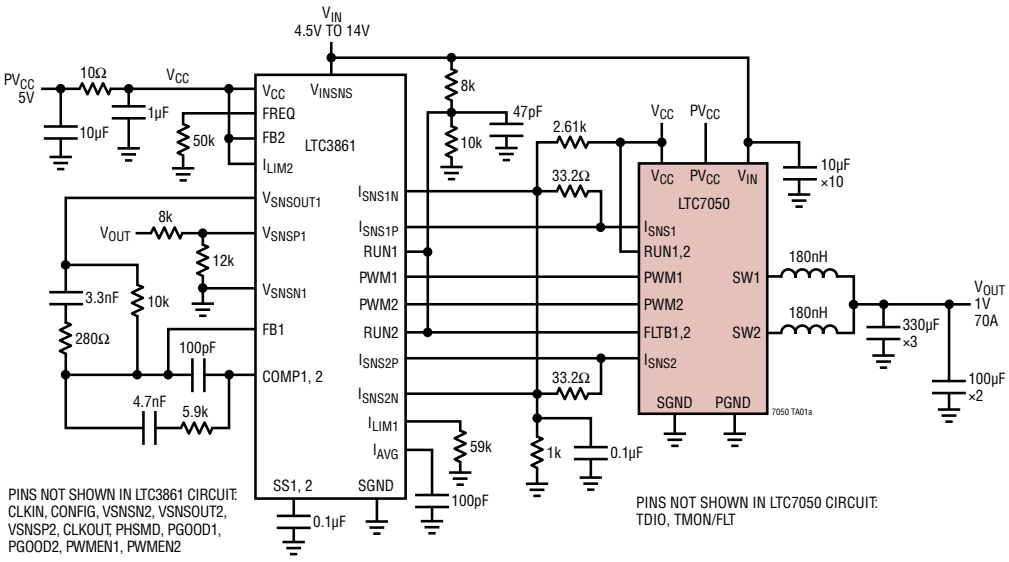
SilentMOS technology utilizes second generation Silent Switcher 2 architecture reducing both EMI and switch-node voltage overshoot while maximizing efficiency at high switching frequencies.

High speed current sensing provides low latency switch current information, enabling tight current balancing and immediate overcurrent protection.

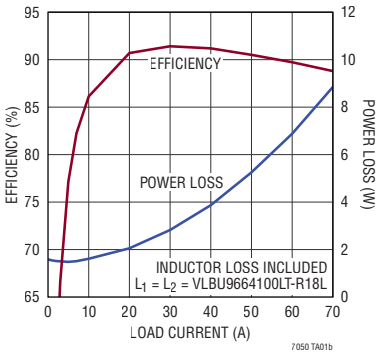
Thermally-enhanced packaging provides dual 40A rated continuous output current capability.

TYPICAL APPLICATION

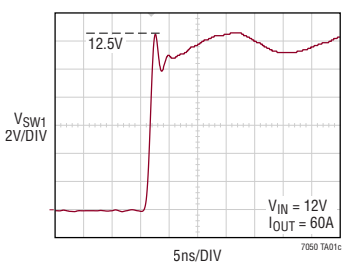
12V_{IN}, 1V/70A_{OUT} 1MHz Dual-Phase POL Converter



Efficiency vs I_{OUT} at 1MHz



V_{SW} Waveform at 1MHz



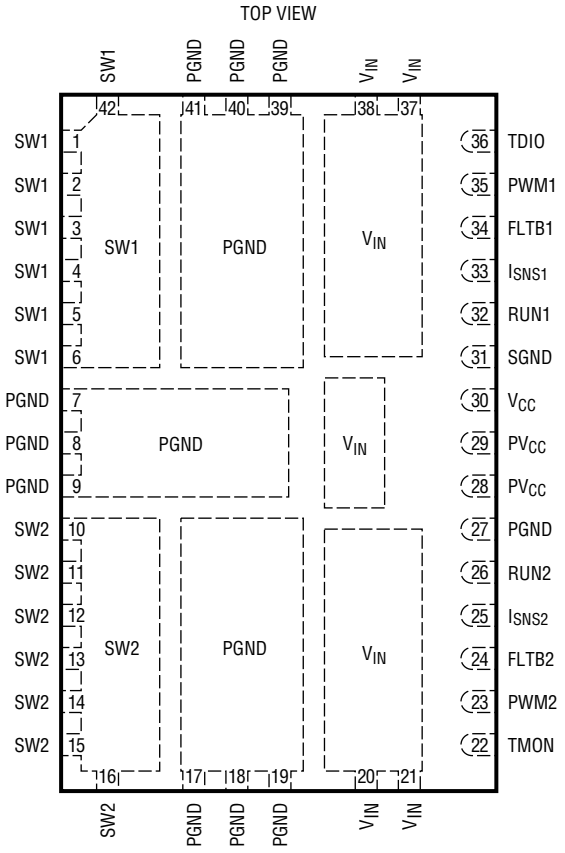
Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} DC Voltage ..... –0.3V to 16V
V_{IN} Transient Voltage ..... –0.3V to 20V
SW1, SW2 Voltage ..... –0.3V to 16V DC
SW1, SW2 Voltage (20ns) ..... –2V to 20V
PV_{CC}, V_{CC} Voltage ..... –0.3V to 6V
RUN1, RUN2 ..... –0.3V to (V_{CC} + 0.3V)
PWM1, PWM2 ..... –0.3V to (V_{CC} + 0.3V)
I_{SNS1}, I_{SNS2} ..... –0.3V to (V_{CC} + 0.3V)
FLTB1, FLTB2 ..... –0.3V to (V_{CC} + 0.3V)
TDIO Voltage/Current ..... –0.3V to –5mA
AbsMax Junction Temperature ..... 125°C
Storage Temperature ..... –55°C to 150°C
Reflow (Package Body) Temperature ..... 260°C

PIN CONFIGURATION



LQFN PACKAGE
42-LEAD (8mm × 5mm × 0.95mm)
$T_{J(MAX\ OPER)}$ = 125°C, θ_{JA} = 10.8°C/W ON OPTIMIZED
6-LAYER 3.6 INCH × 2.8 INCH PCB
EXPOSED PADS (V_{IN}, PGND, SW) MUST BE SOLDERED TO PCB

ORDER INFORMATION

PART NUMBER	PART MARKING*	FINISH CODE	PAD FINISH	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
LTC7050AV#PBF	7050	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- *Device temperature grade is identified by a label on the shipping container.

Parts ending with PBF are RoHS and WEEE compliant.

- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Power Input Supply Range		●			14	V
	V_{IN} Overvoltage Lockout Threshold	V_{IN} Rising	●	14.9		15.7	V
	V_{IN} Overvoltage Lockout Hysteresis				0.4		V
	V_{IN} Overvoltage Lockout Delay	(Note 3)			1		µs
	V_{IN} Shutdown Current	V_{IN} = 12V, RUN1 = RUN2 = 0			25		µA
V_{CC}	V_{CC} Input Supply Range		●	4.5	5	5.5	V
$V_{CC(UVLO)}$	V_{CC} Undervoltage Lockout Threshold	V_{CC} Rising	●	4.05	4.15	4.25	V
V_{UVLO_HYST}	V_{CC} Undervoltage Lockout Hysteresis				0.2		V
$I_{VCC(SD)}$	V_{CC} Supply Current in Shutdown	RUN1 = RUN2 = 0V			14		µA
I_{VCC_active}	V_{CC} Supply Current in Active	RUN1 = RUN2 = 5V, PWM = Float			2.5		mA
PV_{CC}	Driver Input Supply Range		●	4.5	5	5.5	V
$PV_{CC(UVLO)}$	PV_{CC} Undervoltage Lockout Threshold	PV_{CC} Rising	●	3.9	4.0	4.1	V
PV_{UVLO_HYST}	PV_{CC} Undervoltage Lockout Hysteresis				0.35		V
$I_{PVCC(SD)}$	PV_{CC} Supply Current in Shutdown	RUN1 = RUN2 = 0V			300		µA
I_{PVCC_active}	PV_{CC} and V_{CC} Supply Current in Active	RUN1 = RUN2 = 5V, PWM = Float			2.5		mA
t_{UVLO}	Undervoltage Time Lockout Delay, from V_{CC} and PV_{CC} to SW Low	PV_{CC}, V_{CC} Rising RUN = 5V PWM = 0 (Note 3)			1		µs
RUN Input							
V_{IH_RUN}	RUN High Threshold	RUN Rising	●	2.2	2.45	2.7	V
V_{RUN_HYS}	RUN Hysteresis				0.2		V
R_{PD_RUN}	EN Pull-Down Resistor				30		kΩ
T_{d_RUNH}	Propagation Delay for RUN Low to High	From RUN Low ≥ High to SW = 0, PWM = 0 (Note 3)			12		µs
T_{d_RUNL}	Propagation Delay for RUN High to Low	From RUN High ≥ Low to SW High Z, PWM = 0 (Note 3)				0.1	µs
PWM Input							
V_{IH_PWM}	PWM High Threshold		●			2.7	V
V_{IL_PWM}	PWM Low Threshold		●	0.8			V
V_{TR_PWM}	PWM Tri-State Range		●	1.5		2.1	V
V_{PWM_HYS}	PWM Hysterisis	Active to Tri-State or Tri-State to Active			300		mV
R_{PD_PWM}	PWM Pull-Down Resistor	To SGND			9.6		kΩ
R_{PU_PWM}	PWM Pull-Up Resistor	To V_{CC}			18.8		kΩ
$t_{PWMHI-SW}$	Delay Time, PWM High to SW High	No Fault Condition (Note 3)			10		ns
$t_{PWMLO-SW}$	Delay Time, PWM Low to SW Low	No Fault Condition(Note 3)			10		ns
$t_{Tri\_Lo\_Delay}$	Tri-State to Low Propagation Delay	PWM Going Low to SW Going Low			20		ns
$t_{Tri\_Hi\_Delay}$	Tri-State to High Propagation Delay	PWM Going High to SW Going High			30		ns
t_{Tri_Hold}	Active to Tri-State Delay Time	PWM Going to High Z to SW High Z (Note 3)			20		ns
t_{PWM_MINON}	PWM Minimum ON-Time				20		ns
V_{PWM_FLOAT}	PWM Floating Voltage		●	1.6	1.7	1.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SNS} Output							
A_{IMON}	Current Sense Gain (I_{MON}/I_{OUT})	V_{ISNS} = 1.5V I_{OUT} = 5A to 25A, PWM = 0		8.5	10	11.5	µA/A
I_{SNS}	Overall Accuracy	I_{OUT} = 25A, V_{ISNS} = 1.5V, PWM = 0, Accuracy at Trim			250 ±12.5		µA
		I_{OUT} = –10A, V_{ISNS} = 1.5V, PWM = 0			100		µA
V_{IMON}	IMON Operational Voltage Range		●	1.2		2.0	V
FLTB Output							
$R_{FLTB-PD}$	Fault Bar Open-Drain Pull-Down Resistance	FLTB Low				1	kΩ
TMON/FLT Output							
A_{TMON}	Thermal Monitor Gain	0°C < T_J < 150°C (Note 3)			8		mV/°C
V_{TMON}	Thermal Monitor Voltage	T_J = 0°C (Note 3)			0.6		V
		T_J = 25°C		780	800	825	mV
		T_J = 125°C (Note 3)			1.6		V
OTP	Overtemperature Protection Accuracy	(Note 3)			150		°C
OTP_Hys	Overtemperature Hysteresis	(Note 3)			40		°C
I_{SOURCE_TMON}	Thermal Monitor Maximum Source Current	T_J = 25°C, T_{MON} Forced at 0V		1			mA
I_{SINK_TMON}	Thermal Monitor Maximum Sink Current	T_J = 25°C, T_{MON} Forced at 1.28V				60	µA
V_{Tdiode}	Tdiode Forward Voltage Drop	T_J = 25°C, I_F = 0.1mA			678		mV
	Tdiode Voltage Drop Temperature Coefficient	I_F = 0.1mA (Note 3)			–1.8		mV/°C
SW Node							
V_{SW_Float}	SW Floating Voltage	V_{IN} = 12V			0.7		V
$R_{SW-PGND}$	SW Pull-Down Resistance				1.2		kΩ
Overcurrent Limits							
$I_{\_OCP}$	Positive Overcurrent Threshold	PWM = H		80	90	100	A
$I_{\_NCP}$	Negative Overcurrent Threshold	PWM = L			–45		A
t_{Blank_OC}	Positive Overcurrent Blanking Time	PWM = H (Note 3)			22		nS
t_{Blank_NC}	Negative Overcurrent Blanking Time	PWM = L (Note 3)			55		nS
$I_{\_ZCP}$	Positive Zero Current Threshold				5		A
$I_{\_ZCN}$	Negative Zero Current Threshold				–8		A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7050A is specified over the –40°C to 125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This parameter is not tested but is guaranteed by design.

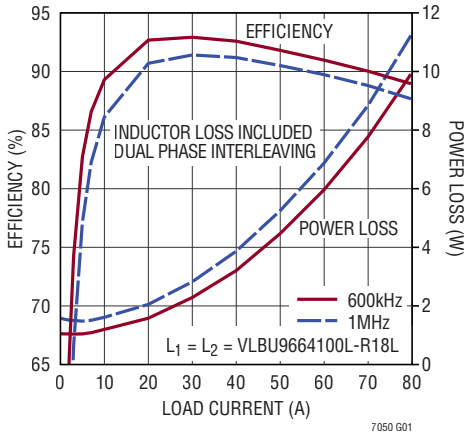
Note 4: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 5: The LTC7050 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

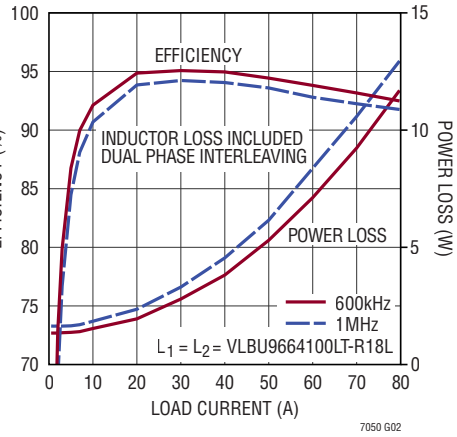
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V unless otherwise noted.

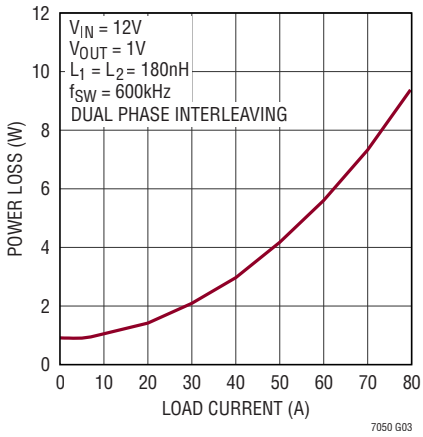
12V_{IN} to 1V_{OUT} Efficiency



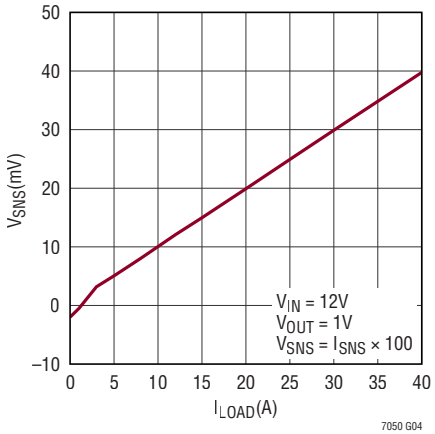
12V_{IN} to 1.8V_{OUT} Efficiency



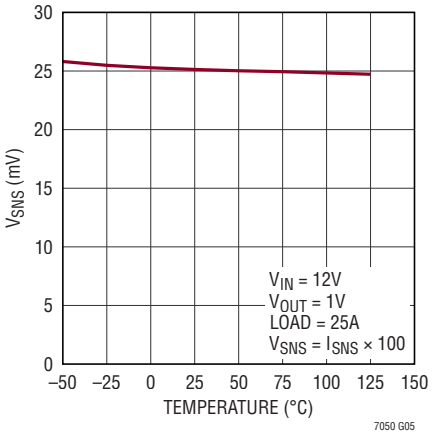
Power Dissipation vs Load



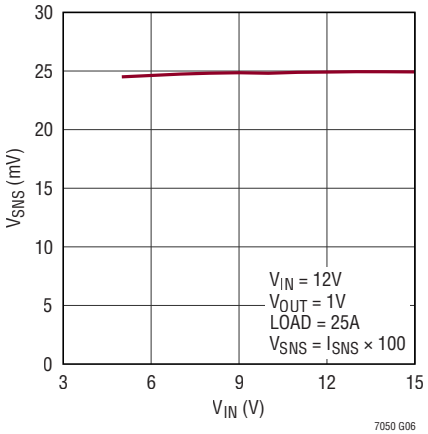
V_{SNS} vs I_{LOAD}



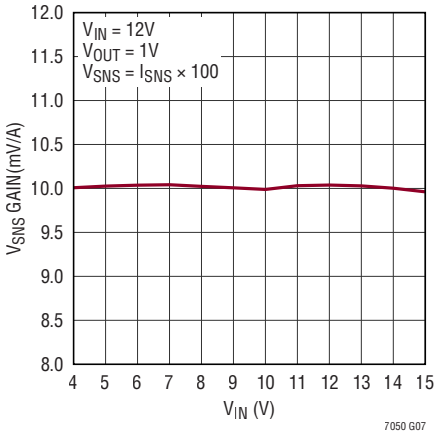
V_{SNS} vs Temperature



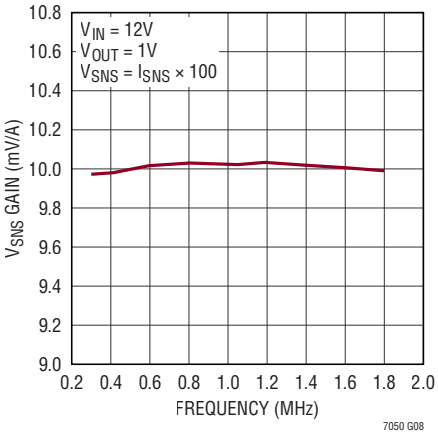
V_{SNS} vs V_{IN}



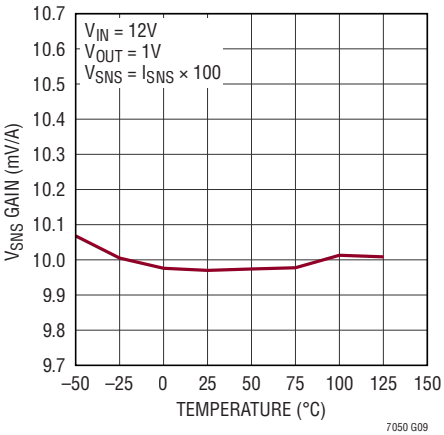
V_{SNS} Gain vs V_{IN}



V_{SNS} Gain vs Frequency



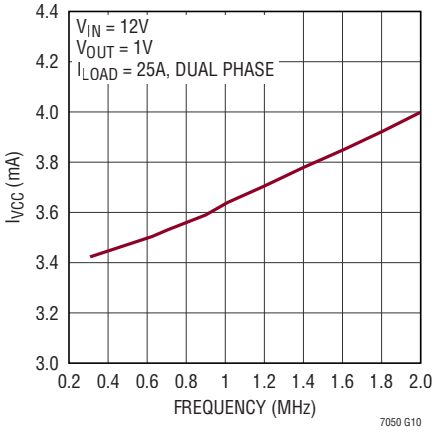
V_{SNS} Gain vs Temperature



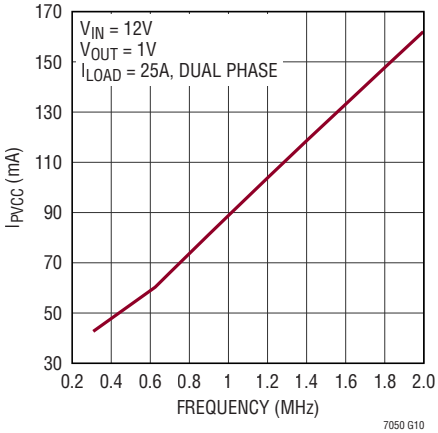
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V unless otherwise noted.

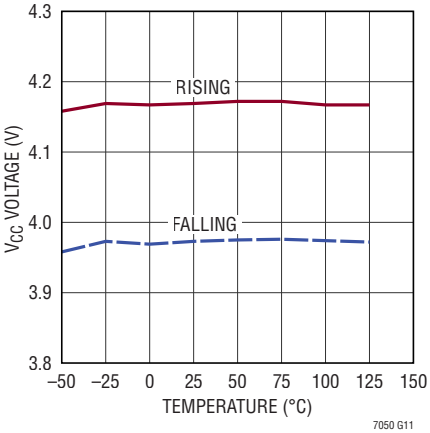
I_{VCC} vs Frequency



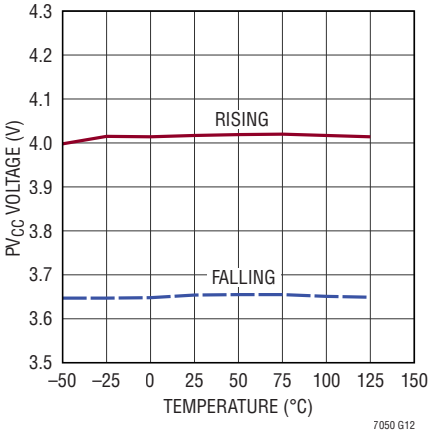
IPV_{CC} vs Frequency



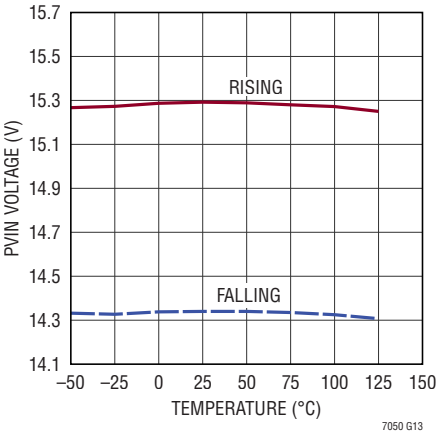
V_{CC} UVLO vs Temperature



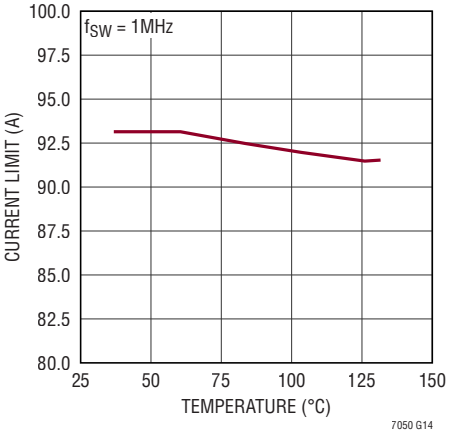
PV_{CC} UVLO vs Temperature



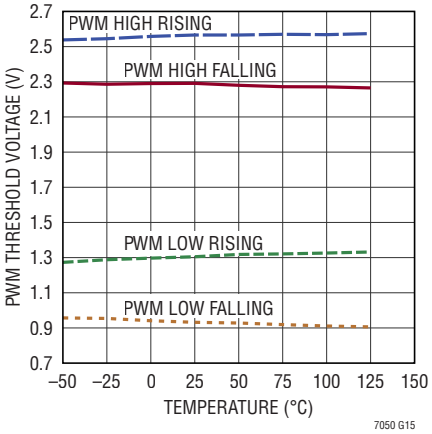
PV_{IN} OVLO vs Temperature



Current Limit vs Temperature



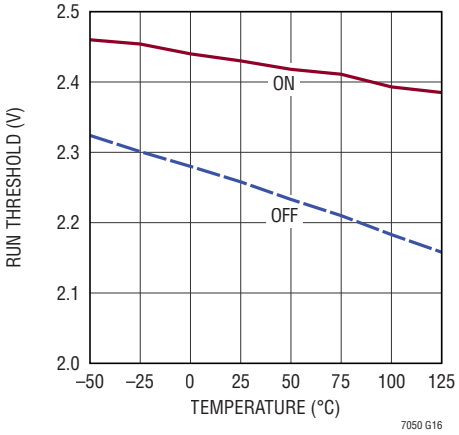
PWM Threshold vs Temperature



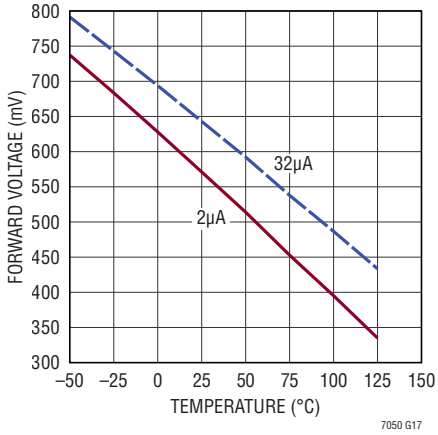
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V unless otherwise noted.

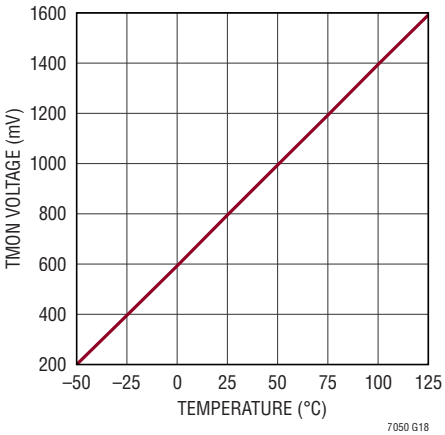
RUN Threshold vs Temperature



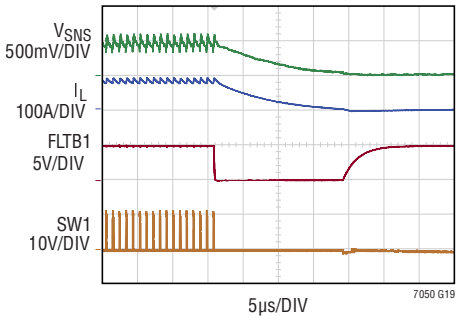
TDIO Forward Voltage



TMON vs Temperature

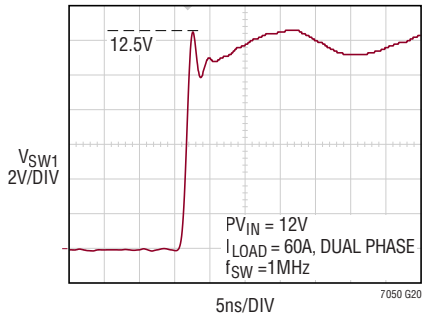


Overcurrent Protection



V_{SNS} = ISNSx500

Switching Rising Edge



PIN FUNCTIONS

RUN1, RUN2: Run Pin. When this pin is driven high, the is enabled. SW node is in high-Z state when RUN is low.

PWM1, PWM2: PWM Input Pin. With RUN driven high, SW will nominally follow this pin high, low, and high-Z. Nominal 3V CMOS logic levels; can be driven with 3V to 5V CMOS signals. Resistor divider holds voltage at 1.7V when in high-Z state.

I_{SNS1}, I_{SNS2}: Current Sense Pin. This pin sources/sinks instantaneous current equal to 1/100,000 the SW node current, positive and negative.

FLTB1, FLTB2: Fault Bar Pin. This open-drain pin pulls down when the chip/channel encounters a fault condition such as OC or OCN.

TMON/FLT: Temperature Monitor/Fault Pin. This pin provides a voltage, referred to SGND, of 0.6V to 1.8V corresponding to die temperature of 0°C to 150°C for a gain of 8mV/°C. Above 150°C, the pin is pulled high to indicate an overtemperature (OT) fault. The pin has limited current sinking capability, so multiple like pins can be tied together for highest temperature and single-OT-fault reporting.

TDIO: Temperature Diode Pin. This pin provides a reference diode to SGND for use in measuring die temperature.

PV_{CC}: 5V Driver Supply. This pin powers the low side gate driver directly and the high side gate driver through an internal bootstrapped supply riding on SW. Bypass this pin with a 10µF ceramic capacitor to PGND in close proximity to chip.

V_{CC}: 5V Supply. Bypass this pin with a 1µF ceramic capacitor to SGND in close proximity to chip.

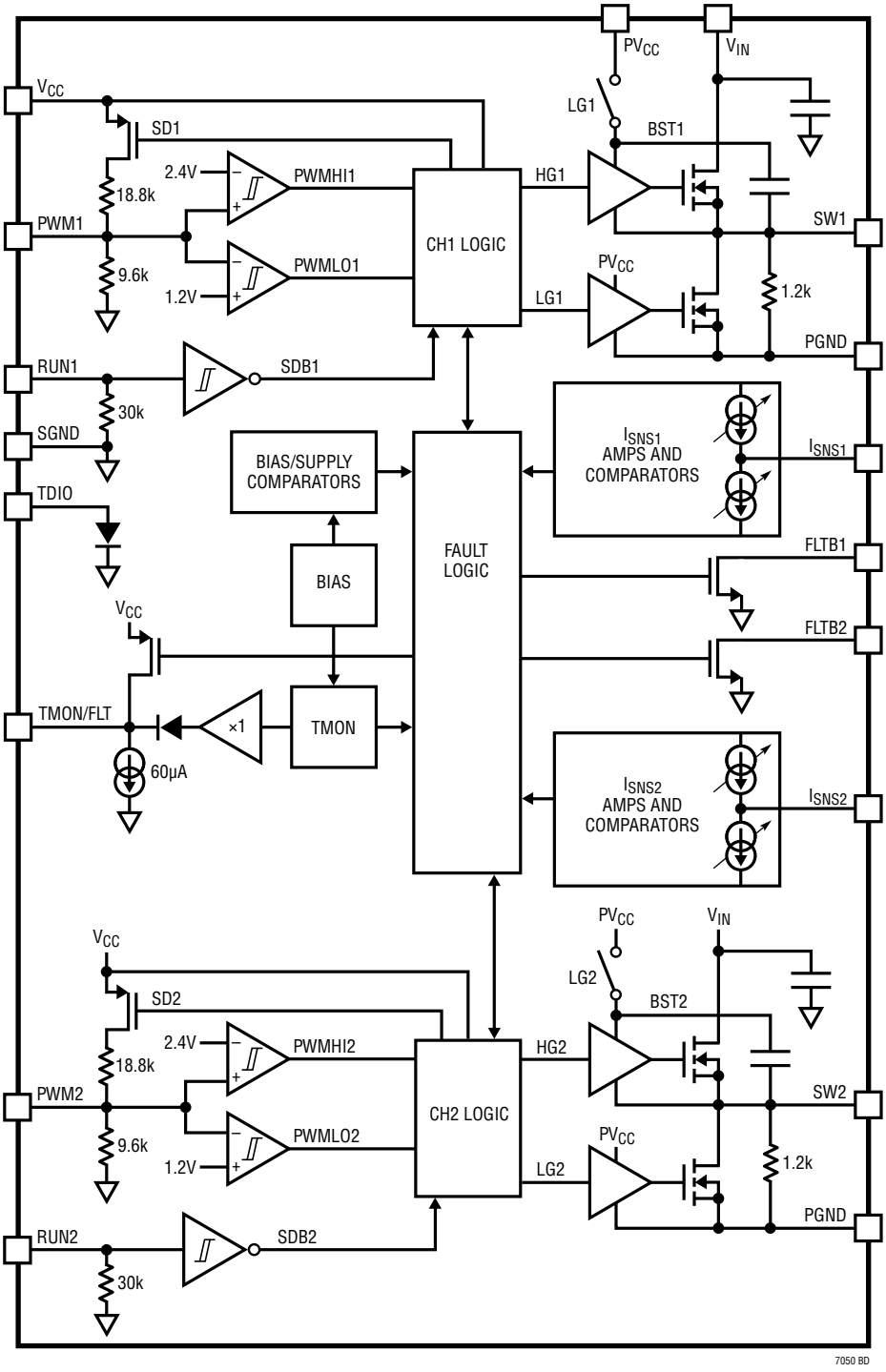
V_{IN}: Power Stage Supply. This pin is connected to SW through the high side N-channel FET.

SW1, SW2: Power Stage Switch Node. The output of the power stage, this node is connected to V_{IN} through the high side N-channel FET and to PGND through the low side N-channel FET.

PGND: Power Stage Ground. This pin is connected to SW through the low side N-channel FET. Also powers the drivers.

SGND: Circuit Ground.

BLOCK DIAGRAM



OPERATION

Main Control Architecture

The LTC7050 is a dual-channel or dual-phase integrated-driver half-bridge power MOSFET stage for DC/DC step-down applications. It is designed to be used in a synchronous switching architecture with a logic-level controller providing PWM three-state control outputs. The relationship between the transition thresholds and the three input states of the LTC7050 is illustrated in Figure 1.

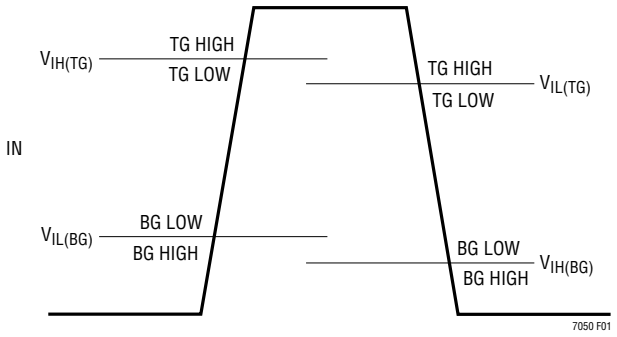


Figure 1. Three-State Input Operation

In normal operation, PWMHI turns on the high side FET, and PWMLO turns on the low side FET. SW node follows the PWM pin with a typical 10ns delay. There is <1ns dead time before SW rises from PGND to V_{IN} and a typical 3ns dead time after SW falls.

The high side FET driver is powered from the internal BST node to SW via an internal integrated switch and capacitor, which allows lower dropout than achievable with a typical diode as well as higher-frequency operation.

Current Sense

Real-time current sense amplifiers provide a scaled-down version of SW current. During PWMHI or PWMLO, the I_{SNS} pin sources or sinks, according to SW current direction, a current equal to 1/100,000 the instantaneous SW current.

Associated current comparators flag high side FET positive overcurrent (OC) and low side FET negative overcurrent (OCN) conditions. Zero-current of both FETs are also detected by associated current comparators.

Temperature Monitor and Overtemperature Fault

Normally, TMON outputs a voltage from 0.6V to 1.8V, corresponding to a die temperature range of 0°C to 150°C. The TMON voltage is calculated by:

$$V_{TMON}\ (V) = 800mV + (T_J\ (°C) – 25°C) \bullet (8mV/°C)$$

Figure 2 illustrates the relationship between V_{TMON} and die temperature.

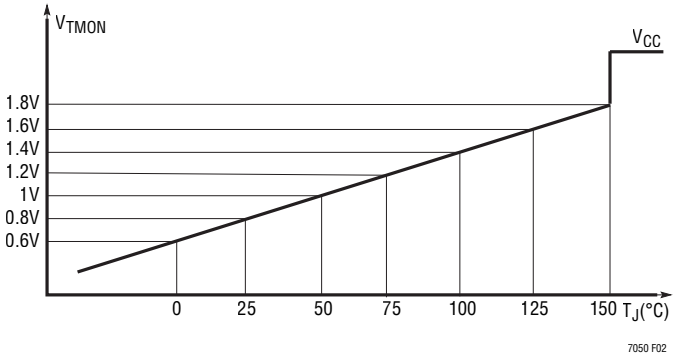


Figure 2. V_{TMON} vs Die Temperature

TMON is driven by an amplifier that can source current but has limited sinking capacity. This allows multiple TMON pins to be paralleled, with the highest temperature being reported. Overtemperature is triggered at 150°C (typical), and it causes the TMON pin to be pulled high to V_{CC}. The overtemperature fault will be cleared once the internal temperature falls 20°C (typical) below the threshold.

TDIO pin is internally connected to the anode of a P/N junction diode while the cathode is connected to SGND. It provides an alternative measurement of die temperature for the controllers, such as LTC3884-1, to measure the die temperature using direct V_{BE} method or ΔV_{BE} method.

Voltage Fault Conditions

When V_{CC} or PV_{CC} is in UVLO, or V_{IN} is in OVLO, SW will not respond to PWM and both top FET and bottom FET are off.

When BST-to-SW voltage is in UVLO, SW will not respond to a PWMHI until a PWMLO is provided such that BST-to-SW voltage is recharged sufficiently.

OPERATION

Over Current Fault Conditions

When the high side FET is on, instantaneous SW current of >93A (net current flowing out of SW) will trip the overcurrent (OC) comparator and set the internal OC state. When this happens, regardless of PWM pin state, the high side FET will be turned off, and the low side FET will be turned on until SW current decreases to 5A, at which point OC state will be reset. Normal PWMHI-to-high-side-FET and PWMLO-to-low-side-FET operation resumes.

When the low side FET is on, instantaneous SW current of <–45A (net current flowing into SW) will trip the OCN comparator. When this happens, regardless of PWM pin state, the low side FET will be turned off and the high side FET will be turned on until SW current increases to –8A, at which point OCN state will be reset. Normal PWMHI-to-high-side-FET and PWMLO-to-low-side-FET operation resumes. The trigger and reset of over current condition are illustrated in Figure 3.

In either OC or OCN condition, FLTB is pulled down.

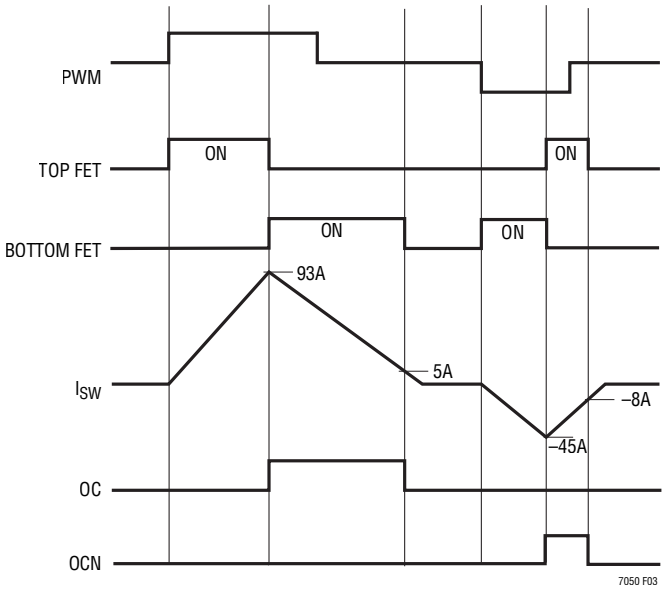


Figure 3. Over Current Conditions

Active Diode Mode

If PWM goes from high to Hi-Z state while large (>5A) currents are still flowing through the top FET from V_{IN} to SW, the top at FET will turn off and the bottom FET will turn on to freewheel the current until it has been ramped down. If PWM goes from high to Hi-Z state while large (≥8A) currents are still flowing through the top FET from SW to V_{IN}, the top FET will not turn off until the current has been ramped down.

Similarly, if PWM goes from low to Hi-Z state while large (≥8A) currents are still flowing through the bottom FET from SW to PGND, the bottom FET will turn off, and the top FET will turn on to freewheel the current until it has been ramped down. If PWM goes from high to Hi-Z state while large (>5A) currents are still flowing through the bottom FET from PGND to SW, the bottom FET will not turn off until the current has been ramped down.

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Power Sequence

The V_{CC} and PV_{CC} of LTC7050 should be biased before V_{IN} is present and power down after V_{IN} is removed. Do not force RUN pin voltages above V_{CC} voltage. Make sure that the LTC7050 has been biased appropriately and the RUN pin of LTC7050 is pulled up before enabling the PWM controller.

Fault Management

The fault management and shutdown mode of LTC7050 is summarized in Table 1. Connecting the open-drain output FLTB pin to the controller's RUN pin can prevent the controller from starting up and force the converter to restart once the LTC7050 runs into fault conditions, except BST-to-SW undervoltage fault.

Table 1. Fault Management and Shutdown Mode Summary

	FLTB	RESPOND TO PWM	TMON
V_{IN} OVLO	Low	No, Both FETs Off Until I_{SW} = 0	Report Temperature
V_{CC} UVLO	Low	No, Immediate Off	Floating
PV_{CC} UVLO	Low	No, FETs Off Until I_{SW} = 0.	Report Temperature
Positive OC	Low	No, Top FET Immediate Off	Report Temperature
Negative OC	Low	No, Bottom FET Immediate Off	Report Temperature
Overtemperature	Low	Yes	Pull Up to V_{CC}.
BST-to-SW UV	High	Ignore PWMHI	Report Temperature
RUN Shutdown	Low	No, Both FETs Off	Floating

Current Sense and Current Limit

I_{SNS} sources and sinks a current which is 1/100,000 of the SW current. According to the controller's maximum current sense signal range, select a proper resistor to convert the I_{SNS} current into a differential voltage signal reflecting the real-time SW current. The resistor should be biased at a low impedance common mode voltage, which has current sinking and sourcing capability. Make sure that at the maximum positive current and negative current, the I_{SNS} pin voltage is in the specified range so that the gain I_{SNS}/I_{SW} remains constant.

A general LTC7050 application circuit is shown on the first page of this data sheet. LTC7050 is optimized for the application of high frequency high current voltage regulator. External component selection is largely driven by the load requirement and begins with the selection of the switching frequency f_{SW} and inductor L. Refer to Frequency Selection and Inductor Selection sections for the guidance. The I_{SNS} resistors are selected to set the current limit.

In high frequency high current applications, the switching spikes coupled to the I_{SNS} signal may result in a reading offset in heavy load range, but does not impact the $\Delta I_{SNS}/\Delta I_{SW}$ gain. An optional resistor between I_{SNS} pin to GND can mitigate the offset. The resistor value ROS is calculated by I_{SNS} pin voltage (referring to GND) divided by the offset current observed. The resistor value may be different for a different switching frequency. This modification does not impact the internal overcurrent protection and negative overcurrent protection.

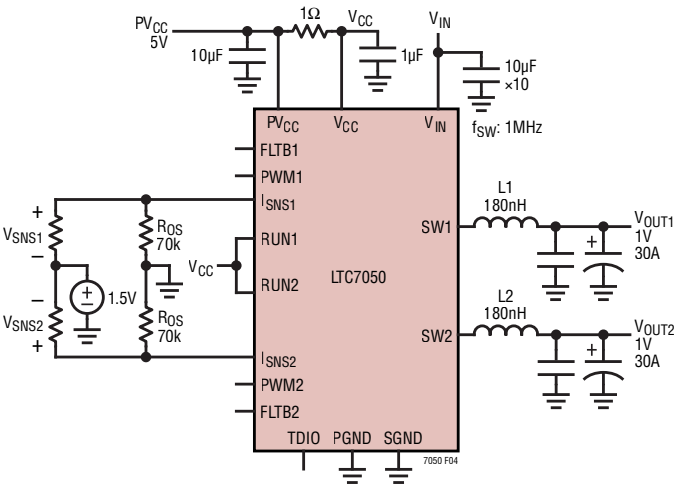

Figure 4.

Frequency Selection

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing FET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. In the selection of switching frequency, make sure that the high side on-time at maximum input voltage is longer than LTC7050's minimum on-time, $t_{ON(MIN)}$, which is the smallest time duration that the LTC7050 is capable of turning on the top FET. It is determined by internal timing delays, power

APPLICATIONS INFORMATION

stage timing delays and the gate charge required to turn on the top FET. Low duty cycle applications may approach this minimum on-time limit (see Equation 1).

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f_{SW}} \quad (1)$$

Input Capacitors

The LTC7050 should be connected to a V_{IN} supply through low impedance power planes. Ceramic input capacitors should be placed as close to the package as physically possible, with size and quantity appropriate for temperature rise with ripple current as calculated below.

For a buck converter, the switching duty cycle can be estimated by Equation 2.

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated by Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)} \quad (3)$$

where η is the estimated efficiency of the power section.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency, f_{SW}, directly determine the inductor's peak-to-peak ripple current (Equation 4).

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \bullet L} \right) \quad (4)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to Equation 5.

$$L \geq \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \bullet I_{RIPPLE}} \right) \bullet \frac{V_{OUT}}{V_{IN}} \quad (5)$$

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates **hard**, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Output Capacitors

The LTC7050 is designed for high frequency switching and low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor, or ceramic capacitors. At 1MHz, the typical output capacitance range is from 500µF to 1000µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required.

Bypassing and Grounding

The LTC7050 requires proper bypassing on the PV_{CC} and V_{CC} supplies due to its high speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot. Follow the following steps to obtain the optimum performance from the LTC7050.

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- Mount the bypass capacitors as close as possible between the V_{CC} and SGND pins, and the PV_{CC} and PGND pins. The traces should be shortened as much as possible to reduce lead inductance.
- Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Any significant ground drop will degrade signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- Be sure to solder the Exposed Pad on the back side of the LTC7050 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in far greater thermal resistances.

PCB Layout

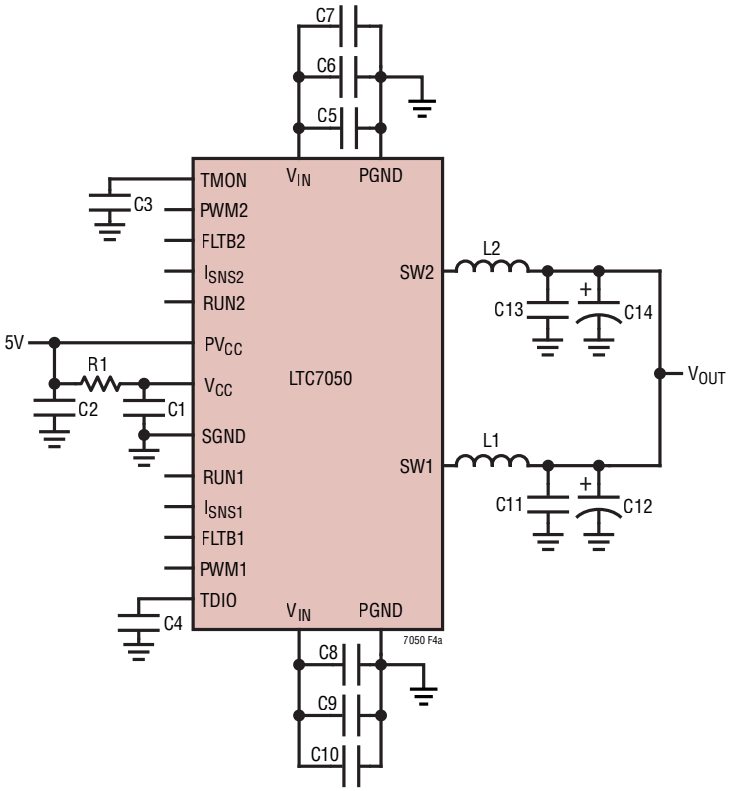
Due to the LTC7050's high power density and high speed, high frequency operation, proper PCB layout and composition are critical to maximizing performance.

At a minimum, the PCB should be 4-layer with at least top and bottom layers 2oz. copper. As much as possible, top and bottom layers should be continuous V_{IN} and PGND areas. At least one inner layer, preferably the second, should be a continuous PGND plane.

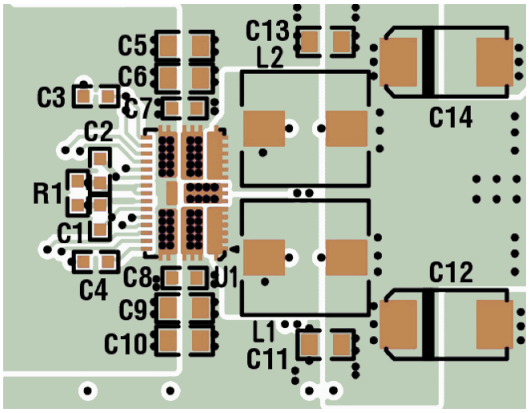
Copper-filled vias should be used under the package exposed pads to connect top and bottom PCB layers. $\theta_{JCbottom}$ is <1°C /W. Anything less than copper-filled vias will compromise θ_{JA} greatly.

The inductor pads should be placed as close as possible to the package, with traces as short and wide as possible. If possible, SW traces should be doubled up with the second layer, taking care not to couple to sensitive traces.

A recommended PCB layout is shown in Figure 5b.



(a) Schematic

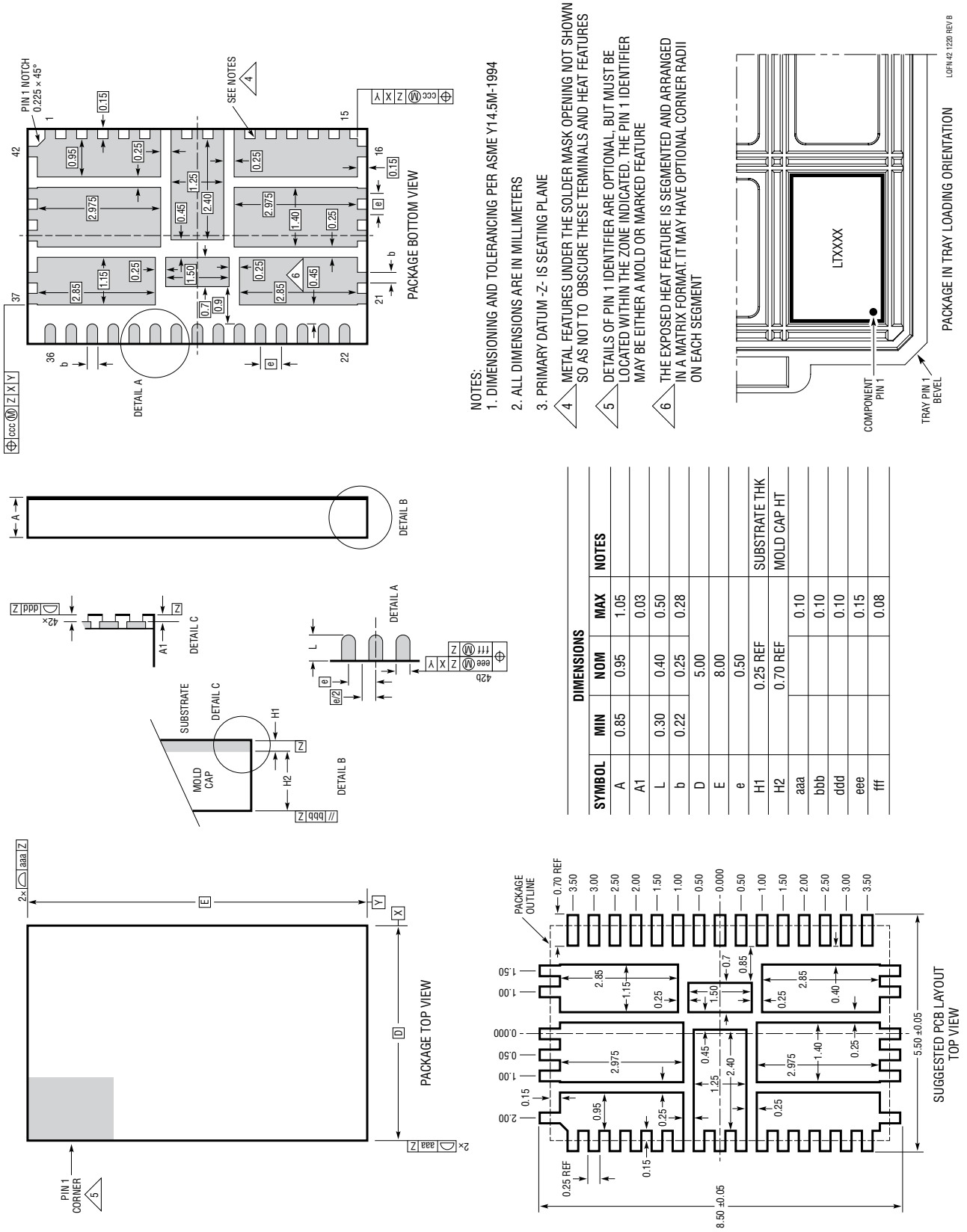


(b) Example PCB Layout

Figure 5.

PACKAGE DESCRIPTION

LQFN Package
42-Lead (5mm × 8mm × 0.95mm)
(Reference LTC DWG # 05-08-1571 Rev B)

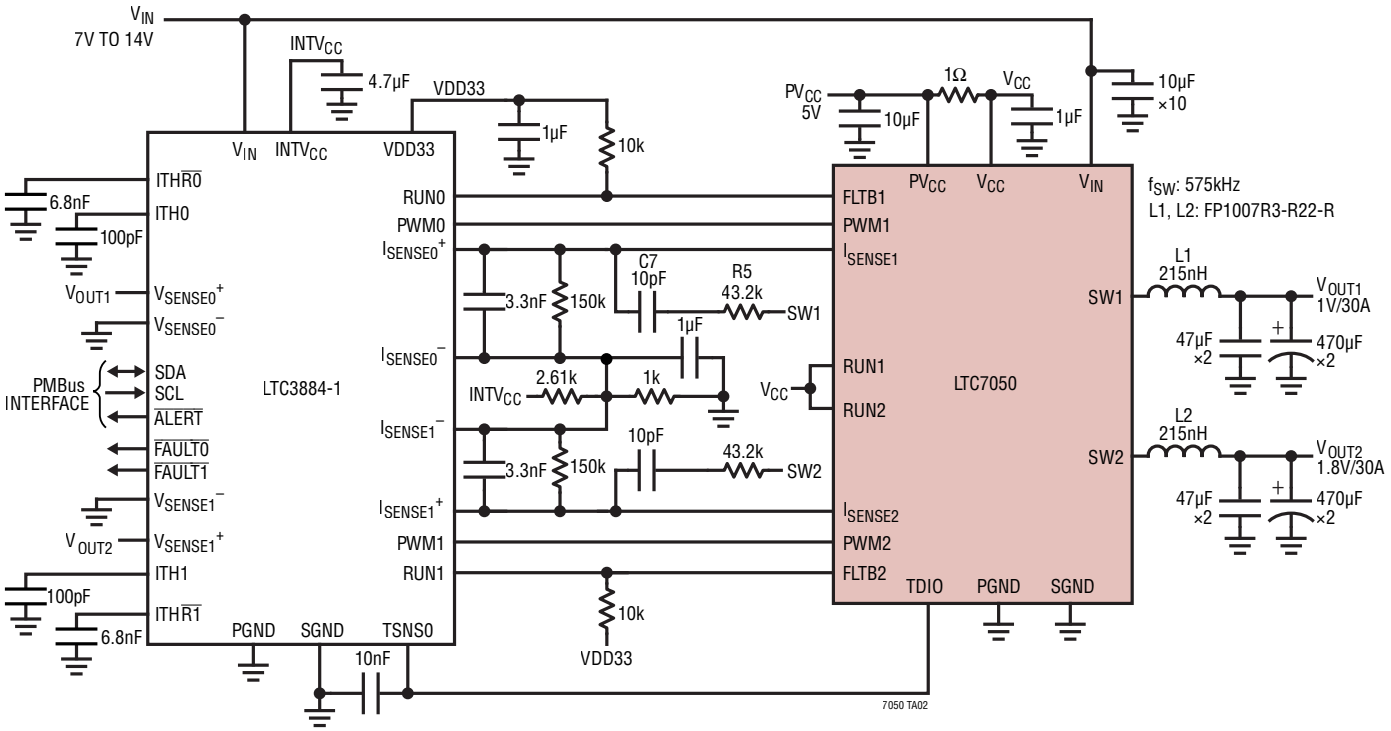


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		5.00		
E		8.00		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

TYPICAL APPLICATIONS

LTC7050 and LTC3884-1 Schematic



PINS NOT SHOWN IN LTC3884-1 CIRCUIT: PGOOD0, PGOOD1, TSNS1, SYNC, ASEL0, ASEL1, VOUT0_CFG, VOUT1_CFG, FREQ_CFG,PHASE_CFG

PINS NOT SHOWN IN LTC7050 CIRCUIT: TMON

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7051	SilentMOS Smart Power Stage in 5mm × 8mm LQFN	140A Peak Current, Silent Switcher 2 Architecture, V_{IN} Up to 14V, 5mm × 8mm LQFN Package
LTC7050-1	Dual SilentMOS Smart Power Stage in 5mm × 8mm LQFN	70A Peak Current per Channel, Silent Switcher 2 Architecture, V_{IN} Up to 16V, 5mm × 8mm LQFN Package
LTC7051-1	SilentMOS Smart Power Stage in 5mm × 8mm LQFN	140A Peak Current, Silent Switcher 2 Architecture, V_{IN} Up to 16V, 5mm × 8mm LQFN Package
LTC3888/LTC3888-1	Dual Output 8-Phase Step-Down DC/DC Controller with Digital Power System Management	$4.5V \le V_{IN} \le 26.5V$, $0.3V \le V_{OUT} \le 3.45V$, I^2C/PMBus Control, Programmable Loop Compesation, 5mm × 8mm QFN-52
LTC3884/LTC3884-1	Dual Output PolyPhase® Step-Down Controller with Sub-Milliohm DCR Sensing and Digital Power System Management	$4.5V \le V_{IN} \le 38V$, $0.5V \le V_{OUT} \le 5.5V$, I^2C/PMBus Control, Programmable Loop Compesation, 5mm × 8mm QFN-52
LTC7851	Quad Output Multiphase Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with DrMOS, Power Blocks or External Drivers/MOSFETs, V_{IN} Range Depends on External Components, $4.5V \le V_{CC} \le 5.5V$, $0.6V \le V_{OUT} \le V_{CC} - 0.5V$
LTC7852/LTC7252-1	Dual Output 6-Phase Current Mode Synchronous Buck Controller with Current Monitoring	Operates with DrMOS, Power Blocks, $0.5V \le V_{OUT} \le 2V$, Hiccup Mode Overcurrent Protection, Flexible Phase Configuration
LTC3861	Dual, Multiphase Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with Power Blocks, DrMOS or External MOSFETs $3V \le V_{IN} \le 24V$
LTC3882/LTC3882-1	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	$3V \le V_{IN} \le 38V$, $0.5V \le V_{OUT1,2} \le 5.25V$, ±0.5% V_{OUT} Accuracy I^2C/PMBus Interface, uses DrMOS or Power Blocks
LTC3887/LTC3887-1	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management, 70mS Start-Up	$4.5V \le V_{IN} \le 24V$, $0.5V \le V_{OUT0,1}$ (±0.5%) $\le 5.5V$, 70mS Start-Up, I^2C/PMBus Interface, –1 Version uses DrMOS or Power Blocks