Four-Channel Transimpedance Amplifier with Output Multiplexing

FEATURES

- 500MHz –3dB Bandwidth with 1pF Input Capacitance
- Differential Output
- Built-In High-Speed ADC Driver with Output MUX
- 22.2kΩ Transimpedance Gain
- 4.5pA/√Hz Input Current Noise Density 500MHz (1pF)
- 69nA$_{RMS}$ Integrated Input-Referred Current Noise Over 500MHz (1pF)
- Large Linear Input Current Range 0µA to 90µA
- Large Overload Current > –400mA Peak
- Fast Overload Recovery
- Fast Channel Switchover: 10ns
- Single 3.3V Supply
- Power Dissipation: 191mW to 324mW, Varies with Output Mode
- Up to 2V$_{P-P}$ Output Swing on 50Ω Differential Load
- Output MUX Combines Multiple 4-Channel Devices to Create 8, 12, 16 … 32 Channel Solutions
- 3mm × 5mm, 24-Lead QFN Package, Wettable Flanks

APPLICATIONS

- Automotive LIDAR Receiver
- Industrial LIDAR Receiver

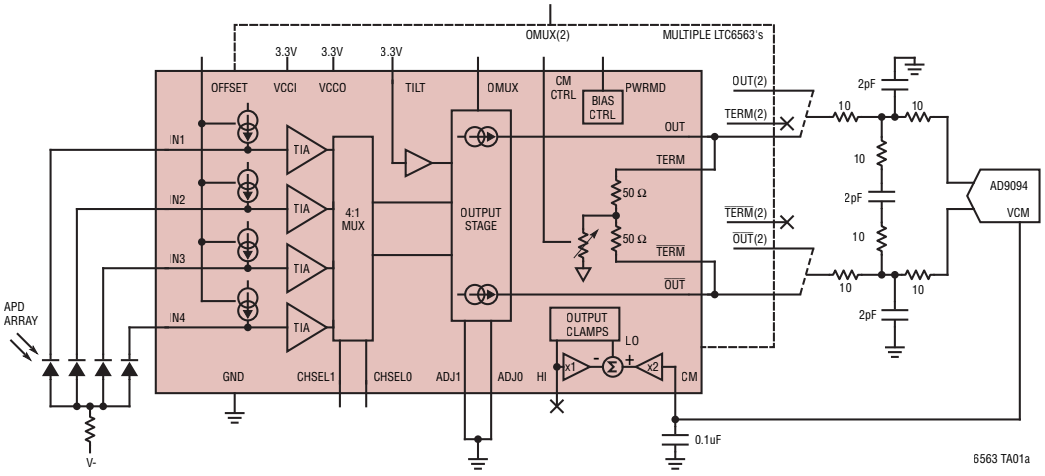
DESCRIPTION

The LTC®6563 is a low-noise four-channel transimpedance amplifier (TIA) with 500MHz bandwidth. The LTC6563 TIA's low noise, wide linear range, and low power dissipation are ideal for LIDAR receivers using Avalanche photodiodes (APDs) and photodiodes (PDs). The amplifier features 22.2kΩ transimpednace gain (RT) and 90µA linear input current range. Using an APD with a total input capacitance of 1pF, the input current noise density is 4.5pA/√Hz at 500MHz. The LTC6563 consumes between 191mW and 324mW on a 3.3V supply depending on output mode. An internal 4-to-1 MUX simplifies the system design. In addition, external multiplexing capability allows channel expansion up to 64 channels, saving space and power. Fast overload recovery and fast channel switchover make the LTC6563 well suited for LIDAR receivers with multiple APDs. The built-in high-speed differential ADC driver can swing as much as 2V$_{P-P}$ on a 50Ω differential load. Separate built-in termination resistors ease output multiplexing.

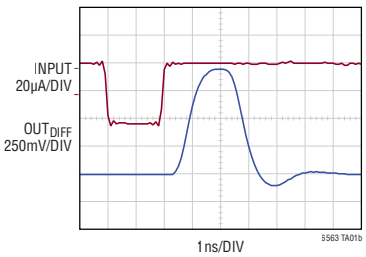
The LTC6563 is packaged in a 3mm × 5mm 24-pin exposed pad QFN package for thermal management and low inductance.

TYPICAL APPLICATION

Typical Application with DC-Coupled Inputs Driving an ADC



Pulse Response



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage:
- V_{CCI} to GND ..... –0.3V to 3.6V
- V_{CCO} to GND ..... –0.3V to 3.6V

Input Current (CHSEL0, CHSEL1, ADJ0, ADJ1, PWRMD, OMUX, CM, HI, OFFSET, TILT) ..... ±10mA

Amplifier Inputs (IN1, IN2, IN3, IN4):
- Voltage..... –0.3V to 3.6V
- Current..... $\pm 400mA_{RMS}$
- Current.....–1A Transient

Amplifier Outputs (OUT, $\overline{OUT}$):
- Voltage..... –0.3V to 3.6V
- Current..... ±100mA

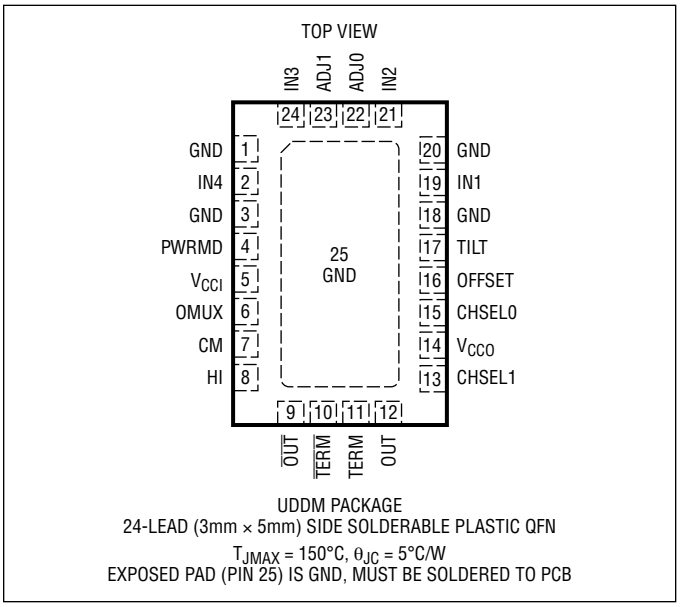
Amplifier Output Termination (TERM, $\overline{TERM}$):
- Voltage..... –0.3V to 3.6V
- Current..... ±100mA

Operating Temperature Range:
- LTC6563I (Note 2) .....–40°C to 85°C
- LTC6563H (Note 3).....–40°C to 125°C

Storage Temperature Range .....–65°C to 150°C

Junction Temperature ..... 150°C

PIN CONFIGURATION



UDDM PACKAGE
24-LEAD (3mm × 5mm) SIDE SOLDERABLE PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V. All other input pins are floating unless stated otherwise. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BW	–3dB Bandwidth	200mV$_{P-P,OUT}$ and $C_{IN,TOT}$ = 1pF			500		MHz
R_T Differential	Small Signal Transimpedance	I_{IN} < 2μA$_{P-P}$, R_L = 50Ω Differential	 ●		22.2 **TBD**		kΩ kΩ
R_{IN}	Input Impedance	f = 100kHz Active Channel f = 100kHz Inactive Channel			225 409		Ω Ω
R_{OUT}, R_{OUT}	Output Impedance	f = 100kHz			50		Ω
I_n	Input Current Noise Density	f = 100MHz, $C_{IN,TOT}$ = 1pF			2.1		pA/√Hz
		f = 200MHz, $C_{IN,TOT}$ = 1pF			2.7		pA/√Hz
		f = 300MHz, $C_{IN,TOT}$ = 1pF			3.2		pA/√Hz
		f = 400MHz, $C_{IN,TOT}$ = 1pF			4		pA/√Hz
		f = 500MHz, $C_{IN,TOT}$ = 1pF			4.5		pA/√Hz
		f = 600MHz, $C_{IN,TOT}$ = 1pF		5.3			pA/√Hz
	Integrated Input Current Noise	f = 0.1MHz to 100MHz, $C_{IN,TOT}$ = 1pF			17		nA$_{RMS}$
		f = 0.1MHz to 200MHz, $C_{IN,TOT}$ = 1pF			29		nA$_{RMS}$
		f = 0.1MHz to 300MHz, $C_{IN,TOT}$ = 1pF			41		nA$_{RMS}$
		f = 0.1MHz to 400MHz, $C_{IN,TOT}$ = 1pF			54		nA$_{RMS}$
		f = 0.1MHz to 500MHz, $C_{IN,TOT}$ = 1pF			69		nA$_{RMS}$
		f = 0.1MHz to 600MHz, $C_{IN,TOT}$ = 1pF		85			nA$_{RMS}$
$t_{RECOVER}$	Overload Recovery Time	I_{IN} = –400μA, $C_{IN,TOT}$ = 1pF			6		ns
t_{CH_SWITCH}	Channel Switching Time	CHSEL (0, 1)			10		ns
t_{OMUX_SWITCH}	Output MUX Switchover Time	OMUX			20		ns

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V. All other input pins are floating unless stated otherwise. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN1, IN2, IN3, IN4 Pins							
V_{IN}	Input Bias Voltage	Active Channel	 ●		0.8 **TBD**		V V
		Inactive Channel	 ●		0.7 **TBD**		V V
OUT and $\overline{OUT}$ Pins							
$V_{OUT,\overline{OUT}\_DEFAULT}$	Output Default Voltage	CM Floating	 ●		0.7 **TBD**		V V
$V_{SWINGDIFF}$	Differential Output Voltage Swing		 ●	**TBD** **TBD**	2.08		V$_{P-P}$ V$_{P-P}$
$V_{SWINGMIN}$	Output Voltage Swing Low	Single-Ended Measurement of OUT, $\overline{OUT}$	 ●		**TBD**	**TBD** **TBD**	V V
$V_{SWINGMAX}$	Output Voltage Swing High	Single-Ended Measurement of OUT, $\overline{OUT}$	 ●	**TBD** **TBD**	**TBD**		V V
Output Common Mode Voltage Control (CM Pin)							
A_{CM}	CM Pin Voltage Gain CM Pin to Differential OUT	V_{CM} = 0.65V to 1.15V where V_{OUTCM} Slope = 1	 ●	**TBD** **TBD**	1		V/V V/V

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V. All other input pins are floating unless stated otherwise. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CM\_DEFAULT}$	Default CM Pin Voltage	V_{CM} Pin Floating	 ●	**TBD** **TBD**	0.9	**TBD** **TBD**	V V
V_{CM_OS}	Common Mode Offset Voltage	$V_{OUTCM} – V_{CM}$	 ●	**TBD** **TBD**	10	**TBD** **TBD**	mV mV
V_{OUTCM_MIN}	V_{OUTCM} Minimum Voltage	V_{CM} = 0V	 ●		0.2	**TBD** **TBD**	V V
V_{OUTCM_MAX}	V_{OUTCM} Maximum Voltage	V_{CM} = 2V	 ●	**TBD** **TBD**	1.8		V V
R_{CM}	CM Pin Input Resistance		 ●	**TBD** **TBD**	16.3	**TBD** **TBD**	kΩ kΩ
C_{CM}	CM Pin Input Capacitance				1.5		pF
Output Clamping (HI Pin, CM Pin)							
$V_{HI\_DEFAULT}$	Default HI Pin Voltage		 ●	**TBD** **TBD**	1.8	**TBD** **TBD**	V V
$V_{HI\ OS}$	High Side Clamp Offset Voltage	$V_{OUT(MAX)} – V_{HI}$, $V_{OUTBAR(MAX)} – V_{HI}$	 ●	**TBD** **TBD**	10	**TBD** **TBD**	mV mV
V_{LO_OS}	Low Side Clamp Offset Voltage	$V_{OUT(MIN)} – (2 • V_{CM} – V_{HI})$, $V_{OUTBAR(MIN)} – (2 • V_{CM} – V_{HI})$	 ●	**TBD** **TBD**	10	**TBD** **TBD**	mV mV
V_{HI} Range		V_{HI} Needs to Be > V_{CM}		0		3.3	V
A_{HI}	High Side Clamp Gain HI Pin to Output Clamp	V_{HI} = 1.8V, V_{CM} = 0.9V, I_{IN} = 200µA	 ●	**TBD** **TBD**	1	**TBD** **TBD**	V/V V/V
A_{LO}	Low Side Clamp Gain HI Pin to Output Clamp	V_{HI} = 1.8V, V_{CM} = 0.9V, I_{IN} = 200µA	 ●	**TBD** **TBD**	–1	**TBD** **TBD**	V/V V/V
R_{HI}	HI Pin Input Impedance		 ●	**TBD** **TBD**	13.6	**TBD** **TBD**	kΩ kΩ
C_{HI}	HI Pin Input Capacitance				1.5		pF
Input Current Cancellation (OFFSET Pin)							
$V_{OFFSET\_DEFAULT}$	OFFSET Pin Default Voltage		 ●	**TBD** **TBD**	0	**TBD** **TBD**	V V
I_{OFFSET_MIN}	Minimum Input Offset Current	V_{OFFSET} = 0V	 ●		0	**TBD** **TBD**	mA mA
I_{OFFSET_MAX}	Maximum Input Offset Current	V_{OFFSET} = 3.3V	 ●	**TBD** **TBD**	200		µA µA
G_{OFFSET}	OFFSET Pin Transconductance OFFSET Voltage to Input Offset Current	V_{OFFSET} = 0.2V to 0.4V, I_{IN} = 40µA	 ●	**TBD** **TBD**	0.48	**TBD** **TBD**	mA/V mA/V
R_{OFFSET}	OFFSET Pin Impedance		 ●	**TBD** **TBD**	6.6	**TBD** **TBD**	kΩ kΩ
Output Offset (TILT Pin)							
$V_{TILT\_DEFAULT}$	Default Tilt Pin Voltage		 ●	**TBD** **TBD**	2	**TBD** **TBD**	mV mV
A_{TILT}	TILT Pin Slope TILT to Differential Out	V_{TILT} = 0.2V to 0.4V	 ●	**TBD** **TBD**	1	**TBD** **TBD**	V/V V/V
R_{TILT}	TILT Pin Input Impedance		 ●	**TBD** **TBD**	22.7	**TBD** **TBD**	kΩ kΩ
ADJ0, ADJ1, CHSEL0, CHSEL1 Pins with Internal Pull-Down Resistors							
V_{IL}	Input Low Voltage		●			0.8	V
V_{IH}	Input High Voltage		●	1.5			V

Rev PrB

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V. All other input pins are floating unless stated otherwise. V_{OUTCM} is defined as (OUT + $\overline{OUT}$)/2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input Low Current	Pin Voltage = 0.8V	 ●	**TBD** **TBD**	3.8	**TBD** **TBD**	µA µA
I_{IH}	Input High Current	Pin Voltage = 1.5V	 ●	**TBD** **TBD**	7.2	**TBD** **TBD**	µA µA
C_{IN}	Input Capacitance				1.5		pF
R_{IN}	Input Impedance	To GND	 ●	**TBD** **TBD**	218	**TBD** **TBD**	kΩ kΩ
OMUX, PWRMD, Pins with Internal Pull-Up Resistors							
V_{IL}	Input Low Voltage		●			0.8	V
V_{IH}	Input High Voltage		●	1.5			V
I_{IL}	Input Low Current	Pin Voltage = 0.8V	 ●	**TBD** **TBD**	12	**TBD** **TBD**	µA µA
I_{IH}	Input High Current	Pin Voltage = 1.5V	 ●	**TBD** **TBD**	8.6	**TBD** **TBD**	µA µA
C_{IN}	Input Capacitance				1.5		pF
R_{IN}	Input Impedance	To V_{CCI}	 ●	**TBD** **TBD**	208	**TBD** **TBD**	kΩ kΩ
Power Supply							
V_S	Operating Supply Range			3.15	3.3	3.45	V
I_{VCCI}	Input Supply Current	Any Adjust Setting	 ●	**TBD** **TBD**	34	**TBD** **TBD**	mA mA
$I_{VCCI\_SHUTDOWN}$	Input Supply Current	PWRMD = OMUX = LO	 ●	**TBD** **TBD**	3.8	**TBD** **TBD**	mA mA
I_{VCCO}	Output Supply Current	ADJ1 = HI, ADJ0 = HI	●	**TBD** **TBD**	64.5	**TBD** **TBD**	mA mA
		ADJ1 = HI, ADJ0 = LO	 ●	**TBD** **TBD**	51.5	**TBD** **TBD**	mA mA
		ADJ1 = LO, ADJ0 = HI	 ●	**TBD** **TBD**	38	**TBD** **TBD**	mA mA
		ADJ1 = LO, ADJ0 = LO	 ●	**TBD** **TBD**	24.5	**TBD** **TBD**	mA mA
$I_{VCCO\_SHUTDOWN}$	Output Supply Current	PWRMD = OMUX = LO	 ●	**TBD** **TBD**	0.1	**TBD** **TBD**	mA mA
I_S	Total Supply Current ($I_{S(VCCI)}$ + $I_{S(VCCO)}$)	ADJ1 = HI, ADJ0 = HI	 ●	**TBD** **TBD**	98.5	**TBD** **TBD**	mA mA
		ADJ1 = HI, ADJ0 = LO	 ●	**TBD** **TBD**	85.5	**TBD** **TBD**	mA mA
		ADJ1 = LO, ADJ0 = HI	 ●	**TBD** **TBD**	72	**TBD** **TBD**	mA mA
		ADJ1 = LO, ADJ0 = LO	 ●	**TBD** **TBD**	58.5	**TBD** **TBD**	mA mA
$I_{S\_SHUTDOWN}$	Total Supply Current ($I_{S(VCCI)}$ + $I_{S(VCCO)}$)	PWRMD = OMUX = LO	 ●	**TBD** **TBD**	3.9	**TBD** **TBD**	mA mA
PSRR(V_{CCI})	Input Power Supply Rejection Ratio	V_{CCI} = 3.15V to 3.45V, V_{CCO} = 3.3V	 ●	**TBD** **TBD**	36		dB dB
PSRR(V_{CCO})	Output Power Supply Rejection Ratio	V_{CCO} = 3.15V to 3.45V, V_{CCI} = 3.3V	 ●	**TBD** **TBD**	38		dB dB

DC ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

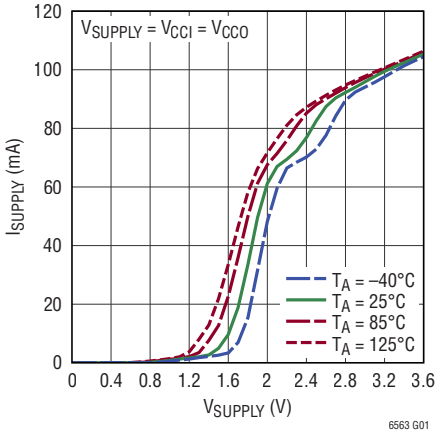
Note 2: The LTC6563I is guaranteed to meet specified performance from –40°C to 85°C.

Note 3: The LTC6563H is guaranteed to meet specified performance from –40°C to 125°C.

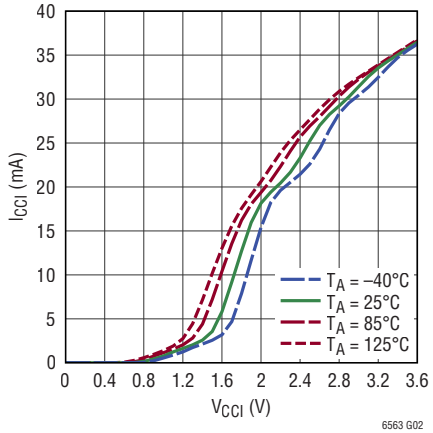
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 0.9V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$) /2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential.

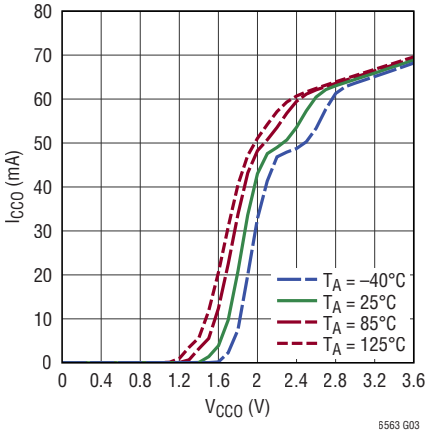
I_{SUPPLY} vs V_{SUPPLY} Over Temperature



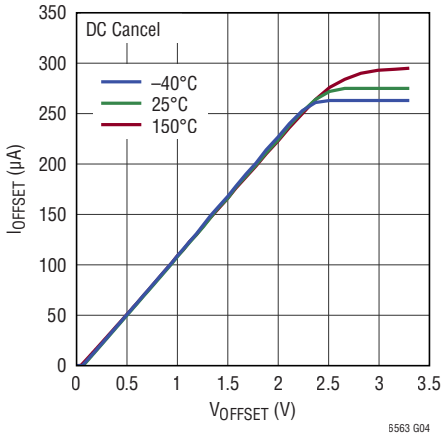
I_{CCI} vs V_{CCI} Over Temperature



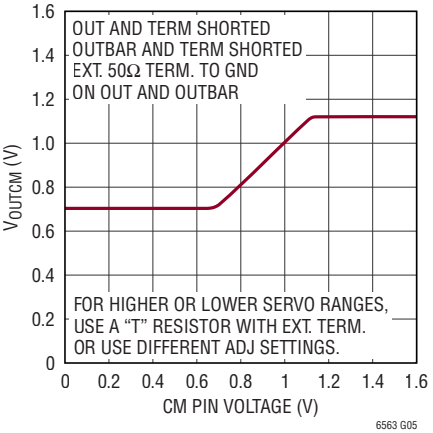
I_{CCO} vs V_{CCO} Over Temperature



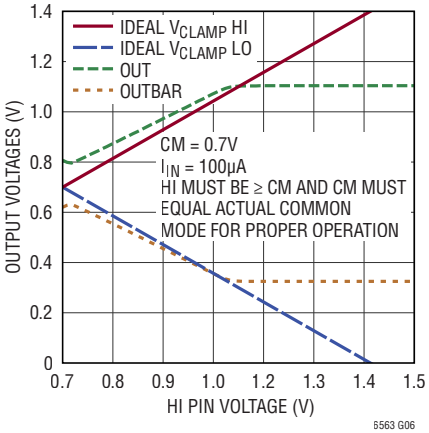
I_{OFFSET} vs V_{OFFSET}



Output Common Mode Control



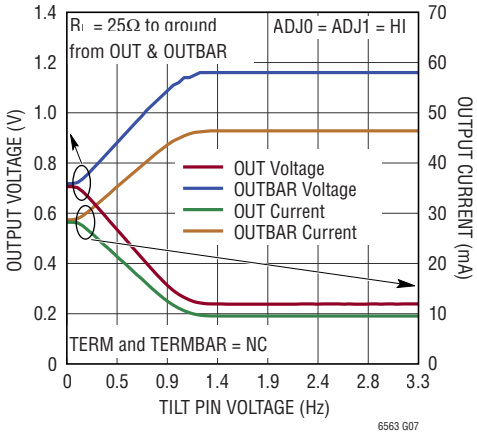
Output Clamps



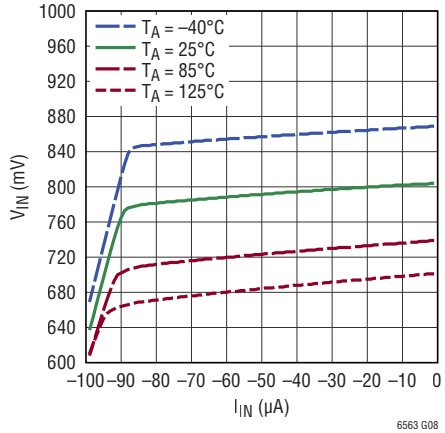
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 0.9V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$) /2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential.

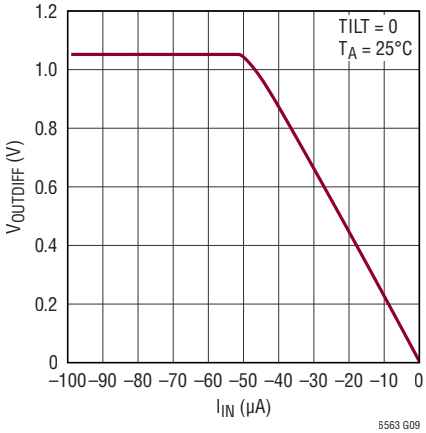
Output Tilt Control



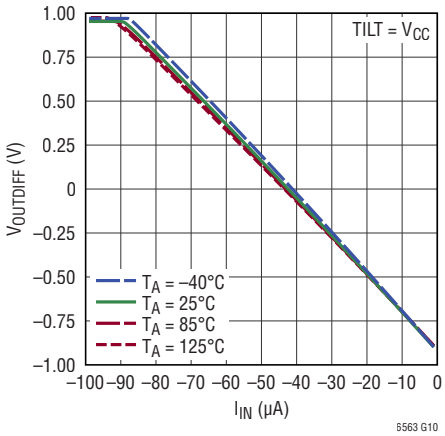
V_{IN} vs I_{IN} Over Temperature



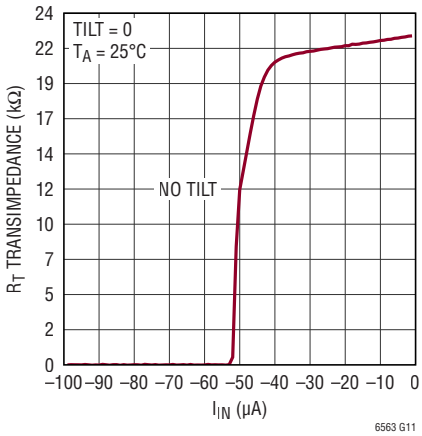
$V_{OUTDIFF}$ vs I_{IN}



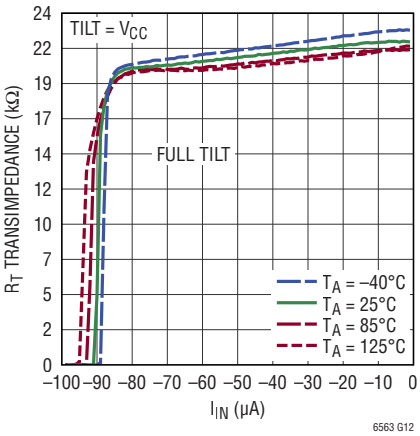
$V_{OUTDIFF}$ vs I_{IN} Over Temperature



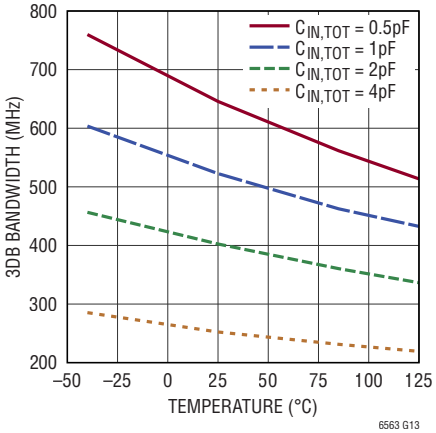
R_T Transimpedance vs I_{IN}



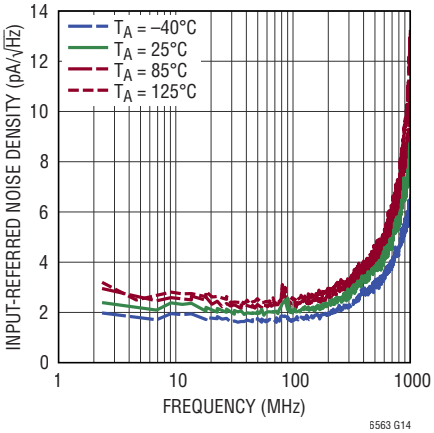
R_T Transimpedance vs I_{IN} Over Temperature



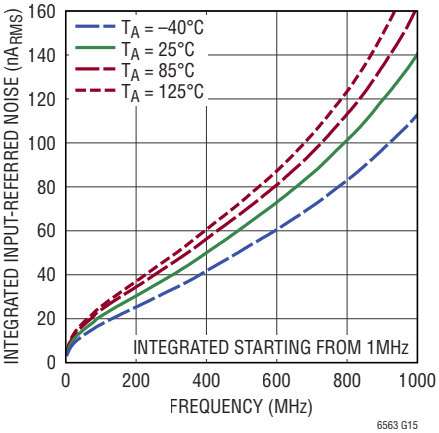
3dB Bandwidth vs Temperature Over $C_{IN,TOT}$



Input-Referred Noise Density with $C_{IN,TOT}$ = 0.5pF



Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 0.5pF

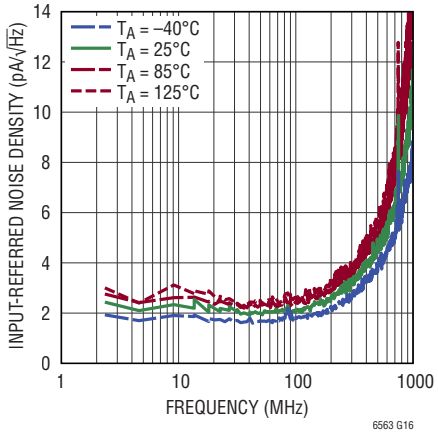


Rev PrB

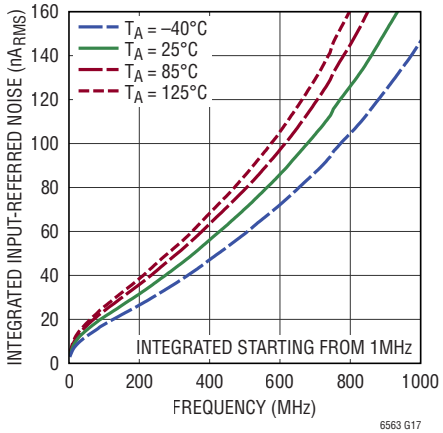
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 0.9V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$) /2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential.

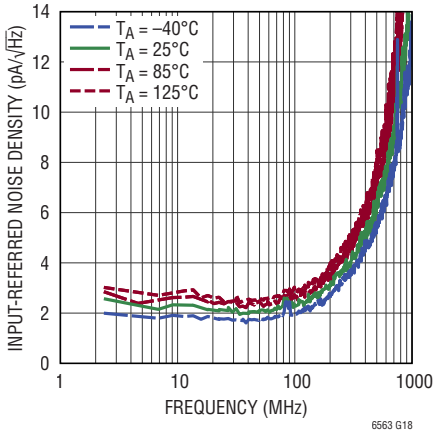
Input-Referred Noise Density with $C_{IN,TOT}$ = 1.0pF



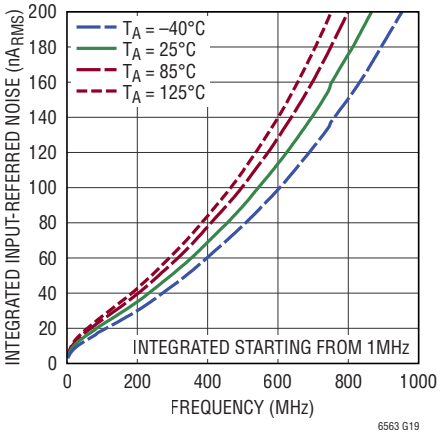
Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 1.0pF



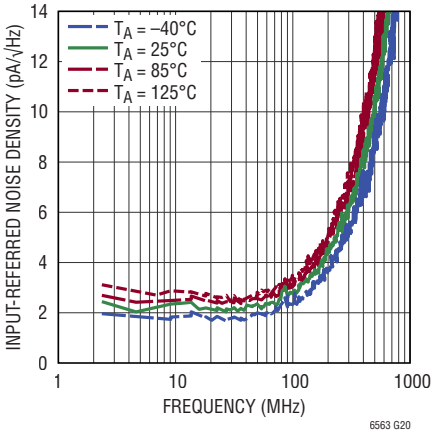
Input-Referred Noise Density with $C_{IN,TOT}$ = 2.0pF



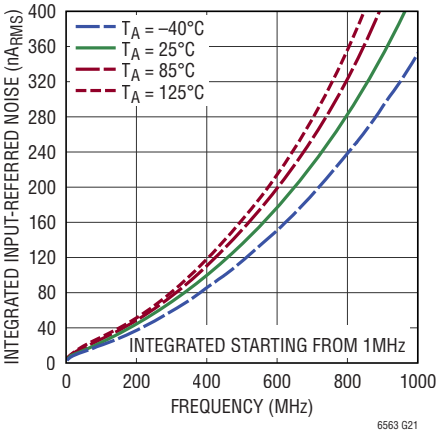
Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 2.0pF



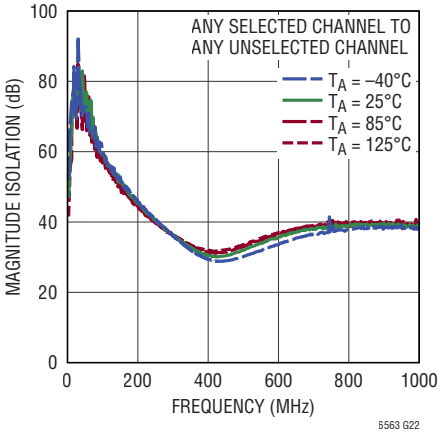
Input-Referred Noise Density with $C_{IN,TOT}$ = 4.0pF



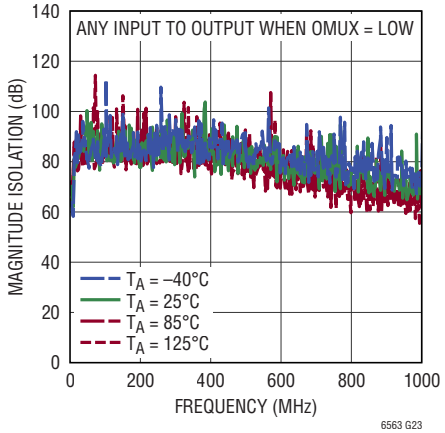
Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 4.0pF



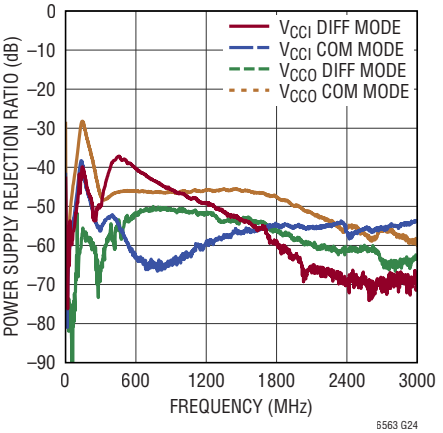
Channel to Channel Isolation vs Frequency Over Temperature



OMUX Isolation vs Frequency Over Temperature



PSRR Out to V_{CCI}, V_{CCO}

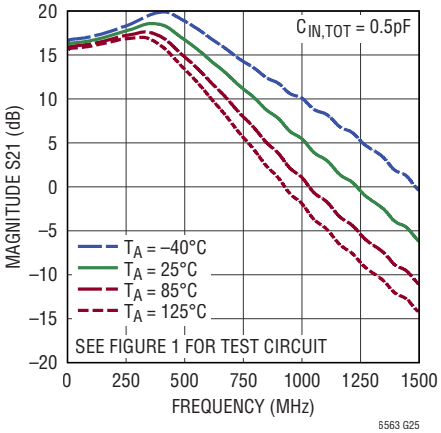


Rev PrB

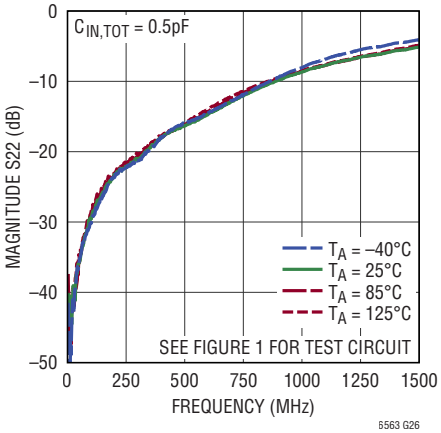
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 0.9V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$) /2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential using 2kΩ for input V to I conversion.

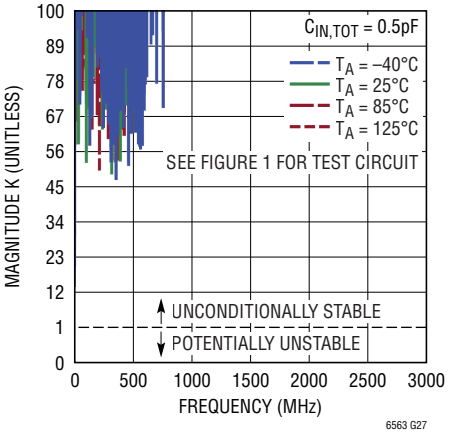
S21ds (Gain) vs Frequency Over Temperature



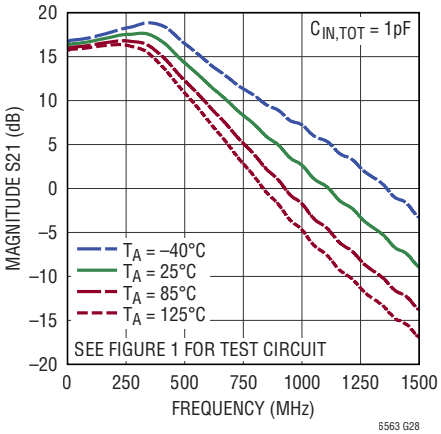
S22dd vs Frequency Over Temperature



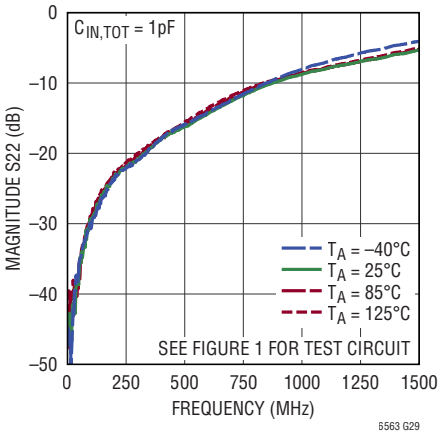
Stability Factor K vs Frequency Over Temperature



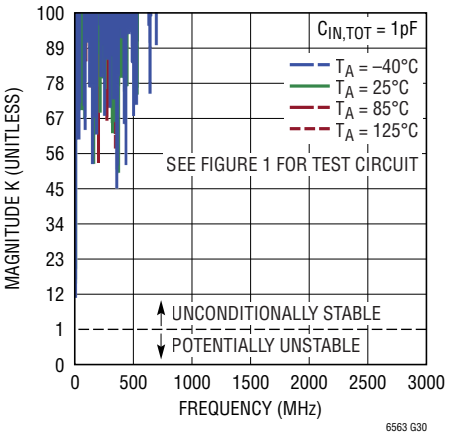
S21ds (Gain) vs Frequency Over Temperature



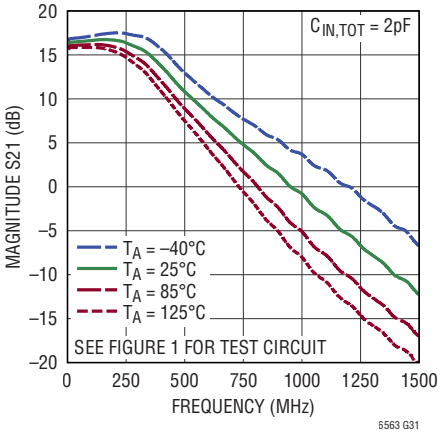
S22dd vs Frequency Over Temperature



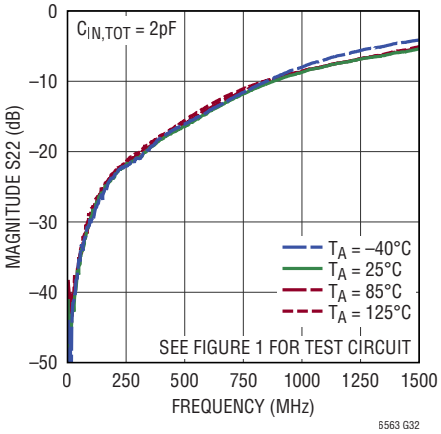
Stability Factor K vs Frequency Over Temperature



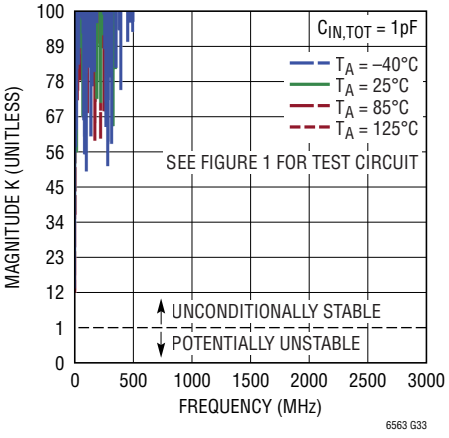
S21ds (Gain) vs Frequency Over Temperature



S22dd vs Frequency Over Temperature



Stability Factor K vs Frequency Over Temperature

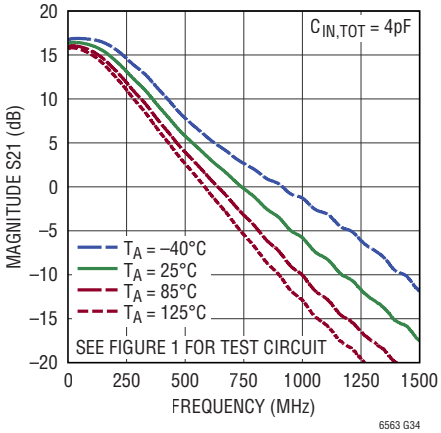


Rev PrB

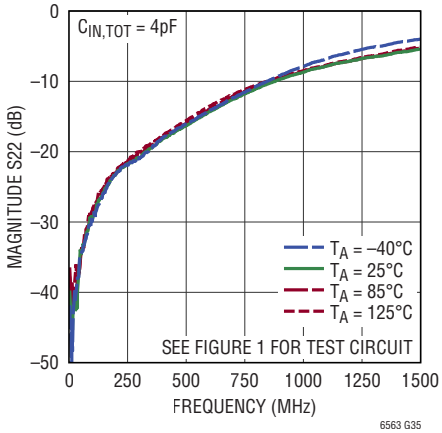
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V_{CCI} = V_{CCO} = 3.3V, and CM = 0.9V. V_{OUTCM} is defined as (OUT + $\overline{OUT}$) /2 and $V_{OUTDIFF}$ is defined as (OUT – $\overline{OUT}$), R_L = 50Ω differential using 2kΩ for input V to I conversion.

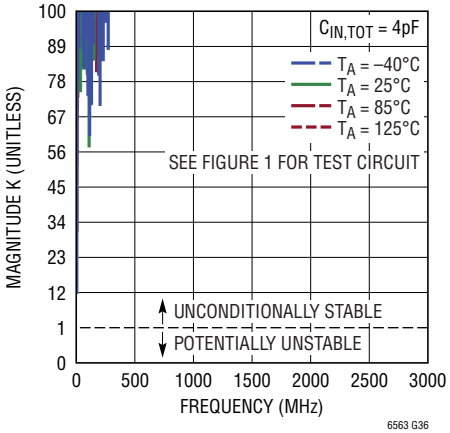
S21ds (Gain) vs Frequency Over Temperature



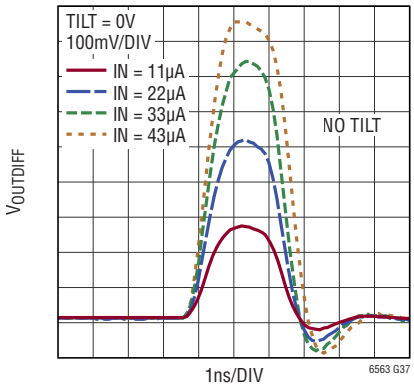
S22dd vs Frequency Over Temperature



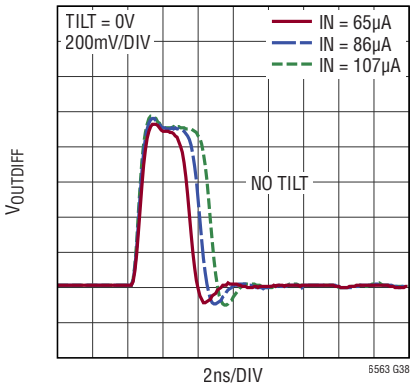
Stability Factor K vs Frequency Over Temperature



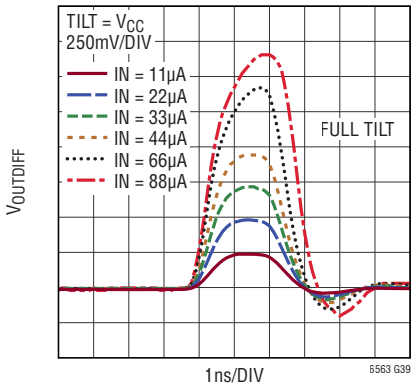
Pulse Response Linear Range C_{IN} = 1pF



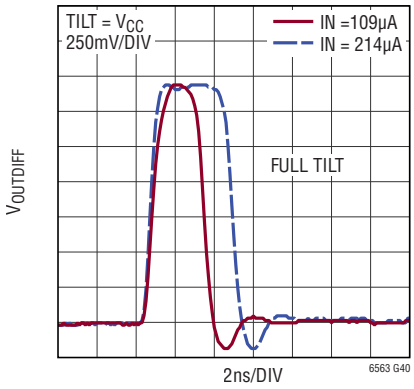
Pulse Response Overload Range C_{IN} = 1pF



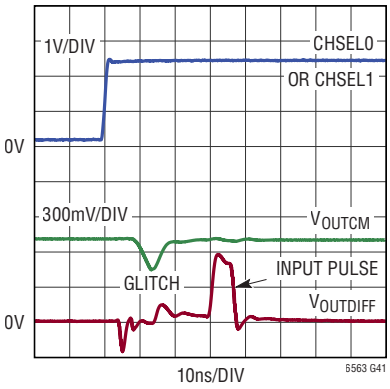
Pulse Response Linear Range C_{IN} = 1pF



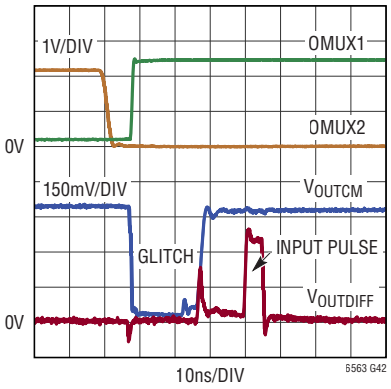
Pulse Response Overload Range C_{IN} = 1pF



Channel Select Switching Glitch



OMUX Switching Glitch



Rev PrB

TYPICAL PERFORMANCE CHARACTERISTICS

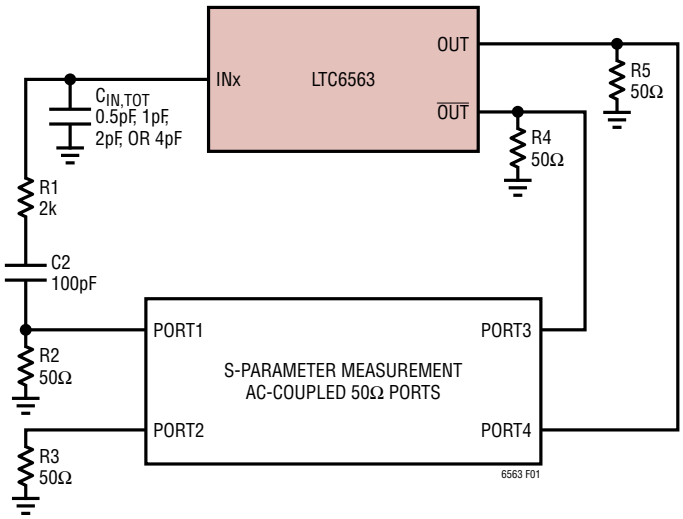


Figure 1. S-Parameters Test Circuit

PIN FUNCTIONS

GND (Pins 1, 3, 18, 20, Exposed Pad Pin 25): Negative Power Supply. Normally tied to ground. All GND pins and the exposed pad must be tied to the same voltage. The exposed pad (pin 25) should have multiple via holes to the underlying ground plane for low inductance and good heat transfer.

IN4, IN1, IN2, IN3 (Pins 2, 19, 21, 24,): Input pins for the transimpedance amplifier for channels 4, 1, 2, and 3 respectively. The active channel is internally biased to 0.8V. See the Applications Information section for specific recommendation.

PWRMD (Pin 4): Power mode is a CMOS input for controlling the power consumption. The PWRMD pin has a 218k internal pull-up resistor to V_{CCI}. Default value is 3.3V.

V_{CCI} (Pin 5): Positive power supply for the input stages. Typically, 3.3V. A series ferrite bead such as the MPZ1005A331ETD25 should be used and bypass capacitor of 680pF and 0.1µF should be placed as close to the part as possible between V_{CCI} and ground.

OMUX (Pin 6): Output MUX is a CMOS input for controlling the output multiplexing function. The OMUX pin has internal 218k pull-up resistor to V_{CCI}. Default value is 3.3V.

CM (Pin 7): Output Common Mode Reference Voltage. The voltage on this pin sets the output common mode voltage level. On a 3.3V supply, the CM pin floats to a default 0.9V. The CM pin has an input impedance of 16.3kΩ. The CM pin should be bypassed with a high-quality ceramic capacitor of at least 0.01µF.

HI (Pin 8): High Side Clamp Voltage. The voltage applied to the HI pin sets the upper voltage limit to OUT and $\overline{OUT}$ pins. The HI voltage also limits the lower voltage swing on both output pins to "$2V_{CM}$ - HI", for symmetrical clamping around the CM voltage. On a 3.3V supply, the HI pin will float to a default 1.8V. The HI pin has an input impedance of 13.7kΩ. The HI pin should be bypassed with a high-quality ceramic capacitor of at least 0.01µF.

$\overline{OUT}$, OUT (Pins 9, 12): Differential Output Pins. For voltage mode output, connect $\overline{OUT}$ to $\overline{TERM}$ and OUT to TERM. For current mode output or when using external load resistors, float $\overline{TERM}$ and TERM.

$\overline{TERM}$, TERM (Pins 10, 11): Internal Termination. These pins have 50Ω load resistors coupled to GND and are intended to connect to the differential output pins.

CHSEL1, CHSEL0 (Pins 13, 15): MSB and LSB for Channel Selection. These pins are CMOS inputs with internal 218k pull-down resistors to GND.

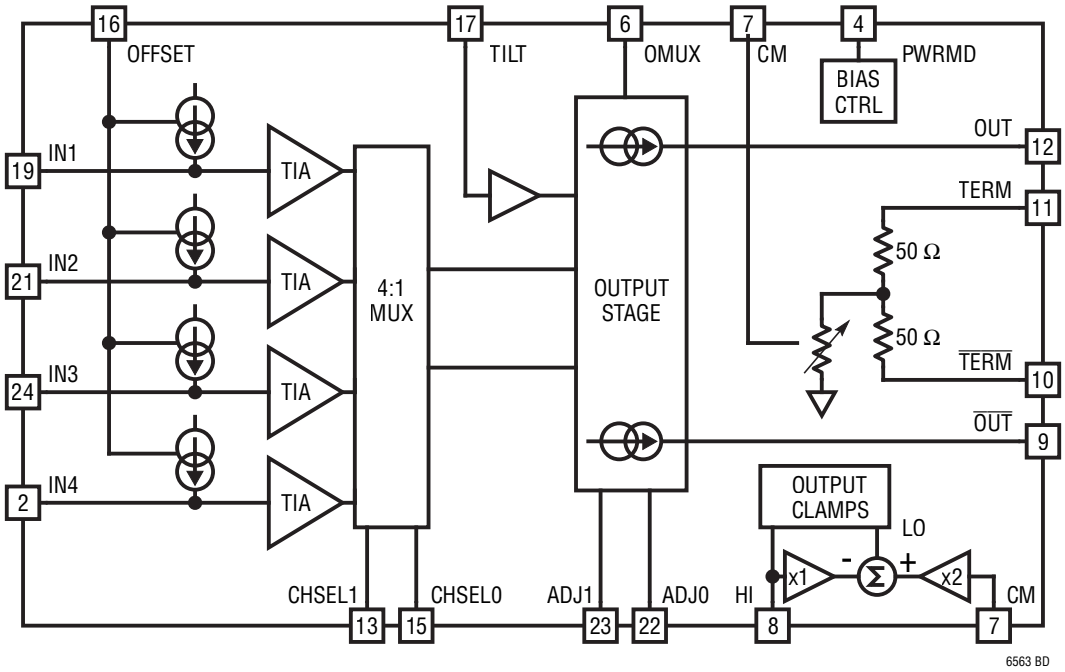
V_{CCO} (Pin 14): Positive power supply for the output stage. Typically, 3.3V. V_{CCO} can be tied to V_{CCI} for single supply operation. A series ferrite bead such as the MPZ1005A331ETD25 should be used and bypass capacitors of 680pF and 0.1µF should be placed as close as possible between V_{CCO} and ground.

OFFSET (Pin 16): Input Offset Adjust. A voltage controlled current source that can be used to cancel DC current at the input pins. The OFFSET pin has an internal pull-down resistor to GND.

TILT (Pin 17): Output Differential Offset. The voltage on this pin controls the outputs' differential offset. The TILT pin has an internal 218k pull-down resistor to GND.

ADJ0, ADJ1 (Pins 22, 23): LSB and MSB for Output Gain and Current Adjusts. The adjust pins set the output stage quiescent current and current gain. See Application Section to optimize the ADC interface. These pins are CMOS inputs with internal 218k pull-down resistors to GND.

BLOCK DIAGRAM



OPERATION

The LTC6563 is a four channel transimpedance amplifier with an integrated 4-to-1 multiplexer and ADC driver stage. Each of the transimpedance amplifiers converts an input current to an output voltage. The integrated multiplexer simplifies the system design while saving space and power. In addition, the output multiplexer capabilities (OMUX) allows multiple 4-channel LTC6563 devices to be combined. 8,12,16 … 32 input channels are easily multiplexed into a single differential output.

The LTC6563 is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). OUT and $\overline{OUT}$ can swing almost from ground to about V_{CCO} – 1V. The LTC6563 provides four modes of output drive for matching input swing of high-speed ADCs. The tilt feature allows the output stage to offset to take advantage of the full differential input range of the ADCs. The outputs have programmable clamps that limit the output swing in saturation events. These clamps provide protection to the front end of the ADC. The HI pin sets the maximum swing, while a symmetric minimum swing limit is set up internally. In typical LIDAR applications, the LTC6563 amplifies the output current of an APD. APD are biased near breakdown to achieve high current gain. Under intense optical illumination, they can conduct large currents, often in excess of 1A. The LTC6563 survives and quickly recovers from large overload currents of this magnitude. During recover, any TIA is blinded from subsequent pulses. The LTC6563 recovers from 1mA saturation events in less than 15ns without phase reversal, minimizing this form of data loss. As the level of input current exceeds the linear range, the output pulse width will widen. However, the recovery time remains in the 10's of ns.

Ambient light is problematic for LIDAR receiver chains. The DC current can easily saturate the linear range of any TIA. The LTC6563 provides a control for DC cancelation to the inputs and can cancel up to 200µA of DC current. The DC cancelation is designed to minimizing additive noise.

APPLICATIONS INFORMATION

Output Offset and Current Control

The output stage of the LTC6563 has many options. The ADJ1 and ADJ0 pins provide four options for the output current drive. The output voltage swing is dependent on the adjust setting, the termination resistor, and the Tilt input. The purpose of the Tilt input is to offset the output stage increasing the output swing of the TIA for unipolar inputs. Output TILT is essential for the ADC as the input from the photodetector is unipolar. To maximize the input swing of the ADC, the resting position of V_{OUT} is offset low while the $\overline{OUT}$ resting position is offset high. This allows the LTC6563 to maximize the full dynamic range of the ADC. These pins should be connected to low noise inputs.

APPLICATIONS INFORMATION

Table 1. Output Stage when Tilt Pin = 0V

I_{IN} (µA)	ADJ1	ADJ0	OUT (mA)	OUT_{BAR} (mA)	RT (Ω) RL_{DIFF} = 50Ω	RT (Ω) RL_{DIFF} = 66.7Ω	RT (Ω) RL_{DIFF} = 100Ω	RT (Ω) RL_{DIFF} = 200Ω
0	0	0	7	7	5.55k	7.4k	11.1k	22.2k
	0	1	14	14	11.1k	14.8k	22.2k	44.4k
	1	0	21	21	16.65k	22.2k	33.3k	66.6k
	1	1	28	28	22.2k	29.6k	44.4k	88.8k
45	0	0	12	2	5.55k	7.4k	11.1k	22.2k
	0	1	24	4	11.1k	14.8k	22.2k	44.4k
	1	0	36	6	16.65k	22.2k	33.3k	66.6k
	1	1	48	8	22.2k	29.6k	44.4k	88.8k

Table 2. Output Stage when Tilt Pin = V_{CC}

I_{IN} (µA)	ADJ1	ADJ0	OUT (mA)	OUT_{BAR} (mA)	RT (Ω) RL_{DIFF} = 50Ω	RT (Ω) RL_{DIFF} = 66.7Ω	RT (Ω) RL_{DIFF} = 100Ω	RT (Ω) RL_{DIFF} = 200Ω
0	0	0	2	12	5.55k	7.4k	11.1k	22.2k
	0	1	4	24	11.1k	14.8k	22.2k	44.4k
	1	0	6	36	16.65k	22.2k	33.3k	66.6k
	1	1	8	48	22.2k	29.6k	44.4k	88.8k
90	0	0	12	2	5.55k	7.4k	11.1k	22.2k
	0	1	24	4	11.1k	14.8k	22.2k	44.4k
	1	0	36	6	16.65k	22.2k	33.3k	66.6k
	1	1	48	8	22.2k	29.6k	44.4k	88.8k

LTC6563 transimpedance gain (RT) consists of the overall gain from the multi-stages involved in producing the output for a given input current. The output is differential and ½ RT is achieved if only one of the outputs is utilized.

It is possible to change the Transimpedance Gain (RT) by changing the total differential load (RLdiff) as shown in the tables above. Also, since the ADJ pins respond in less than 100ns, these pins can be used for "on the fly" gain switching if the application needs that. An example would be to reduce the TIA gain if an overly strong signal is received by the LTC6563. It's important to note the following regarding gain adjustment:

- The linear input current range (45uA) is not affected by these changes.
- RLdiff refers to the total load "seen" by the differential output(s). Refer to Figure 6-8 to see examples of various total load (50Ω, 75Ω, and 100Ω) illustrated.
- Increasing RLdiff reduces the signal bandwidth.

APPLICATIONS INFORMATION

Table 3. Output Stage when Tilt Pin = V_{CC}

I_{IN} (µA)	ADJ1	ADJ0	OUT (mA)	$\overline{OUT}$ (mA)	R_{TDIFF} (Ω) FOR R_L (Ω)
0	0	0	2	12	20k for 200
	0	1	4	24	20k for 150
	1	0	6	36	20k for 100
	1	1	8	48	20k for 50
90	1	0	12	2	20k for 200
	0	0	24	4	20k for 150
	0	1	36	6	20k for 100
	1	1	48	8	20k for 50

Power Considerations

The LTC6563 has many power modes of operation. The state of the PWRMD, OMUX and ADJ pins will dictate the amount of current the LTC6563 will draw. Multiple power modes are offered to allow the user to minimize switching times and power dissipation, while maximizing channel isolation.

Coupling the TIA Input – AC vs DC

Although the LTC6563 can AC-couple to the detector, best performance is achieved when DC-coupled to a negatively biased APD. DC-coupling reduces component count while allowing a DC current path from the APD. The LTC6563 OFFSET feature is designed to cancel DC currents. The maximum performance for switching speeds and saturation recovery occurs in this DC-coupled configuration.

When AC-coupling to the TIA input, R_B, is needed to establish a bias point for the detector. It is worth noting that R_B is a parallel path with the TIA for the APD current to flow through and it will impact the effective signal chain output gain.

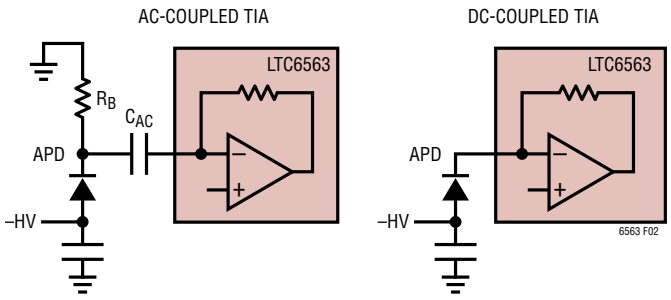


Figure 2. AC-Coupled Detector Circuit

This value of the biasing resistor and AC-coupling capacitor, C_{AC}, can potentially create a long time-constant. C_{AC} is chosen based on the reactance at the frequency of interest. However, R_B ideally should be large to avoid stealing current from the TIA path from APD signal. On one hand large R_B causes large RC time constants, while low R_B reduces the effective gain of the APD.

Another negative impact of this RC network is in the case for saturation events. When a large signal is received from

Table 3. LTC6563 Power Dissipation Modes. X = don't care

PWRMD	OMUX	ADJ1	ADJ0	I_{CCI} (mA)	I_{CCO} (mA)	I_{TOTAL} (mA)	Description
0	0	X	X	3.8	0.1	3.9	LTC6563 shutdown.
0	1	0	0	21	24.5	45.5	LTC6563 enabled, non-selected inputs powered down, <500ns channel switching time, channel to channel isolation > –60dB.
0	1	0	1	21	38	59	
0	1	1	0	21	51.5	72.5	
0	1	1	1	21	64.5	85.5	
1	0	X	X	35	0.1	35.1	LTC6563 deselected (outputs stage off), non-selected inputs powered up.
1	1	0	0	34	24.5	58.5	LTC6563 enabled, non-selected inputs powered up, <10ns channel switching time, channel to channel isolation > 35dB.
1	1	0	1	34	38	72	
1	1	1	0	34	51.5	85.5	
1	1	1	1	34	64.5	98.5	

APPLICATIONS INFORMATION

the APD, this event will charge C_{AC}. This will negatively move the input bias of the TIAs and change the TIAs input impedance to transimpedance 14kΩ. This 14kΩ coupled with R_B and C_{AC} time constant will add the saturation recover time. Practical values of 100pF C_{AC} and R_B of 2.2kΩ will have large saturation recovery times >1µs with >50mA input signals. This effectively blinds the signal chain for the next input signal.

Channel switching times are also compromised when AC-coupling. The impressive LTC6563 switching time of <50ns will be increased to >1µs with practical values of R_B and C_{IN}.

Channel Selection

There are four TIA inputs to the LTC6563. The active channel is selected using two channel selection bits CHSEL0 and CHSEL1. When a channel is changed and PWRMD is high, an output glitch takes <10ns to settle. When PWRMD is low and a channel is changed, an output glitch takes <500ns to settle. Inactive channels have 35dB of channel to channel isolation when PWRMD pin is high. When PWRMD is low the channel isolation is increased to more than 60dB.

Table 4. Channel Selection

CHSEL1	CHSEL0	OMUX	ACTIVE Channel
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4
X	X	0	High Z

DC Input Cancelation

The LTC6563 features a voltage controlled current source for DC input current cancelation with minimal noise impact. Identical currents are applied to each TIA input. The maximum current cancelation is 200µA. The OFFSET pin was designed to accommodate external closed loop design for fast settling and fast switching times. See V_{OFFSET} vs I_{OFFSET} curve for the transfer function. It is recommended to use a high-speed DAC to control the OFFSET pin.

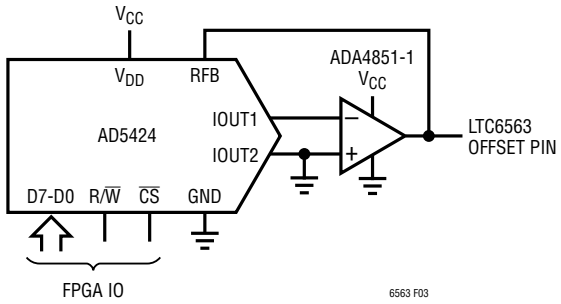


Figure 3. Recommended DC Cancel Circuit

Output MUXing

Refer to Figure 4 schematic. The output multiplexing (OMUX) requires at least one additional LTC6563 devices to operate in a controller / responder relationship. To multiplex multiple LTC6563's they need to share a DC connection at their outputs. The controller LTC6563 (U1) output stage needs to be connected to the internal termination resistors. For the CM control to function, the controller PWRMD pin must remain HIGH during the time any of the inputs of all the parallel network are enabled. That is because the CM servo loop is disabled if PWRMD is deasserted (low). The controller LTC6563 output circuit (U1) will control the common mode for all the multiplexing. All CM pins (U1-U4) are to be connected to the common mode of the ADC. If the output clamping feature (HI pin) is implemented, all CM pins (U1-U4) need to be connected to the same voltage for proper operation. Also, tie all HI pins (U1-U4) together and apply the required clamping voltage to them. The HI pin is used to set the high side clamp voltage at outputs. Internal circuity generates a symmetric low side clamp voltage with respect to the common mode voltage V_{CM}.

Maximum output high side voltage = HI pin voltage

Minimum output low side voltage = $V_{CM} – (HI – V_{CM}) = 2V_{CM}$ - HI

TYPICAL APPLICATIONS

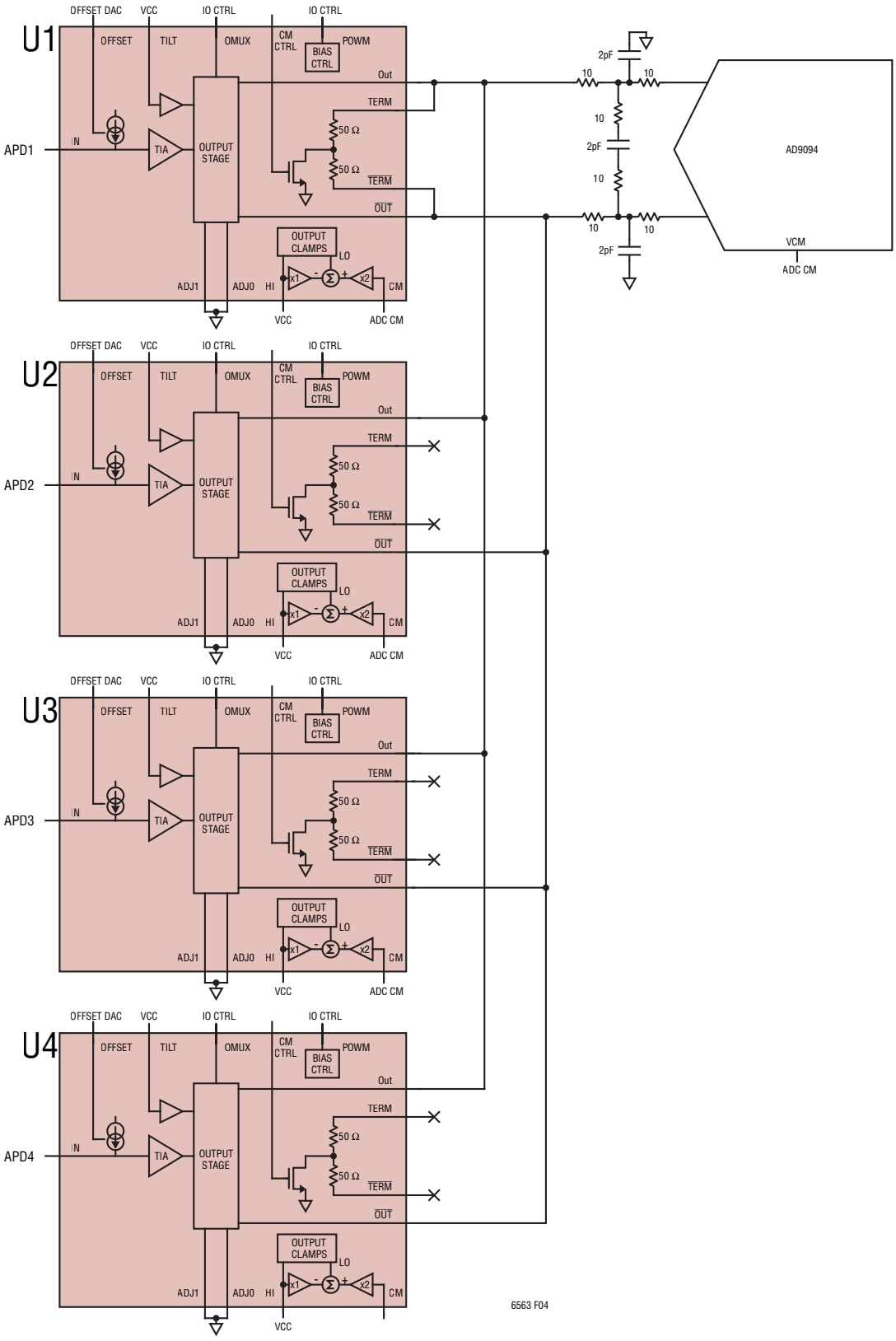
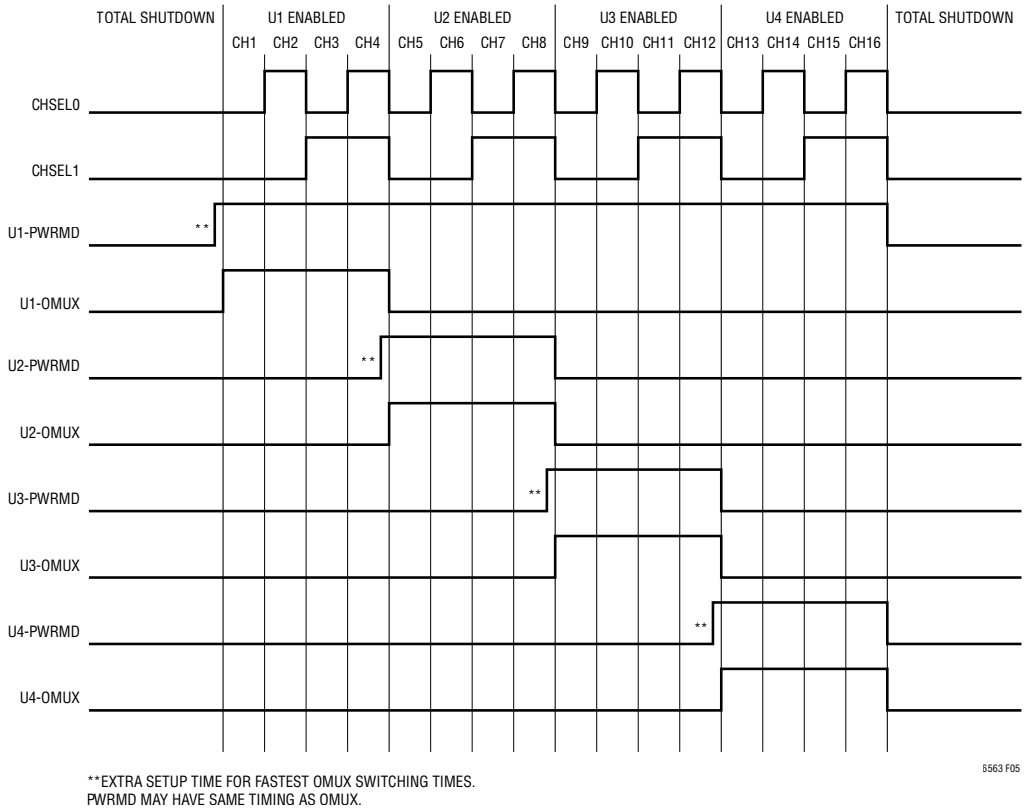


Figure 4. Typical Application with Multiplexed Outputs

TYPICAL APPLICATIONS



**EXTRA SETUP TIME FOR FASTEST OMUX SWITCHING TIMES.
PWRMD MAY HAVE SAME TIMING AS OMUX.

Figure 5. Timing Diagram for OMUX and Channel Control

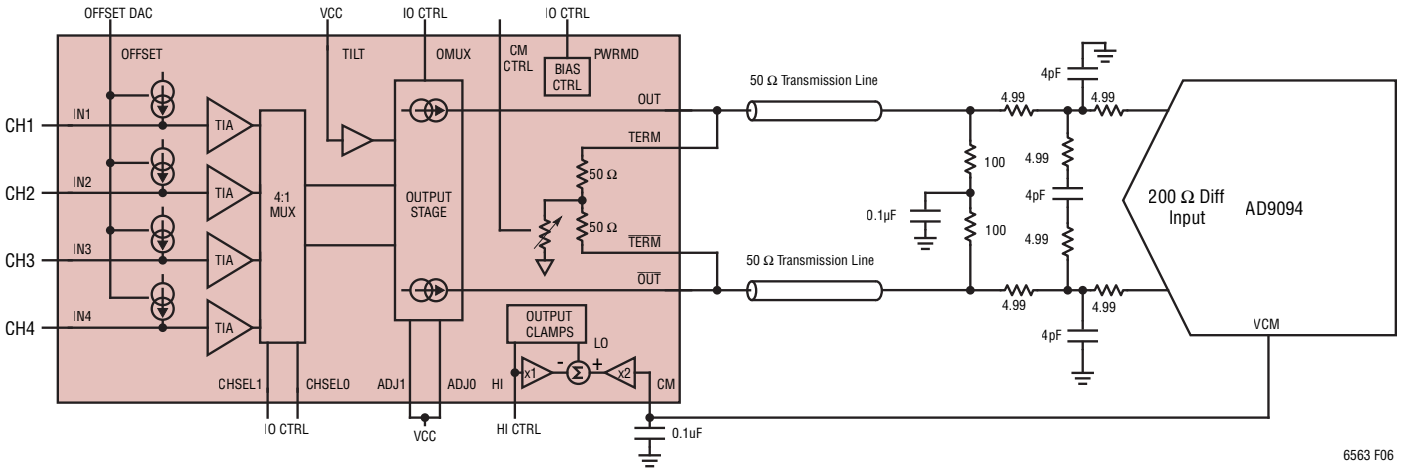


Figure 6. LTC6563 50Ω Transmission Line Circuit

TYPICAL APPLICATIONS

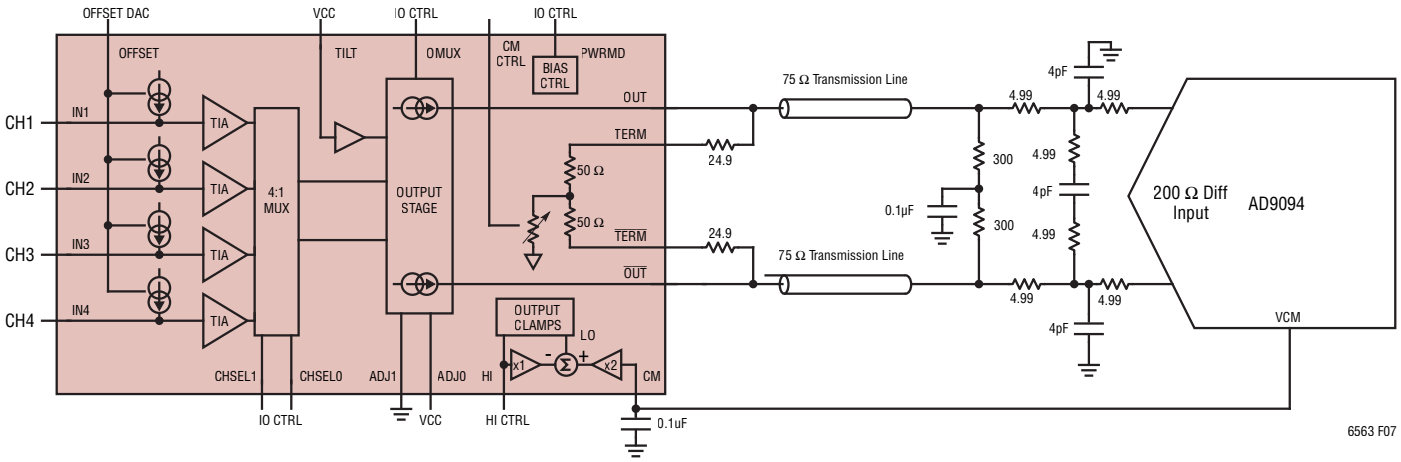


Figure 7. LTC6563 75Ω Transmission Line Circuit

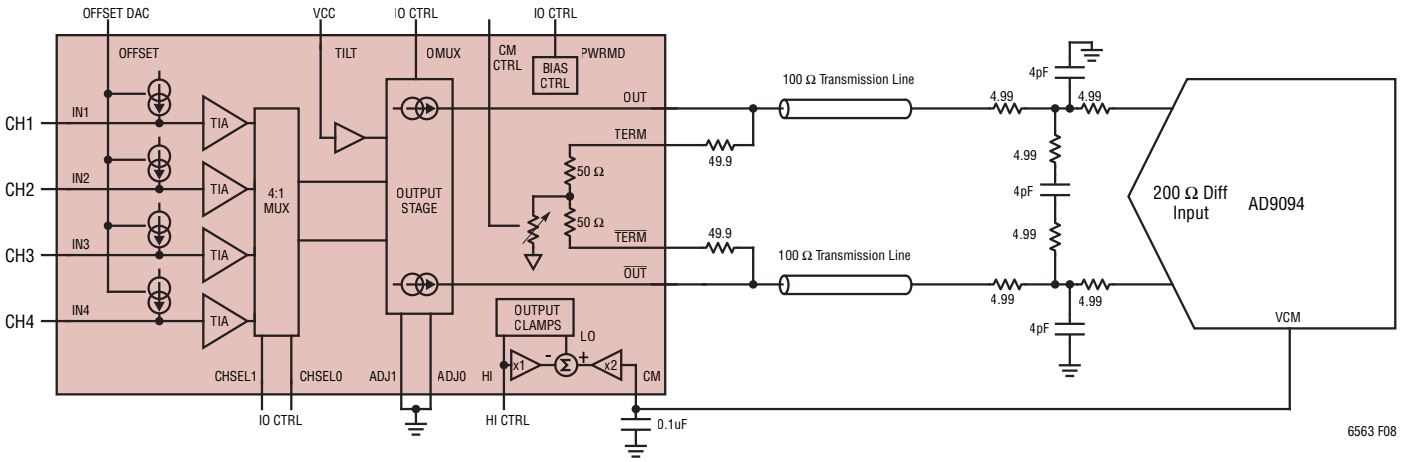
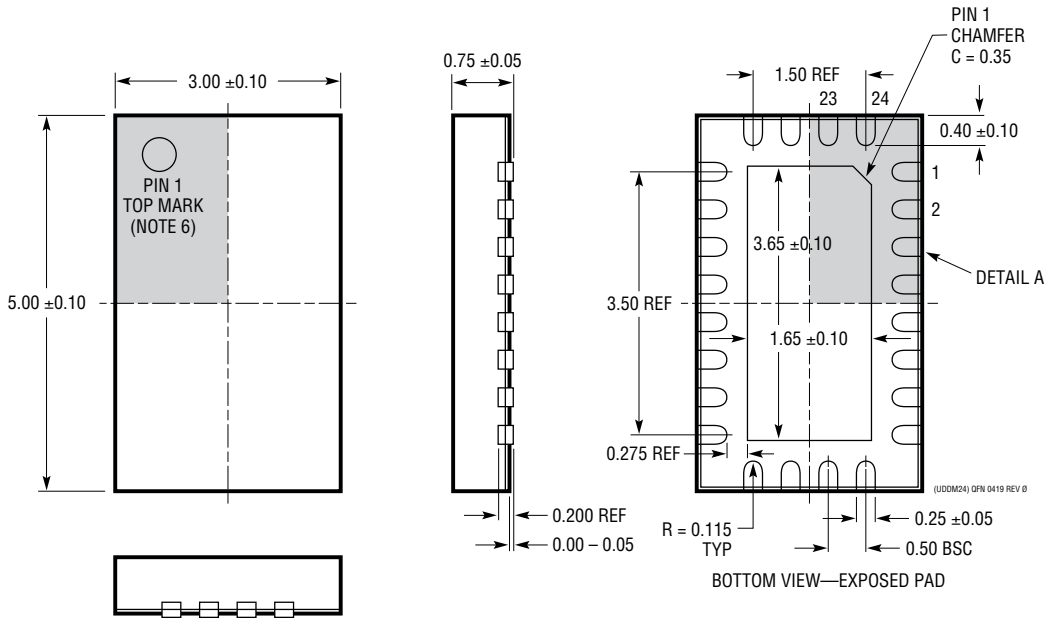
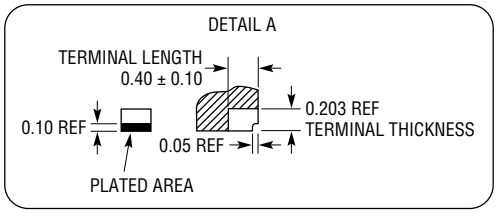


Figure 8. LTC6563 100Ω Transmission Line Circuit

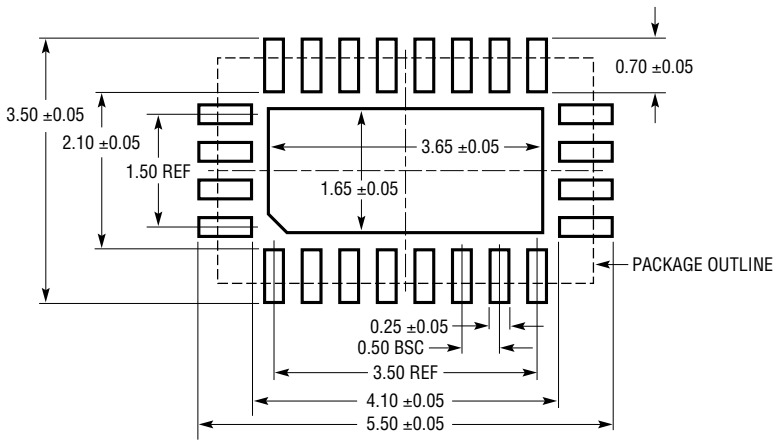
PACKAGE DESCRIPTION

UDDM Package
24-Lead Plastic Side Solderable QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1795 Rev Ø)





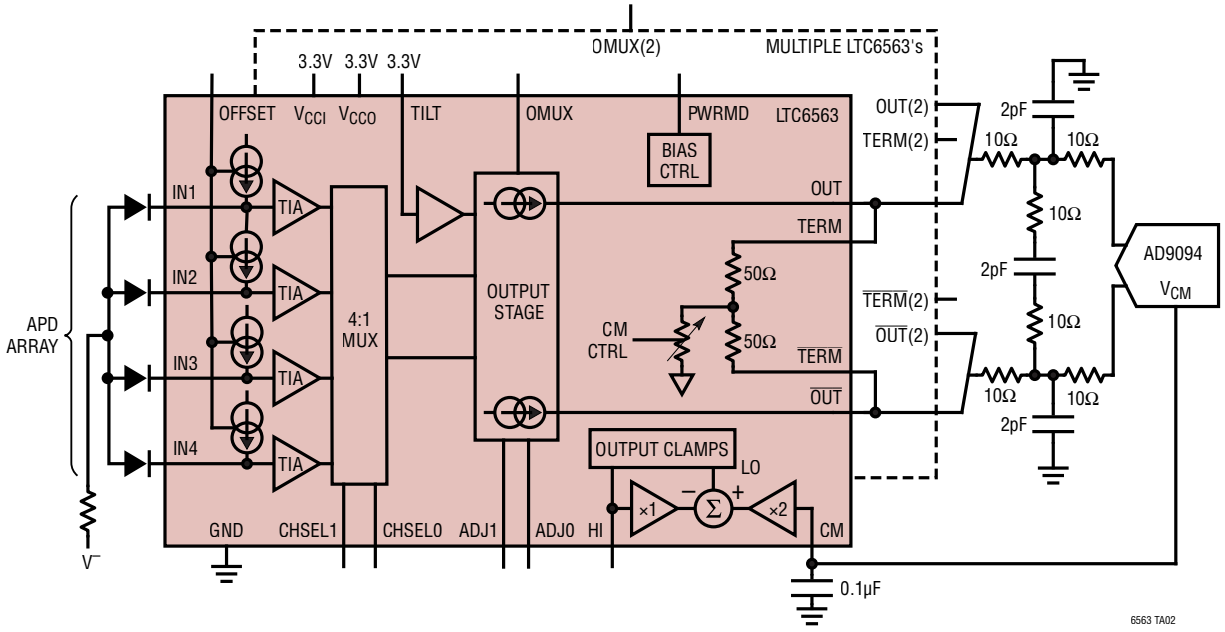
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION

Typical Application with DC-Coupled Inputs Driving an ADC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6560	1-Channel Transimpedance Amp with Output Muxing	220MHz, 74kΩ Transimpedance S/E Output
LTC6561	4-Channel Transimpedance Amp with Output Muxing	220MHz, 74kΩ Transimpedance S/E Output
AD8465	Single-Supply LVDS Comparator	1.6ns Propagation Delay
ADCMP604	Single-Supply LVDS Comparator	1.6ns Propagation Delay
LTC6754	High Speed Rail-to-Rail Input Comparator with LVDS Compatible Outputs	1.8ns Propagation Delay
LTC6752	280MHz Comparator	2.9ns Propagation Delay
LTC6268	500MHz Ultra Low Bias Current FET Input Op Amp	GBW = 500MHz, –3dB BW = 350MHz, I_b = ±3FA
LTC6268-10	4GHz Ultra Low Bias Current FET Input Op Amp	De-Comped Version of the LTC6268, GBW = 4GHz
LTC6409	10GHz Bandwidth, 1.1nV/√Hz Differential Amplifier/ADC Driver	GBW = 10GHz, e_n = 1.1nV/√Hz
AD9094	8-Bit, 1 GSPS, JESD204B, Quad Analog-to-Digital Converter	4x JESD204B
AD9694	Quad 14-Bit, 500Msps, 1.2V/2.5V ADC	4x JESD204B
LT8331	Low I_Q Boost/SEPIC/Flyback/Inverting Converter	0.5A, 140V Switch
LT8365	Low I_Q Boost/SEPIC/Inverting Converter	1.5A, 150V Switch