TPS65014 Power- and Battery-Management IC for Li-Ion Powered Systems

1 Features

- Linear Charger Management for Single Li-Ion or Li-Polymer Cells
- Dual Input Ports for Charging From USB or From Wall Plug, Handles 100-mA and 500-mA USB Requirements
- Charge Current Programmable Through External Resistor
- 1-A, 95% Efficient Step-Down Converter for I/O and Peripheral Components (VMAIN)
- 400-mA, 90% Efficient Step-Down Converter for Processor Core (VCORE)
- 2× 200-mA LDOs for I/O and Peripheral Components, LDO Enable Through Bus
- Serial Interface Compatible With I^2C, Supports 100-kHz, 400-kHz Operation
- LOW_PWR Pin to Lower or Disable Processor Core Supply Voltage in Deep-Sleep Mode
- 70-µA Quiescent Current
- 1% Reference Voltage
- Thermal-Shutdown Protection

2 Applications

- All Single Li-Ion Cell-Operated Products Requiring Multiple Supplies Including:
  - PDAs
  - Cellular and Smart Phones
  - Internet Audio Players
  - Digital Still Cameras
- Digital Radio Players
- Split-Supply DSP and µP Solutions

3 Description

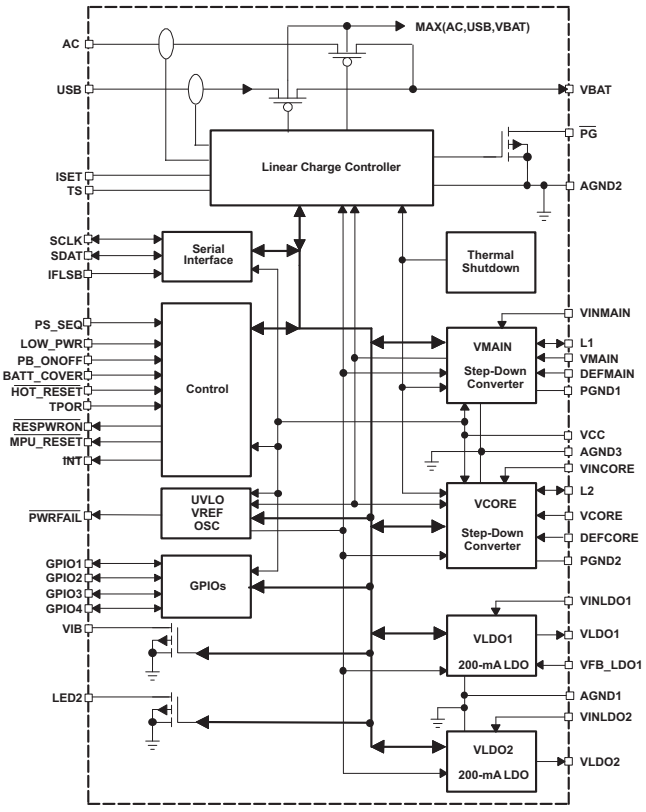
The TPS65014 device is an integrated power- and battery-management IC for applications powered by one Li-ion or Li-polymer cell and which require multiple power rails. The TPS65014 provides two highly efficient, step-down converters targeted at providing the core voltage and peripheral I/O rails in a processor-based system. Both step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. The LOW_PWR pin allows the core converter to lower its output voltage when the application processor goes into deep sleep. The TPS65014 also integrates two 200-mA LDO voltage regulators, which are enabled through the serial interface. Each LDO operates with an input voltage range of 1.8 V to 6.5 V, thus allowing them to be supplied from one of the step-down converters or directly from the battery.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65014	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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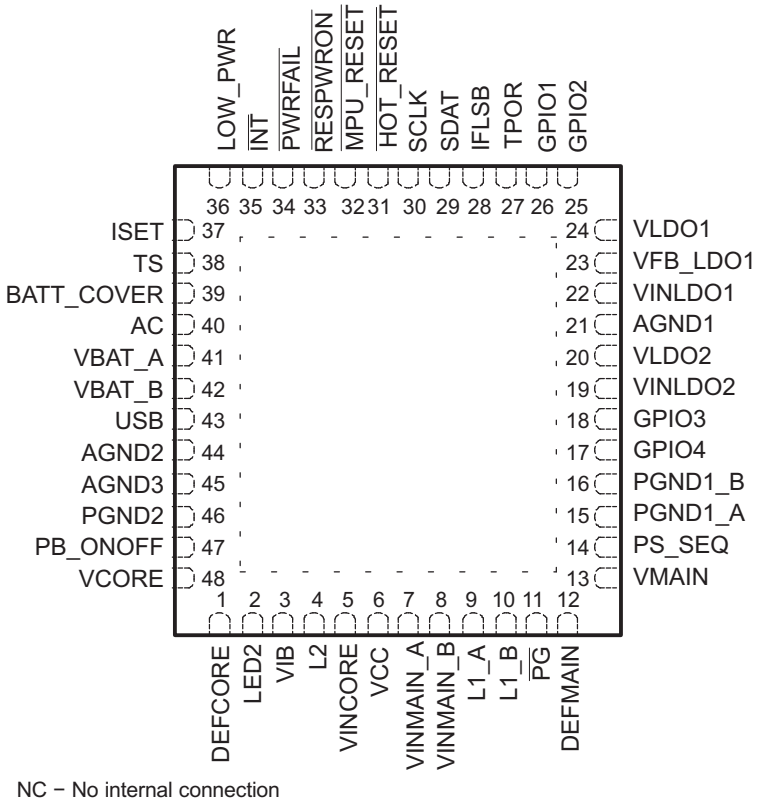
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2004) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



NC − No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CHARGER SECTION			
AC	40	I	Charger input voltage from AC adapter. The AC pin can be left open or can be connected to ground if the charger is not used.
AGND2	44	—	Analog ground connection. All analog ground pins are connected internally on the chip.
ISET	37	I	External charge current setting resistor connection for use with AC adapter
$\overline{PG}$	11	O	Indicates when a valid power supply is present for the charger (open-drain)
TS	38	I	Battery temperature sense input
USB	43	I	Charger input voltage from USB port. The USB pin can be left open or can be connected to ground if the charger is not used.
VBAT_A	41	I	Sense input for the battery voltage. Connect directly with the battery.
VBAT_B	42	O	Power output of the battery charger. Connect directly with the battery.
Thermal Pad	—	—	Connect the thermal pad to GND
SWITCHING REGULATOR SECTION			
AGND3	45	—	Analog ground connection. All analog ground pins are connected internally on the chip.
L1_A, L1_B	9, 10	—	Switch pin of VMAIN converter. The VMAIN inductor is connected here.
L2	4	—	Switch pin of VCORE converter. The VCORE inductor is connected here.
PGND1_A, PGND1_B	15, 16	—	Power ground for VMAIN converter
PGND2	46	—	Power ground for VCORE converter

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCHING REGULATOR SECTION (continued)			
VCC	6	I	Power supply for digital and analog circuitry of MAIN and CORE DC-DC converters. This must be connected to the same voltage supply as VINCORE and VINMAIN. Also supplies serial interface block
VCORE	48	I	VCORE feedback voltage sense input, connect directly to VCORE
VMAIN	13	I	VMAIN feedback voltage sense input, connect directly to VMAIN
VINMAIN_A, VINMAIN_B	7, 8	I	Input voltage for VMAIN step-down converter. This must be connected to the same voltage supply as VINCORE and VCC.
VINCORE	5	I	Input voltage for VCORE step-down converter. This must be connected to the same voltage supply as VINMAIN and VCC.
LDO REGULATOR SECTION			
AGND1	21	—	Analog ground connection. All analog ground pins are connected internally on the chip.
VFB_LDO1	23	I	Feedback input from external resistive divider for LDO1
VINLDO1	22	I	Input voltage for LDO1
VINLDO2	19	I	Input voltage for LDO2
VLDO1	24	O	Output voltage for LDO1
VLDO2	20	O	Output and feedback voltage for LDO2
DRIVER SECTION			
LED2	2	O	LED driver, with blink rate programmable through the serial interface
VIB	3	O	Vibrator driver, enabled through the serial interface
CONTROL AND I2C SECTION			
BATT_COVER	39	I	Indicates if battery cover is in place
DEFCORE	1	I	Input signal indicating default VCORE voltage, 0 = 1.5 V, 1 = 1.8 V
DEFMAIN	12	I	Input signal indicating default VMAIN voltage, 0 = 3 V, 1 = 3.3 V
GPIO1	26	I/O	General-purpose open-drain input/output
GPIO2	25	I/O	General-purpose open-drain input/output
GPIO3	18	I/O	General-purpose open-drain input/output
GPIO4	17	I/O	General-purpose open-drain input/output
$\overline{\text{HOT\_RESET}}$	31	I	Push-button reset input used to reboot or wake up processor through the TPS65014
IFLSB	28	I	LSB of serial interface address used to distinguish two devices with the same address
$\overline{\text{INT}}$	35	O	Indicates a charge fault or termination, or if any of the regulator outputs are below the lower tolerance level, active low (open-drain)
LOW_PWR	36	I	Input signal indicating deep sleep mode, VCORE is lowered to predefined value or disabled
$\overline{\text{MPU\_RESET}}$	32	O	Open-drain reset output generated by user activated $\overline{\text{HOT\_RESET}}$
PB_ONOFF	47	I	Push-button enable pin, also used to wake up processor from *low power* mode
PS_SEQ	14	I	Sets power-up/down sequence of step-down converters
$\overline{\text{PWRFAIL}}$	34	O	Open-drain output. Active low when UVLO comparator indicates low VBAT condition or when shutdown is about to occur due to an overtemperature condition or when the battery cover is removed (BATT_COVER has gone low).
$\overline{\text{RESPWRON}}$	33	O	Open-drain system reset output, generated according to the state of the VMAIN output voltage. If the main output is disabled, $\overline{\text{RESPWRON}}$ is active (in other words, low).
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data/address
TPOR	27	I	Sets the reset delay time at $\overline{\text{RESPWRON}}$. TPOR = 0: $T_{n(\overline{\text{RESPWRON}})}$ = 100 ms. TPOR = 1: $T_{n(\overline{\text{RESPWRON}})}$ = 1 s.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

	MIN	MAX	UNIT
Input voltage on VAC pin with respect to AGND		20	V
Input voltage range on all other pins except AGND/PGND pins with respect to AGND	–0.3	7	V
Current at AC, VBAT, VINMAIN, L1, PGND1		1800	mA
Peak current at all other pins		1000	mA
Continuous power dissipation		See *Dissipation Ratings*	
Operating free-air temperature, T_A	–40	85	°C
Maximum junction temperature, T_J		125	°C
Storage temperature, T_{stg}	–65	150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(3)(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.
(2) At pins VIB, $\overline{PG}$, and LED2
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{(AC)}$	Supply voltage from AC adapter	4.5		6.5	V
$V_{(USB)}$	Supply voltage from USB	4.4		5.25	V
$V_{(BAT)}$	Voltage at battery	2.5		4.2	V
$V_{I(MAIN)}$,$V_{I(CORE)}$,V_{CC}	Input voltage range step-down converters	2.5		6.0	V
$V_{I(LDO1)}$, $V_{I(LDO2)}$	Input voltage range for LDOs	1.8		6.5	V
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C
$R_{(CC)}$	Resistor from $V_{I(main)}$,$V_{I(core)}$ to V_{CC} used for filtering, $C_{I(VCC)}$ = 1 µF		10	100	Ω

6.4 Thermal Information

THERMAL METRIC[1]		TPS65014 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)} = 3.6$ V, $T_A = –40°C$ to 85°C, typical values are at $T_A = 25°C$ battery charger specifications are valid in the range $0°C < T_A < 85°C$ unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS: LOW_PWR, SCLK, SDAT (INPUT)						
V_{IH}	High-level input voltage	I_{IH} = 20 µA [1]	2		V_{CC}	V
V_{IL}	Low-level input voltage	I_{IL} = 10 µA	0		0.8	V
I_{IB}	Input bias current			0.01	1	µA
CONTROL SIGNALS: PB_ONOFF, $\overline{\text{HOT\_RESET}}$, BATT_COVER						
V_{IH}	High-level input voltage	I_{IH} = 20 µA[1]	0.8 V_{CC}		6	V
V_{IL}	Low-level input voltage	I_{IL} = 10 µA	0		0.4	V
$R_{(pb\_onoff)}$	Pulldown resistor at PB_ONOFF			1000		kΩ
$R_{(hot\_reset)}$	Pullup resistor at $\overline{\text{HOT\_RESET}}$, connected to VCC			1000		kΩ
$R_{(batt\_cover)}$	Pulldown resistor at BATT_COVER			2000		kΩ
CONTROL SIGNALS: $\overline{\text{MPU\_RESET}}$, $\overline{\text{PWRFAIL}}$, $\overline{\text{RESPWRON}}$, $\overline{\text{INT}}$, SDAT (OUTPUT)						
V_{OH}	High-level output voltage				6	V
V_{OL}	Low-level output voltage	I_{IL} = 10 mA	0		0.3	V
SUPPLY PIN: VCC						
$I_{(Q)}$	Operating quiescent current	V_I = 3.6 V, current into Main + Core + V_{CC}			70	µA
$I_{O(SD)}$	Shutdown supply current	V_I = 3.6 V, BATT_COVER = GND, Current into Main + Core + V_{CC}		15	25	µA

(1) If the input voltage is higher than V_{CC}, an additional input current, limited by an internal 10-kΩ resister, flows.

Electrical Characteristics (continued)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)} = 3.6$ V, $T_A = –40°C$ to 85°C, typical values are at $T_A = 25°C$ battery charger specifications are valid in the range $0°C < T_A < 85°C$ unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VMAIN STEP-DOWN CONVERTER							
V_I	Input voltage range			2.5		6	V
I_O	Maximum output current			1000			mA
$I_{O(SD)}$	Shutdown supply current		BATT_COVER = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		$V_{I(MAIN)} = V_{GS} = 3.6$ V		110	210	mΩ
$I_{lkg(p)}$	P-channel leakage current		$V_{(DS)} = 6$ V			1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		$V_{I(MAIN)} = V_{GS} = 3.6$ V		110	200	mΩ
$I_{lkg(N)}$	N-channel leakage current		$V_{(DS)} = 6$ V			1	µA
I_L	P-channel current limit		2.5 V< $V_{I(MAIN)}$ < 6 V	1.4	1.75	2.1	A
f_S	Oscillator frequency			1	1.25	1.5	MHz
$V_{O(MAIN)}$	Fixed output voltage	2.5 V	$V_{I(MAIN)}$ = 2.7 V to 6 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 2.7 V to 6 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
		2.75 V	$V_{I(MAIN)}$ = 2.95 V to 6 V; I_O = 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 2.95 V to 6 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
		3.0 V	$V_{I(MAIN)}$ = 3.2 V to 6 V; I_O= 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 3.2 V to 6 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
		3.3 V	$V_{I(MAIN)}$ = 3.5 V to 6 V; I_O= 0 mA	0%		3%	
			$V_{I(MAIN)}$ = 3.5 V to 6 V; 0 mA ≤ I_O ≤ 1000 mA	3%		3%	
	Line regulation		$V_{I(MAIN)} = V_{O(MAIN)}$ + 0.5 V (min. 2.5 V) to 6 V, I_O = 10 mA		0.5		%/V
	Load regulation		I_O = 10 mA to 1000 mA		0.12		%/A
$R_{(VMAIN)}$	VMAIN discharge resistance				400		Ω
VCORE STEP-DOWN CONVERTER							
V_I	Input voltage range			2.5		6	V
I_O	Maximum output current			400			mA
$I_{O(SD)}$	Shutdown supply current		BATT_COVER = GND		0.1	1	µA
$r_{DS(on)}$	P-channel MOSFET on-resistance		$V_{I(CORE)} = V_{GS} = 3.6$ V		275	530	mΩ
$I_{lkg(p)}$	P-channel leakage current		$V_{DS} = 6$ V		0.1	1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		$V_{I(CORE)} = V_{GS} = 3.6$ V		275	500	mΩ
$I_{lkg(N)}$	N-channel leakage current		$V_{DS} = 6$ V		0.1	1	µA
I_L	P-channel current limit		2.5 V < $V_{I(CORE)}$ < 6 V	600	700	900	mA
f_S	Oscillator frequency			1	1.25	1.5	MHz

Electrical Characteristics (continued)

$V_{I(MAIN)} = V_{I(CORE)} = V_{CC} = V_{I(LDO1)} = V_{I(LDO2)} = 3.6$ V, $T_A = –40°C$ to 85°C, typical values are at $T_A = 25°C$ battery charger specifications are valid in the range $0°C < T_A < 85°C$ unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCORE STEP-DOWN CONVERTER (continued)							
$V_{O(CORE)}$	Fixed output voltage	0.85 V	$V_{I(CORE)}$ = 2.5 V to 6 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	3%		3%	
		1.0 V	$V_{I(CORE)}$ = 2.5 V to 6 V; I_O = 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	3%		3%	
		1.1 V	$V_{I(CORE)}$ = 2.5 V to 6 V; I_O= 0 mA, C_O = 22 µF	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 400 mA, C_O = 22 µF	3%		3%	
		1.2 V	$V_{I(CORE)}$ = 2.5 V to 0 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O≤ 400 mA	3%		3%	
		1.3 V	$V_{I(CORE)}$ = 2.5 V to 6 V; I_O= 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 400 mA	3%		3%	
		1.4 V	$V_{I(CORE)}$ = 2.5 V to 6 V; I_O= 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O≤ 400 mA	3%		3%	
		1.5 V	$V_{I(CORE)}$ = 2.5 V to 6 V; I_O = 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 400 mA	3%		3%	
		1.8 V	$V_{I(CORE)}$ = 2.5 V to 6 V; I_O= 0 mA	0%		3%	
			$V_{I(CORE)}$ = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 400 mA	3%		3%	
	Line regulation		$V_{I(CORE)} = V_{O(MAIN)}$ + 0.5 V (min. 2.5 V) to 6 V, I_O = 10 mA		1		%/V
	Load regulation		I_O = 10 mA to 400 mA		0.002		%/mA
$R_{(VCORE)}$	VCORE discharge resistance				400		Ω
VLDO1 and VLDO2 LOW-DROPOUT REGULATORS							
V_I	Input voltage range	LD01		1.8		6.5	V
		LD02		1.8		V_{CC}	
V_O	LDO1 output voltage range			0.9		VINLDO1	V
V_{ref}	Reference voltage			485	500	515	mV
V_O	LDO2 output voltage range			1.8		3.3	V
I_O	Maximum output current		Full-power mode	200			mA
			Low-power mode	30			
$I_{(SC)}$	LDO1 and LDO2 short-circuit current limit		VLDO1 = GND, VLDO2 = GND			650	mA
	Dropout voltage		I_O = 200 mA, VINLDO1,2 = 1.8 V			300	mV
	Total accuracy					±3%	
	Line regulation		VINLDO1,2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5 V, I_O = 10 mA		0.75		%/V
	Load regulation		I_O = 10 mA to 200 mA		0.011		%/mA
	Regulation time		Load change from 10% to 90%			0.1	ms
			Low-power mode		0.1		
$I_{(QFP)}$	LDO quiescent current (each LDO)		Full-power mode		16	30	µA
$I_{(QLPM)}$	LDO quiescent current (each LDO)		Low-power mode		12	18	µA
$I_{O(SD)}$	LDO shutdown current (each LDO)				0.1	1	µA
$I_{lkg(FB)}$	Leakage current feedback				0.01	0.1	µA

6.6 Electrical Characteristics: Battery Charger

$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \le 1$ A, 0°C < T_A < 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLDO1 and VLDO2 LOW-DROPOUT REGULATORS (continued)						
$V_{(AC)}$	Input voltage range		4.5		6.5	V
$V_{(USB)}$	Input voltage range		4.35		5.25	V
$I_{CC(VCHG)}$	Supply current	$V_{(CHG)} > V_{(CHG)}$min		1.2	2	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into VBAT pin, $V_{(CHG)} < V_{(SLP-ENTRY)}$, 0°C ≤ T_J ≤ 85°C		2	5	µA
$I_{CC(STBY)}$	Standby current	Current into USB pin			45	µA
		Current into AC pin		200	400	
VOLTAGE REGULATOR						
V_O	Output voltage	$V_{(CHG)}$min ≥ 4.5 V	4.15	4.20	4.25	V
V_{DO}	Dropout voltage ($V_{(AC)}$ – VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)}$, $I_{O(OUT)}$ = 1 A		500	800	mV
	Dropout voltage ($V_{(USB)}$ – VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)}$, $I_{O(OUT)}$ = 0.5 A		300	500	
	Dropout voltage ($V_{(USB)}$ – VBAT)	$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)}$, $I_{O(OUT)}$ = 0.1 A		100	150	
CURRENT REGULATION						
$I_{O(AC)}$	Output current range for ac operation (1)	V_{CHG} ≥ 4.5 V, $V_{I(OUT)} > V_{(LOWV)}$, $V_{(AC)} - V_{I(BAT)} > V_{(DO-MAX)}$	100		1000	mA
$V_{(SET)}$	Output current set voltage for ac operation at ISET pin. 100% output current I^2C register CHGCONFIG<4:3> = 11	V_{min} ≥ 4.5 V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{(AC)} - V_{I(BAT)} > V_{(DO-MAX)}$	2.45	2.50	2.55	V
	75% output current I^2C register CHGCONFIG<4:3> = 10		1.83	1.91	1.99	
	50% output current I^2C register CHGCONFIG<4:3> = 01		1.23	1.31	1.39	
	32% output current I^2C register CHGCONFIG<4:3> = 00		0.76	0.81	0.86	
KSET	Output current set factor for ac operation	100 mA < I_O < 1000 mA	310	330	350	
		10 mA < I_O < 100 mA	300	340	380	
$I_{O(USB)}$	Output current range for USB operation	$V_{(CHG)}$min ≥ 4.35 V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{(USB)} - V_{I(BAT)} > V_{(DO-MAX)}$, I^2C register CHGCONFIG<2> = 0	80		100	mA
		$V_{(CHG)}$min ≥ 4.5 V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{USB} - V_{I(BAT)} > V_{(DO-MAX)}$, I^2C register CHGCONFIG<2> = 1	400		500	
$R_{(ISET)}$	Resistor range at ISET pin		825		8250	Ω
PRECHARGE CURRENT REGULATION, SHORT-CIRCUIT CURRENT, AND BATTERY DETECTION CURRENT						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold, voltage on VBAT pin.	$V_{(CHG)}$ min ≥ 4.5 V	2.8	3	3.2	V
$I_{(PRECHG)}$	Precharge current (2)	0 ≤ $V_{I(OUT)} < V_{(LOWV)}$, t < $t_{(PRECHG)}$	10		100	mA
$I_{(DETECT)}$	Battery detection current			200		µA
$V_{(SET-PRECHG)}$	Voltage at ISET pin	0 ≤ $V_{I(OUT)} < V_{(LOWV)}$, t < $t_{(PRECHG)}$	240	255	270	mV

(1) $$I_{O(AC)} = \frac{KSET \times V_{(SET)}}{R_{(ISET)}}$$

(2) $$I_{(PRECHG)} = \frac{KSET \times V_{(SET\_PRECHG)}}{R_{(ISET)}}$$

Electrical Characteristics: Battery Charger (continued)

$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \le 1$ A, 0°C < T_A < 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE TAPER AND TERMINATION DETECTION						
$I_{(TAPER)}$	Taper current detect range (3)	$V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	10		100	mA
$V_{(SET\_TAPER)}$	Voltage at ISET pin for charge TAPER detection	$V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	235	250	265	mV
$V_{(SET\_TERM)}$	Voltage at ISET pin for charger termination detection (4)	$V_{I(OUT)} > V_{(RCH)}$	11	18	25	mV
TEMPERATURE COMPARATOR						
$V_{(LTF)}$	Low (cold) temperature threshold		2.475	2.50	2.525	V
$V_{(HTF)}$	High (hot) temperature threshold		0.485	0.5	0.515	V
$I_{(TS)}$	TS current source		95	102	110	µA
BATTERY RECHARGE THRESHOLD						
$V_{(RCH)}$	Recharge threshold	$V_{(CHG)}$min ≥ 4.5 V	$V_{O(REG)}$ – 0.115	$V_{O(REG)}$ – 0.1	$V_{O(REG)}$ – 0.085	V
SLEEP AND STANDBY						
$V_{(SLP-ENTRY)}$	Sleep-mode entry threshold, $\overline{PG}$ output = high	2.3 V ≤ $V_{I(OUT)} \le V_{O(REG)}$			$V_{(CHG)} \le V_{I(OUT)}$ +150 mV	V
$V_{(SLP\_EXIT)}$	Sleep-mode exit threshold, $\overline{PG}$ output = low	2.3 V ≤ $V_{I(OUT)} \le V_{O(REG)}$	$V_{(CHG)} \ge V_{I(OUT)}$ + 250 mV			V
CHARGER POWER-ON-RESET, UVLO, AND $V_{(IN)}$ RAMP RATE						
$V_{(CHGUVLO)}$	Charger undervoltage lockout	$V_{(CHG)}$ decreasing	2.27	2.5	2.75	V
	Hysteresis			27		mV
$V_{(CHGOVLO)}$	Charger overvoltage lockout		6.5			V
CHARGER OVERTEMPERATURE SUSPEND						
$T_{(suspend)}$	Temperature at which charger suspends operation			145		°C
$T_{(hyst)}$	Hysteresis of suspend threshold			20		°C

(3) $$I_{(TAPER)} = \frac{KSET \times V_{(SET\_TAPER)}}{R_{(ISET)}}$$

(4) $$I_{(TERM)} = \frac{KSET \times V_{(SET\_TERM)}}{R_{(ISET)}}$$

Electrical Characteristics: Battery Charger (continued)

$V_{O(REG)} + V_{(DO-MAX)} \le V_{(CHG)} = V_{(AC)}$ or $V_{(USB)}$, $I_{(TERM)} < I_O \le 1$ A, 0°C < T_A < 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC SIGNALS DEFMAIN, DEFCORE, PS_SEQ, IFLSB							
V_{IH}	High-level input voltage		I_{IH} = 20 µA	V_{CC} – 0.5		V_{CC}	V
V_{IL}	Low-level input voltage		I_{IL} = 10 µA	0		0.4	V
I_{IB}	Input bias current				0.01	1	µA
LOGIC SIGNALS GPIO1-4							
V_{OL}	Low-level output voltage		I_{OL} = 1 mA, configured as an open-drain output			0.3	V
V_{OH}	High-level output voltage		Configured as an open-drain output			6	V
V_{IL}	Low -level input voltage			0		0.8	V
V_{IH}	High-level input voltage			2		V_{CC} (5)	V
I_I	Input leakage current					1	µA
$r_{DS(on)}$	Internal NMOS		V_{OL} = 0.3 V		150		Ω
LOGIC SIGNALS $\overline{PG}$, LED2							
V_{OL}	Low-level output voltage		I_{OL} = 20 mA			0.5	V
V_{OH}	High-level output voltage					6	V
$V_{(PG)}$	$\overline{PG}$ threshold voltage USB and AC			$V_{(BAT)}$ + xx mV			V
VIBRATOR DRIVER VIB							
V_{OL}	Low-level output voltage		I_{OL} = 100 mA		0.3	0.5	V
V_{OH}	High-level output voltage					6	V
THERMAL SHUTDOWN							
$T_{(SD)}$	Thermal shutdown		Increasing junction temperature		160		°C
UNDERVOLTAGE LOCKOUT							
$V_{(UVLO)}$	Undervoltage lockout threshold. The default value for UVLO is 2.75 V	$V_{(UVLO)}$ 2.5 V	Filter resistor = 10R in series with V_{CC}, V_{CC} decreasing	-3%		3%	
		$V_{(UVLO)}$ 2.75 V		-3%		3%	
		$V_{(UVLO)}$ 3.0 V		-3%		3%	
		$V_{(UVLO)}$ 3.25 V		-3%		3%	
$V_{(UVLO\_HYST)}$	UVLO comparator hysteresis		V_{CC} rising	350	400	450	mV
POWER GOOD							
	Decreasing rail voltage		VMAIN, VCORE, VLDO1, VLDO2 decreasing	–12%	–10%	–8%	
	Increasing rail voltage		VMAIN, VCORE, VLDO1, VLDO2 increasing	–7%	–5%	–3%	

(5) If the input voltage is higher than V_{CC} an additional current flows, limited by an internal 10-kΩ resistor.

6.7 Dissipation Ratings

See (1)

AMBIENT TEMPERATURE	MAX POWER DISSIPATION FOR T_j = 125°C (2)	DERATING FACTOR ABOVE T_A = 55°C
25°C	3 W	30 mW/°C
55°C	2.1 W	

(1) The TPS65014 is housed in a 48-pin QFN package with exposed leadframe on the underside. This 7-mm × 7-mm package exhibits a thermal impedance (junction-to-ambient) of 33 K/W when mounted on a JEDEC high-k board.
(2) Consideration needs to be given to the maximum charge current when the assembled application board exhibits a thermal impedance which differs significantly from the JEDEC high-k board.

6.8 Serial Interface Timing Requirements

	MIN	MAX	UNIT
Clock frequency, f_{MAX}		400	kHz
Clock high time, $t_{wH(HIGH)}$	600		ns
Clock low time, $t_{wL(LOW)}$	1300		ns
DATA and CLK rise time, t_R		300	ns
DATA and CLK fall time, t_F		300	ns
Hold time (repeated) START condition (after this period the first clock pulse is generated), $t_{h(STA)}$	600		ns
Setup time for repeated START condition, $t_{h(DATA)}$	600		ns
Data input hold time, $t_{h(DATA)}$	0		ns
Data input setup time, $t_{su(DATA)}$	100		ns
STOP condition setup time, $t_{su(STO)}$	600		ns
Bus free time, $t_{(BUF)}$	1300		ns

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS: PB_ONOFF, $\overline{\text{HOT\_RESET}}$, BATT_COVER						
$t_{(glitch)}$	Deglitch time at all 3 pins		38	56	77	ms
$t_{(batt\_cover)}$	Delay after $t_{(glitch)}$ ($\overline{\text{PWRFAIL}}$ goes low) before supplies are disabled when BATT_COVER goes low.		1.68	2.4	3.2	ms
CONTROL SIGNALS: $\overline{\text{MPU\_RESET}}$, $\overline{\text{PWRFAIL}}$, $\overline{\text{RESPWRON}}$, $\overline{\text{INT}}$, SDAT (OUTPUT)						
$t_{d(mpu\_nreset)}$	Duration of low pulse at $\overline{\text{MPU\_RESET}}$		100			µs
$t_{d(nrespwron)}$	Duration of low pulse at $\overline{\text{RESPWRON}}$ after VMAIN is in regulation	TPOR = 0	80	100	120	ms
		TPOR = 1	800	1000	1200	
$t_{d(uvlo)}$	Time between UVLO going active ($\overline{\text{PWRFAIL}}$ going low) and supplies being disabled		1.68	2.4	3.2	ms
$t_{d(overtemp)}$	Time between chip overtemperature condition being recognized ($\overline{\text{PWRFAIL}}$ going low) and supplies being disabled		1.68	2.4	3.2	ms
PRECHARGE CURRENT REGULATION, SHORT-CIRCUIT CURRENT, AND BATTERY DETECTION CURRENT						
	Deglitch time	$V_{(CHG)}$ min ≥ 4.5 V, $V_{I(OUT)}$ decreasing below threshold; 100-ns fall time, 10-mV overdrive	8.8	23	60	ms
CHARGE TAPER AND TERMINATION DETECTION						
	Deglitch time for $I_{(TAPER)}$	$V_{(CHG)}$ min ≥ 4.5V, charging current increasing or decreasing above and below; 100-ns fall time, 10-mV overdrive	8.8	23	60	ms
	Deglitch time for $I_{(TERM)}$	$V_{(CHG)}$ min ≥ 4.5 V, charging current decreasing below;100-ns fall time, 10-mV overdrive	8.8	23	60	ms
TEMPERATURE COMPARATOR						
	Deglitch time for temperature fault		8.8	23	60	ms
BATTERY RECHARGE THRESHOLD						
	Deglitch time	$V_{(CHG)}$min ≥ 4.5 V, $V_{I(OUT)}$ decreasing below threshold; 100-ns fall time, 10-mV overdrive	8.8	23	60	ms

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMERS						
$t_{(PRECHG)}$	Precharge timer	$V_{(CHG)}$min ≥ 4.5 V	1500	1800	2160	s
$t_{(TAPER)}$	Taper timer	$V_{(CHG)}$min ≥ 4.5 V	1500	1800	2160	s
$t_{(CHG)}$	Charge timer	$V_{(CHG)}$min ≥ 4.5 V	15000	18000	21600	s
SLEEP AND STANDBY						
	Deglitch time for sleep mode entry and exit	AC or USB decreasing below threshold; 100-ns fall time, 10-mV overdrive	8.8	23	60	ms
$t_{(USB\_DEL)}$	Delay between valid USB voltage being applied and start of charging process from USB			5		ms

6.10 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Efficiency	vs Output current	Figure 1, Figure 2
Quiescent current	vs Input voltage	Figure 3
Switching frequency	vs Temperature	Figure 4
LDO1 Output voltage	vs Output current	Figure 5-Figure 8
LDO2 Output voltage	vs Output current	Figure 9
Line transient response (main)		Figure 9
Line transient response (core)		Figure 10
Line transient response (LDO1)		Figure 11
Line transient response (LDO2)		Figure 12
Load transient response (main)		Figure 13
Load transient response (core)		Figure 14
Load transient response (LDO1)		Figure 15
Load transient response (LDO2)		Figure 16
Output voltage ripple (PFM)		Figure 17
Output voltage ripple (PWM)		Figure 18
Start-up timing		Figure 19
Dropout voltage	vs Output current	Figure 20, Figure 21
PSRR (LDO1 and LDO2)	vs Frequency	Figure 22

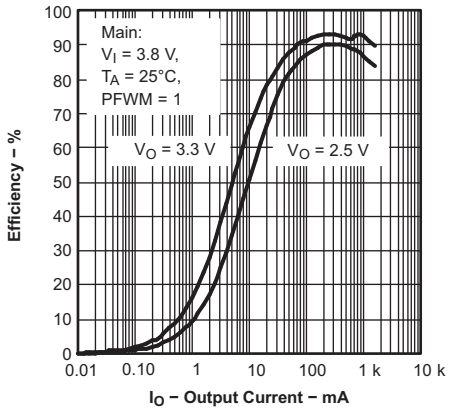


Figure 1. Efficiency vs Output Current

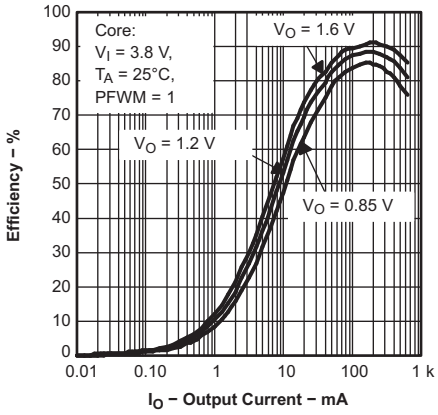


Figure 2. Efficiency vs Output Current

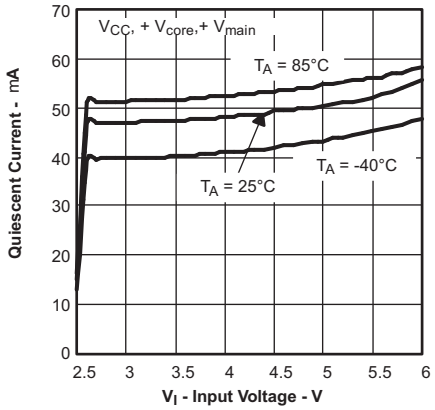


Figure 3. Quiescent Current vs Input Voltage

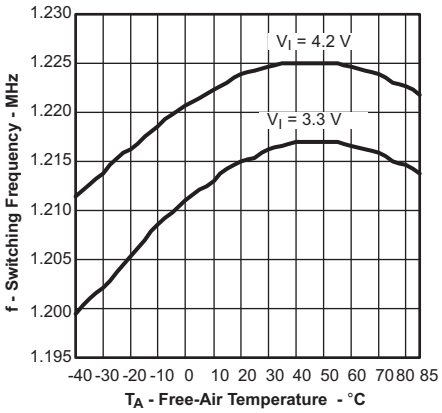


Figure 4. Switching Frequency vs Temperature

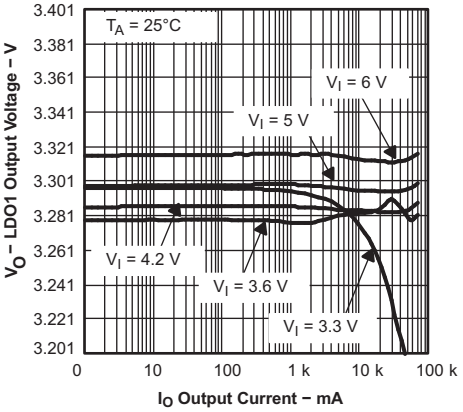


Figure 5. LD01 Output Voltage vs Output Current

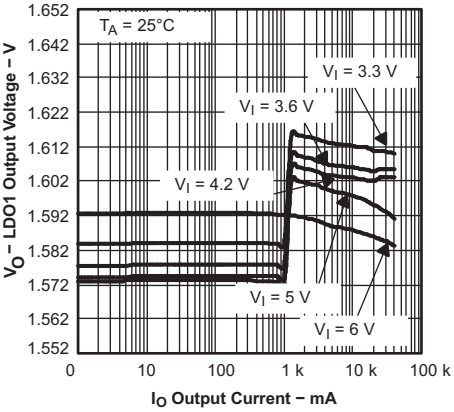


Figure 6. LD01 Output Voltage vs Output Current

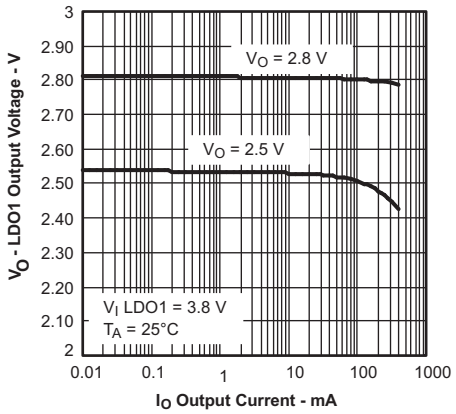


Figure 7. LDO1 Output Voltage vs Output Current

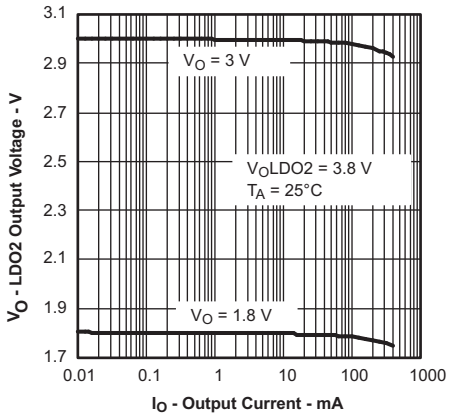


Figure 8. LDO2 Output Voltage vs Output Current

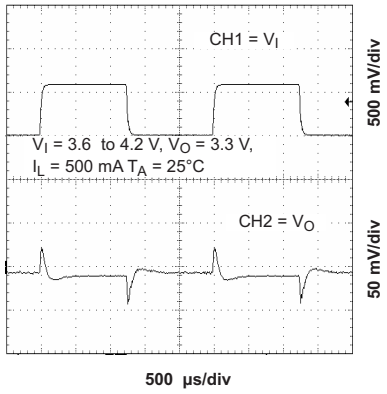


Figure 9. Line Transient Response (Main)

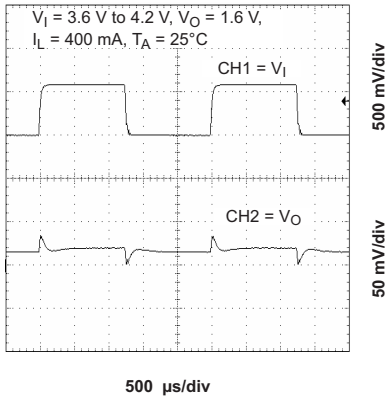


Figure 10. Line Transient Response (Core)

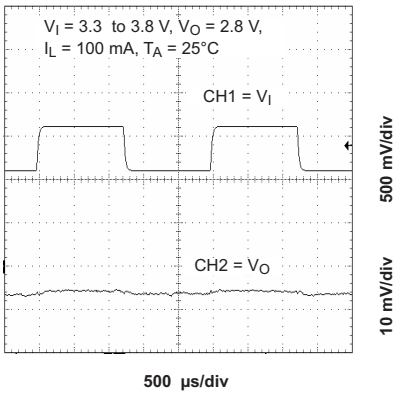


Figure 11. Line Transient Response (LDO1)

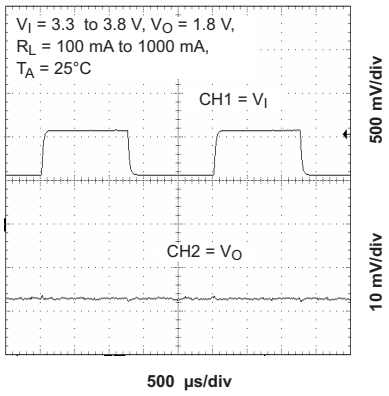


Figure 12. Line Transient Response (LDO2)

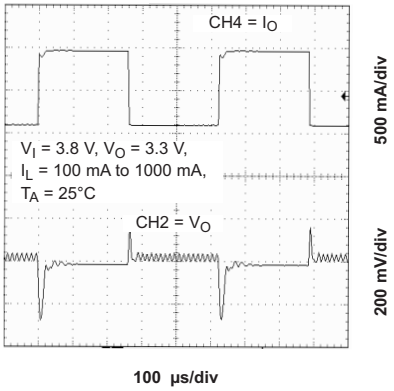


Figure 13. Load Transient Response (Main)

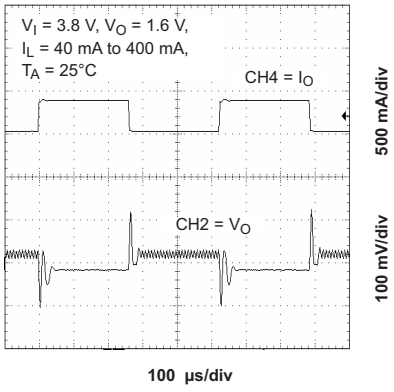


Figure 14. Load Transient Response (Core)

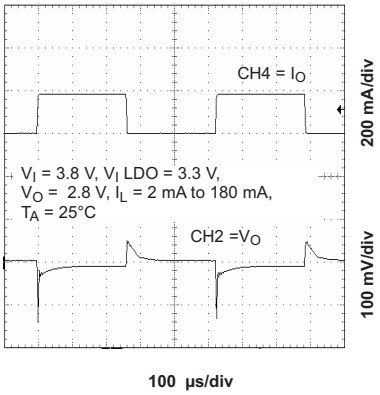


Figure 15. Load Transient Response (LDO1)

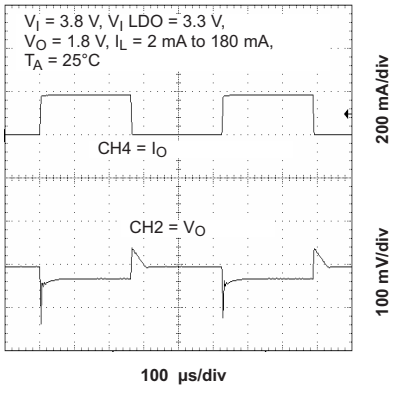


Figure 16. Load Transient Response (LDO2)

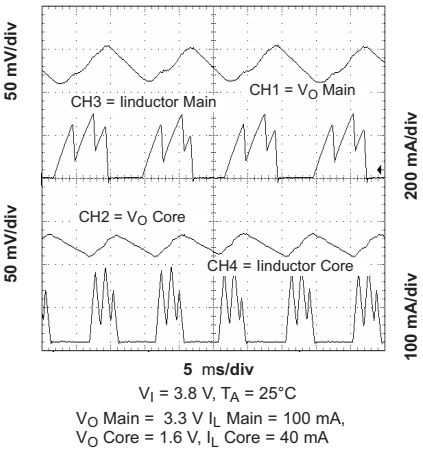


Figure 17. Output Ripple (PFM)

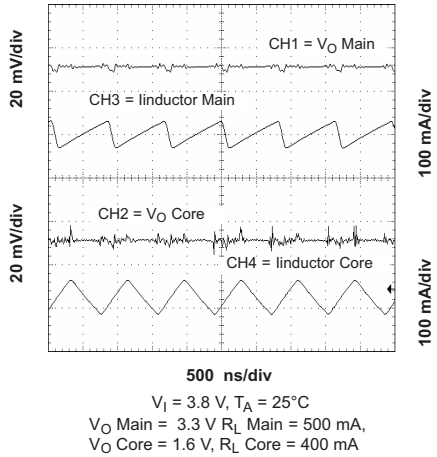
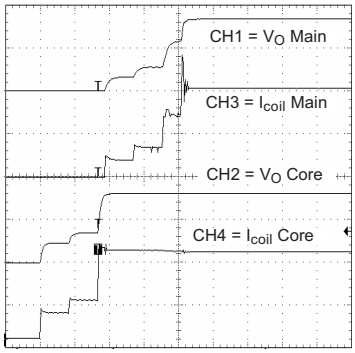


Figure 18. Output Ripple (PWM)



V_I = 3.8 V, V_O Main = 3.3 V,
R_L Main = 1 A, V_O Core = 1.6 V,
R_L Core = 400 mA, T_A = 25°C

Figure 19. Start-Up Timing

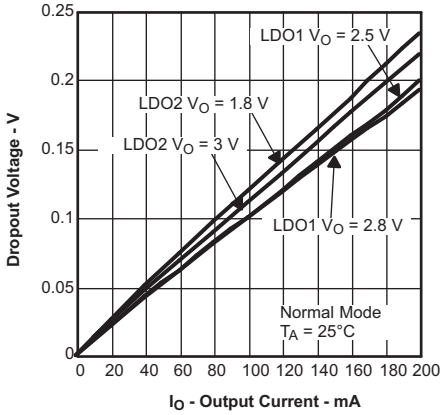


Figure 20. Dropout Voltage vs Output Current

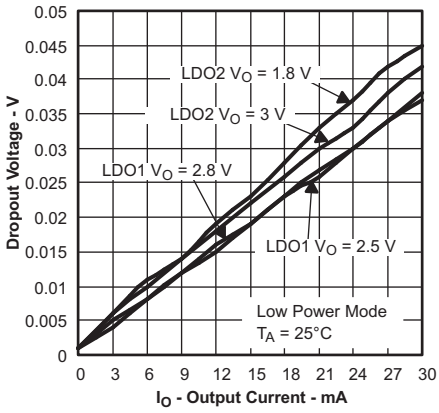


Figure 21. Dropout Voltage vs Output Current

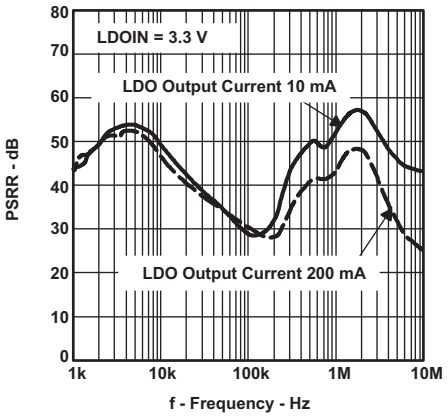


Figure 22. PSRR (LDO1, LDO2) vs Frequency

7 Detailed Description

7.1 Overview

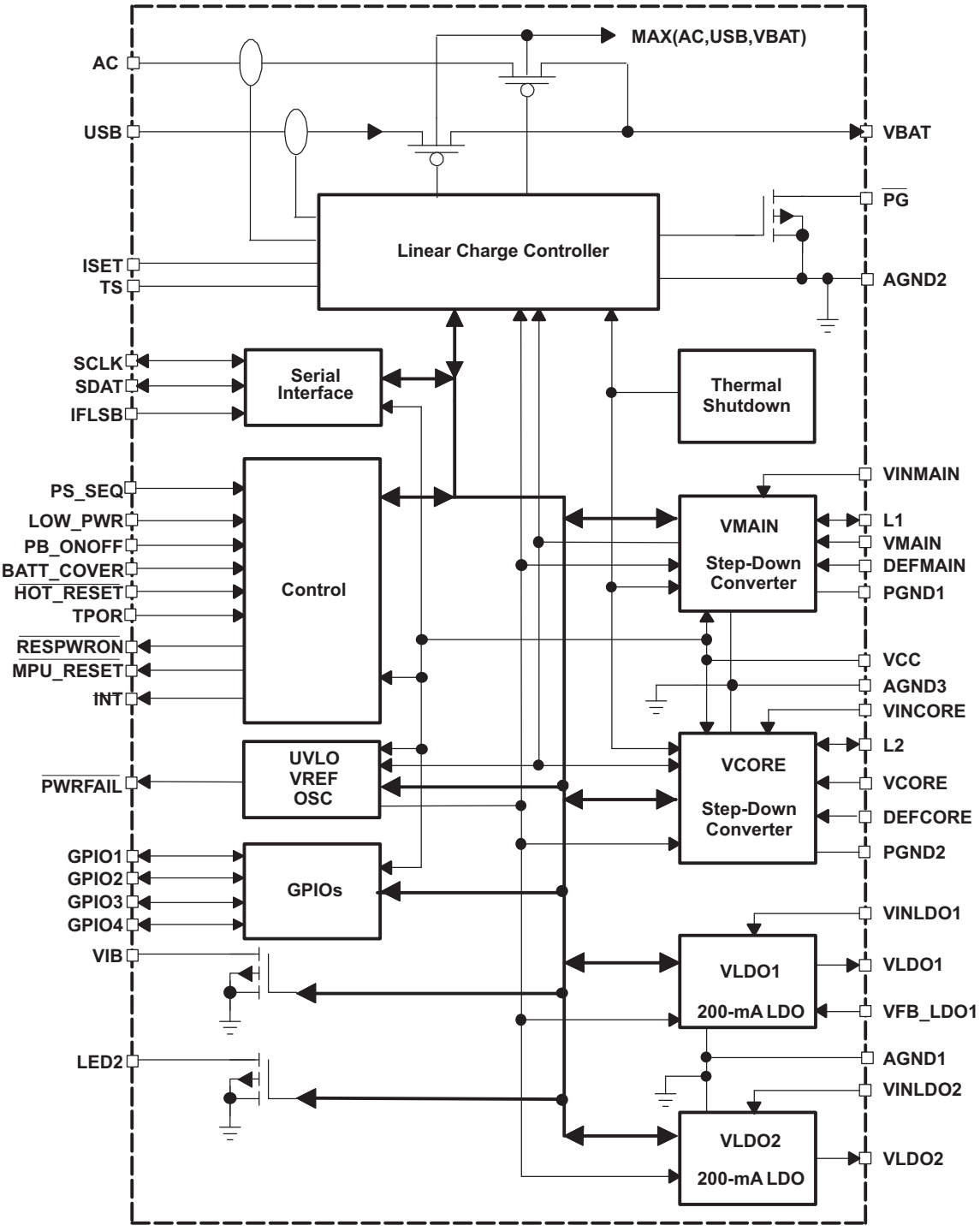
The TPS65014 has a highly integrated and flexible Li-Ion linear charger and system power management. It offers an integrated USB port and AC-adapter supply management with autonomous power-source selection, power FET and current sensor, high accuracy current and voltage regulation, charge status, and charge termination.

The TPS65014 charger automatically selects the USB port or the AC adapter as the power source for the system. In the USB configuration, the host can increase the charge current from the default value of maximum 100 mA to 500 mA through the interface. In the AC adapter configuration, an external resistor sets the maximum value of charge current.

The battery is charged in three phases: conditioning, constant current, and constant voltage. Charge is normally terminated based on minimum current. An internal charge timer provides a safety backup for charge termination. The TPS65014 automatically restarts the charge if the battery voltage falls below an internal threshold. The charger automatically enters sleep mode when both supplies are removed.

The serial interface can be used for dynamic voltage scaling, for collecting information on and controlling the battery charger status, for optionally controlling 2-LED driver outputs, a vibrator driver, masking interrupts, or for disabling, enabling, and setting the LDO output voltages. The interface is compatible with the fast- and standard-mode I^2C specification, thus allowing transfers up to 400 kHz.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Step-Down Converters, VMAIN and VCORE

The TPS65014 incorporates two synchronous step-down converters operating typically at 1.25-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter power-save mode and operate with pulse frequency modulation (PFM). The main converter is capable of delivering 1-A output current and the core converter is capable of delivering 400 mA.

The converter output voltages are programmed through the VDCDC1 and VDCDC2 registers in the serial interface. The main converter defaults to 3-V or 3.3-V output voltage depending on the DEFMAIN configuration pin, if DEFMAIN is tied to ground, the default is 3 V; if it is tied to V_{CC}, the default is 3.3 V. The core converter defaults to either 1.5 V or 1.8 V, depending on whether the DEFCORE configuration pin is tied to GND or to V_{CC}, respectively. Both the main and core output voltages can subsequently be reprogrammed after start-up through the serial interface. In addition, the LOW_PWR pin can be used either to lower the core voltage to a value defined in the VDCDC2 register when the application processor is in deep sleep mode, or to disable the core converter. An active signal at LOW_PWR is ignored if the ENABLE_LP bit is not set in the VDCDC1 register.

The step-down converter outputs (when enabled) are monitored by power-good comparators, the outputs of which are available through the serial interface. The outputs of the DC-DC converters can be optionally discharged when the DC-DC converters are disabled.

During PWM operation, the converters use a fast response voltage-mode controller scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle, initiated by the clock signal, the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The error amplifier, together with the input voltage, determines the rise time of the saw-tooth generator, and therefore any change in input voltage or output voltage directly controls the duty cycle of the converter, giving a good line and load transient regulation.

The two DC-DC converters operate synchronized to each other, with the MAIN converter as the master. A 270° phase shift between the MAIN switch turnon and the CORE switch turnon decreases the input RMS current, and smaller input capacitors can be used. This is optimized for a typical application where the MAIN converter regulates a Li-ion battery voltage of 3.7 V to 3.3 V and the CORE from 3.7 V to 1.5 V.

7.3.1.1 Forced PWM

The core and main converters are forced into PWM mode by setting bit 7 in the VDCDC1 register. This feature is used to minimize ripple on the output voltages.

7.3.1.2 Dynamic Voltage Positioning

As described in the power-save mode operation sections and as detailed in Figure 11, the output voltage is typically 1.2% above the nominal output voltage at light load currents, as the device is in power-save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel rectifier switch.

7.3.1.3 Soft-Start

Both converters have an internal soft-start circuit that limits the inrush current during start-up. The soft start is implemented as a digital circuit, increasing the switch current in 4 steps up to the typical maximum switch current limit of 700 mA (core) and 1.75 A (main). Therefore, the start-up time mainly depends on the output capacitor and load current.

Feature Description (continued)

7.3.1.4 100% Duty Cycle Low Dropout Operation

The TPS65014 converters offer a low input to output voltage difference while maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage and is calculated in Equation 1:

$$V_{I(min)} = V_{O(max)} + I_{O(max)} \times \left(r_{DS(on)\,max} + R_L\right)$$

where

- $I_{O(max)}$ = maximum output current plus inductor ripple current
- $r_{DS(on)max}$ = maximum P-channel switch r_{DSon}
- R_L = DC resistance of the inductor
- $V_{O(max)}$ = nominal output voltage plus maximum output voltage tolerance (1)

7.3.1.5 Active Discharge When Disabled

When the CORE and MAIN converters are disabled, due to an UVLO, BATT_COVER, or OVERTEMP condition, it is possible to actively pull down the outputs. This feature is disabled per default and is individually enabled through the VDCDC1 and VDCDC2 registers in the serial interface. When this feature is enabled, the core and main outputs are discharged by a 400-Ω (typical) load.

7.3.1.6 Power-Good Monitoring

Both the MAIN and CORE converters have power-good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value, with 5% hysteresis. The outputs of these comparators are available in the REGSTATUS register through the serial interface. A maskable interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled. The status of the power-good comparator for VMAIN is used to generate the RESPWRON signal.

7.3.1.7 Overtemperature Shutdown

The MAIN and CORE converters are automatically shut down if the temperature exceeds the trip point (see *Electrical Characteristics*). This detection is only active if the converters are in PWM mode, either by setting FPWM = 1, or if the output current is high enough that the device runs in PWM mode automatically.

7.3.2 Low-Dropout Voltage Regulators

The low-dropout voltage regulators are designed to operate with low value ceramic input and output capacitors. They operate with input voltages down to 1.8 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO has a current limit feature. Both LDOs are enabled per default; both LDOs can be disabled or programmed through the serial interface using the VREGS1 register. The LDO outputs (when enabled) are monitored by power-good comparators, the outputs of which are available through the serial interface. The LDOs also have reverse conduction prevention when disabled. This allows the possibility to connect external regulators in parallel in systems with a backup battery.

7.3.2.1 Power-Good Monitoring

Both the LDO1 and LDO2 linear regulators have power-good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value, with 5% hysteresis. The outputs of these comparators are available in the REGSTATUS register through the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The LDO2 comparator is disabled when LDO2 is disabled.

Feature Description (continued)

7.3.2.2 Enabling and Sequencing

Enabling and sequencing of the DC-DC converters and LDOs are described in the power-up sequencing section. The OMAP1510 processor from Texas Instruments requires that the core power supply is enabled before the I/O power supply, which means that the CORE converter should power up before the MAIN converter. This is achieved by connecting PS_SEQ to GND.

7.3.3 Undervoltage Lockout

The undervoltage lockout circuit for the four regulators on TPS65014 prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. Basically, it prevents the converter from turning on the power switch or rectifier FET under undefined conditions. The undervoltage threshold voltage is set by default to 2.75 V. After power up, the threshold voltage can be reprogrammed through the serial interface. The undervoltage lockout comparator compares the voltage on the VCC pin with the UVLO threshold. When the VCC voltage drops below this threshold, the TPS65014 sets the $\overline{\text{PWRFAIL}}$ pin low and after a time $t_{(UVLO)}$ disables the voltage regulators in the sequence defined by PS_SEQ. The same procedure is followed when the TPS65014 detects that its junction temperature has exceeded the overtemperature threshold, typically 160°C, with a delay $t_{(overtemp)}$. The TPS65014 automatically restarts when the UVLO (or overtemperature) condition is no longer present.

The battery charger circuit has a separate UVLO circuit with a threshold of typically 2.5 V, which is compared with the voltage on AC and USB supply pins.

7.3.4 Power-Up Sequencing

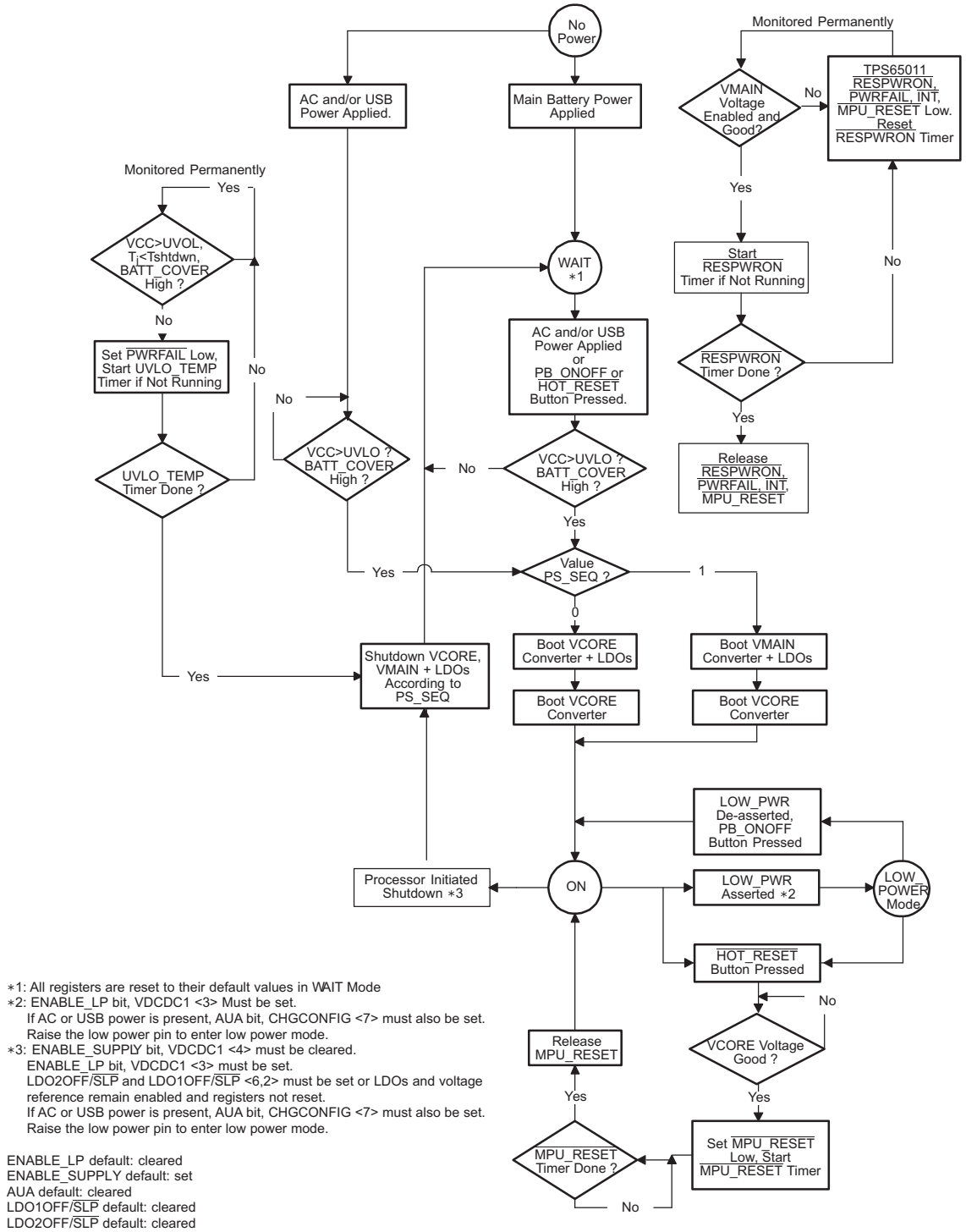
The TPS65014 power-up sequencing is designed to allow the maximum flexibility without generating excessive logistical or system complexity. The relevant control pins are described in Table 2.

Feature Description (continued)

Table 2. Control Pins

PIN NAME	INPUT/OUTPUT	FUNCTION
PS_SEQ	I	Input signal indicating power-up and power-down sequence of the switching converters. PS_SEQ = 0 forces the core regulator to ramp up first and down last. PS_SEQ = 1 forces the main regulator to ramp up first and down last.
DEFCORE	I	Defines the default voltage of the VCORE switching converter. DEFCORE = 0 defaults VCORE to 1.5 V, DEFCORE = VCC defaults VCORE to 1.8 V.
DEFMAIN	I	Defines the default voltage of the VMAIN switching converter. DEFMAIN = 0 defaults VMAIN to 3 V, DEFMAIN = VCC defaults VMAIN to 3.3 V.
LOW_PWR	I	The LOW_PWR pin is used to lower VCORE to the preset voltage in the VDCDC2 register when the processor is in deep sleep mode. Alternatively, VCORE can be disabled in low power mode if the LP_COREOFF bit is set in the VDCDC2 register. LOW_PWR is ignored if the ENABLE LP bit is not set in the VDCDC1 register. The TPS65014 uses the rising edge of the internal signal formed by a logical AND of LOW_PWR and ENABLE LP to enter low power mode. TPS65014 is forced out of low power mode by deasserting LOW_PWR, by resetting ENABLE LP to 0, by activating the PB_ONOFF pin or by activating the $\overline{\text{HOT\_RESET}}$ pin. There are two ways to get the device back into low power mode: a) toggle the LOW_PWR pin, or b) toggle the low power bit when the LOW_PWR pin is held high. The LOW_PWR pin is also used to set the TPS65014 into WAIT mode. If USB or AC is present, the AUA bit (CHCONFIG<7>) must be set to enter the WAIT mode, see Figure 23.
PB_ONOFF	I	PB_ONOFF can be used to exit the low power mode and return the core voltage to the value before low power mode was entered. If PB_ONOFF is used to exit the low power mode, then the low power mode can be reentered by toggling the LOW_PWR pin or by toggling the low power bit when the LOW_PWR pin is held high. A 1-MΩ pulldown resistor is integrated in TPS65014. PB_ONOFF is internally de-bounced by the TPS65014. A maskable interrupt is generated when PB_ONOFF is activated.
$\overline{\text{HOT\_RESET}}$	I	The $\overline{\text{HOT\_RESET}}$ pin has a similar functionality to the PB_ONOFF pin. In addition, it generates a reset ($\overline{\text{MPU\_RESET}}$) for the MPU when the VCORE voltage is in regulation. $\overline{\text{HOT\_RESET}}$ does not alter any TPS65014 settings unless low power mode was active in which case it is exited. A 1-MΩ pullup resistor to V_{CC} is integrated in TPS65014. $\overline{\text{HOT\_RESET}}$ is internally de-bounced by the TPS65014.
BATT_COVER	I	The BATT_COVER pin is used as an early warning that the main battery is about to be removed. BATT_COVER = V_{CC} indicates that the cover is in place, BATT_COVER = 0 indicates that the cover is not in place. TPS65014 generates a maskable interrupt when the BATT_COVER pin goes low. $\overline{\text{PWRFAIL}}$ is also held low when BATT_COVER goes low. This feature may be disabled by tying BATT_COVER permanently to VCC. The TPS65014 shuts down the main and the core converter and sets the LDOs into low power mode. A 2-MΩ pulldown resistor is integrated in the TPS65014 at the BATT_COVER pin. BATT_COVER is internally de-bounced by the TPS65014.
$\overline{\text{RESPWRON}}$	O	$\overline{\text{RESPWRON}}$ is held low while the switching converters (and any LDOs defined as default on) are starting up. It is determined by the state of MAIN's output voltage; when the voltage is higher than the power-good comparator threshold; then $\overline{\text{RESPWRON}}$ is high when VMAIN is low; then $\overline{\text{RESPWRON}}$ is low. $\overline{\text{RESPWRON}}$ is held low for $t_{h(\text{RESPWRON})}$ seconds after VMAIN has settled.
$\overline{\text{MPU\_RESET}}$	O	$\overline{\text{MPU\_RESET}}$ can be used to reset the processor if the user activates the $\overline{\text{HOT\_RESET}}$ button. The $\overline{\text{MPU\_RESET}}$ output is active for $t_{(\text{MPU\_nRESET})}$ sec. It also forces TPS65014 to leave low power mode. $\overline{\text{MPU\_RESET}}$ is also held low as long as $\overline{\text{RESPWRON}}$ is held low.
$\overline{\text{PWRFAIL}}$	O	$\overline{\text{PWRFAIL}}$ indicates when $V_{CC} < V_{(\text{UVLO})}$, when the TPS65014 is about to shut down due to an internal overtemperature condition or when BATT_COVER is low. $\overline{\text{PWRFAIL}}$ is also held low as long as $\overline{\text{RESPWRON}}$ is held low.
TPOR	I	TPOR is used to set the delay time for the $\overline{\text{RESPWRON}}$ reset signal. TPOR = 0 sets the delay time to 100 ms. TPOR = 1 sets the delay time to 1 s.

Figure 23 shows the state diagram for TPS65014 power sequencing. The charger function is not shown in the state diagram because this function is independent of these states.



*1: All registers are reset to their default values in WAIT Mode
*2: ENABLE_LP bit, VDCDC1 <3> Must be set.
If AC or USB power is present, AUA bit, CHGCONFIG <7> must also be set.
Raise the low power pin to enter low power mode.
*3: ENABLE_SUPPLY bit, VDCDC1 <4> must be cleared.
ENABLE_LP bit, VDCDC1 <3> must be set.
LDO2OFF/SLP and LDO1OFF/SLP <6,2> must be set or LDOs and voltage reference remain enabled and registers not reset.
If AC or USB power is present, AUA bit, CHGCONFIG <7> must also be set.
Raise the low power pin to enter low power mode.

ENABLE_LP default: cleared
ENABLE_SUPPLY default: set
AUA default: cleared
LDO1OFF/SLP default: cleared
LDO2OFF/SLP default: cleared

Figure 23. TPS65014 Power-On State Diagram

7.3.4.1 TPS65014 Power State Descriptions

7.3.4.1.1 State 1: No Power

No batteries are connected to the TPS65014. When main power is applied, the bandgap reference, LDOs, and UVLO comparator start up. The RESPWRON, PWRFAIL, INT, and MPU_RESET signals are held low. When BATT_COVER goes high (de-bounced internally by the TPS65014), indicating that the battery cover has been put in place and if VCC > UVLO, the power supplies are ramped in the sequence defined by PS_SEQ. RESPWRON, PWRFAIL, INT, and MPU_RESET are released when the RESPWRON timer has timed out after $t_{n(RESPWRON)}$ seconds. If VCC remains valid and no OVERTEMP condition occurs, then the TPS65014 arrives in State 2: ON. If VCC < UVLO, the TPS65014 keeps the bandgap reference and UVLO comparator active such that when VCC>UVLO (during battery charge), the supplies are automatically activated.

7.3.4.1.2 State 2: ON

In this state, the TPS65014 is fired up and ready for operation. The switching converter output voltages can be programmed. The LDOs can be disabled or programmed. The TPS65014 can exit this state due to an overtemperature condition, an undervoltage condition at VCC, BATT_COVER going low, or by the processor programming low power mode. State 2 is left temporarily if the user activates the HOT_RESET pin.

7.3.4.1.3 State 3: Low-Power Mode

This state is entered through the processor setting the ENABLE_LP bit in the serial interface and then raising the LOW_PWR pin. The TPS65014 uses the rising edge of the internal signal formed by a logical AND of the LOW_PWR and ENABLE LP signals to enter low power mode. The VMAIN switching converter remains active, but the VCORE converter may be disabled in low power mode through the serial interface by setting the LP_COREOFF bit in the VDCDC2 register. If left enabled, the VCORE voltage is set to the value predefined by the CORELP0/1 bits in the VDCDC2 register. The LDO1OFF/nSLP and LDO2OFF/nSLP bits in the VREGS1 register determine whether the LDOs are turned off or put in a reduced power mode (transient speed-up circuitry disabled in order to minimize quiescent current) in low power mode. All TPS65014 features remain addressable through the serial interface. The TPS65014 can exit this state either due to an undervoltage condition at VCC, due to BATT_COVER going low, due to an OVERTEMP condition, by the processor deasserting the LOW_POWER pin, or by the user activating the HOT_RESET pin or the PB_ONOFF pin.

7.3.4.1.4 State 4: Shutdown

There are two scenarios for entering this state. The first is from State 1: No Power. As soon as main battery power is applied, the device automatically enters the WAIT mode.

The second scenario occurs when the device is in ON mode and the processor initiates a shutdown by resetting the ENABLE SUPPLY bit in the VDCDC1 register (ENABLE_LP must be high), and then raising the LOW_PWR pin. When this happens, the power rails are ramped down in the predefined sequence, and all circuitry is then disabled. In this state, the TPS65014 waits for the PB_ONOFF or HOT_RESET pin to be activated before enabling any of the supply rails. When the PB_ONOFF or HOT_RESET pin is activated, the TPS65014 powers up the supplies according to the same constraints as at the initial application of power. Complete shutdown is only achieved by setting the LDO1OFF/nSLP and LDO2OFF/nSLP bits high in the VREGS1 register before activating the shutdown.

In this case, the I^2C interface is deactivated, and the registers are reset to their default value after leaving the WAIT mode.

To enter the WAIT mode when USB or AC is present, set the AUA bit (CHCONFIG<7>). The WAIT mode is automatically left if bit 7 in register CHCONFIG is set to 0 (default), and a voltage is present at either the AC pin or the USB pin in the appropriate range for charging, and the voltage at V_{CC} is above the UVLO threshold. This feature allows the converters to start up automatically if the device is plugged in for charging.

If all supplies are turned off in WAIT mode, the internal bandgap is switched off, and the internal registers are reset to their default state when the device returns to ON mode.

Table 3 lists possible configurations in LOW POWER mode and WAIT mode.

Table 3. TPS65014 Possible Configurations(1)

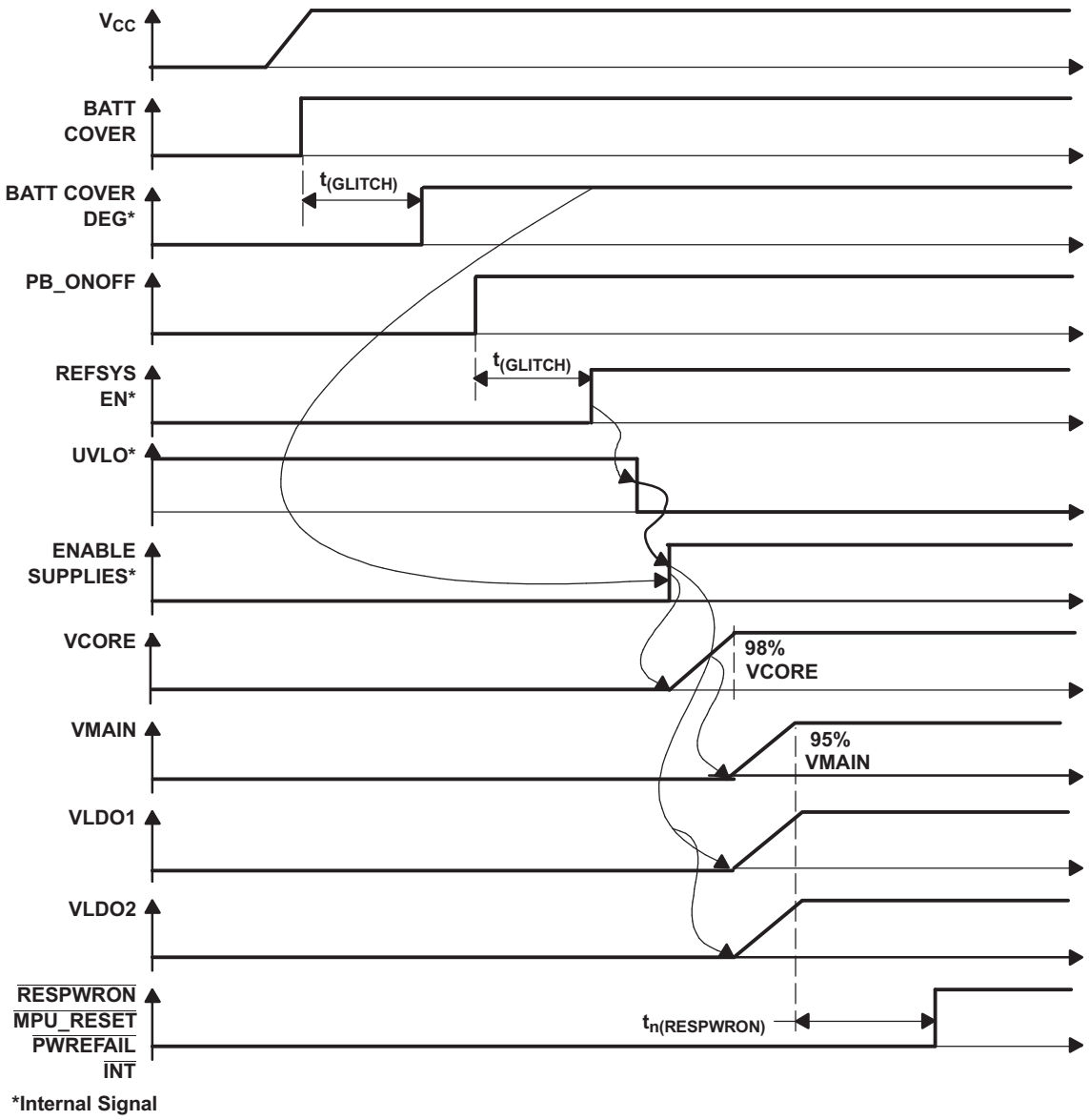
CONVERTER	MAIN	CORE	LDO1	LDO2
LOW POWER mode	1	0/1	0/1	0/1
WAIT mode	0	0	0/1	0/1

(1) 0 = converter is disabled
1 = converter is enabled

Table 4 indicates the typical quiescent-current consumption in each power state.

Table 4. TPS65014 Typical Current Consumption

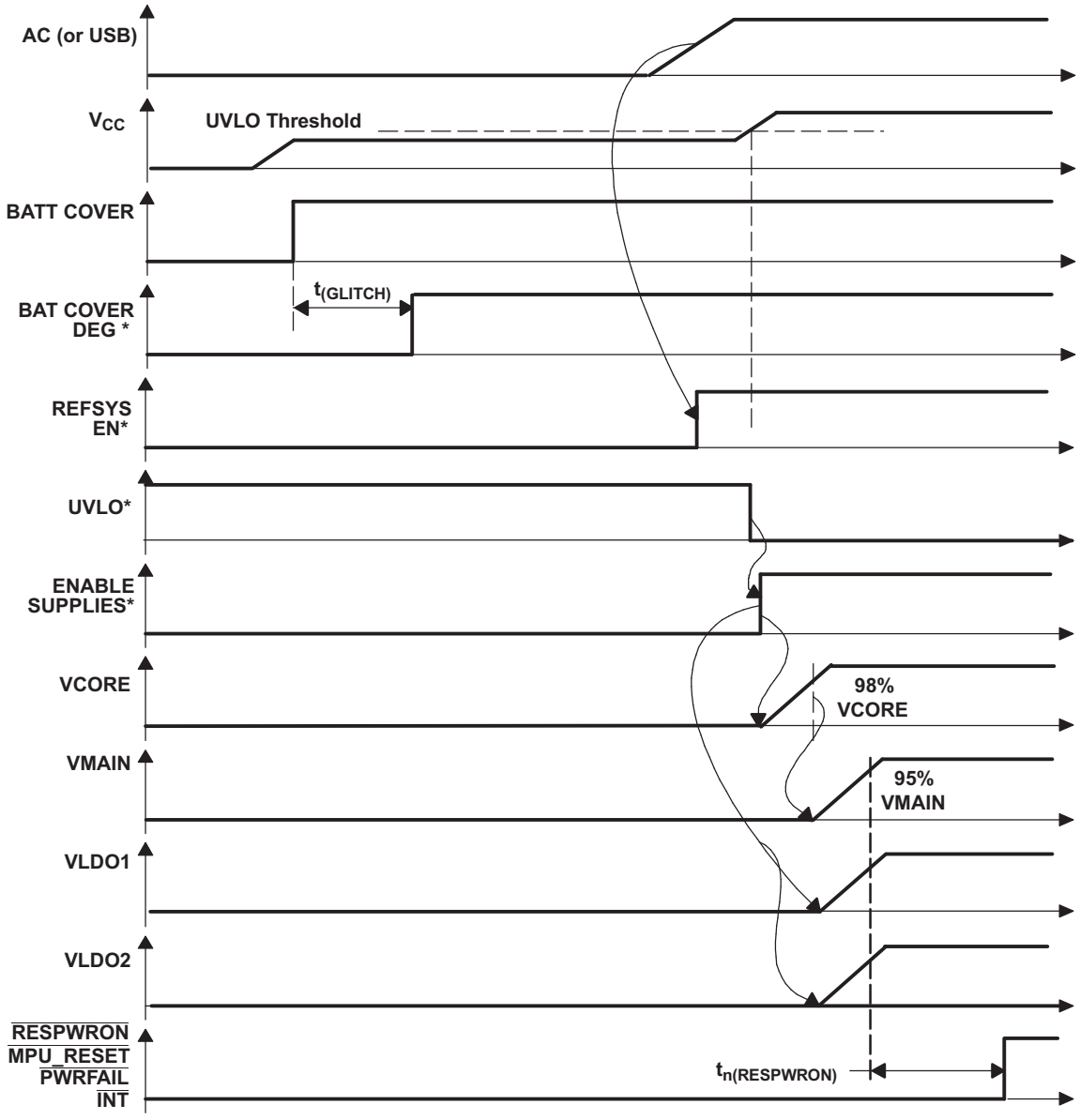
STATE	TOTAL QUIESCENT CURRENT	QUIESCENT CURRENT BREAKDOWN
1	0	
2	30 µA–70 µA	VMAIN (12 µA) + VCORE (12 µA) + LDOs (20 µA each, max 2) + UVLO + reference + PowerGood
3	30 µA–55 µA	VMAIN (12 µA) + VCORE (12 µA) + LDOs (10 µA each, max 2) + UVLO + reference + PowerGood
4	13 µA	UVLO + reference circuitry



Note: Valid for LDO1 supplied from VMAIN as described earlier in this *Application Section.*

Figure 24. State 1 to State 2 Transition (PS_SEQ = 0, V_{CC} > V_{UVLO} + HYST)

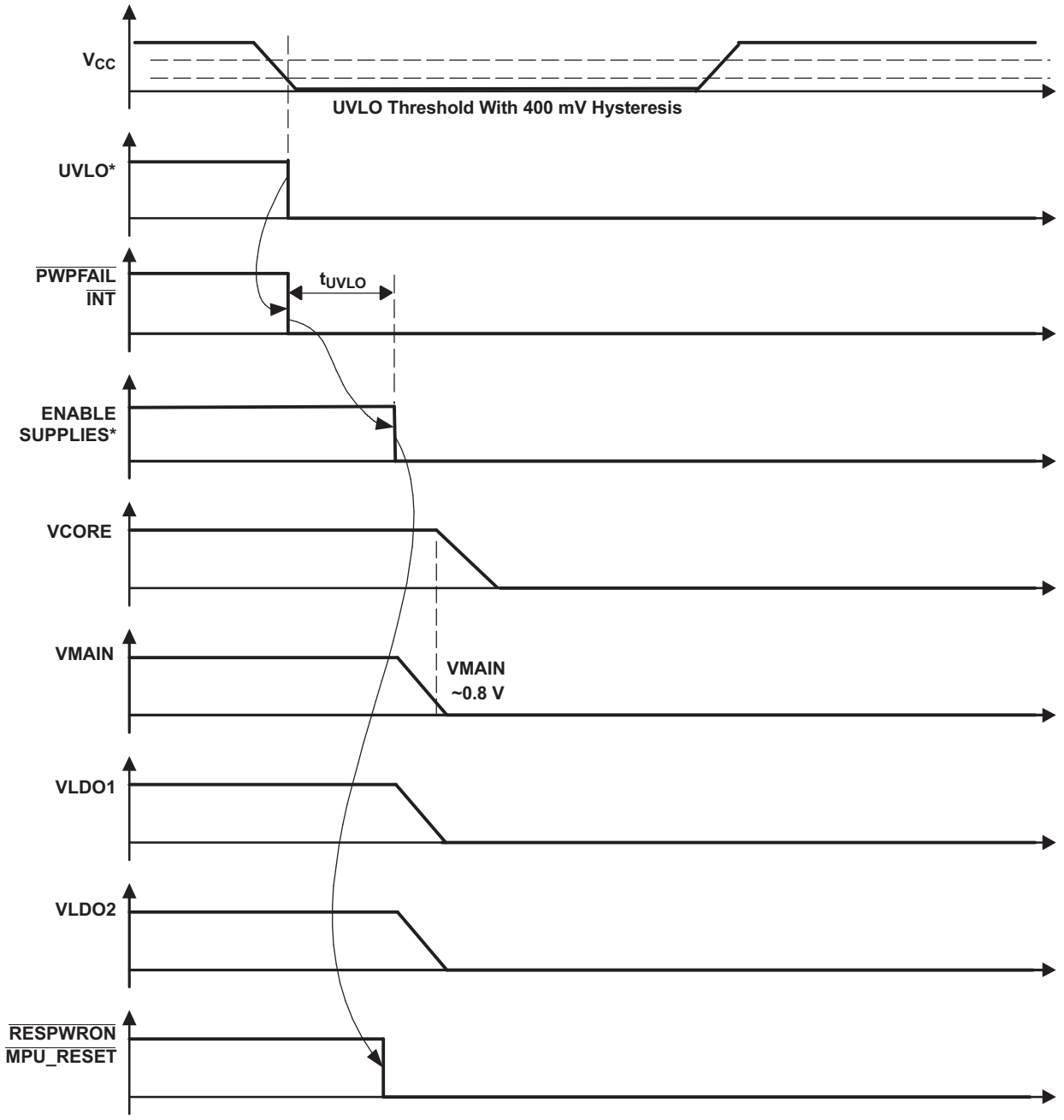
If 2.4 ms after application V_{CC} is still below the default UVLO threshold (3.15 V for V_{CC} rising), then start up is as shown in Figure 25.



*** Internal Signal**

Note: Valid for LDO1 supplied from VMAIN as described earlier in this *Application Section*

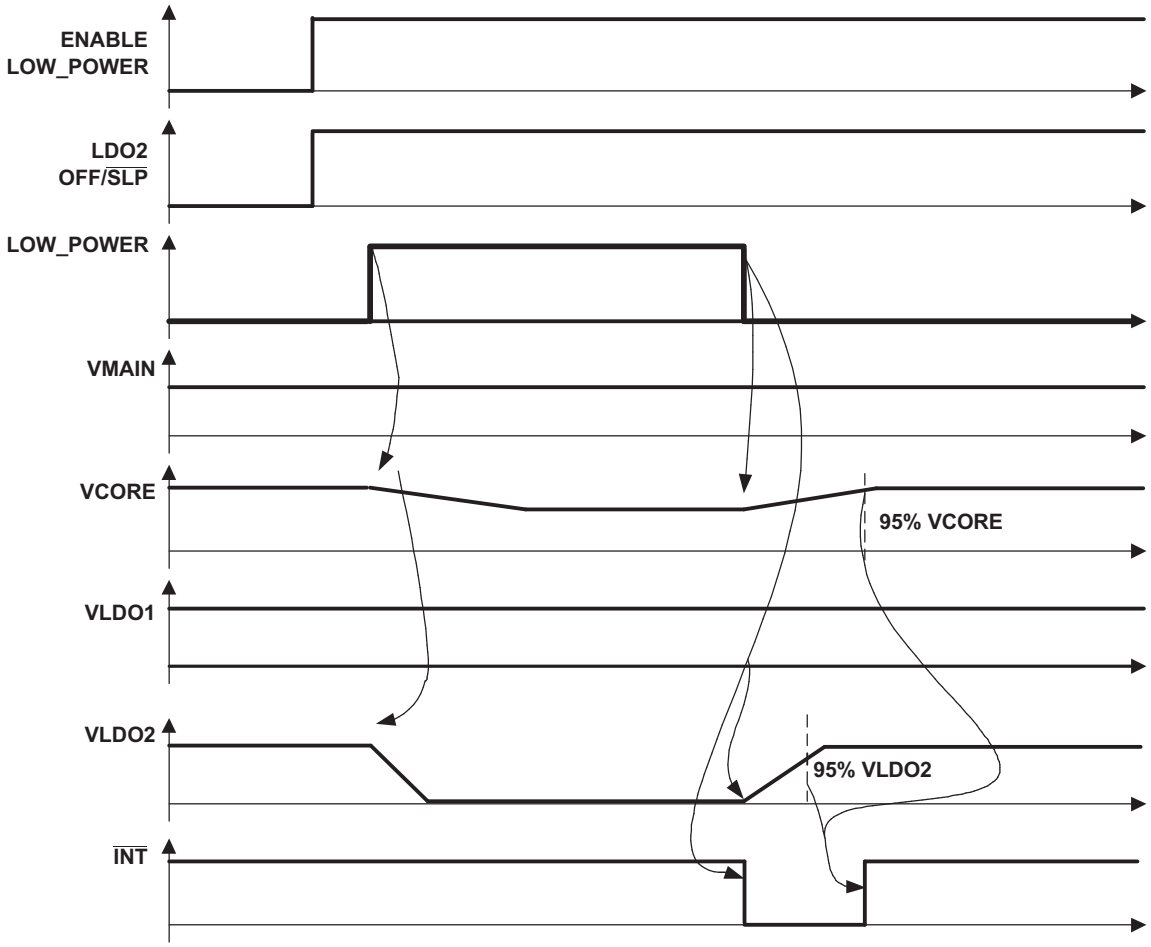
Figure 25. State 1 to State 4 to State 2 Transition (Power-Up Behavior When Charge Voltage is Applied)



*** Internal Signal**

Note: Valid for LDO1 supplied from VMAIN as described earlier in this *Application Section*

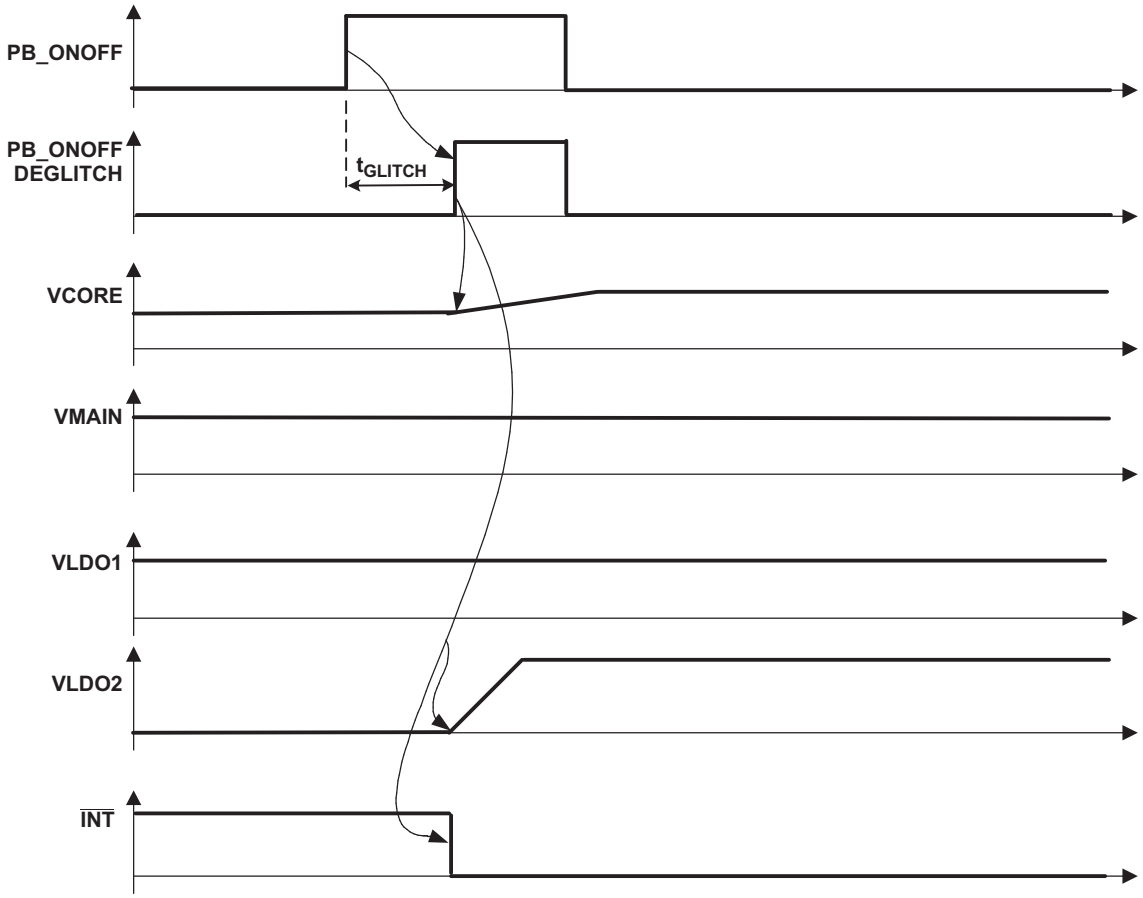
Figure 26. State 2 to State 4 Transition



Note: VCORE Lowered, LDO2 Disabled

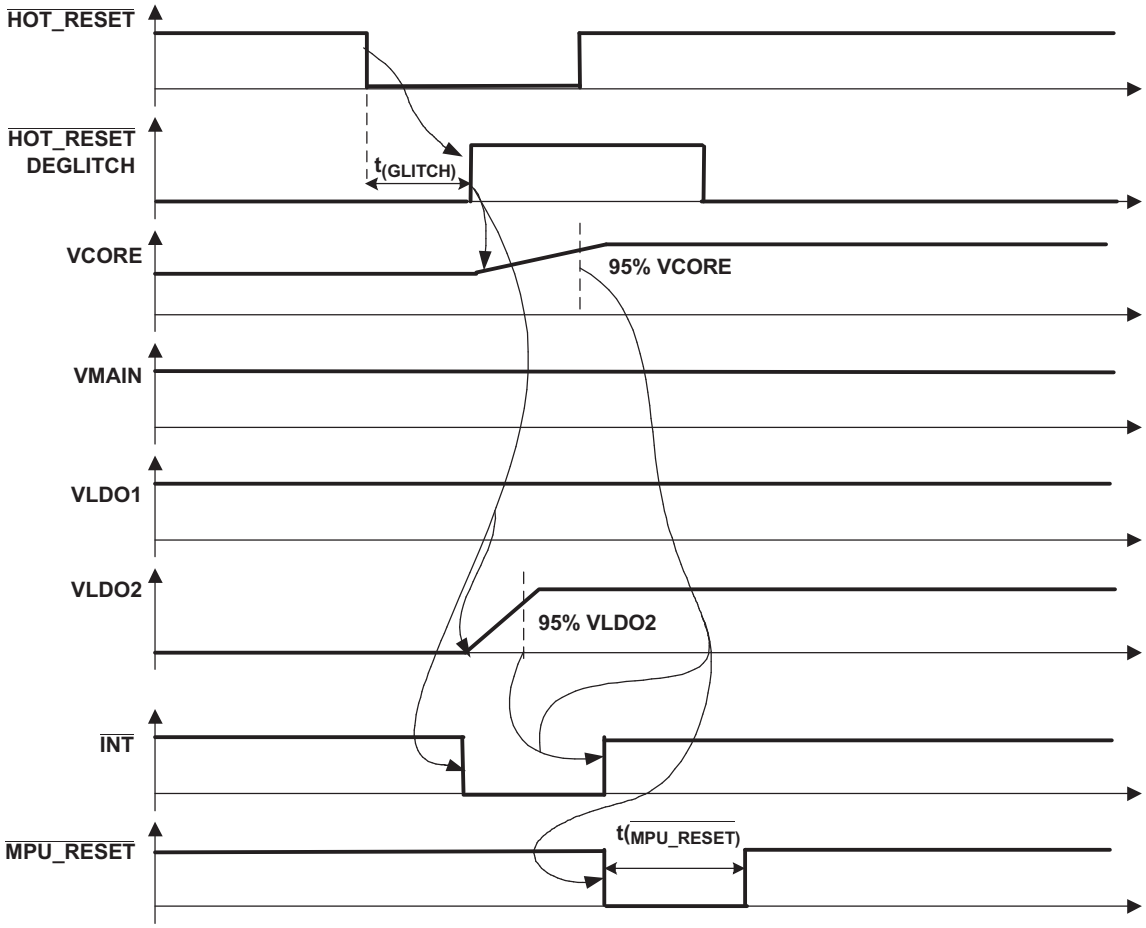
Note: Subsequent State 3 to State 2 Transition When LOW POWER Is Deasserted.

Figure 27. State 2 to State 3 Transition



Note: PB_ONFF Activated (See *Interrupt Management* for $\overline{\text{INT}}$ Behavior)

Figure 28. State 3 to State 2 Transition



Note: HOT_RESET Activated (See *Interrupt Management* for INT Behavior)

Figure 29. State 3 to State 2 Transition

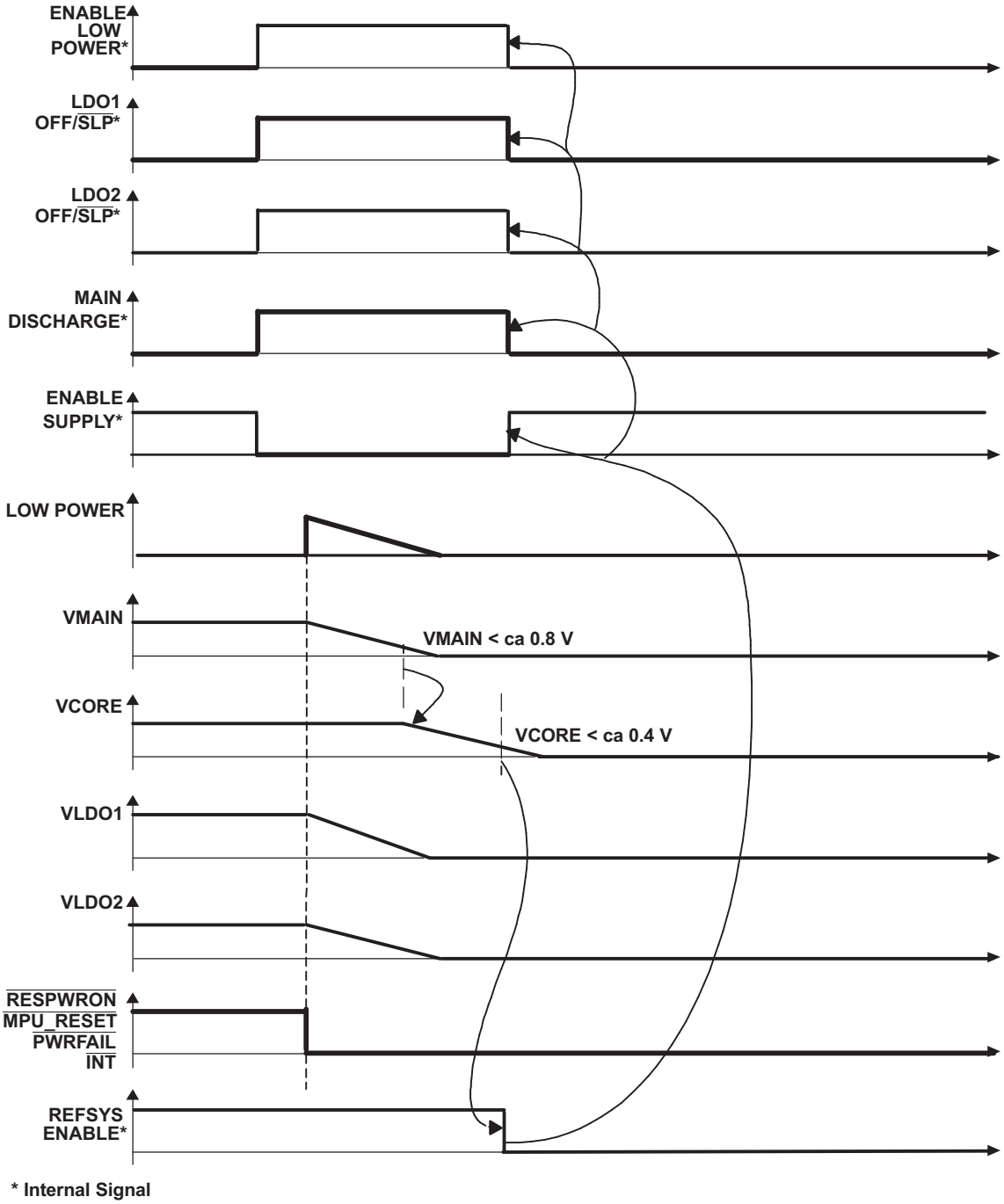


Figure 30. State 1 to State 4 Transition

7.3.5 System Reset and Control Signals

The RESPWRON signal is used as a global reset for the application. It is an open-drain output. The RESPWRON signal is generated according to the power good comparator linked to VMAIN and remains low for $t_{n(RESPWRON)}$ seconds after VMAIN has stabilized. When RESPWRON is low, PWRFAIL, MPU_RESET, and INT are also held low.

If the output voltage of MAIN is less than 90% of its nominal value, as RESPWRON is generated, and if the output voltage of MAIN is programmed to a higher value, which causes the output voltage to fall out of the 90% window, then a RESPWRON signal is generated.

The $\overline{\text{PWRFAIL}}$ signal indicates when VCC < UVLO or when the TPS65014 junction temperature has exceeded a reliable value or if BATT_COVER is taken low. This open-drain output can be connected at a fast interrupt pin for immediate attention by the application processor. All supplies are disabled $t_{(uvlo)}$, $t_{(overtemp)}$, or $t_{(batt\_cover)}$ seconds after $\overline{\text{PWRFAIL}}$ has gone low, giving time for the application processor to shut down cleanly.

BATT_COVER is used to detect whether the battery cover is in place or not. If the battery cover is removed, the TPS65014 generates a warning to the processor that the battery is likely to be removed and that it may be prudent to shut down the system. If not required, this feature may be disabled by connecting the BATT_COVER pin to the VCC pin. BATT_COVER is de-bounced internally. Typical de-bounce time is 56 ms. BATT_COVER has an internal 2-MΩ pulldown resistor.

The $\overline{\text{HOT\_RESET}}$ input is used to generate an $\overline{\text{MPU\_RESET}}$ signal for the application processor. The $\overline{\text{HOT\_RESET}}$ pin could be connected to a user-activated button in the application. It can also be used to exit low power mode. In this case, the TPS65014 waits until the VCORE voltage has stabilized before generating the $\overline{\text{MPU\_RESET}}$ pulse. The $\overline{\text{MPU\_RESET}}$ pulse is active low for $t_{(mpu\_nreset)}$ seconds. $\overline{\text{HOT\_RESET}}$ has an internal 1-MΩ pullup resistor to V_{CC}.

The PB_ONOFF input can be used to exit LOW POWER MODE. It is typically driven by a user-activated pushbutton in the application. Both $\overline{\text{HOT\_RESET}}$ and PB_ONOFF are de-bounced internally by the TPS65014. Typical debounce time is 56 ms. PB_ONOFF has an internal 1-MΩ pulldown resistor.

PB_ONOFF, BATT_COVER and UVLO events also cause a normal, maskable interrupt to be generated and are noted in the REGSTATUS register.

7.3.6 Vibrator Driver

The VIB open-drain output is provided to drive a vibrator motor, controlled through the serial interface register VDCDC2. It has a maximum dropout of 0.5 V at 100-mA load. Typically, an external resistor is required to limit the motor current and a freewheel diode to limit the VIB overshoot voltage at turnoff.

7.3.7 LED2 Output

The LED2 output can be programmed in the same way as the $\overline{\text{PG}}$ output to blink or to be permanently on or off. The LED2_ON and LED2_PER registers are used to control the blink rate. For both $\overline{\text{PG}}$ and LED2, the minimum blink-on time is 10 ms, and this can be increased in 127 10-ms steps to 1280 ms. For both $\overline{\text{PG}}$ and LED2, the minimum blink period is 100 ms, and this can be increased in 127 100-ms steps to 12800 ms.

7.3.8 Interrupt Management

The open-drain $\overline{\text{INT}}$ pin is used to combine and report all possible conditions through a single pin. Battery and chip temperature faults, precharge timeout, charge timeout, taper timeout, and termination current are each capable of setting $\overline{\text{INT}}$ low, that is, active. $\overline{\text{INT}}$ can also be activated if any of the regulators are below the regulation threshold. Interrupts can also be generated by any of the GPIO pins programmed to be inputs. These inputs can be programmed to generate an interrupt either at the rising or falling edge of the input signal. It is possible to mask an interrupt from any of these conditions individually by setting the appropriate bits in the MASK1, MASK2, or MASK3 registers. By default, all interrupts are masked. Interrupts are stored in the CHGSTATUS, REGSTATUS, and DEFGPIO registers in the serial interface. CHGSTATUS and REGSTATUS interrupts are acknowledged by reading these registers. If a 1 is present in any location, then the TPS65014 automatically sets the corresponding bit in the ACKINT1 or ACKINT2 registers and releases the $\overline{\text{INT}}$ pin. The ACKINT register contents are self-clearing when the condition, which caused the interrupt, is removed. The applications processor should not normally need to access the ACKINT1 or ACKINT2 registers.

Interrupt events are always captured; thus when an interrupt source is unmasked, $\overline{\text{INT}}$ may immediately go active due to a previous interrupt condition. This can be prevented by first reading the relevant STATUS register before unmasking the interrupt source.

If an interrupt condition occurs, then the $\overline{\text{INT}}$ pin is set low. The CHGSTATUS, REGSTATUS, and DEFGPIO registers should be read. Bit positions containing a 1 (or possibly a 0 in DEFGPIO) are noted by the CPU and the corresponding situation resolved. The reading of the CHGSTATUS and REGSTATUS registers automatically acknowledges any interrupt condition in those registers and blocks the path to the $\overline{\text{INT}}$ pin from the relevant bits. No interrupt should be missed during the read process because this process starts by latching the contents of the register before shifting them out at SDAT. Once the contents have been latched (which takes a couple of nanoseconds), the register is free to capture new interrupt conditions. Thus, for practical purposes the probability of missing anything is zero.

The following describes how registers 0x01 (CHGSTATUS) and 0x02 (REGSTATUS) are handled:

- CHGSTATUS(5,0) are positive edge set. Read of set CHGSTATUS(5,0) bits sets ACKINT1(5,0) bits.
- CHGSTATUS(7-6,4-1) are level set. Read of set CHGSTATUS(7-6,4-1) bits sets ACKINT1(7-6,4-1) bits.
- CHGSTATUS(5,0) clear when input signal low, and ACKINT1(5,0) bits are already set.
- CHGSTATUS(7-6,4-1) clear when input signal is low.
- ACKINT1(7-0) clear when CHGSTATUS(7-0) is clear.
- REGSTATUS(7-5) are positive edge set. Read of set REGSTATUS(7-5) bits sets ACKINT2(7-5) bits.
- REGSTATUS(3-0) are level set. Read of set REGSTATUS(3-0) bits sets ACKINT2(3-0) bits.
- REGSTATUS(7-5) clear when input signal low, and ACKINT1(7-5) bit are already set.
- REGSTATUS(3-0) clear when input signal is low.
- ACKINT2(7-0) clear when REGSTATUS(7-0) is clear.

The following describes the function of the 0x05 (ACKINT1) and 0x06 (ACKINT2) registers. These are not usually written to by the CPU because the TPS65014 internally sets/clears these registers:

- ACKINT1(7:0): Bit is set when the corresponding CHGSTATUS set bit is read through I^2C.
- ACKINT1(7:0): Bit is cleared when the corresponding CHGSTATUS set bit clears.
- ACKINT2(7:0): Bit is set when the corresponding REGSTATUS set bit is read through I^2C.
- ACKINT2(7:0): Bit is cleared when the corresponding REGSTATUS set bit clears.
- ACKINT1(7:0): A bit set masks the corresponding CHGSTATUS bit from $\overline{INT}$.
- ACKINT2(7:0): A bit set masks the corresponding REGSTATUS bit from $\overline{INT}$.

The following describes the function of the 0x03 (MASK1), 0x04 (MASK2) and 0x0F (MASK3) registers:

- MASK1(7:0): A bit set in this register masks CHGSTATUS from $\overline{INT}$.
- MASK2(7:0): A bit set in this register masks REGSTATUS from $\overline{INT}$.
- MASK3(7:4): A bit set in this register detects a rising edge on GPIO.
- MASK3(7:4): A bit cleared in this register detects a falling edge on GPIO.
- MASK3(3:0): A bit set in this register clears GPIO Detect signal from $\overline{INT}$.

GPIO interrupts are located by reading the 0x10 (DEFGPIO) register. The application CPU stores, or can read from DEFGPIO<7:4>, which GPIO is set to input or output. This information together with the information on which edge the interrupt was generated (the CPU either knows this or can read it from MASK3<7:4>) determines whether the CPU is looking for a 0 or a 1 in DEFGPIO<3:0>. A GPIO interrupt is blocked from the $\overline{INT}$ pin by setting the relevant MASK3<3:0> bit; this must be done by the CPU, there is no auto-acknowledge for the GPIO interrupts.

7.3.9 Serial Interface

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as V_{CC} remains above 2 V. The TPS65014 has a 7-bit address with the LSB set by the IFLSB pin; this allows the connection of two devices with the same address to the same bus. The 6 MSBs are 100100. Attempting to read data from register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65014 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65014 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65014 device must leave the data line high to enable the master to generate the stop condition.

The I^2C interface accepts data as soon as the voltage at V_{CC} is higher than the undervoltage lockout threshold and one power rail of the converter (main, core, or one of the LDOs) is operating. Therefore, the I^2C interface is not operating after applying the battery voltage as the device automatically enters the WAIT mode with all rails off.

When the device is in WAIT mode, the I^2C registers are reset to their default values if all voltage rails are off. If the device is in WAIT mode and one power rail is left on, the I^2C interface is operating and the registers are not reset after leaving the WAIT mode.

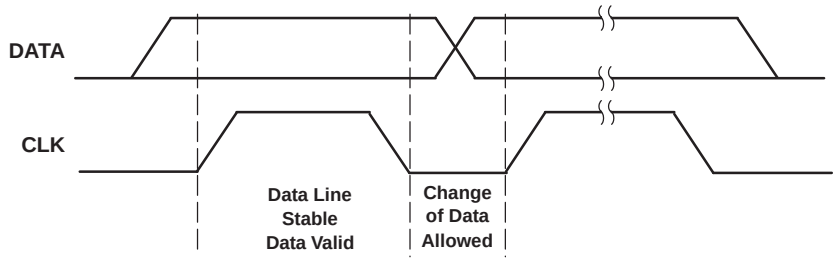


Figure 31. Bit Transfer on the Serial Interface

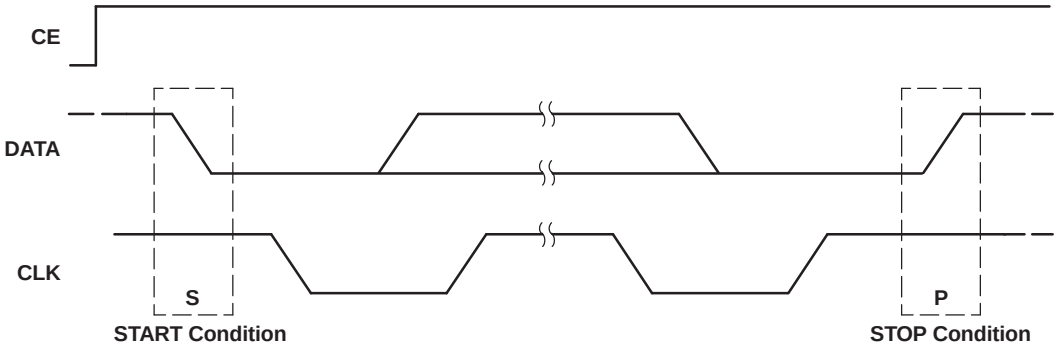
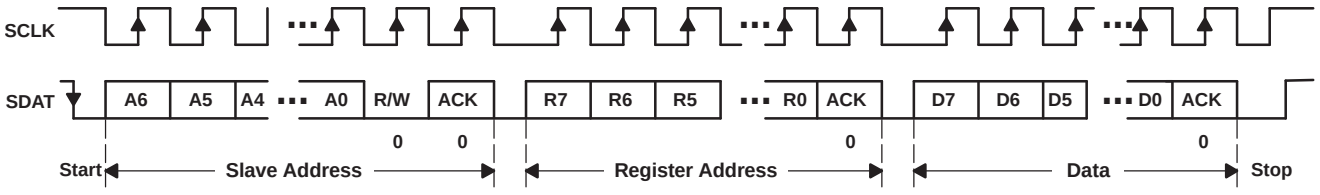
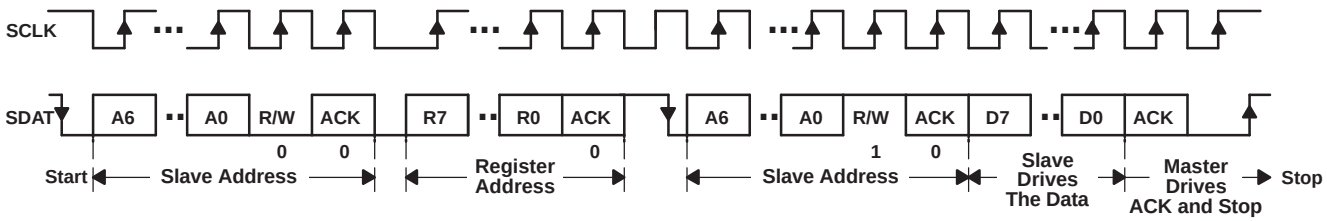


Figure 32. START and STOP Conditions



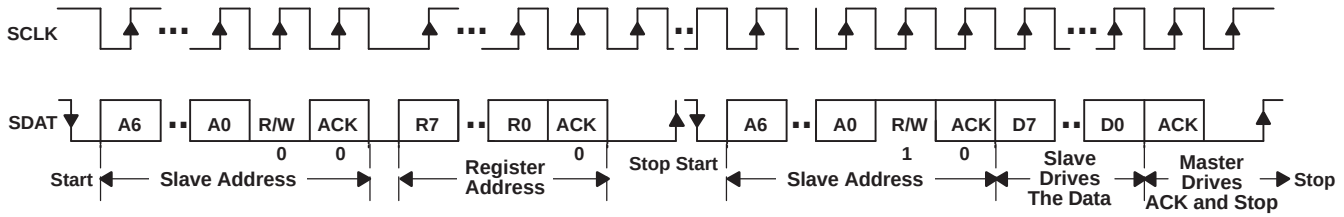
Note: SLAVE = TPS65014

Figure 33. Serial Interface WRITE to TPS65014 Device



Note: SLAVE = TPS65014

Figure 34. Serial Interface READ From TPS65014: Protocol A



Note: SLAVE = TPS65014

Figure 35. Serial Interface READ From TPS65014: Protocol B

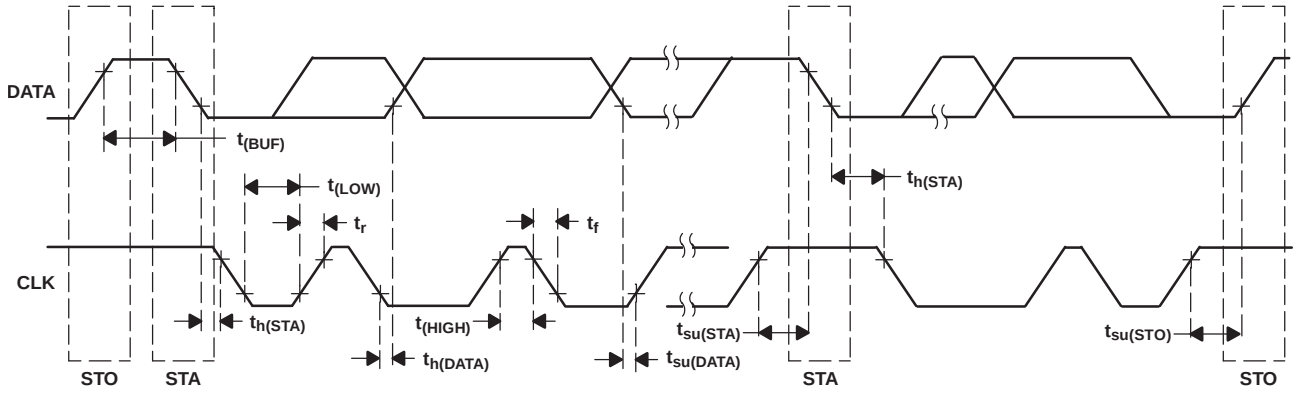


Figure 36. Serial Interface Timing Diagram

7.4 Device Functional Modes

7.4.1 Power Save Mode Operation

As the load current decreases, the converter enters the power-save mode operation. During power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

To optimize the converter efficiency at light load, the average current is monitored; if in PWM mode, the inductor current remains below a certain threshold, and then power-save mode is entered. The typical threshold can be calculated as in Equation 2:

$$I_{(skipmain)} = \frac{V_{I(MAIN)}}{17\ \Omega} \qquad I_{(skipcore)} = \frac{V_{I(CORE)}}{42\ \Omega} \tag{2}$$

During the power-save mode, the output voltage is monitored with the comparator by the thresholds comp low and comp high. As the output voltage falls below the comp low threshold, set to typically 0.8% above the nominal V_{out}, the P-channel switch turns on. The converter then runs at 50% of the nominal switching frequency. If the load is below the delivered current, then the output voltage rises until the comp high threshold is reached, typically 1.6% above the nominal V_{out}. At this point, all switching activity ceases, thus reducing the quiescent current to a minimum until the output voltage has dropped below comp low again. If the load current is greater than the delivered current, then the output voltage falls until it crosses the nominal output voltage threshold (comp low 2 threshold), whereupon power-save mode is exited, and the converter returns to PWM mode.

These control methods reduce the quiescent current typically to 12 µA per converter and the switching frequency to a minimum, achieving the highest converter efficiency. Setting the comparator thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic voltage positioning achieving lower absolute voltage drops during heavy load transient changes. This allows the converters to operate with a small output capacitor of just 10 µF for the core and 22 µF for the main output and still have a low absolute voltage drop during heavy load transient changes. See Figure 37 for detailed operation of the power-save mode. The power-save mode can be disabled through the I^2C interface to force the converters to stay in fixed frequency PWM mode.

Device Functional Modes (continued)

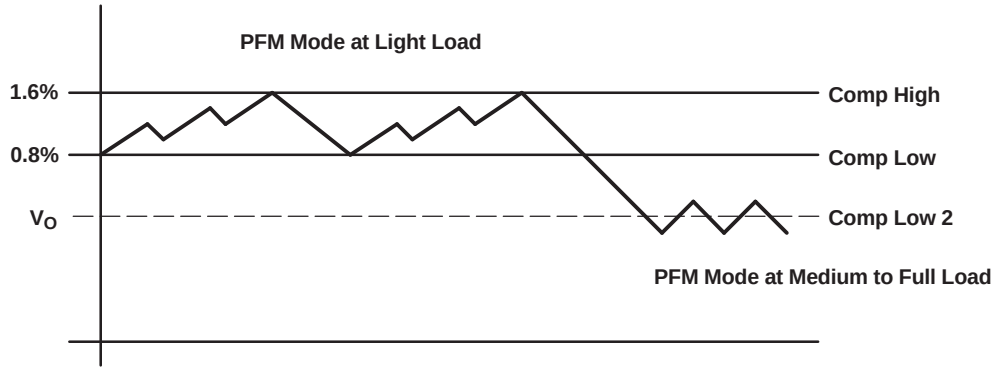


Figure 37. Power-Save Mode Thresholds and Dynamic Voltage Positioning

7.4.2 Sleep Mode

The TPS65014 charger enters the low-power sleep mode if both input sources are removed from the circuit. This feature prevents draining the battery during the absence of input power.

7.5 Register Maps

7.5.1 CHGSTATUS Register (offset = 01h) (reset: 00h)

Bits 1-4 may be reset through the serial interface in order to force a reset of the charger. Any attempt to write to Bit 0 and Bits 5-7 is ignored. A *1* in <7:0> sets the $\overline{INT}$ pin active unless the corresponding bit in the MASK register is set.

Figure 38. CHGSTATUS Register

7	6	5	4	3	2	1	0
USB Charge	AC Charge	Thermal Suspend	Term Current	Taper Timeout	Chg Timeout	Prechg Timeout	BattTemp Error
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. CHGSTATUS Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	USB charge	R	0h	0h = Inactive 1h = USB source is present and in the range valid for charging. B7 remains active as long as the charge source is present.
6	AC charge	R	0h	0h = Wall plug source is not present and/or not in the range valid for charging 1h = Wall plug source is present and in the range valid for charging. B6 remains active as long as the charge source is present.
5	Thermal suspend	R	0h	0h = Charging is allowed 1h = Charging is momentarily suspended due to excessive power dissipation on chip.
4	Term current	R	0h	0h = Charging, charge termination current threshold has not been crossed. 1h = Charge termination current threshold has been crossed and charging has been stopped. This can be due to a battery reaching full capacity, or to a battery removal condition.

Table 5. CHGSTATUS Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	Taper Timeout	R/W	0h	If CHCONFIG<5>=0: Bit 3 equals the output of the taper voltage comparator directly, without any timer delay. If CHCONFIG<5>=1: there is a delay of 30 minutes because the timers have to time out first. 0h = Charging, timers did not time out 1h = One of the timers has timed out and charging has been terminated.
2	Chg Timeout	R/W	0h	If CHCONFIG<5>=0: Bit 3 equals the output of the taper voltage comparator directly, without any timer delay. If CHCONFIG<5>=1: there is a delay of 30 minutes because the timers have to time out first. 0h = Charging, timers did not time out 1h = One of the timers has timed out and charging has been terminated.
1	Prechg Timeout	R/W	0h	If CHCONFIG<5>=0: Bit 3 equals the output of the taper voltage comparator directly, without any timer delay. If CHCONFIG<5>=1: there is a delay of 30 minutes because the timers have to time out first. 0h = Charging, timers did not time out 1h = One of the timers has timed out and charging has been terminated.
0	BattTempError	R	0h	Battery temperature error • 0 = Battery temperature is inside the allowed range and that charging is allowed. • 1 = Battery temperature is outside of the allowed range and that charging is suspended.

7.5.2 REGSTATUS Register (offset = 02h) (reset: 00h)

A rising edge in the REGSTATUS register contents causes $\overline{INT}$ to be driven low if it is not masked in the MASK2.

Figure 39. REGSTATUS Register

7	6	5	4	3	2	1	0
PB_ONOFF	BATT_COVER	UVLO	Rsvd	$\overline{PGOOD}$ LDO2	$\overline{PGOOD}$ LDO1	$\overline{PGOOD}$ MAIN	$\overline{PGOOD}$ CORE
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. REGSTATUS Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	PB_ONOFF	R	0h	0h = Inactive 1h = User activated the PB_ONOFF switch to request that all rails are shut down.
6	BATT_COVER	R	0h	0h = BATT_COVER pin is high 1h = BATT_COVER pin is low
5	UVLO	R	0h	0h = Voltage at the VCC pin above UVLO threshold 1h = Voltage at the VCC pin has dropped below the UVLO threshold
4	Reserved	R	0h	
3	$\overline{PGOOD}$ LDO2	R	0h	0h = LDO2 output in regulation, or LDO2 disabled with VREGS1 <7> = 0 1h = LDO2 output out of regulation
2	$\overline{PGOOD}$ LDO1	R	0h	0h = LDO1 output in regulation, or LDO1 disabled with VREGS1 <3> = 0 1h = LDO1 output out of regulation
1	$\overline{PGOOD}$ MAIN	R	0h	0h = Main converter output in regulation 1h = Main converter output out of regulation
0	$\overline{PGOOD}$ CORE	R	0h	0h = Core converter output in regulation 1h = Core converter output out of regulation, or VDCDC2 <7> = 1 in low power mode

7.5.3 MASK1 Register (offset = 03h) (reset: FFh)

The MASK1 register is used to mask all or any of the conditions in the corresponding CHGSTATUS<7:0> positions indicated at the $\overline{INT}$ pin. Default is to mask all.

Figure 40. MASK1 Register

7	6	5	4	3	2	1	0
Mask USB	Mask AC	Mask Thermal Suspend	Mask Term	Mask Taper	Mask Chg	Mask Prechg	Mask BattTemp
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. MASK1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Mask USB	R/W	1h	INT Mask for Bit 7 in CHGSTATUS register. Refer to Table 5.
6	Mask AC	R/W	1h	INT Mask for Bit 6 in CHGSTATUS register. Refer to Table 5.
5	Mask Thermal Suspend	R/W	1h	INT Mask for Bit 5 in CHGSTATUS register. Refer to Table 5.
4	Mask Term	R/W	1h	INT Mask for Bit 4 in CHGSTATUS register. Refer to Table 5.
3	Mask Taper	R/W	1h	INT Mask for Bit 3 in CHGSTATUS register. Refer to Table 5.
2	Mask Chg	R/W	1h	INT Mask for Bit 2 in CHGSTATUS register. Refer to Table 5.
1	Mask Prechg	R/W	1h	INT Mask for Bit 1 in CHGSTATUS register. Refer to Table 5.
0	Mask BattTemp	R/W	1h	INT Mask for Bit 0 in CHGSTATUS register. Refer to Table 5.

7.5.4 MASK2 Register (offset = 04h) (reset: FFh)

The MASK2 register is used to mask all or any of the conditions in the corresponding REGSTATUS<7:0> positions indicated at the $\overline{INT}$ pin. Default is to mask all.

Figure 41. MASK2 Register

7	6	5	4	3	2	1	0
Mask PB_ONOFF	Mask BATT_COVER	Mask UVLO	Rsvd	Mask $\overline{PGOOD}$ LDO2	Mask $\overline{PGOOD}$ LDO1	Mask $\overline{PGOOD}$ MAIN	Mask $\overline{PGOOD}$ CORE
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. MASK2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Mask PB_ONOFF	R/W	1h	INT Mask for Bit 7 in REGSTATUS register. Refer to Table 6.
6	Mask BATT_COVER	R/W	1h	INT Mask for Bit 6 in REGSTATUS register. Refer to Table 6.
5	Mask UVLO	R/W	1h	INT Mask for Bit 5 in REGSTATUS register. Refer to Table 6.
4	Reserved	R/W	1h	Reserved
3	Mask $\overline{PGOOD}$ LDO2	R/W	1h	INT Mask for Bit 3 in REGSTATUS register. Refer to Table 6.
2	Mask $\overline{PGOOD}$ LDO1	R/W	1h	INT Mask for Bit 2 in REGSTATUS register. Refer to Table 6.
1	Mask $\overline{PGOOD}$ MAIN	R/W	1h	INT Mask for Bit 1 in REGSTATUS register. Refer to Table 6.
0	Mask $\overline{PGOOD}$ CORE	R/W	1h	INT Mask for Bit 0 in REGSTATUS register. Refer to Table 6.

7.5.5 ACKINT1 Register (offset = 05h) (reset: 00h)

The ACKINT1 register is internally used to acknowledge any of the interrupts in the corresponding CHGSTATUS<7:0> positions. When this is done, the acknowledged interrupt is no longer fed through to the $\overline{INT}$ pin and so the $\overline{INT}$ pin becomes free to indicate the next pending interrupt. If none exists, then the $\overline{INT}$ pin goes high, else it will remain low. A *1* at any position in ACKINT1 is automatically cleared when the corresponding interrupt condition in CHGSTATUS is removed. The application processor should not normally need to access the ACKINT1 register.

Figure 42. ACKINT1 Register

7	6	5	4	3	2	1	0
Ack USB	Ack AC	Ack Thermal Shutdown	Ack Term	Ack Taper	Ack Chg	Ack Prechg	Ack BattTemp
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. ACKINT1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Ack USB	R	0h	Internal ack for Bit 7 in CHGSTATUS register. Refer to Table 5.
6	Ack AC	R	0h	Internal ack for Bit 6 in CHGSTATUS register. Refer to Table 5.
5	Ack Thermal Shutdown	R	0h	Internal ack for Bit 5 in CHGSTATUS register. Refer to Table 5.
4	Ack Term	R	0h	Internal ack for Bit 4 in CHGSTATUS register. Refer to Table 5.
3	Ack Taper	R	0h	Internal ack for Bit 3 in CHGSTATUS register. Refer to Table 5.
2	Ack Chg	R	0h	Internal ack for Bit 2 in CHGSTATUS register. Refer to Table 5.
1	Ack Prechg	R	0h	Internal ack for Bit 1 in CHGSTATUS register. Refer to Table 5.
0	Ack BattTemp	R	0h	Internal ack for Bit 0 in CHGSTATUS register. Refer to Table 5.

7.5.6 ACKINT2 Register (offset: 06h) (reset: 00h)

The ACKINT2 register is internally used to acknowledge any of the interrupts in the corresponding REGSTATUS<7:0> positions. When this is done, the acknowledged interrupt is no longer fed through to the $\overline{INT}$ pin and so the $\overline{INT}$ pin becomes free to indicate the next pending interrupt. If none exists, then the $\overline{INT}$ pin goes high, else it will remain low. A *1* at any position in ACKINT2 is automatically cleared when the corresponding interrupt condition in REGSTATUS is removed. The application processor should not normally need to access the ACKINT2 register.

Figure 43. ACKINT2 Register

7	6	5	4	3	2	1	0
Ack PB_ONOFF	Ack BATT_ COVER	Ack UVLO	Rsvd	Ack $\overline{PGOOD}$ LDO2	Ack $\overline{PGOOD}$ LDO1	Ack $\overline{PGOOD}$ MAIN	Ack $\overline{PGOOD}$ CORE
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. ACKINT2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Ack PB_ONOFF	R	0h	Internal ack for Bit 7 in REGSTATUS register. Refer to Table 6.
6	Ack BATT_ COVER	R	0h	Internal ack for Bit 6 in REGSTATUS register. Refer to Table 6.
5	Ack UVLO	R	0h	Internal ack for Bit 5 in REGSTATUS register. Refer to Table 6.
4	Reserved	R	0h	Reserved
3	Ack $\overline{PGOOD}$ LDO2	R	0h	Internal ack for Bit 3 in REGSTATUS register. Refer to Table 6.
2	Ack $\overline{PGOOD}$ LDO1	R	0h	Internal ack for Bit 2 in REGSTATUS register. Refer to Table 6.
1	Ack $\overline{PGOOD}$ MAIN	R	0h	Internal ack for Bit 1 in REGSTATUS register. Refer to Table 6.
0	Ack $\overline{PGOOD}$ CORE	R	0h	Internal ack for Bit 0 in REGSTATUS register. Refer to Table 6.

7.5.7 CHGCONFIG Register (offset: 07h) (reset: 1Bh)

The CHGCONFIG register is used to configure the charger.

Figure 44. CHGCONFIG Register

7	6	5	4	3	2	1	0
AUA	Charger reset	Fast charge timer + taper timer enabled	MSB charge current	LSB charge current	USB / 100 mA 500 mA	USB charge allowed	Charge enable
R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. CHGCONFIG Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	AUA	R/W	0h	0h = If a voltage is present at AC or USB in the appropriate range for charging, and if V_{CC} > UVLO, the TPS65014 is forced into ON mode. The WAIT mode is disabled. 1h = If a voltage source at AC or USB is present, the WAIT mode is enabled, and the TPS65014 does not automatically turn on the converters.
6	Charger reset	R/W	0h	Clears all the timers in the charger and forces a restart of the charge algorithm. 0/1 = This bit must be set and then reset through the serial interface.
5	Fast charge timer + taper timer enabled	R/W	0h	0h = Fast charge timer disabled (default), CHSTATUS <3>= status of the taper detect comparator output. 1h = Enables the fast charge timer and taper timer. CHSTATUS <3>= status of the taper timer.
4	MSB charge current	R/W	1h	Used to set the constant current in the current regulation phase. See Table 12.
3	LSB charge current	R/W	1h	Used to set the constant current in the current regulation phase. See Table 12.
2	USB / 100 mA 500 mA	R/W	0h	0h = Sets the USB charging current to max 100 mA. 1h = Sets the USB charging current to max 500 mA. B2 is ignored if B1 = 0.
1	USB charge allowed	R/W	1h	0h = Prevents any charging from the USB input. 1h = Charging from the USB input is allowed.
0	Charge enable	R/W	1h	0h = Charging is not allowed. 1h = Charger is free to charge from either of the two input sources. If both sources are present and valid, the TPS65014 charges from the AC pin source.

Table 12. Charge Current Rate

B4:B3	CHARGE CURRENT RATE
11	Maximum current set by the external resistor at the ISET pin
10	75% of maximum
01	50% of maximum
00	25% of maximum

7.5.8 LED1_ON Register (offset: 08h) (reset: 00h)

The LED1_ON and LED1_PER registers can be used to take control of the $\overline{PG}$ open-drain output normally controlled by the charger.

Figure 45. LED1_ON Register

7	6	5	4	3	2	1	0
$\overline{PG1}$	LED1 ON6	LED1 ON5	LED1 ON4	LED1 ON3	LED1 ON2	LED1 ON1	LED1 ON0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. LED1_ON Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	$\overline{PG1}$	R/W	0h	Control of the $\overline{PG}$ pin is determined by $\overline{PG1}$ and $\overline{PG2}$ according to the table under LED1_PER register
6-0	LED1 ONx	R/W	0h	LED1_ON[6:0] are used to program the on-time of the open-drain output transistor at the $\overline{PG}$ pin. The minimum on-time is typically 10 ms and one LSB corresponds to a 10-ms step change in the on-time.

7.5.9 LED1_PER Register (offset: 09h) (reset: 00h)

Figure 46. LED1_PER Register

7	6	5	4	3	2	1	0
$\overline{PG2}$	LED1 PER6	LED1 PER5	LED1 PER4	LED1 PER3	LED1 PER2	LED1 PER1	LED1 PER0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. LED1_PER Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	$\overline{PG2}$	R/W	0h	Control of the $\overline{PG}$ pin is determined by $\overline{PG1}$ and $\overline{PG2}$ according to Table 15. Default shown in **bold**.
6-0	LED1 PERx	R/W	0h	LED1_PER<6:0> are used to program the time period of the open-drain output transistor at the $\overline{PG}$ pin. The minimum period is typically 100 ms and one LSB corresponds to a 100-ms, step change in the period.

Table 15. Control of the $\overline{PG}$ Pin

$\overline{PG1}$	$\overline{PG2}$	BEHAVIOR OF $\overline{PG}$ OPEN-DRAIN OUTPUT
0	**0**	**Under charger control**
0	1	Blink
1	0	Off
1	1	Always On

7.5.10 LED2_ON Register (offset: 0Ah) (reset: 00h)

The LED2_ON and LED2_PER registers are used to control the LED2 open-drain output.

Figure 47. LED2_ON Register

7	6	5	4	3	2	1	0
LED21	LED2 ON6	LED2 ON5	LED2 ON4	LED2 ON3	LED2 ON2	LED2 ON1	LED2 ON0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. LED2_ON Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LED21	R/W	0h	Control is determined by LED21 and LED22 according to Table 18.
6-0	LED2 ONx	R/W	0h	LED2_ON<6:0> are used to program the on-time of the open-drain output transistor at the LED2 pin. The minimum on-time is typically 10 ms and one LSB corresponds to a 10-ms, step change in the on-time.

7.5.11 LED2_PER (offset: 0Bh) (reset: 00h)

Figure 48. LED2_PER Register

7	6	5	4	3	2	1	0
LED22	LED2 PER6	LED2 PER5	LED2 PER4	LED2 PER3	LED2 PER2	LED2 PER1	LED2 PER0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. LED2_PER Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LED22	R/W	0h	Control is determined by LED21 and LED22 according to Table 18.
6-0	LED2 PERx	R/W	0h	LED2_ON<6:0> are used to program the on-time of the open-drain output transistor at the LED2 pin. The minimum on-time is typically 100 ms and one LSB corresponds to a 100-ms, step change in the on-time.

Table 18. LED Control

LED21	LED22	BEHAVIOR OF LED2 OPEN-DRAIN OUTPUT
0	**0**	**Off**
0	1	Blink
1	0	Off
1	1	Always On

7.5.12 VDCDC1 Register (offset: 0Ch) (reset: 32h/33h)

The VDCDC1 register is used to program the VMAIN switching converter.

Figure 49. VDCDC1 Register

7	6	5	4	3	2	1	0
FPWM	UVLO1	UVLO0	ENABLE SUPPLY	ENABLE LP	MAIN DISCHARGE	MAIN1	MAIN0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. VDCDC1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	FPWM	R/W	0h	Forced PWM mode for DC-DC converters. 0h = MAIN and the CORE DC-DC converter are allowed to switch into PFM mode. 1h = MAIN and the CORE DC-DC converter operate with forced fixed-frequency PWM mode and are not allowed to switch into PFM mode, at light load.
6-5	UVLOx	R/W	0h	The undervoltage threshold voltage is set by UVLO1 and UVLO0 according to Table 20, with the default value in **bold**.
4	ENABLE SUPPLY	R/W	1h	Selects between LOW POWER mode and WAIT mode 0h = WAIT mode allowed, activated when LOW_PWR pin = 1 and VDCDC1 <3>= 1. 1h = The TPS65014 enters LOW POWER mode when LOW_PWR pin = 1 and VDCDC1 <3>= 1
3	ENABLE LP	R/W	0h	0h = Disables the low power function of the LOW_PWR pin 1h = Enables the low power function of the LOW_PWR pin.
2	MAIN DISCHARGE	R/W	0h	0h = disables the active discharge of the VMAIN converter output. 1h = enables the active discharge of the VMAIN converter output, when the converter is disabled (that is, in WAIT mode).
1-0	MAINx	R/W	1h	The VMAIN converter output voltages are set according to Table 21, with the default values in bold set by the DEFMAIN pin. The default voltage can subsequently be overwritten through the serial interface after start-up.

Table 20. Undervoltage Threshold Voltage

UVLO1	UVLO0	V_{UVLO}
0	0	2.5 V
0	1	2.75 V
1	0	3.0 V
1	1	3.25 V

Table 21. VMAIN Converter Output Voltage

MAIN1	MAIN0	VMAIN
0	0	2.5 V
0	1	2.75 V
1	0	3.0 V
1	1	3.3 V

7.5.13 VDCDC2 Register (offset: 0Dh) (reset: 60h/70h)

The VDCDC2 register is used to program the VCORE switching converter output voltage. It is programmable in 8 steps between 0.85 V and 1.8 V. The default value is governed by the DEFCORE pin; DEFCORE=0 sets an output voltage of 1.5 V. DEFCORE=1 sets an output voltage of 1.8 V.

Figure 50. VDCDC2 Register

7	6	5	4	3	2	1	0
LP_COREOFF	CORE2	CORE1	CORE0	CORELP1	CORELP0	VIB	CORE DISCHARGE
R/W-0	R/W-1	R/W-1	R/W-DEFCORE	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. VDCDC2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LP_COREOFF	R/W	0h	0h = VCORE converter is enabled in low power mode. 1h = VCORE converter is disabled in low power mode.
6-5	COREx	R/W	1h	Table 23 shows all possible values of VCORE. The default value can subsequently be overwritten through the serial interface after start-up.
4	CORE0	R/W	DEFCORE	Table 23 shows all possible values of VCORE. The default value can subsequently be overwritten through the serial interface after start-up.
3	CORELP1	R/W	1h	CORELP1 and CORELP0 can be used to set the VCORE voltage in low power mode. In low power mode, CORE2 is effectively *0*, and CORE1, CORE0 take on the values programmed at CORELP1 and CORELP0, default *10* giving VCORE = 1.1 V as default in low power mode. When low power mode is exited, VCORE reverts to the value set by CORE2, CORE1, and CORE0.
2	CORELP0	R/W	0h	CORELP1 and CORELP0 can be used to set the VCORE voltage in low power mode. In low power mode, CORE2 is effectively *0*, and CORE1, CORE0 take on the values programmed at CORELP1 and CORELP0, default *10* giving VCORE = 1.1 V as default in low power mode. When low power mode is exited, VCORE reverts to the value set by CORE2, CORE1, and CORE0.
1	VIB	R/W	0h	0h = Disables the VIB output transistor 1h = Enables the VIB output transistor to drive the vibrator motor.
0	CORE DISCHARGE	R/W	0h	0h = Disables the active discharge of the VCORE converter output. 1h = Enables the active discharge of the VCORE converter output in WAIT mode, or if VDCDC2 <7>= 1 in LOW POWER mode.

Table 23. VCORE Values

CORE2	CORE1	CORE0	VCORE
0	0	0	0.85 V
0	0	1	1.0 V
0	1	0	1.1 V
0	1	1	1.2 V
1	0	0	1.3 V
1	0	1	1.4 V
1	1	0	1.5 V
1	1	1	1.8 V

7.5.14 VREGS1 Register (offset: 0Eh) (reset: 88h)

The VREGS1 register is used to program and enable LDO1 and LDO2 and to set their behavior when low power mode is active. The LDO output voltages can be set either on the fly, while the relevant LDO is disabled, or simultaneously when the relevant enable bit is set. Note that both LDOs are per default ON.

Figure 51. VREGS1 Register

7	6	5	4	3	2	1	0
LDO2 enable	LDO2 OFF/ nSLP	LDO21	LDO20	LDO1 enable	LDO1 OFF/ nSLP	LDO11	LDO10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. VREGS1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LDO2 enable	R/W	1h	The function of the LDO2 enable and LDO2 OFF/nSLP bits is shown in Table 25. See the power-on sequencing section for details of low power mode.
6	LDO2 OFF / nSLP	R/W	0h	The function of the LDO2 enable and LDO2 OFF/nSLP bits is shown in Table 25. See the power-on sequencing section for details of low power mode.
5-4	LDO2x	R/W	0h	LDO2 has a default output voltage of 1.8 V. If desired, this can be changed at the same time as it is enabled through the serial interface. See Table 26.
3	LDO1 enable	R/W	1h	The function of the LDO1 enable and LDO1 OFF/nSLP bits is shown in Table 27. See the power-on sequencing section for details of low-power mode. Note that programming LDO1 to a higher voltage may force a system power-on reset if the increase is in the 10% or greater range.
2	LDO1 OFF / nSLP	R/W	0h	The function of the LDO1 enable and LDO1 OFF/nSLP bits is shown in Table 27. See the power-on sequencing section for details of low-power mode. Note that programming LDO1 to a higher voltage may force a system power-on reset if the increase is in the 10% or greater range.
1-0	LDO1x	R/W	0h	The LDO1 output voltage is per default set externally. If so desired, this can be changed through the serial interface. See Table 28.

Table 25. LDO2 Enable and LDO2 OFF/nSLP Functions

LDO2 ENABLE	LDO2 OFF / nSLP	LDO STATUS IN NORMAL MODE	LDO STATUS IN LOW-POWER MODE
0	X	OFF	OFF
1	0	ON, full power	ON, reduced power and performance
1	1	ON, full power	OFF

Table 26. LDO21/LDO20

LDO21	LDO20	VLDO2
0	0	1.8 V
0	1	2.5 V
1	0	3.0 V
1	1	3.3 V

Table 27. LDO1 Enable and LDO1 OFF/nSLP Functions

LDO1 ENABLE	LDO1 OFF / nSLP	LDO STATUS IN NORMAL MODE	LDO STATUS IN LOW-POWER MODE
0	X	OFF	OFF
1	0	ON, full power	ON, reduced power and performance
1	1	ON, full power	OFF

Table 28. LDO11/LDO10

LDO11	LDO10	VLDO1
0	0	ADJ
0	1	2.5 V
1	0	2.75 V
1	1	3.0 V

7.5.15 MASK3 Register (offset: 0Fh) (reset: 00h)

The MASK3 register must be considered when any of the GPIO pins are programmed as inputs.

Figure 52. MASK3 Register

7	6	5	4	3	2	1	0
Edge trigger GPIO4	Edge trigger GPIO3	Edge trigger GPIO2	Edge trigger GPIO1	Mask GPIO4	Mask GPIO3	Mask GPIO2	Mask GPIO1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. MASK3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-4	Edge trigger GPIOx	R/W	0h	Determines whether the respective GPIO generates an interrupt at a rising or a falling edge. 0h = Falling edge triggered. 1h = Rising edge triggered.
3-0	Mask GPIOx	R/W	0h	Used to mask the corresponding interrupt. Default is unmasked (mask GPIOx = 0).

7.5.16 DEFGPIO Register (offset = 10h) (reset: 00h)

The DEFGPIO register is used to define the GPIO pins to be either input or output.

Figure 53. DEFGPIO Register

7	6	5	4	3	2	1	0
IO4	IO3	IO2	IO1	Value GPIO4	Value GPIO3	Value GPIO2	Value GPIO1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. DEFGPIO Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-4	IOx	R/W	0h	0h = Sets the corresponding GPIO to be an input. 1h = Sets the corresponding GPIO to be an output.
3-0	Value GPIOx	R/W	0h	If a GPIO is programmed to be an output, then the signal output is determined by the corresponding bit. The output circuit for each GPIO is an open-drain NMOS requiring an external pullup resistor. 1h = Activates the relevant NMOS, hence forcing a logic low signal at the GPIO pin. 0h = Turns the open-drain transistor OFF, hence the voltage at the GPIO pin is determined by the voltage to which the pullup resistor is connected. If a particular GPIO is programmed to be an input, then the contents of the relevant bit in B3-0 is defined by the logic level at the GPIO pin. A logic low forces a *0* and a logic high forces a *1*. If a GPIO is programmed to be an input, then any attempt to write to the relevant bit in B3-0 is ignored.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65014 is an integrated power- and battery-management IC designed to pair with various application processors powered by one Li-ion or Li-polymer cell and which require multiple rails.

8.2 Typical Application

The VCORE and VMAIN converter are always enabled in a typical application. The VCORE output voltage can be disabled or reduced from 1.5 V to a lower, preset voltage under processor control. When the processor enters the sleep mode, a high signal on the LOW_PWR pin initiates the change.

VCORE typically supplies the digital part of the audio codec. When the processor is in sleep or low-power mode, the audio codec is powered off, so the VCORE voltage can be programmed to lower voltages without a problem. A typical audio codec (such as the TI AIC23) consumes about 20-mA to 30-mA current from the VCORE power supply.

Supply LDO1 from VMAIN as shown in Figure 54. If this is not done, then subsequent to a UVLO, OVERTEMP, or BATT_COVER = 0 condition, the $\overline{\text{RESPWRON}}$ signal goes high before the VCORE rail has ramped and stabilized. Therefore, the processor core does not receive a power-on-reset signal.

Typical Application (continued)

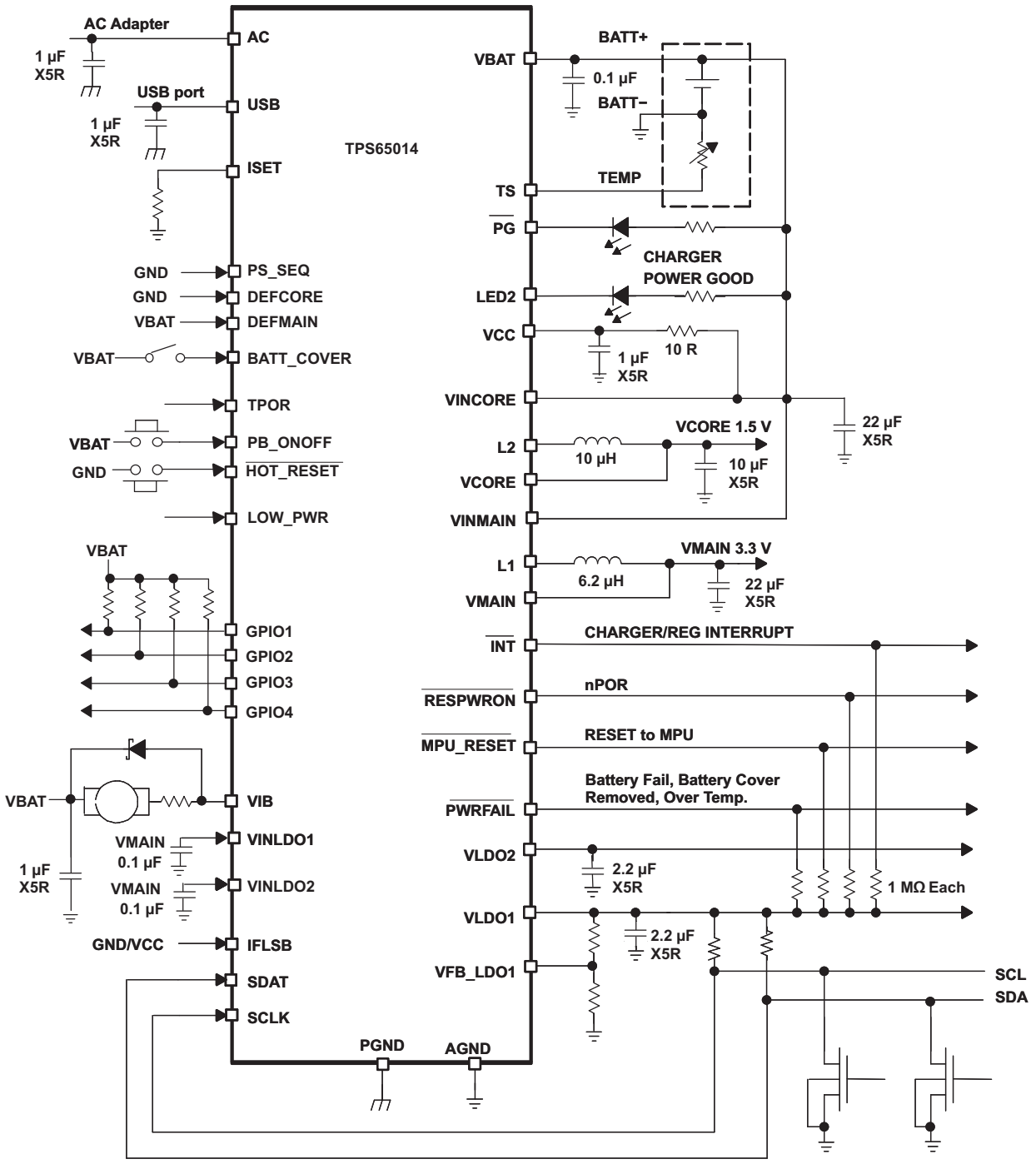


Figure 54. Typical Application Circuit

Typical Application (continued)

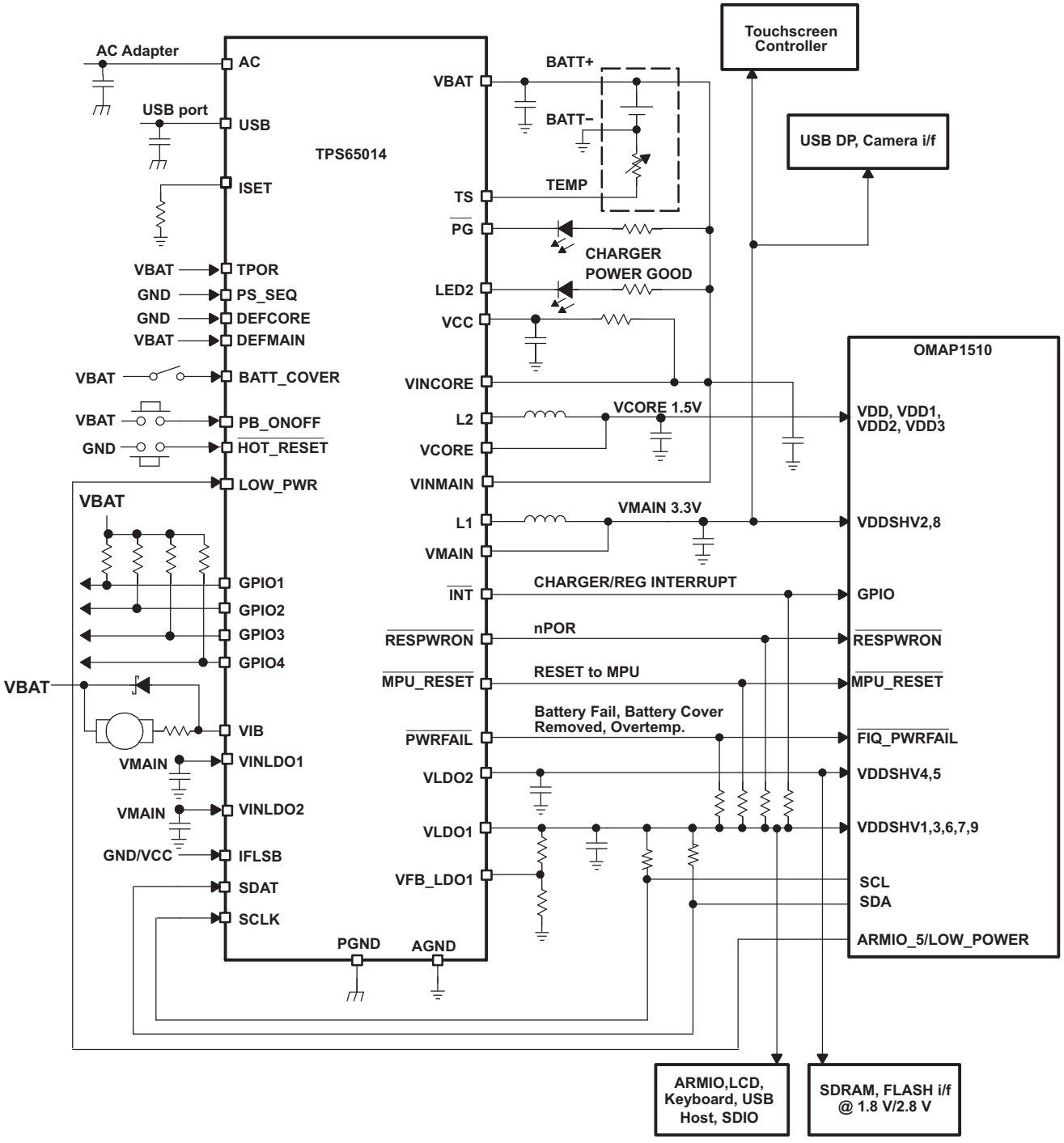


Figure 55. Typical Application Circuit in Low-Power Mode

8.2.1 Design Requirements

Each DC-DC converter requires an external inductor and filter capacitor, capable of sustaining the intended current with an acceptable voltage ripple. LDOs must have external filter capacitors, and LDO1 requires an external feedback network for regulation. Every input supply rail requires a decoupling capacitor close to the pin. To avoid unintended states, logic inputs without internal resistors must not be left floating.

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection for the Main and the Core Converter

The main and the core converters in the TPS65014 typically use a 6.2-µH and a 10-µH output inductor, respectively. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance is selected for highest efficiency.

Equation 3 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 3. This is necessary because during heavy load transient, the inductor current rises above the value calculated in Equation 4.

$$\Delta I_L = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \tag{3}$$

$$I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \tag{4}$$

where

- f = Switching frequency (1.25-MHz typical)
- L = Inductor value
- ΔI_L= Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

The highest inductor current occurs at maximum V_I.

Open core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65014 (2 A for the main converter and 0.8 A for the core converter). The core material from inductor to inductor differs and has an impact on the efficiency, especially at high switching frequencies.

See Table 31 and the typical applications for possible inductors

Table 31. Tested Inductors

DEVICE	INDUCTOR VALUE	DIMENSIONS	COMPONENT SUPPLIER
Core converter	10 µH	6 mm × 6 mm × 2 mm	Sumida CDRH5D18-100
	10 µH	5 mm × 5 mm × 3 mm	Sumida CDRH4D28-100
Main converter	4.7 µH	5.5 mm × 6.6 mm x 1 mm	Coilcraft LPO1704-472M
	4.7 µH	5 mm × 5 mm × 3 mm	Sumida CDRH4D28C-4.7
	4.7 µH	5.2 mm × 5.2 mm × 2.5 mm	Coiltronics SD25-4R7
	5.3 µH	5.7 mm × 5.7 mm × 3 mm	Sumida CDRH5D28-5R3
	6.2 µH	5.7 mm × 5.7 mm × 3 mm	Sumida CDRH5D28-6R2
	6 µH	7 mm × 7 mm × 3 mm	Sumida CDRH6D28-6R0

8.2.2.2 Output Capacitor Selection

The advanced fast response voltage-mode control scheme of the inductive converters implemented in the TPS65014 allows the use of small ceramic capacitors with a typical value of 22 µF for the main converter and 10 µF for the core converter, without having large output voltage undershoots and overshoots during heavy load transients. TI recommends ceramic capacitors with low ESR values and the lowest output voltage ripple. If required, tantalum capacitors with an ESR < 100 Ω may be used as well.

See Table 32 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meet the application requirements. For completeness, the RMS ripple current is calculated as in Equation 5:

$$I_{RMSC(out)} = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

At nominal load current, the inductive converters operate in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor, as in Equation 6:

$$\Delta V_O = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \quad (6)$$

Where the highest output voltage ripple occurs at the highest input voltage V_I.

At light load currents, the converters operate in power save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the nominal output voltage. If the output voltage for the core converter is programmed to its lowest voltage of 0.85 V, the output capacitor must be increased to 22 µF for low output voltage ripple. This is because the current in the inductor decreases slowly during the off-time and further increases the output voltage, even when the PMOS is off. This effect increases with low output voltages.

8.2.2.3 Input Capacitor Selection

A pulsating input current is the nature of the buck converter. Therefore, a low ESR input capacitor is required for best input voltage filtering. It also minimizes the interference with other circuits caused by high input voltage spikes. The main converter requires a 22-µF ceramic input capacitor, and the core converter requires a 10-µF ceramic capacitor. The input capacitor for the main and the core converter can be combined and one 22-µF capacitor can be used instead, because the two converters operate with a phase shift of 270 degrees. The input capacitor can be increased without any limit for better input voltage filtering. The VCC pin should be separated from the input for the main and the core converter. A filter resistor of up to 100 Ω and a 1-µF capacitor is used for decoupling the VCC pin from switching noise.

Table 32. Possible Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	1206	TDK C3216X5R0J226M	Ceramic
22 µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 µF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

8.2.3 Application Curves

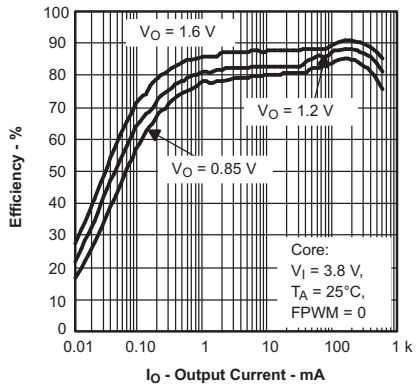


Figure 56. Efficiency vs Output Current

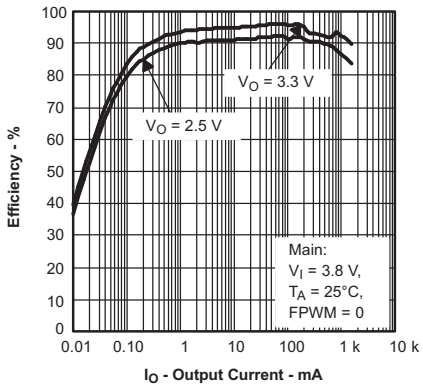


Figure 57. Efficiency vs Output Current

9 Power Supply Recommendations

9.1 Battery Charger

The TPS65014 supports a precision Li-ion or Li-polymer charging system suitable for single cells with either coke or graphite anodes. Charging the battery is possible even without the application processor being powered up. The TPS65014 starts charging when an input voltage on either AC or USB input is present, which is greater than the charger UVLO threshold. See Figure 58 for a typical charge profile.

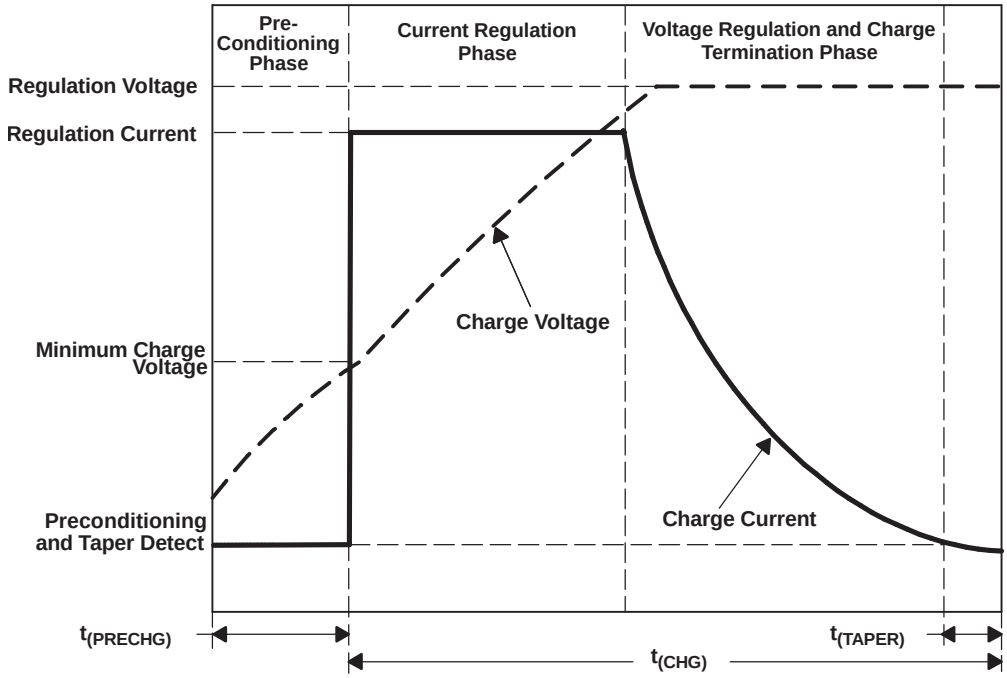


Figure 58. Typical Charging Profile

9.1.1 Autonomous Power Source Selection

By default, the TPS65014 attempts to charge from the AC input. If AC input is not present, USB is selected. If both inputs are available, the AC input has priority. The charge current is initially limited to 100 mA when charging from the USB input. This can be increased to 500 mA through the serial interface. The charger can be completely disabled through the interface or from the USB port. The start of the charging process from the USB port is delayed to allow the application processor time to disable USB charging, for instance if a USB OTG port is recognized. The recommended input voltage for charging from the AC input is 4.5 V < VAC < 6.5 V. However, the TPS65014 is capable of withstanding (but not charging from) up to 20 V. Charging is disabled if VAC is greater than typically 7 V.

9.1.2 Temperature Qualification

The TPS65014 continuously monitors battery temperature by measuring the voltage between the TS and AGND pins. An internal current source provides the bias for most common 10K negative-temperature coefficient thermistors (NTC) (see Figure 59). The IC compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected, the IC immediately suspends the charge. The IC suspends charge by turning off the power FET and holding the timer value (that is, timers are *not* reset). Charge is resumed when the temperature returns to the normal range.

The allowed temperature range for a 103-A T-type thermistor is 0°C to +45°C. However, the user may modify these thresholds by adding two external resistors (see Figure 60).

Battery Charger (continued)

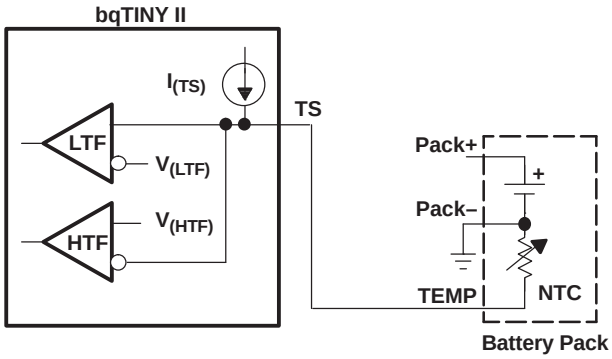


Figure 59. TS Pin Configuration

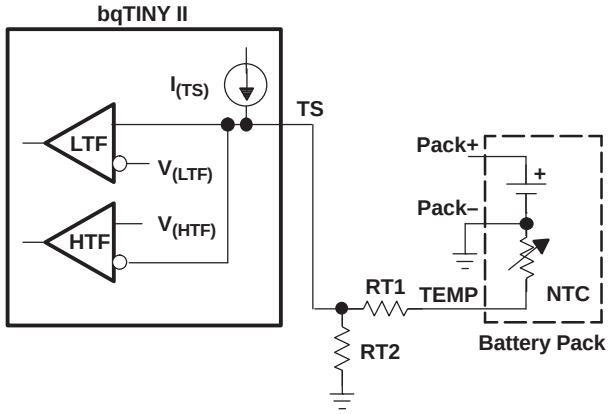


Figure 60. TS Pin Threshold

9.1.3 Battery Preconditioning

On power up, if the battery voltage is below the $V_{(LOWV)}$ threshold, the TPS65014 applies a precharge current, $I_{(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The charge current during this phase is one tenth of the value in current regulation phase, which is set with $I_{O(out)}$ = KSET × $V_{(SET)}$ / $R_{(SET)}$. The load current in the preconditioning phase must be lower than $I_{(PRECHG)}$ and must allow the battery voltage to rise above $V_{(LOWV)}$ within $t_{(Prechg)}$. VBAT_A is the sense pin to the voltage comparator for the battery voltage. This allows a power-on sense measurement if the VBAT_A and VBAT_B pins are connected together at the battery.

The TPS65014 activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the TPS65014 turns off the charger and indicates the fault condition in the CHGSTATUS register. In the case of a fault condition, the TPS65014 reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$ is used to detect a battery replacement condition. Fault condition is cleared by POR or battery replacement or through the serial interface.

9.1.4 Battery Charge Current

The TPS65014 offers on-chip current regulation. When charging from an AC adapter, a resistor connected between the ISET1 and AGND pins determines the charge rate. A maximum of 1-A charger current from the AC adapter is allowed. When charging from a USB port, either a 100-mA or 500-mA charge rate can be selected through the serial interface; default is 100-mA maximum. Two bits are available in the CHGCONFIG register in the serial interface to reduce the charge current in 25% steps. These only influence charging from the AC input, and may be of use if charging is often suspended due to excessive junction temperature in the TPS65014 (such as at high AC input voltages) and low battery voltages.

Battery Charger (continued)

9.1.5 Battery Voltage Regulation

The voltage regulation feedback is through the VBAT pin. This pin is tied directly to the positive side of the battery pack. The TPS65014 monitors the battery-pack voltage between the VBAT and AGND pins. The TPS65014 is offered in a fixed-voltage version of 4.2 V.

As a safety backup, the TPS65014 also monitors the charge time in the fast-charge mode. If taper current is not detected within this time period, $t_{(CHG)}$, the TPS65014 turns off the charger and indicates FAULT in the CHGSTATUS register. In the case of a FAULT condition, the TPS65014 reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$ is used to detect a battery replacement condition. Fault condition is cleared by POR through the serial interface. The safety timer is reset if the TPS65014 is forced out of the voltage regulation mode. The fast-charge timer is disabled by default to allow charging during normal operation of the end equipment. It is enabled through the CHGCONFIG register.

9.1.6 Charge Termination and Recharge

The TPS65014 monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected, the TPS65014 initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The TPS65014 resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$. After a charge termination, the TPS65014 restarts the charge once the voltage on the VBAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times. The fast charge timer and the taper timer must be enabled by programming CHGCONFIG(5)=1. A thermal suspend suspends the fast-charge and taper timers.

In addition to the taper current detection, the TPS65014 terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition. When a full battery is replaced with an empty battery, the TPS65014 detects that the VBAT voltage is below the recharge threshold and starts charging the new battery. The taper and termination bits are cleared in the CHGSTATUS register and if the $\overline{INT}$ pin is still active due to these two interrupt sources, then it is de-asserted. Depending on the transient seen at the VCC pin, all registers may be set to their default values and require reprogramming with any nondefault values required, such as enabling the fast-charge timer and taper termination; this should only happen if VCC drops below approximately 2 V.

9.1.7 $\overline{PG}$ Output

The open-drain, power-good ($\overline{PG}$) output indicates when a valid power supply is present for the charger. This can be either from the AC adapter input or from the USB. The output turns ON when a valid voltage is detected. A valid voltage is detected whenever the voltage on either pin AC or pin USB rises above the voltage on VBAT plus 100 mV. This output is turned off in the sleep mode. The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor. A voltage greater than the $V_{(CHGOVLO)}$ threshold (typ 7-V) at the AC input is not valid and does not activate the $\overline{PG}$ output. The $\overline{PG}$ output is held in high impedance state if the charger is in reset by programming CHGCONFIG(6)=1.

The $\overline{PG}$ output can also be programmed through the LED1_ON and LED1_PER registers in the serial interface. It can then be programmed to be permanently on, off, or to blink with defined on- and period-times. $\overline{PG}$ is controlled by default through the charger.

9.1.8 Thermal Considerations for Setting Charge Current

The TPS65014 is housed in a 48-pin QFN package with exposed leadframe on the underside. This 7-mm × 7-mm package exhibits a thermal impedance (junction-to-ambient) of 33 K/W when mounted on a JEDEC high-k board with zero air flow. Refer to Table 33 for maximum charge current considerations.

Table 33. Power Dissipation Limitations

AMBIENT TEMPERATURE	MAX POWER DISSIPATION FOR T_j = 125°C
25°C	3 W
55°C	2.1 W
Above 55°C	30 mW/°C

Consideration must be given to the maximum charge current when the assembled application board exhibits a thermal impedance, which differs significantly from the JEDEC high-k board. The charger has a thermal shutdown feature, which suspends charging if the TPS65014 junction temperature rises above a threshold of 145°C. This threshold is set 15°C below the threshold used to power down the TPS65014 completely.

9.2 LDO1 Output Voltage Adjustment

The output voltage of LDO1 is set with a resistor divider at the feedback pin. The sum of the two resistors must not exceed 1 MΩ to minimize voltage changes due to leakage current into the feedback pin. The output voltage for LDO1 after start-up is the voltage set by the external resistor divider. It can be reprogrammed with the I^2C interface to the three other values defined in the register VREGS1.

10 Layout

10.1 Layout Guidelines

- The input capacitors for the DC-DC converters must be placed as close as possible to the VINMAIN, VINCORE, and VCC pins.
- The inductor of the output filter must be placed as close as possible to the device to provide the shortest switch node possible, thus reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback must be routed away from noisy sources such as the inductor. If possible, route on the opposite side from the switch node and inductor, and place a GND plane between the feedback and the noisy sources or keepout underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop. This ensures best regulation at the feedback point.
- Place the device as close as possible to the most demanding or sensitive load. The output capacitors must be placed close to the input of the load, which ensures the best AC performance possible.
- The input and output capacitors for the LDOs must be placed close to the device for best regulation performance.
- Use vias to connect the thermal pad to the ground plane.
- TI recommends using the common ground plane for the layout of this device. The AGND can be separated from the PGND, but a large low-parasitic PGND is required to connect the PGNDx pins to the CIN and external PGND connections. If the AGND and PGND planes are separated, have one connection point to reference the grounds together. Place this connection point close to the IC.

10.2 Layout Example

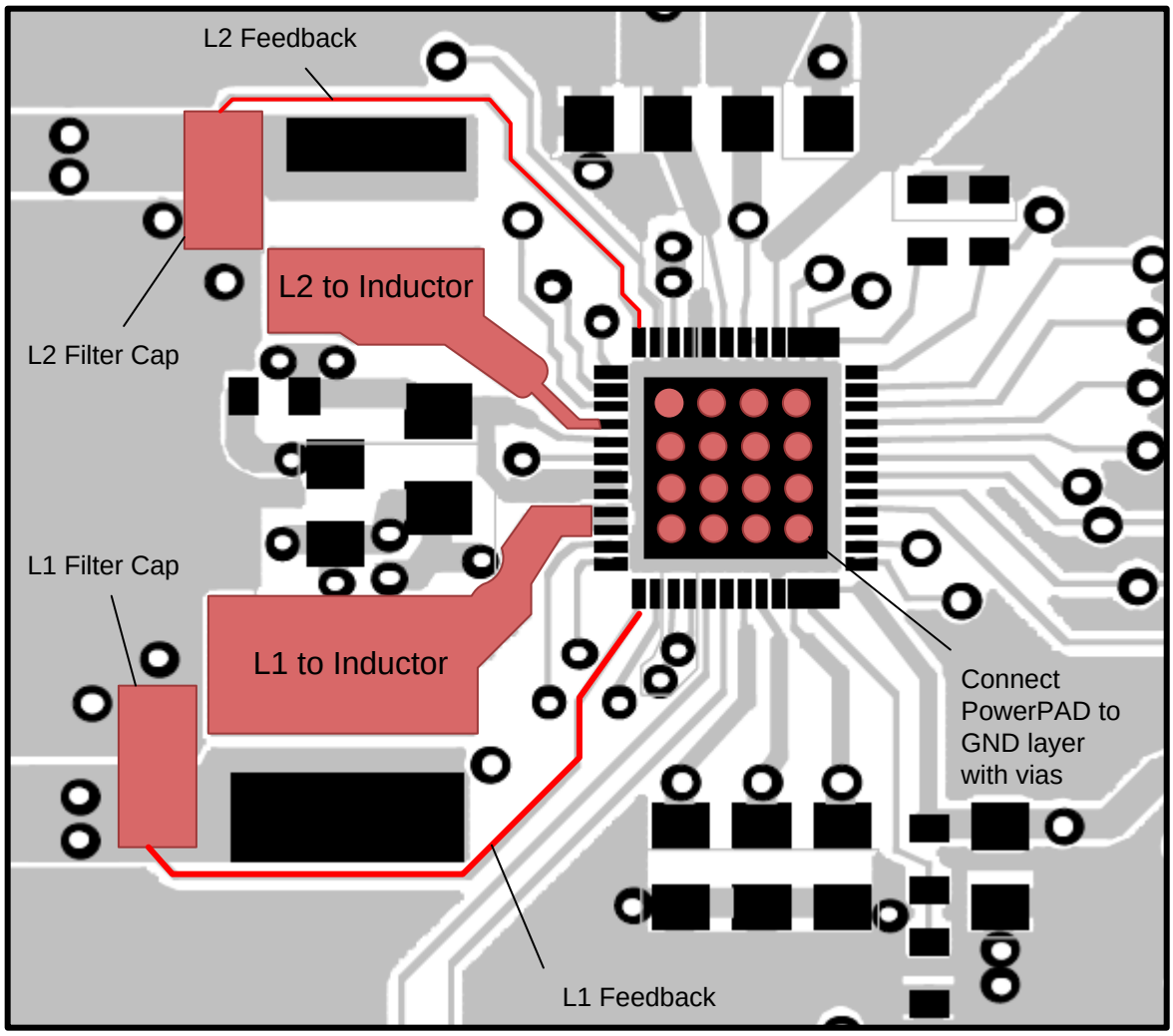


Figure 61. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65014RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65014	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

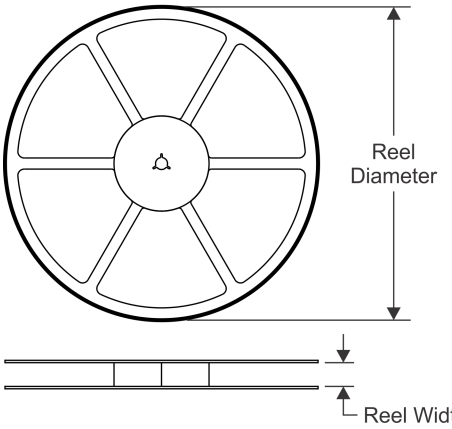
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

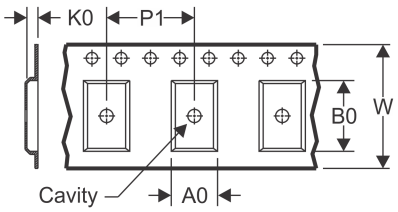
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

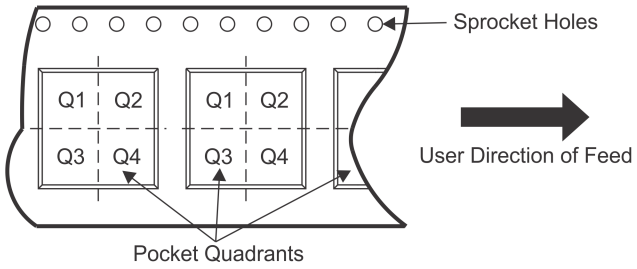


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

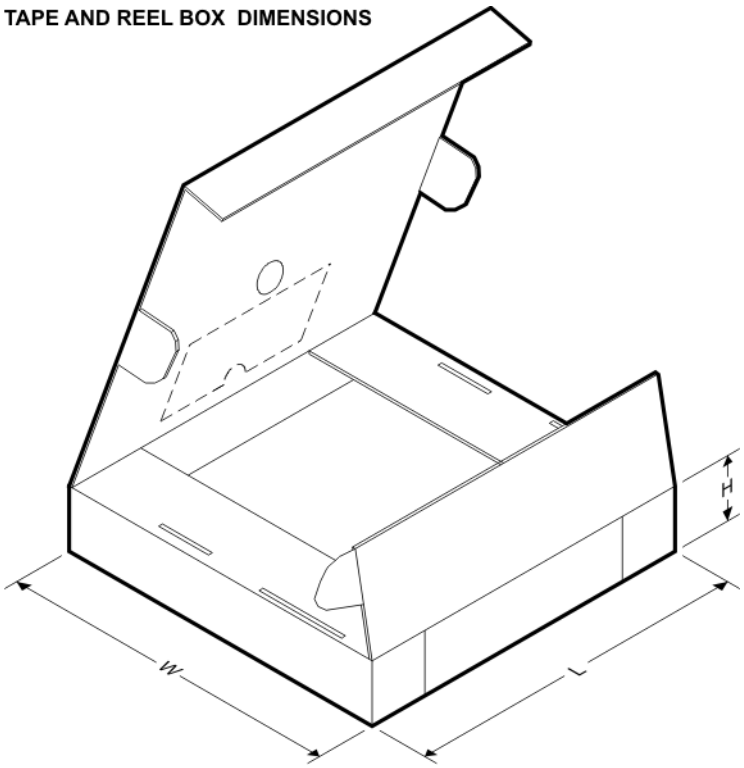
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65014RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65014RGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

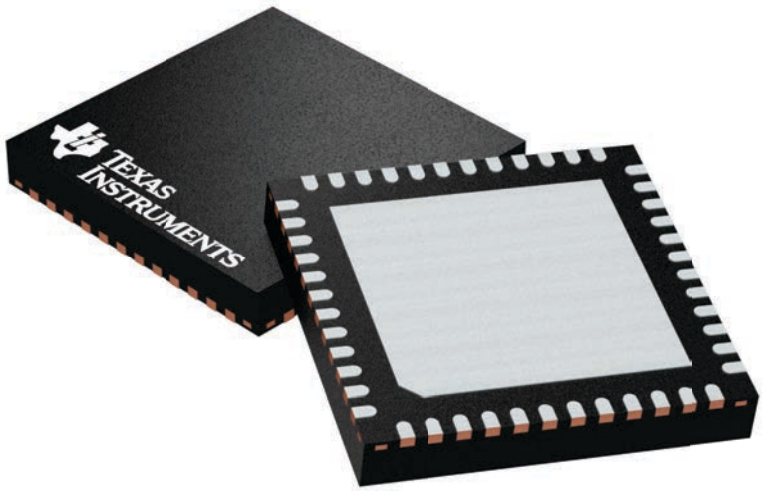
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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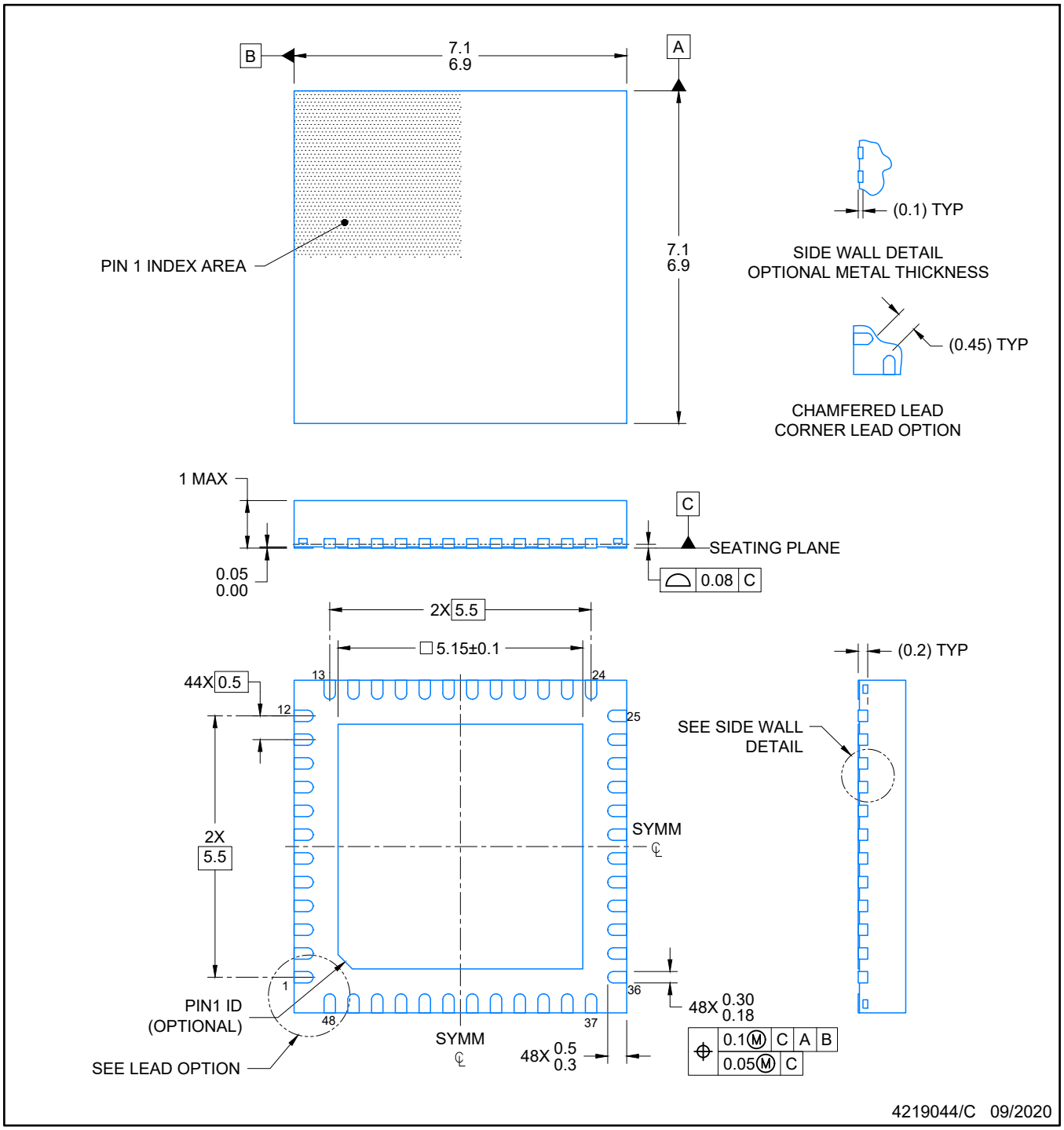
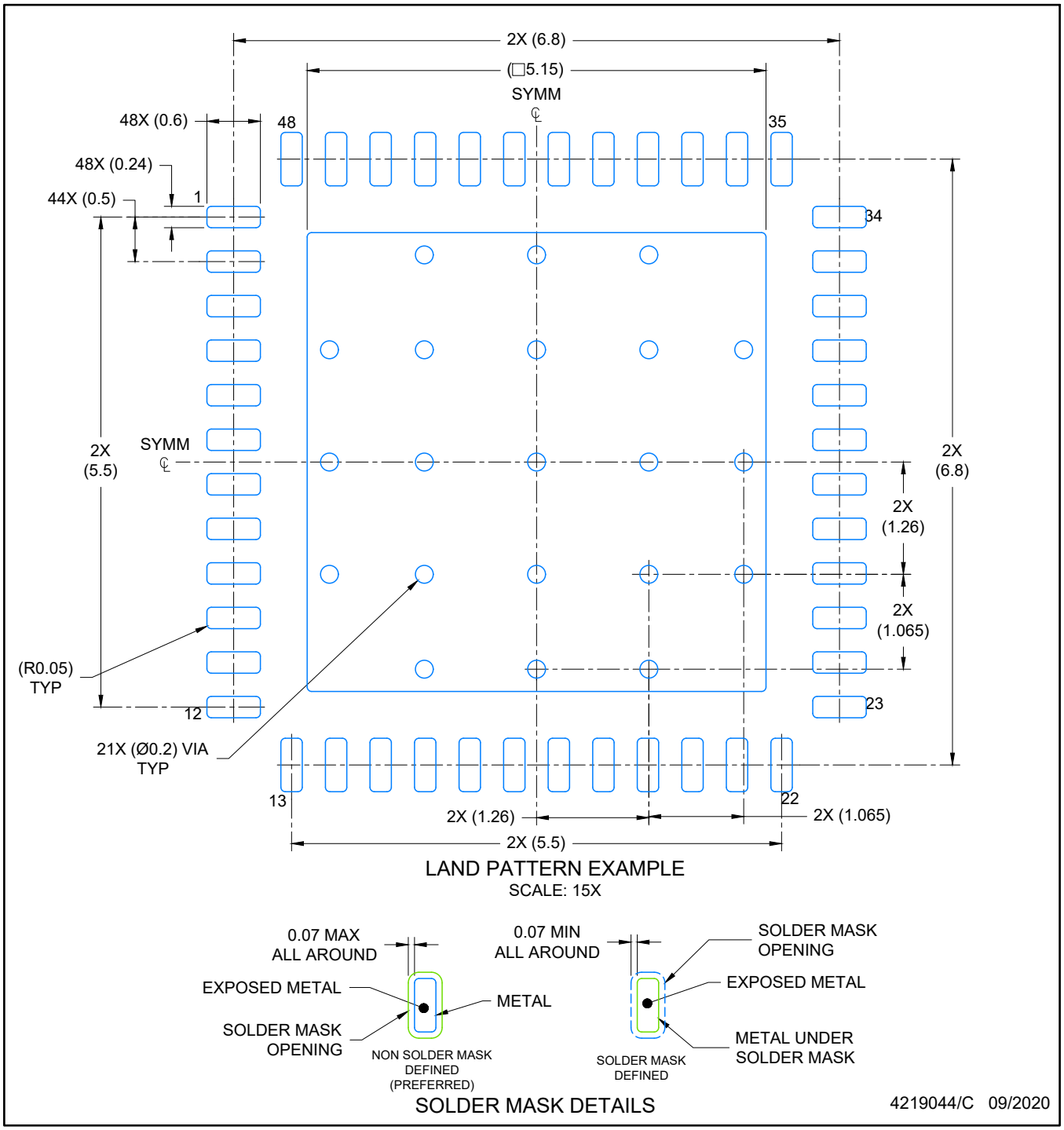
PLASTIC QUADFLAT PACK- NO LEAD



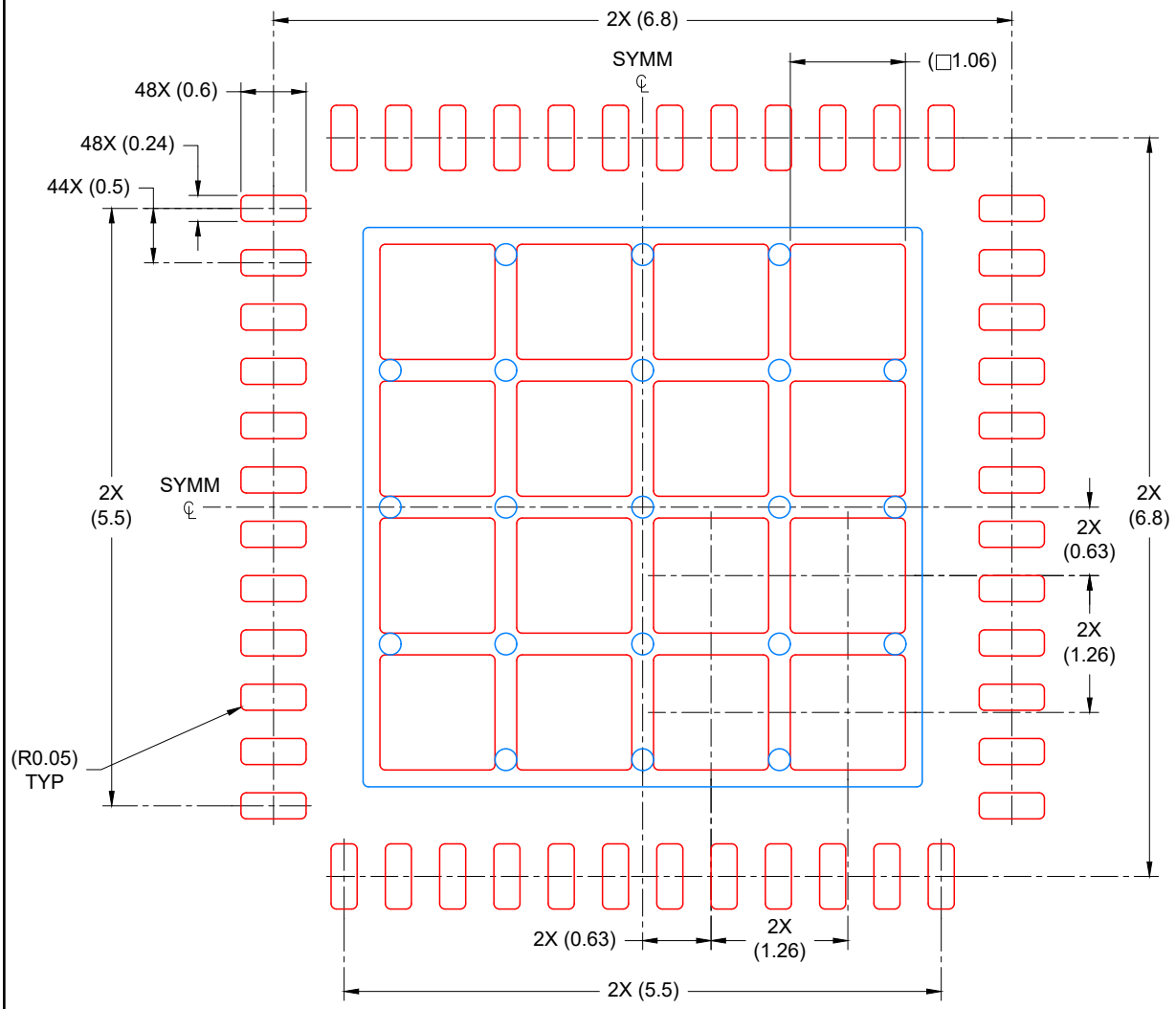
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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