

FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16241 . . . WD PACKAGE
SN74LVTH16241 . . . DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

DESCRIPTION/ORDERING INFORMATION

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide noninverting outputs and complementary output-enable (OE and $\overline{\text{OE}}$) inputs.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Reel of 1000	74LVTH16241DLRG4	LVTH16241
			SN74LVTH16241DLR	
		Tube of 25	SN74LVTH16241DL	
			SN74LVTH16241DLG4	
	TSSOP – DGG	Reel of 2000	74LVTH16241DGGRE4	LVTH16241
			SN74LVTH16241DGGR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54LVTH16241, SN74LVTH16241

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS693D–MAY 1997–REVISED NOVEMBER 2006

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

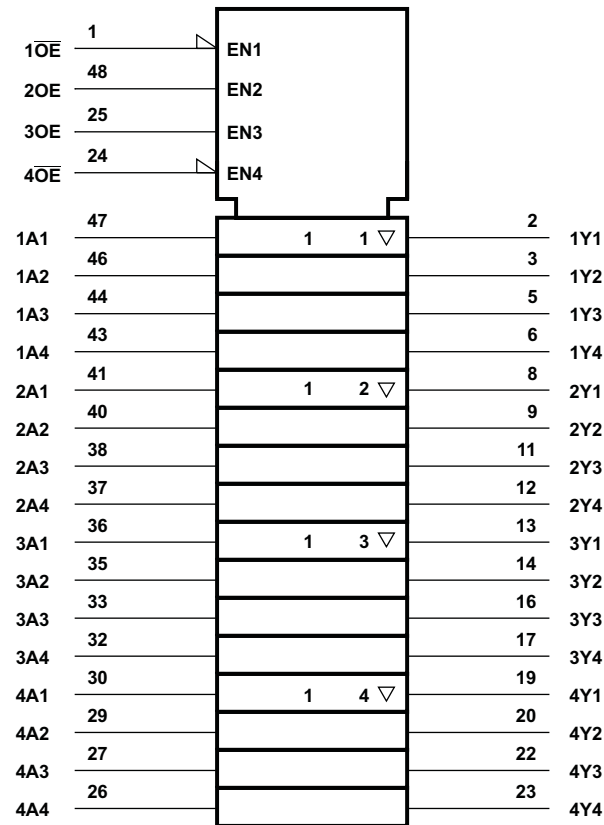
The SN54LVTH16241 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16241 is characterized for operation from -40°C to 85°C .

FUNCTION TABLES

INPUTS		OUTPUTS 1Y, 4Y
$1\overline{OE}$, $4\overline{OE}$	1A, 4A	
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUTS 2Y, 3Y
2OE, 3OE	2A, 3A	
H	H	H
H	L	L
L	X	Z

LOGIC SYMBOL ^(A)



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

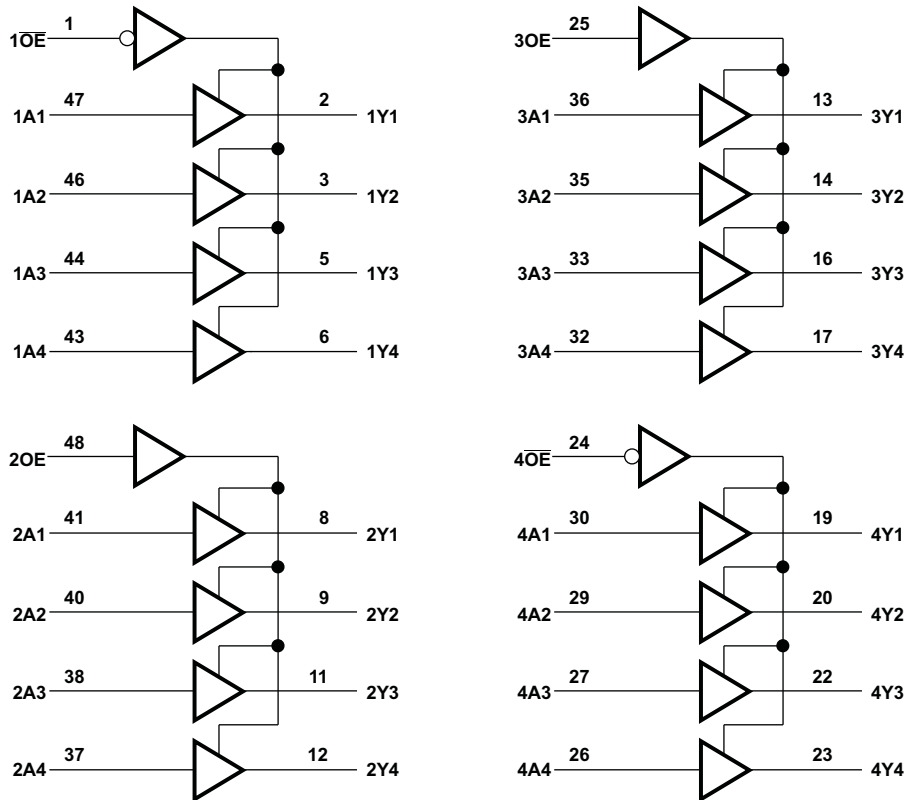
SN54LVTH16241, SN74LVTH16241

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS693D–MAY 1997–REVISED NOVEMBER 2006

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	4.6	V
V_I	Input voltage range ⁽²⁾	–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
V_O	Voltage range applied to any output in the high state ⁽²⁾	–0.5	$V_{CC} + 0.5$	V
I_O	Current into any output in the low state	SN54LVTH16241	96	mA
		SN74LVTH16241	128	
I_O	Current into any output in the high state ⁽³⁾	SN54LVTH16241	48	mA
		SN74LVTH16241	64	
I_{IK}	Input clamp current	$V_I < 0$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	89	°C/W
		DL package	94	
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.

(4) The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

		SN54LVTH16241 ⁽²⁾		SN74LVTH16241		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled					
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Product Preview

SN54LVTH16241, SN74LVTH16241

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16241 ⁽¹⁾		SN74LVTH16241		UNIT
				MIN	TYP ⁽²⁾	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2		−1.2		V
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} − 0.2		V _{CC} − 0.2		V
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4		2.4		
		V _{CC} = 3 V	I _{OH} = −24 mA	2				
			I _{OH} = −32 mA			2		
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA	0.2		0.2		V
			I _{OL} = 24 mA	0.5		0.5		
		V _{CC} = 3 V	I _{OL} = 16 mA	0.4		0.4		
			I _{OL} = 32 mA	0.5		0.5		
			I _{OL} = 48 mA	0.55				
			I _{OL} = 64 mA			0.55		
I _I		V _{CC} = 0 or 3.6 V, V _I = 5.5 V	10		10		μA	
	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND	±1		±1			
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}	1		1		
			V _I = 0	−5		−5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V	±100		±100		μA	
I _{I(hold)}	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75		μA
			V _I = 2 V	−75		−75		
		V _{CC} = 3.6 V ⁽³⁾ , V _I = 0 to 3.6 V			500 −750			
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V	5		5		μA	
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V	−5		−5		μA	
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE/OE = don't care		±100 ⁽⁴⁾		±100		μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE/OE = don't care		±100 ⁽⁴⁾		±100		μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.19		0.19		mA
			Outputs low	5		5		
			Outputs disabled	0.19		0.19		
ΔI _{CC} ⁽⁵⁾		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA
C _i		V _I = 3 V or 0		4		4		pF
C _o		V _O = 3 V or 0		9		9		pF

(1) Product Preview

(2) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16241 ⁽¹⁾				SN74LVTH16241				UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP ⁽²⁾	MAX	MIN		MAX
t _{PLH}	A	Y	1.1	3.7	4		1.2	2.6	3.5	3.8		ns
t _{PHL}			1.1	3.7	4		1.2	2.2	3.5	3.8		
t _{PZH}	OE or OE	Y	1.1	4.7	5.3		1.2	3.2	4.5	5.1		ns
t _{PZL}			1.1	4.7	5.2		1.2	3.2	4.5	4.9		
t _{PHZ}	OE or OE	Y	1.9	5.5	6.1		2	3.7	5.3	5.9		ns
t _{PLZ}			1.9	5.2	5.7		2	3.4	4.9	5.4		
t _{sk(LH)}									0.5	0.5		ns
t _{sk(HL)}									0.5	0.5		

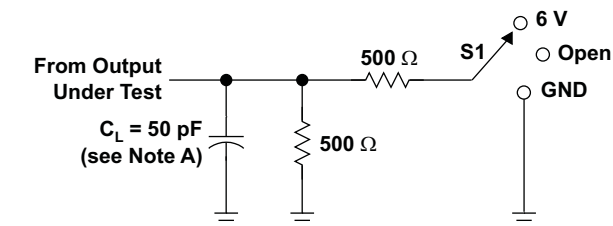
(1) Product Preview

(2) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

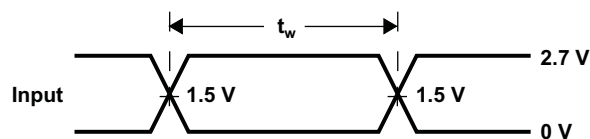
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PARAMETER MEASUREMENT INFORMATION

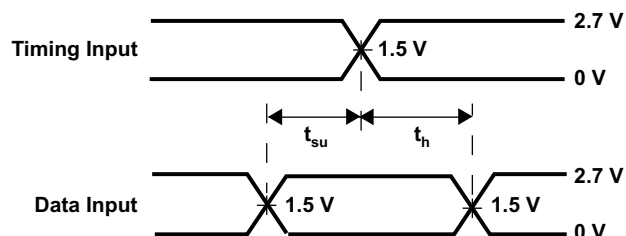


LOAD CIRCUIT

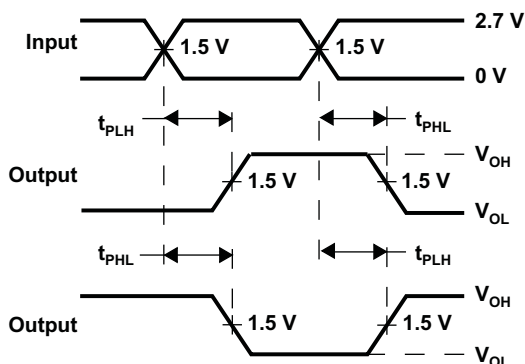
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



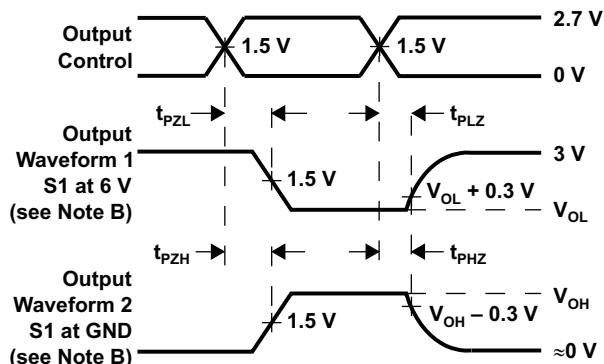
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVTH16241DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16241	Samples
SN74LVTH16241DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16241	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16241DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

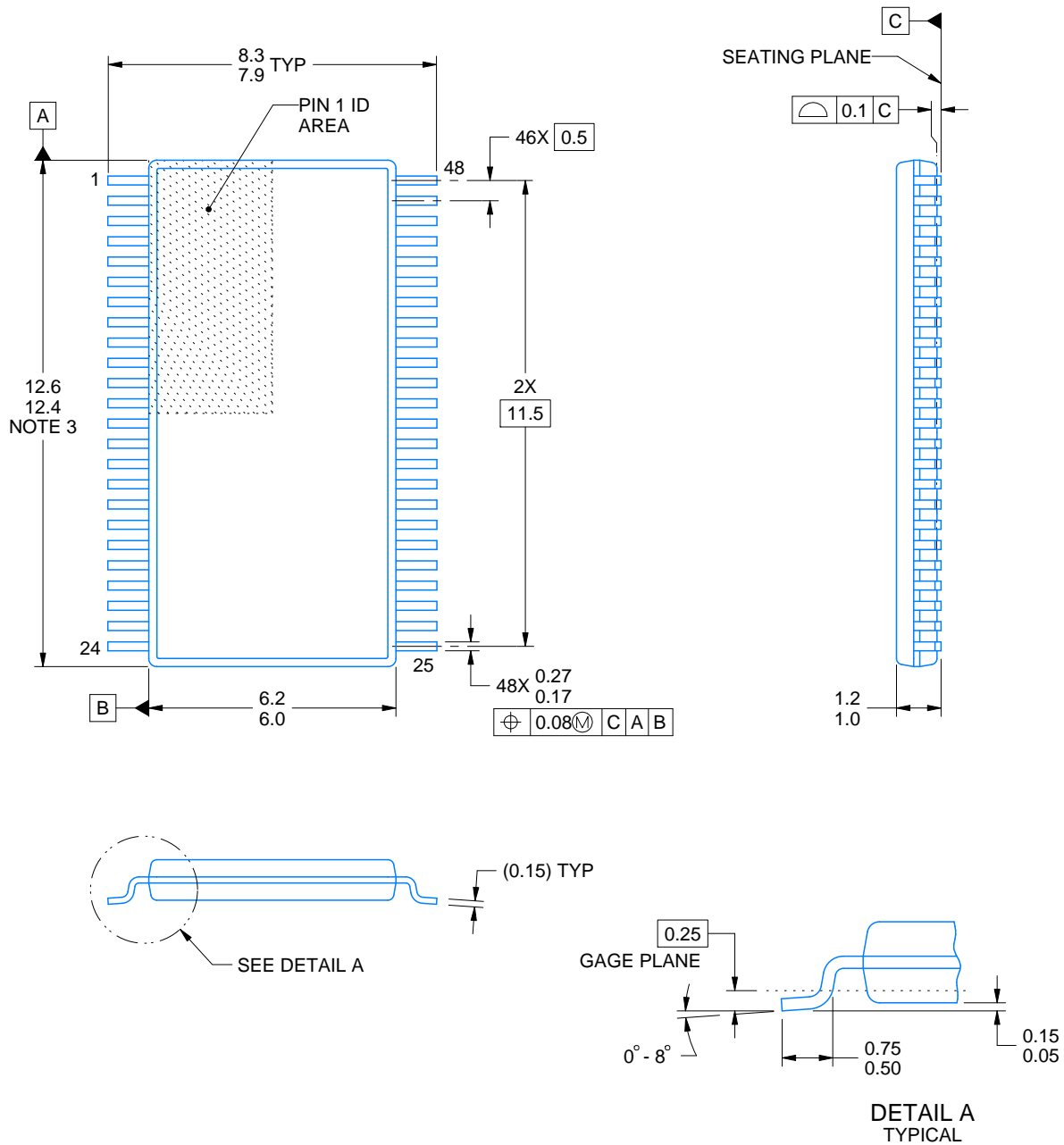
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16241DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



4214859/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

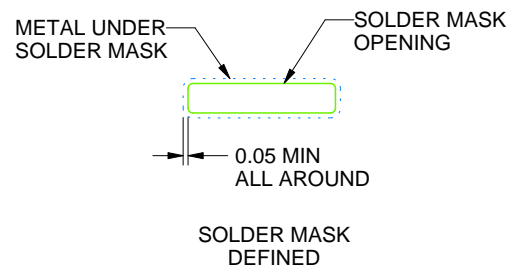
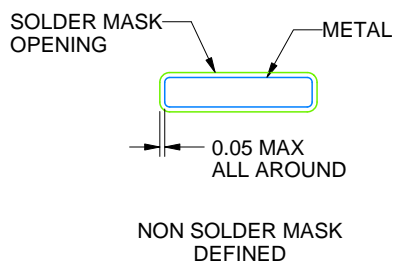
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

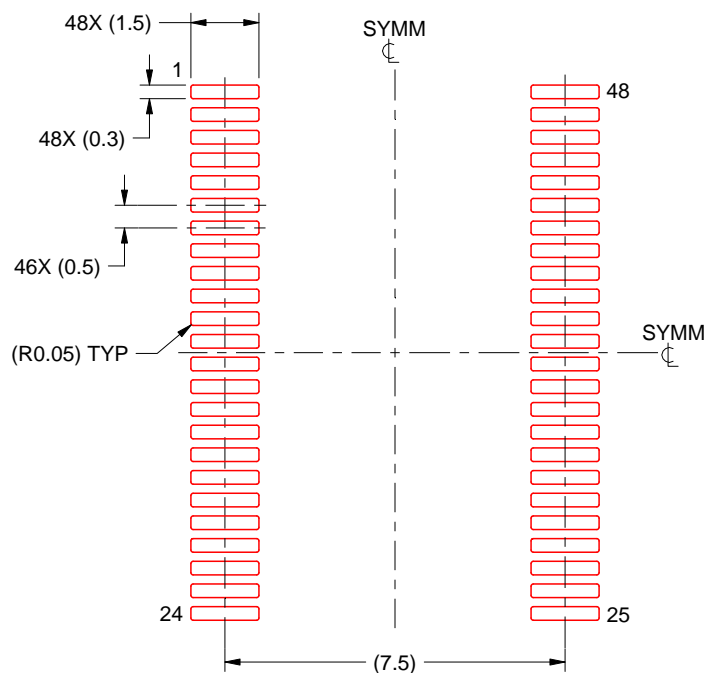
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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