ADS5463-SP Class V, 12-Bit, 500-MSPS Analog-to-Digital Converter

1 Features

- 500-MSPS Sample Rate
- Available With Radiation Hardness Specified (RHA) - Total Ionizing Dose 100 krad(Si), ELDRS Free 100 krad(Si)
- 12-Bit Resolution, 10-Bits Effective Number of Bits (ENOB)
- SNR > 64.5 dBFS at 450 MHz and 500 MSPS
- SFDR > 64.0 dBc at 450 MHz and 500 MSPS
- 2.2-V_{PP} Differential Input Voltage
- LVDS-Compatible Outputs
- Total Power Dissipation: 2.2 W
- Offset Binary Output Format
- Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock
- On-Chip Analog Buffer, Track and Hold, and Reference Circuit
- Available in a 84-Pin Ceramic Nonconductive Tie-Bar Package (HFG)
- Military Temperature Range (–55°C to 125°C T_{case})

2 Applications

- Test and Measurement Instrumentation
- Software-Defined Radio
- Data Acquisition
- Power Amplifier Linearization
- Communication Instrumentation
- Radar
- Engineering Evaluation (/EM) Samples are Available(1)

3 Description

The ADS5463 is a 12-bit, 500-MSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply, while providing LVDS-compatible digital outputs from the 3.3-V supply. The ADS5463 input buffer isolates the internal switching of the onboard track and hold (T and H) from disturbing the signal source. An internal reference generator is also provided to simplify the system design further. The ADS5463 has outstanding low noise and linearity over input frequency.

The ADS5463 is available in a 84-pin ceramic nonconductive tie-bar package (HFG). The ADS5463 is built on state-of-the-art Texas Instruments complementary bipolar process (BiCom3X) and is specified over the full military temperature range (–55°C to 125°C T_{case}).

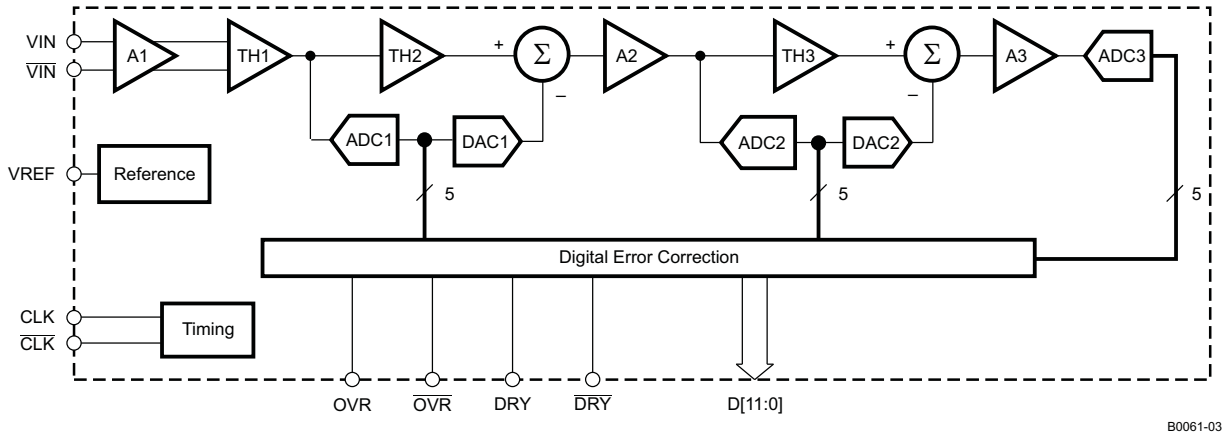
Device Information(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS5463-SP	CFP (84)	16.51 mm × 16.51 mm

(1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (for example, no burn-in, and so forth) and are tested to temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance on full MIL specified temperature range of –55°C to 125°C or operating life.

(2) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2015) to Revision G — **Page**

- Changed $R_{\theta JA}$ from 24°C/W : to 17.9°C/W in the *Thermal Information* section ... 5
- Changed $R_{\theta JC(top)}$ from 12°C/W : to 3.1°C/W in the *Thermal Information* section ... 5
- Changed $R_{\theta JB}$ from 10°C/W : to 6.1°C/W in the *Thermal Information* section ... 5
- Added values for ψ_{JT}, ψ_{JB}, and $R_{\theta JC(bot)}$ in the *Thermal Information* section ... 5
- Changed t_{DATA} NOM and MAX values in the *Timing Requirements* section ... 16
- Changed t_{SKEW} MIN and NOM values in the *Timing Requirements* section ... 16
- Added *Receiving Notification of Documentation Updates* section to the *Device and Documentation Support* section ... 30

Changes from Revision E (January 2014) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision D (August 2012) to Revision E — **Page**

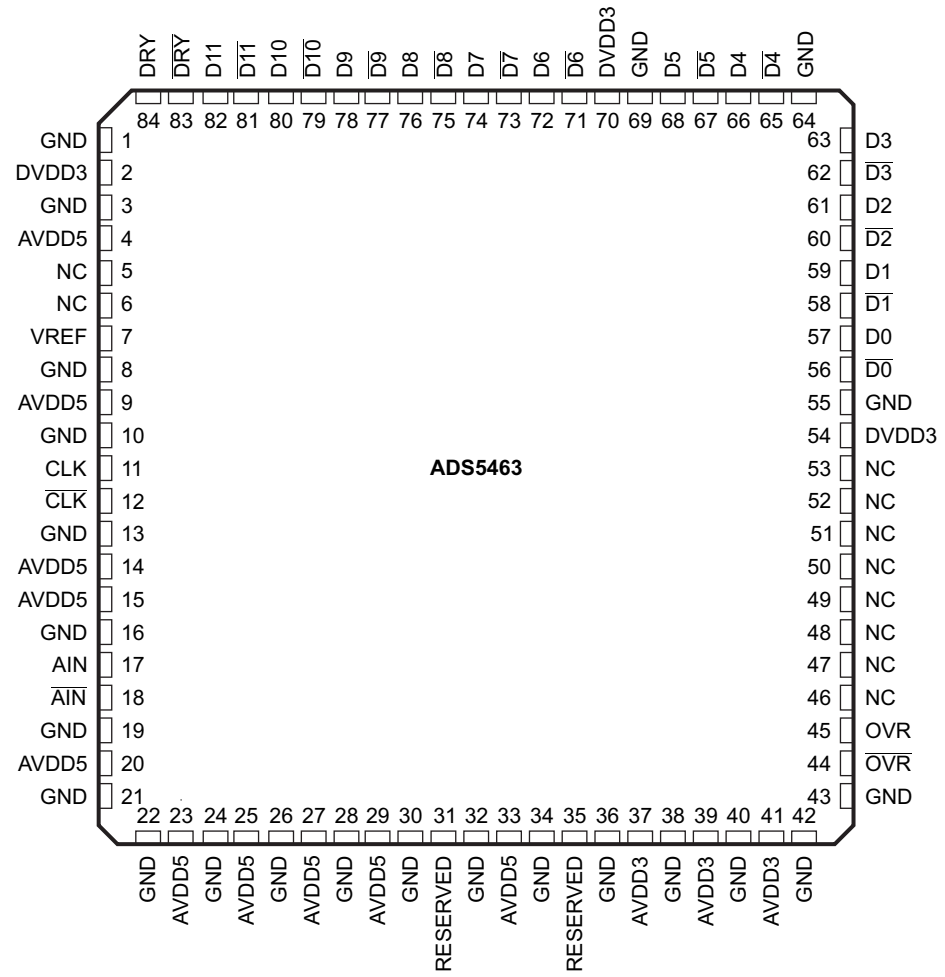
- Added /EM bullet to FEATURES ... 1
- Deleted PACKAGING/ORDERING INFORMATION table ... 1
- Added RECOMMENDED OPERATING CONDITIONS, CLK input sample rate (sine wave) 20 MSPS MIN ... 5

Changes from Revision B (October 2009) to Revision C — **Page**

- Added Feature "Available With Radiation.. " ... 1
- Added orderable 5962R0720802VXC to the Package Ordering table ... 1
- Added ADS5463-RHA Values to the Electrical Characteristics table ... 1

5 Pin Configuration and Functions

HFG Package
84-Pin CFP
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AIN	17	Differential input signal (positive).
$\overline{\text{AIN}}$	18	Differential input signal (negative).
AVDD5	4, 9, 14, 15, 20, 23, 25, 27, 29, 33	Analog power supply (5 V).
AVDD3	37, 39, 41	Analog power supply (3.3 V) (Suggestion for 250 MSPS: leave option to connect to 5 V for ADS5440/4 compatibility).
DVDD3	2, 54, 70	Output driver power supply (3.3 V).
GND	1, 3, 8, 10, 13, 16, 19, 21, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 43, 55, 64, 69	Ground.
CLK	11	Differential input clock (positive). Conversion initiated on rising edge.
$\overline{\text{CLK}}$	12	Differential input clock (negative).

Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
$\overline{D0}$, D0	56, 57	LVDS digital output pair, least-significant bit (LSB).
D1-D3, $\overline{D1}$-$\overline{D3}$	58–63	LVDS digital output pair.
D4–D5, $\overline{D4}$–$\overline{D5}$	65–68	LVDS digital output pairs.
D6–D10, $\overline{D6}$–$\overline{D10}$	71–80	LVDS digital output pairs.
$\overline{D11}$, D11	81, 82	LVDS digital output pair, most-significant bit (MSB).
$\overline{DRY}$, DRY	83, 84	Data ready LVDS output pair.
NC	5–6, 46–53	No connect (5 and 6 should be left floating, 46–53 are possible future bit additions for this pinout and therefore can be connected to a digital bus or left floating).
$\overline{OVR}$, OVR	44, 45	Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
RESERVED	31, 35	Reserved for possible future control features.
VREF	7	Reference voltage.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage	AVDD5 to GND		6		V
	AVDD3 to GND		5		
	DVDD3 to GND		5		
AIN, $\overline{AIN}$ to GND(2)	Voltage difference between pin and ground	AC signal	–0.3	(AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.4	4.4	
		DC signal, T_J = 125°C	1.0	3.8	
AIN to $\overline{AIN}$(2)	Voltage difference between these pins	AC signal	–5.2	5.2	V
		DC signal, T_J = 105°C	–4	4	
		DC signal, T_J = 125°C	–2.8	2.8	
CLK, $\overline{CLK}$ to GND(2)	Voltage difference between pin and ground	AC signal	–0.3	(AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.1	4.7	
		DC signal, T_J = 125°C	1.1	3.7	
CLK to $\overline{CLK}$(2)	Voltage difference between these pins	AC signal	–3.3	3.3	V
		DC signal, T_J = 105°C	–3.3	3.3	
		DC signal, T_J = 125°C	–2.6	2.6	
Data output to GND(2)	LVDS digital outputs		–0.3	(DVDD3 + 0.3)	V
Characterized case operating temperature, T_C			–55	125	°C
Maximum junction temperature, T_J			150		°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Valid when supplies are within recommended operating range.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLIES					
AVDD5	Analog supply voltage	4.75	5	5.25	V
AVDD3	Analog supply voltage	3	3.3	3.6	V
DVDD3	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input		2.2		V_{pp}
V_{CM}	Input common mode		2.4		V
DIGITAL OUTPUT					
	Maximum differential output load		10		pF
CLOCK INPUT					
	CLK input sample rate (sine wave)	20		500	MSPS
	Clock amplitude, differential sine wave		3		V_{pp}
	Clock duty cycle		50%		
T_c	Operating case temperature	–55		125	°C

6.4 Thermal Information (1)

THERMAL METRIC (2)		ADS5463-SP HFG (CFP) 84 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	17.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) This CFP package has built-in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11.9 mm^2 board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically at ground potential.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: ADS5463-RHA

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution					12		Bits
ANALOG INPUTS							
	Differential input range				2.2		V_{PP}
	Input resistance (dc)	Each input to VCM			500		Ω
	Input capacitance	Each input to ground			2.5		pF
	Analog input bandwidth			1000	2000		MHz
INTERNAL REFERENCE VOLTAGE							
V_{REF}	Reference voltage	Full temperature range		2.38	2.4	2.42	V
DYNAMIC ACCURACY							
	No missing codes				Assured		
DNL	Differential linearity error	f_{IN} = 210 MHz	Full temperature range	–0.98	±0.95	1.2	LSB
INL	Integral linearity error	f_{IN} = 210 MHz	Full temperature range	–3.5	±1.5	3.5	LSB
	Offset error	Full temperature range		–0.5		0.5	%FS
	Offset temperature coefficient				0.0009		%FS/°C
	Gain error	Full temperature range		–5		5	%FS
	Gain temperature coefficient				–0.02		%FS/°C
POWER SUPPLY							
I_{AVDD5}	5 V analog supply current	V_{IN} = full scale, f_{IN} = 300 MHz, F_S = 500 MSPS	Full temperature range			345	mA
I_{AVDD3}	3.3 V analog supply current					148	mA
I_{DVDD3}	3.3 V digital supply current(includes LVDS)					88	mA
	Power dissipation					2.450	W

6.6 Electrical Characteristics: ADS5463-RHA

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS							
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz			65.4		dBFS
		f_{IN} = 70 MHz			65.3		
		f_{IN} = 100 MHz	T_C = 25°C	60.5	65.2		
			T_C = $T_{C,MAX}$	60.5			
			T_C = $T_{C,MIN}$	60.5			
		f_{IN} = 210 MHz	T_C = 25°C	60	65		
			T_C = $T_{C,MAX}$	60			
			T_C = $T_{C,MIN}$	60			
		f_{IN} = 300 MHz	T_C = 25°C	58	64.9		
			T_C = $T_{C,MAX}$	58			
			T_C = $T_{C,MIN}$	58			
		f_{IN} = 450 MHz			64.5		
		f_{IN} = 650 MHz			63.7		
		f_{IN} = 900 MHz			62.8		
		f_{IN} = 1.0 GHz			62.2		
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64.2		
		f_{IN} = 100 MHz	T_C = 25°C	57.9	65		
			T_C = $T_{C,MAX}$	57.9			
			T_C = $T_{C,MIN}$	57.9			
		f_{IN} = 210 MHz	T_C = 25°C	55.2	64		
			T_C = $T_{C,MAX}$	55.2			
			T_C = $T_{C,MIN}$	55.2			
		f_{IN} = 300 MHz	T_C = 25°C	51.2	64		
			T_C = $T_{C,MAX}$	51.2			
			T_C = $T_{C,MIN}$	51.2			
		f_{IN} = 450 MHz			64		
		f_{IN} = 650 MHz			61.6		
		f_{IN} = 900 MHz			54.5		
		f_{IN} = 1.0 GHz			51.6		

Electrical Characteristics: ADS5463-RHA (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD2	Second harmonic	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64.2		
		f_{IN} = 100 MHz	T_C = 25°C	57.9	65.4		
			T_C = $T_{C,MAX}$	57.9			
			T_C = $T_{C,MIN}$	57.9			
		f_{IN} = 210 MHz	T_C = 25°C	55.2	64.4		
			T_C = $T_{C,MAX}$	55.2			
			T_C = $T_{C,MIN}$	55.2.			
		f_{IN} = 300 MHz	T_C = 25°C	51.2	64.3		
			T_C = $T_{C,MAX}$	51.2			
			T_C = $T_{C,MIN}$	51.2			
		f_{IN} = 450 MHz			64.4		
		f_{IN} = 650 MHz			67.1		
		f_{IN} = 900 MHz			62.9		
		f_{IN} = 1.0 GHz			58.6		
HD3	Third harmonic	f_{IN} = 10 MHz			104		dBc
		f_{IN} = 70 MHz			104		
		f_{IN} = 100 MHz	T_C = 25°C	64	87		
			T_C = $T_{C,MAX}$	64			
			T_C = $T_{C,MIN}$	64			
		f_{IN} = 210 MHz	T_C = 25°C	59	85		
			T_C = $T_{C,MAX}$	59			
			T_C = $T_{C,MIN}$	59			
		f_{IN} = 300 MHz	T_C = 25°C	61.9	76		
			T_C = $T_{C,MAX}$	61.9			
			T_C = $T_{C,MIN}$	61.9			
		f_{IN} = 450 MHz			73.3		
		f_{IN} = 650 MHz			61.6		
		f_{IN} = 900 MHz			54.5		
		f_{IN} = 1.0 GHz			51.6		

6.7 Electrical Characteristics: ADS5463-RHA

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS (CONT.)							
SINAD	Signal-to-noise and distortion	f_{IN} = 10 MHz			61.9		dBc
		f_{IN} = 70 MHz			62.2		
		f_{IN} = 100 MHz	T_C = 25°C	55.9	62		
			$T_C = T_{C,MAX}$	55.9			
			$T_C = T_{C,MIN}$	55.9			
		f_{IN} = 210 MHz	T_C = 25°C	53.8	62		
			$T_C = T_{C,MAX}$	53.8			
			$T_C = T_{C,MIN}$	53.8			
		f_{IN} = 300 MHz	T_C = 25°C	50.2	61.9		
			$T_C = T_{C,MAX}$	50.2			
			$T_C = T_{C,MIN}$	50.2			
		f_{IN} = 450 MHz			61.6		
		f_{IN} = 650 MHz			59.4		
		f_{IN} = 900 MHz			54.3		
		f_{IN} = 1.0 GHz			51.4		
	Worst harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz			83.1		dBc
		f_{IN} = 70 MHz			80.2		
		f_{IN} = 100 MHz	T_C = 25°C	68	81.8		
			$T_C = T_{C,MAX}$	68			
			$T_C = T_{C,MIN}$	68			
		f_{IN} = 210 MHz	T_C = 25°C	62	77.5		
			$T_C = T_{C,MAX}$	62			
			$T_C = T_{C,MIN}$	62			
		f_{IN} = 300 MHz	T_C = 25°C	62	78.2		
			$T_C = T_{C,MAX}$	62			
			$T_C = T_{C,MIN}$	62			
		f_{IN} = 450 MHz			80.6		
		f_{IN} = 650 MHz			80		
		f_{IN} = 900 MHz			79.4		
		f_{IN} = 1.0 GHz			77.6		

Electrical Characteristics: ADS5463-RHA (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64		
		f_{IN} = 100 MHz	T_C = 25°C	57.8	65.2		
			T_C = $T_{C,MAX}$	57.8			
			T_C = $T_{C,MIN}$	57.8			
		f_{IN} = 210 MHz	T_C = 25°C	55	64.1		
			T_C = $T_{C,MAX}$	55			
			T_C = $T_{C,MIN}$	55			
		f_{IN} = 300 MHz	T_C = 25°C	51	63.8		
			T_C = $T_{C,MAX}$	51			
			T_C = $T_{C,MIN}$	51			
		f_{IN} = 450 MHz			63.7		
		f_{IN} = 650 MHz			60.5		
		f_{IN} = 900 MHz			53.9		
		f_{IN} = 1.0 GHz			50.8		
ENOB	Effective number of bits	f_{IN} = 100 MHz	T_C = 25°C	9	10.1		Bits
			T_C = $T_{C,MAX}$	9			
			T_C = $T_{C,MIN}$	9			
		f_{IN} = 210 MHz	T_C = 25°C	8.65	10		
			T_C = $T_{C,MAX}$	8.65			
			T_C = $T_{C,MIN}$	8.65			
		f_{IN} = 300 MHz	T_C = 25°C	8.05	9.9		
			T_C = $T_{C,MAX}$	8.05			
			T_C = $T_{C,MIN}$	8.05			
	RMS idle-channel noise	Inputs tied to common-mode			0.7		LSB
LVDS DIGITAL OUTPUTS							
VOD	Differential output voltage			247	350	454	mV
VOC	Common mode output voltage			1.125		1.375	V

6.8 Electrical Characteristics: ADS5463-SP

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clockover operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution					12		Bits
ANALOG INPUTS							
	Differential input range				2.2		V_{PP}
	Input resistance (dc)	Each input to VCM			500		Ω
	Input capacitance	Each input to ground			2.5		pF
	Analog input bandwidth			1000	2000		MHz
INTERNAL REFERENCE VOLTAGE							
V_{REF}	Reference voltage	Full temperature range		2.38	2.4	2.42	V
DYNAMIC ACCURACY							
	No missing codes				Assured		
DNL	Differential linearity error	f_{IN} = 210 MHz	Full temperature range	–0.98	±0.95	1.2	LSB
INL	Integral linearity error	f_{IN} = 210 MHz	Full temperature range	–2.9	±1.5	2.9	LSB
	Offset error	Full temperature range		–0.5		0.5	%FS
	Offset temperature coefficient				0.0009		%FS/°C
	Gain error	Full temperature range		–5		5	%FS
	Gain temperature coefficient				–0.02		%FS/°C
POWER SUPPLY							
I_{AVDD5}	5 V analog supply current	V_{IN} = full scale, f_{IN} = 300 MHz, F_S = 500 MSPS	Full temperature range			335	mA
I_{AVDD3}	3.3 V analog supply current					140	mA
I_{DVDD3}	3.3 V digital supply current(includes LVDS)					88	mA
	Power dissipation					2.425	W

6.9 Electrical Characteristics: ADS5463-SP

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clockover operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS							
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz			65.4		dBFS
		f_{IN} = 70 MHz			65.3		
		f_{IN} = 100 MHz	T_C = 25°C	64.1	65.2		
			T_C = $T_{C,MAX}$	62.7			
			T_C = $T_{C,MIN}$	63.5			
		f_{IN} = 210 MHz	T_C = 25°C	63.6	65		
			T_C = $T_{C,MAX}$	62.4			
			T_C = $T_{C,MIN}$	63.2			
		f_{IN} = 300 MHz	T_C = 25°C	62.7	64.9		
			T_C = $T_{C,MAX}$	61.3			
			T_C = $T_{C,MIN}$	61.9			
		f_{IN} = 450 MHz			64.5		
		f_{IN} = 650 MHz			63.7		
		f_{IN} = 900 MHz			62.8		
		f_{IN} = 1.0 GHz			62.2		
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64.2		
		f_{IN} = 100 MHz	T_C = 25°C	57.9	65		
			T_C = $T_{C,MAX}$	58.8			
			T_C = $T_{C,MIN}$	58.6			
		f_{IN} = 210 MHz	T_C = 25°C	55.2	64.0		
			T_C = $T_{C,MAX}$	56.6			
			T_C = $T_{C,MIN}$	56.9			
		f_{IN} = 300 MHz	T_C = 25°C	54.1	64		
			T_C = $T_{C,MAX}$	51.3			
			T_C = $T_{C,MIN}$	56.2			
		f_{IN} = 450 MHz			64		
		f_{IN} = 650 MHz			61.6		
		f_{IN} = 900 MHz			54.5		
		f_{IN} = 1.0 GHz			51.6		

Electrical Characteristics: ADS5463-SP (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clockover operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD2	Second harmonic	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64.2		
		f_{IN} = 100 MHz	T_C = 25°C	57.9	65.4		
			T_C = $T_{C,MAX}$	58.8			
			T_C = $T_{C,MIN}$	58.6			
		f_{IN} = 210 MHz	T_C = 25°C	55.2	64.4		
			T_C = $T_{C,MAX}$	56.6			
			T_C = $T_{C,MIN}$	56.9			
		f_{IN} = 300 MHz	T_C = 25°C	54.1	64.3		
			T_C = $T_{C,MAX}$	51.3			
			T_C = $T_{C,MIN}$	56.2			
		f_{IN} = 450 MHz			64.4		
		f_{IN} = 650 MHz			67.1		
		f_{IN} = 900 MHz			62.9		
		f_{IN} = 1.0 GHz			58.6		
HD3	Third harmonic	f_{IN} = 10 MHz			104		dBc
		f_{IN} = 70 MHz			104		
		f_{IN} = 100 MHz	T_C = 25°C	69	87		
			T_C = $T_{C,MAX}$	68.5			
			T_C = $T_{C,MIN}$	65.6			
		f_{IN} = 210 MHz	T_C = 25°C	66.7	85		
			T_C = $T_{C,MAX}$	65.3			
			T_C = $T_{C,MIN}$	64.1			
		f_{IN} = 300 MHz	T_C = 25°C	70.1	76		
			T_C = $T_{C,MAX}$	61.9			
			T_C = $T_{C,MIN}$	64.8			
		f_{IN} = 450 MHz			73.3		
		f_{IN} = 650 MHz			61.6		
		f_{IN} = 900 MHz			54.5		
		f_{IN} = 1.0 GHz			51.6		

6.10 Electrical Characteristics: ADS5463-SP

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clockover operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS (CONT.)							
SINAD	Signal-to-noise and distortion	f_{IN} = 10 MHz			61.9		dBc
		f_{IN} = 70 MHz			62.2		
		f_{IN} = 100 MHz	T_C = 25°C	58	62		
			T_C = $T_{C,MAX}$	58			
			T_C = $T_{C,MIN}$	58.4			
		f_{IN} = 210 MHz	T_C = 25°C	55.8	62		
			T_C = $T_{C,MAX}$	56.2			
			T_C = $T_{C,MIN}$	56.7			
		f_{IN} = 300 MHz	T_C = 25°C	54.9	61.9		
			T_C = $T_{C,MAX}$	52.2			
			T_C = $T_{C,MIN}$	56.1			
		f_{IN} = 450 MHz			61.6		
		f_{IN} = 650 MHz			59.4		
		f_{IN} = 900 MHz			54.3		
		f_{IN} = 1.0 GHz			51.4		
	Worst harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz			83.1		dBc
		f_{IN} = 70 MHz			80.2		
		f_{IN} = 100 MHz	T_C = 25°C	72.2	81.8		
			T_C = $T_{C,MAX}$	70.6			
			T_C = $T_{C,MIN}$	72.6			
		f_{IN} = 210 MHz	T_C = 25°C	70.6	77.5		
			T_C = $T_{C,MAX}$	67.1			
			T_C = $T_{C,MIN}$	66.5			
		f_{IN} = 300 MHz	T_C = 25°C	69.3	78.2		
			T_C = $T_{C,MAX}$	66.3			
			T_C = $T_{C,MIN}$	66.3			
		f_{IN} = 450 MHz			80.6		
		f_{IN} = 650 MHz			80		
		f_{IN} = 900 MHz			79.4		
		f_{IN} = 1.0 GHz			77.6		

Electrical Characteristics: ADS5463-SP (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clockover operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64		
		f_{IN} = 100 MHz	T_C = 25°C	57.8	65.2		
			T_C = $T_{C,MAX}$	58.3			
			T_C = $T_{C,MIN}$	58.1			
		f_{IN} = 210 MHz	T_C = 25°C	55	64.1		
			T_C = $T_{C,MAX}$	55.9			
			T_C = $T_{C,MIN}$	56.2			
		f_{IN} = 300 MHz	T_C = 25°C	53.9	63.8		
			T_C = $T_{C,MAX}$	51			
			T_C = $T_{C,MIN}$	55.6			
		f_{IN} = 450 MHz			63.7		
		f_{IN} = 650 MHz			60.5		
		f_{IN} = 900 MHz			53.9		
		f_{IN} = 1.0 GHz			50.8		
ENOB	Effective number of bits	f_{IN} = 100 MHz	T_C = 25°C	9.3	10.1		Bits
			T_C = $T_{C,MAX}$	9.3			
			T_C = $T_{C,MIN}$	9.4			
		f_{IN} = 210 MHz	T_C = 25°C	8.9	10		
			T_C = $T_{C,MAX}$	9			
			T_C = $T_{C,MIN}$	9.1			
		f_{IN} = 300 MHz	T_C = 25°C	8.8	9.9		
			T_C = $T_{C,MAX}$	8.3			
			T_C = $T_{C,MIN}$	9			
	RMS idle-channel noise	Inputs tied to common-mode			0.7		LSB
LVDS DIGITAL OUTPUTS							
VOD	Differential output voltage			247	350	454	mV
VOC	Common mode output voltage			1.125		1.375	V

6.11 Timing Requirements

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock (unless otherwise noted)(1).

			MIN	NOM	MAX	UNIT
t_a	Aperture delay			200		ps
	Aperture jitter, rms			160		fs
	Latency			3.5		cycles
t_{CLK}	Clock period		2		50	ns
t_{CLKH}	Clock pulse duration, high		1			ns
t_{CLKL}	Clock pulse duration, low		1			ns
t_{DRY}	CLK to DRY delay(2)	Zero crossing	750	1500	2500	ps
t_{DATA}	CLK to DATA/OVR delay(2)	Zero crossing	650	1500	3100	ps
t_{SKEW}	DATA to DRY skew	t_{DATA}–t_{DRY}	–700	0	700	ps
t_{RISE}	DRY/DATA/OVR rise time			500		ps
t_{FALL}	DRY/DATA/OVR fall time			500		ps

(1) Timing parameters are assured by design or characterization, but not production tested. < 10-pF load on each output pin.
(2) DRY, DATA and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the overall propagation delay.

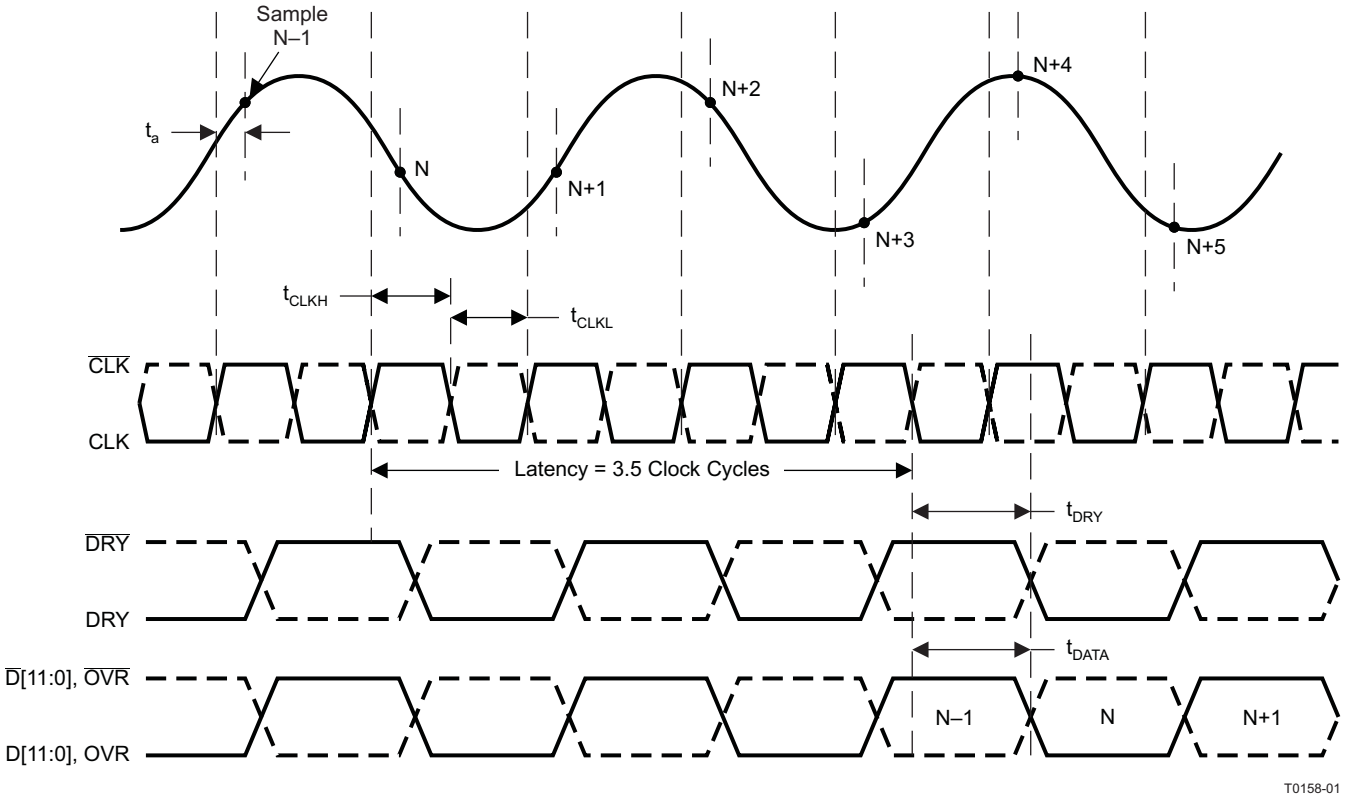


Figure 1. Timing Diagram

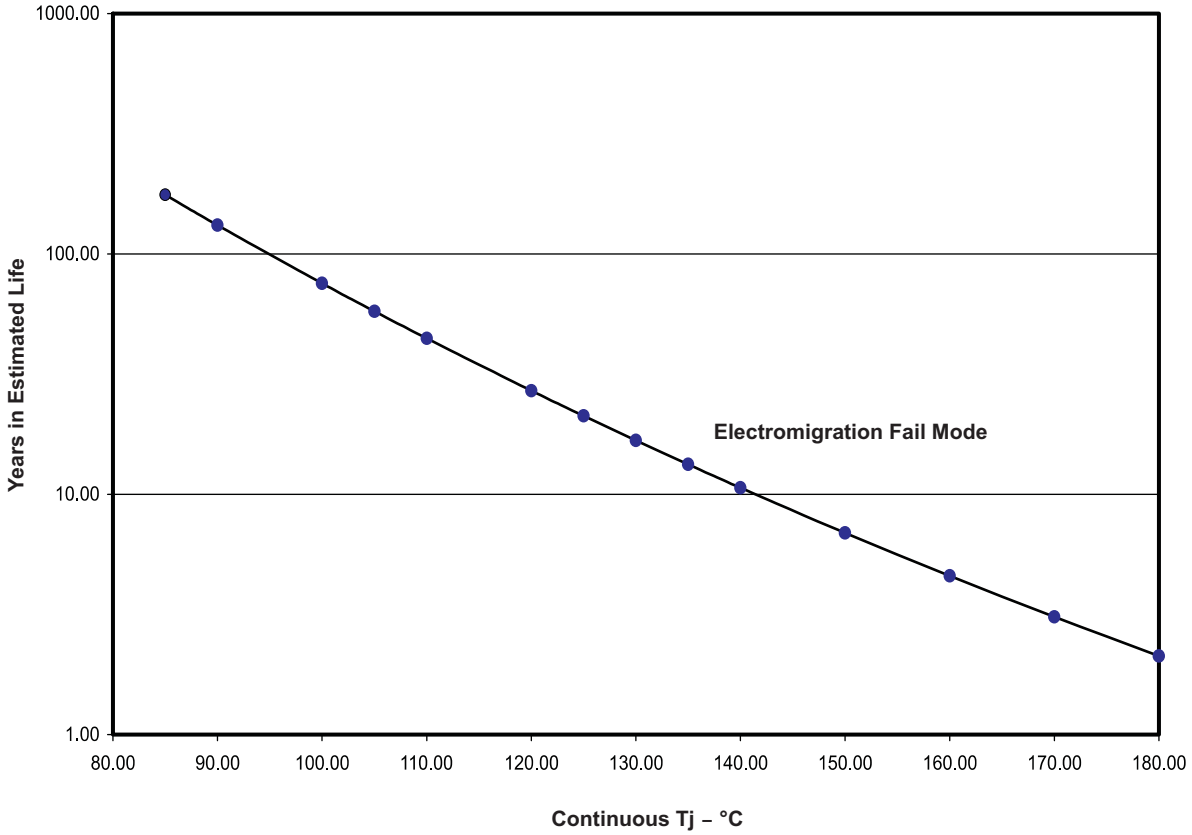


Figure 2. ADS5463 Estimated Life at Elevated Temperature Electromigration Fail Mode

6.12 Typical Characteristics

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

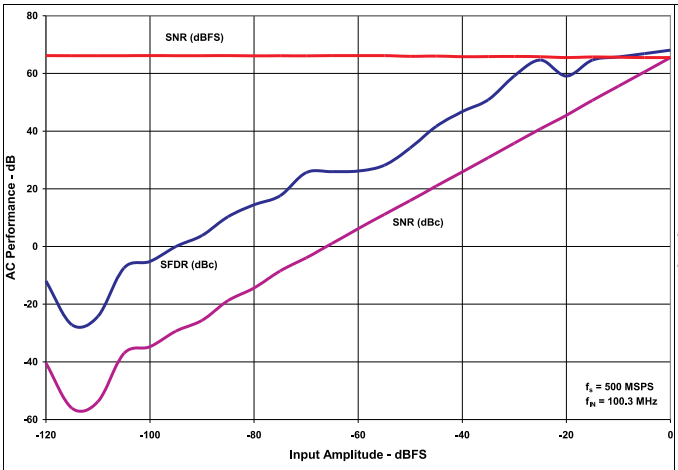


Figure 3. AC Performance vs Input Amplitude (100-MHz Input Signal)

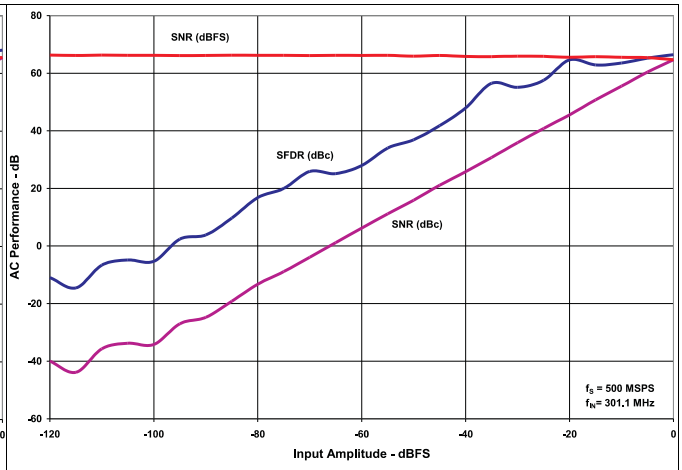


Figure 4. AC Performance vs Input Amplitude (300-MHz Input Signal)

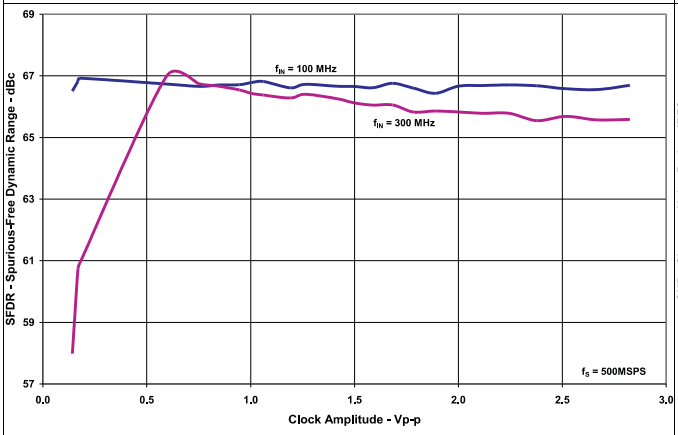


Figure 5. SFDR vs Clock Level

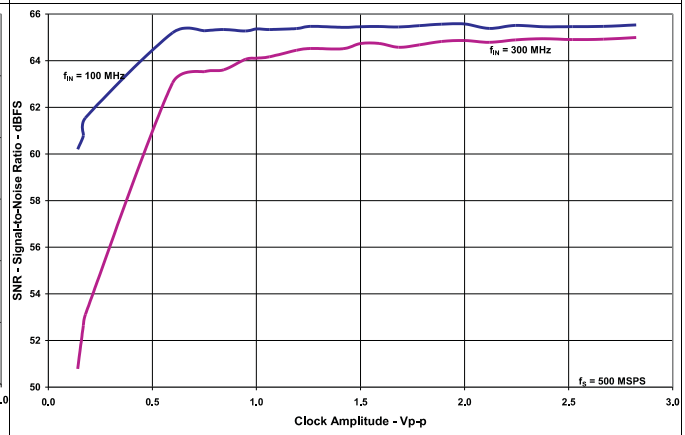


Figure 6. SNR vs Clock Level

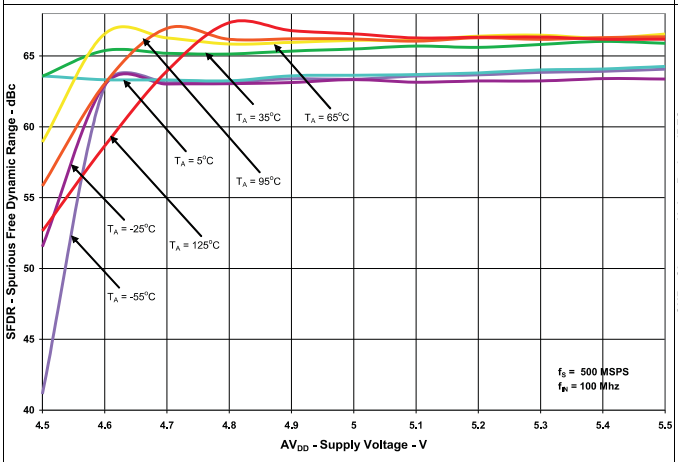


Figure 7. SFDR vs AVDD5 Across Temperature

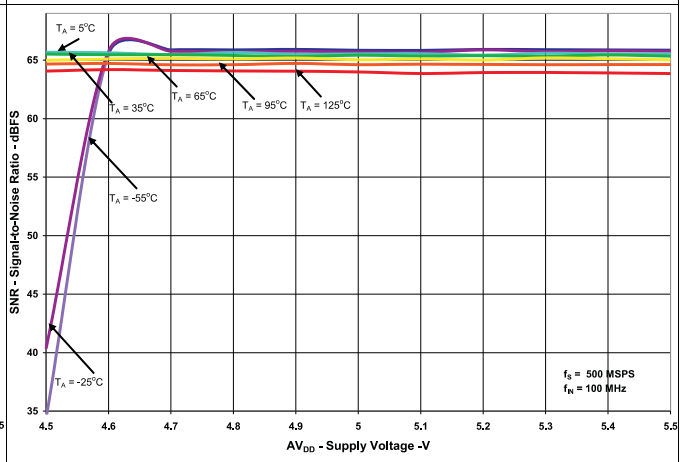


Figure 8. SNR vs AVDD5 Across Temperature

Typical Characteristics (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

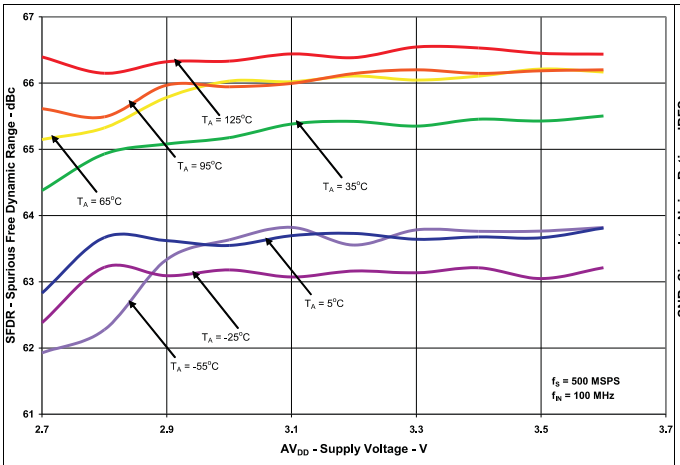


Figure 9. SFDR vs AVDD3 Across Temperature

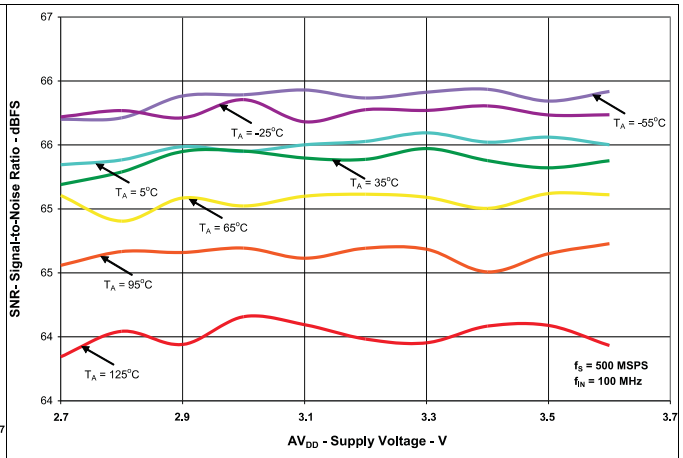


Figure 10. SNR vs AVDD3 Across Temperature

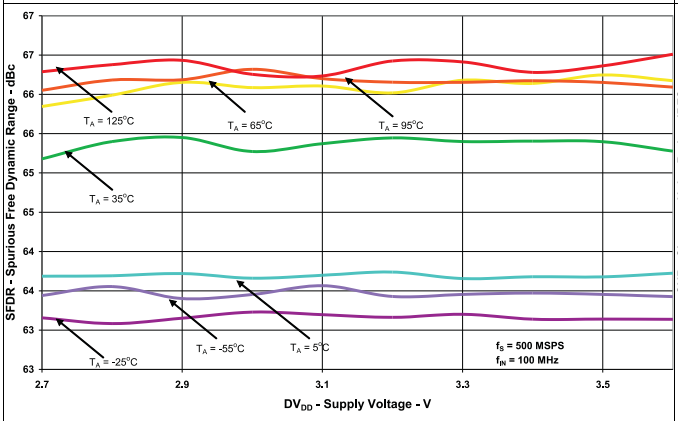


Figure 11. SFDR vs DVDD3 Across Temperature

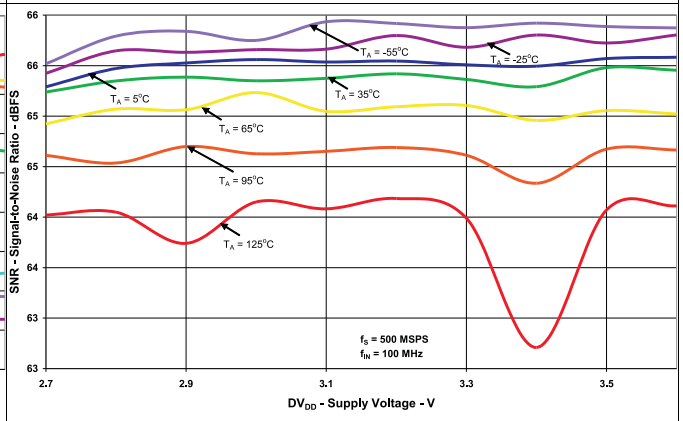


Figure 12. SNR vs DVDD3 Across Temperature

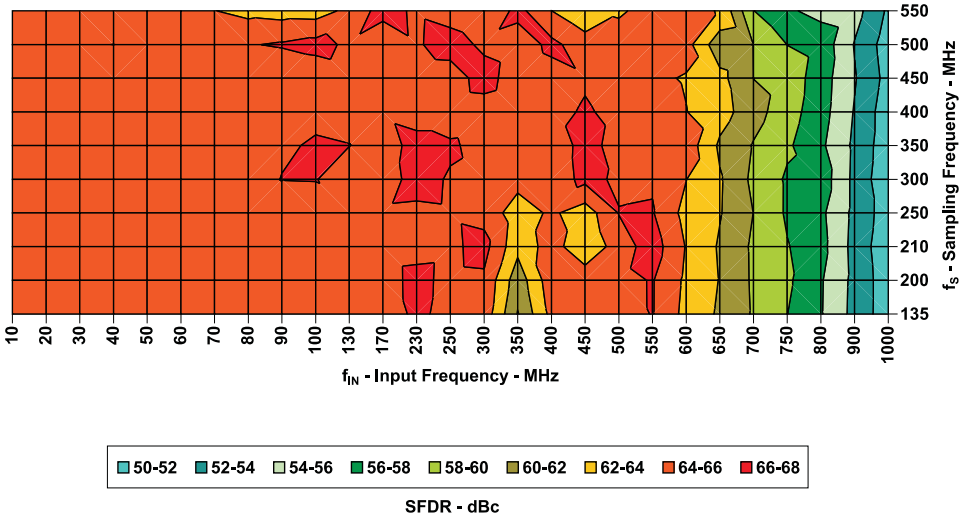


Figure 13. SFDR vs Input Frequency and Sampling Frequency

Typical Characteristics (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

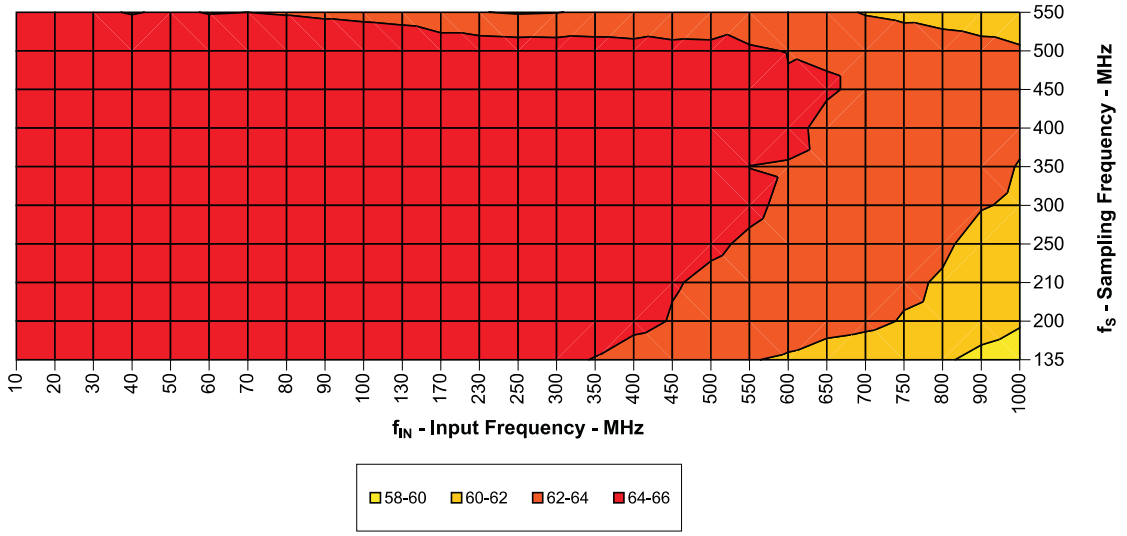


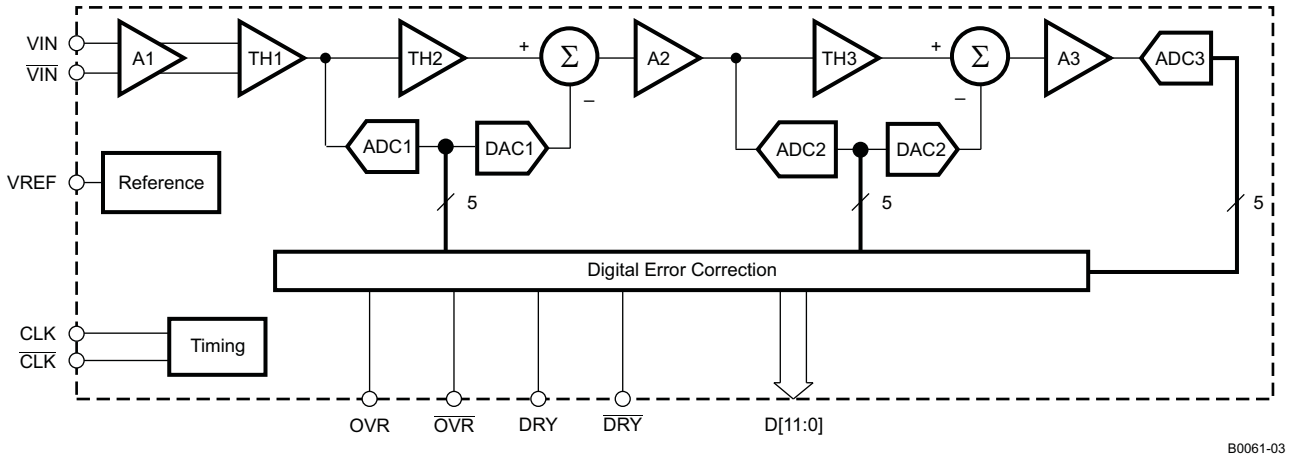
Figure 14. SNR vs Input Frequency and Sampling Frequency

7 Detailed Description

7.1 Overview

The ADS5463 is a 12-bit, 500-MSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply, while providing LVDS-compatible digital outputs from the 3.3-V supply. The ADS5463 input buffer isolates the internal switching of the onboard track and hold (T and H) from disturbing the signal source. An internal reference generator is also provided to simplify the system design further. The ADS5463 has outstanding low noise and linearity over input frequency.

7.2 Functional Block Diagram



7.3 Feature Description

The ADS5463-SP has a maximum sample rate of 500-MSPS with 12 bits of resolution and 10-bit effective number of bits (ENOB). It is available with radiation hardness specified (RHA) designation with total ionizing dose of 100 krad(Si) and ELDRS free 100 krad(Si). Performance characteristics with 450-MHz Fin and 500 MSPS (SNR > 64.5 dBFS and SFDR > 64.0 dBC). The differential analog input accepts a 2.2-V peak to peak input, and outputs are LVDS compatible. It is available in military temperature range (–55°C to 125°C T_{CASE}) with a total power dissipation of 2.2-W assembled in an 84-pin ceramic nonconductive tie-bar package (HFG).

7.4 Device Functional Modes

This device has no specific function modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADS5463 is a 12-bit, 500-MSPS, monolithic-pipeline, analog-to-digital converter. Its bipolar analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible outputs. The conversion process is initiated by the rising edge of the external input clock. The differential input signal is captured by the input track-and-hold (T&H), and the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 3.5 clock cycles, after which the output data is available as a 12-bit parallel word, coded in offset binary format.

8.1.1 Input Configuration

The analog input for the ADS5463 consists of an analog pseudodifferential buffer followed by a bipolar transistor track-and-hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500-Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 17 and 18) swings symmetrically between 2.4 V + 0.55 V and 2.4 V – 0.55 V. This means that each input has a maximum signal swing of 1.1 Vpp for a total differential input signal swing of 2.2 Vpp. The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose.

The ADS5463 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 15 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. In addition, the evaluation module is configured with two back-to-back transformers, which also demonstrate good performance. If voltage gain is required, a step-up transformer can be used.

Besides the transformer configurations, Texas Instruments offers a wide selection of single-ended operational amplifiers that can be selected depending on the application. An RF gain-block amplifier, such as Texas Instruments' THS9001, also can be used for high-input-frequency applications. For large voltage gains at intermediate-frequencies in the 50-MHz – 500-MHz range, the configuration shown in Figure 16 can be used. The component values can be tuned for different intermediate frequencies. The example shown is located on the evaluation module and is tuned for an IF of 170 MHz. More information regarding this configuration can be found in the *ADS5463 EVM User Guide* (SLAU194) and the *THS9001 50 MHz to 350 MHz Cascadeable Amplifier* data sheet (SLOS426).

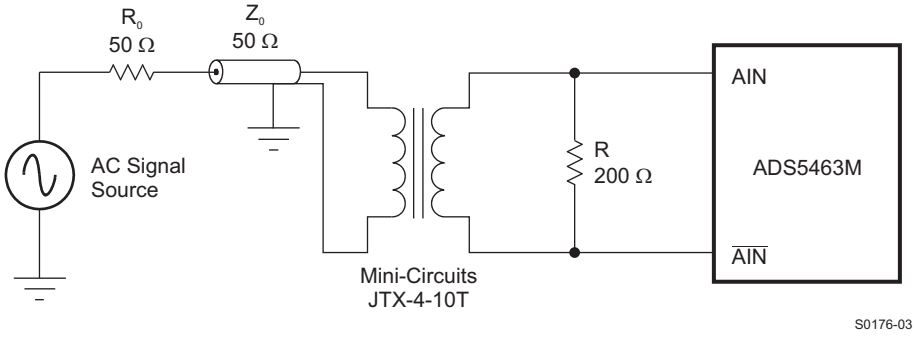


Figure 15. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

Application Information (continued)

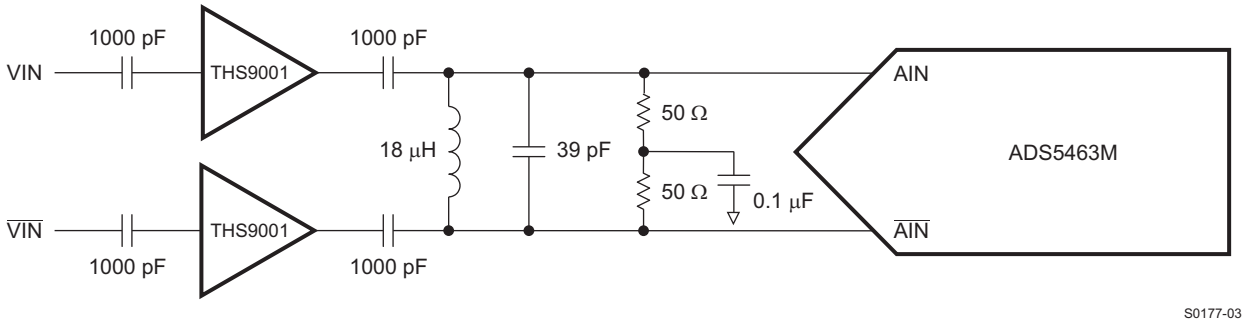


Figure 16. Using the THS9001 IF Amplifier With the ADS5463

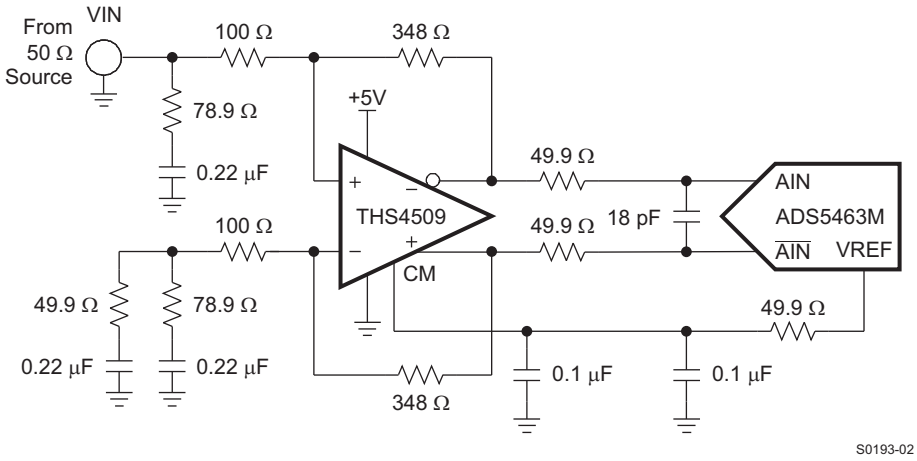


Figure 17. Using the THS4509 With the ADS5463

For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier like the THS4509 (see Figure 17) is a good solution, as it minimizes board space and reduces the number of components.

In this configuration, the THS4509 amplifier circuit provides 10-dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5463. The 50-Ω resistors and 18-pF capacitor between the THS4509 outputs and ADS5463 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 70 MHz (–3 dB). Input termination is accomplished via the 78.9-Ω resistor and 0.22-µF capacitor to ground, in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor are inserted to ground across the 78.9-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50-Ω termination for other common gains. Because the ADS5463 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with V S+ = 5 V and V S– = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

8.1.2 Clock Inputs

The ADS5463 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low-input-frequency applications, where jitter may not be a big concern, the use of a single-ended clock (see Figure 18) could save some cost and board space without any trade-off in performance. When clocked with this configuration, it is best to connect $\overline{\text{CLK}}$ to ground with a 0.01-µF capacitor, while CLK is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 18.

Application Information (continued)

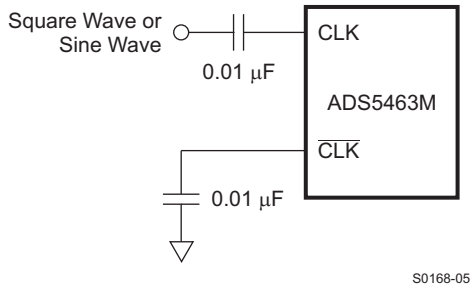


Figure 18. Single-Ended Clock

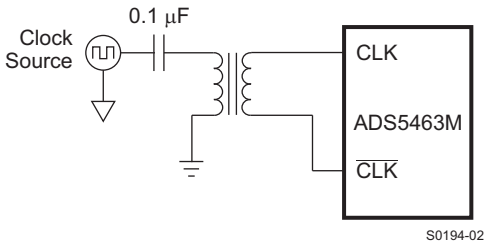


Figure 19. Differential Clock

For jitter-sensitive applications, the use of a differential clock has advantages (as with any other ADC) at the system level. The differential clock allows for common-mode noise rejection at the PCB level. With a differential clock, the signal-to-noise ratio of the ADC is better for high intermediate frequency applications because the board clock jitter is superior.

A differential clock also allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. In the case of a sinusoidal clock, this results in higher slew rates and reduces the impact of clock noise on jitter. Figure 19 shows this approach. See *Clocking High Speed Data Converters* (SLYT075) for more details.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1-kΩ resistors. It is recommended to use ac coupling, but if this scheme is not possible due to, for instance, asynchronous clocking, the ADS5463 features good tolerance to clock common-mode variation. Additionally, the internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty-cycle clock signal should be provided.

8.1.3 Digital Outputs

The ADC provides 12 data outputs (D11 to D0, with D11 being the MSB and D0 the LSB), a data-ready signal (DRY), and an overrange indicator (OVR) that equals a logic high when the output reaches the full-scale limits. The output format is offset binary. It is recommended to use the DRY signal to capture the output data of the ADS5463. DRY is source-synchronous to the DATA/OVR bits and operates at the same frequency, creating a half-rate DDR interface that updates data on both the rising and falling edges of DRY. The ADS5463 digital outputs are LVDS-compatible. Due to the high data rates, care should be taken not to overload the digital outputs with too much capacitance, which shortens the data-valid timing window. The values given for timing were obtained with a measured 14-pF parasitic board capacitance to ground on each LVDS line (or 7-pF differential parasitic capacitance).

8.2 Typical Application

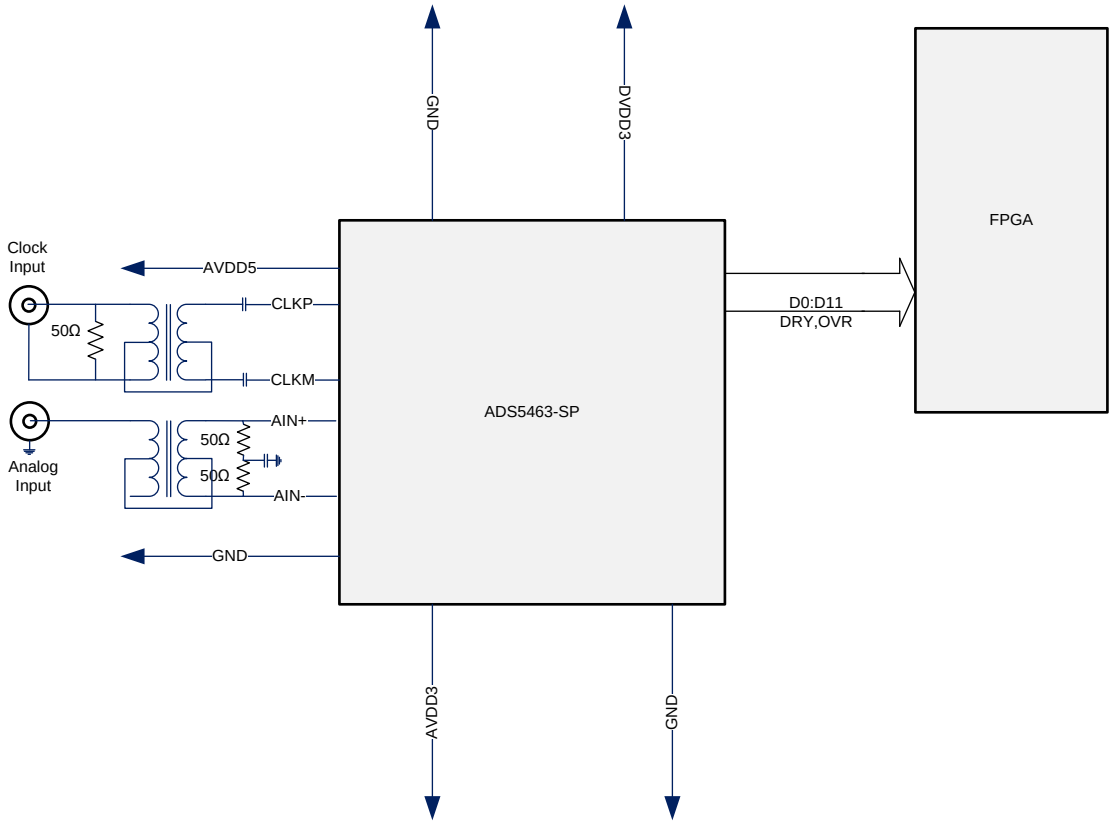


Figure 20. Application Diagram for ADS5463

8.2.1 Design Requirements

By using the simple drive circuit of Figure 2, Figure 15, or Figure 16, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device can help isolate the external drive source from the switching currents of the sampling circuit.

8.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves the common-mode noise immunity and even-order harmonic rejection.

Typical Application (continued)

8.2.3 Application Curve

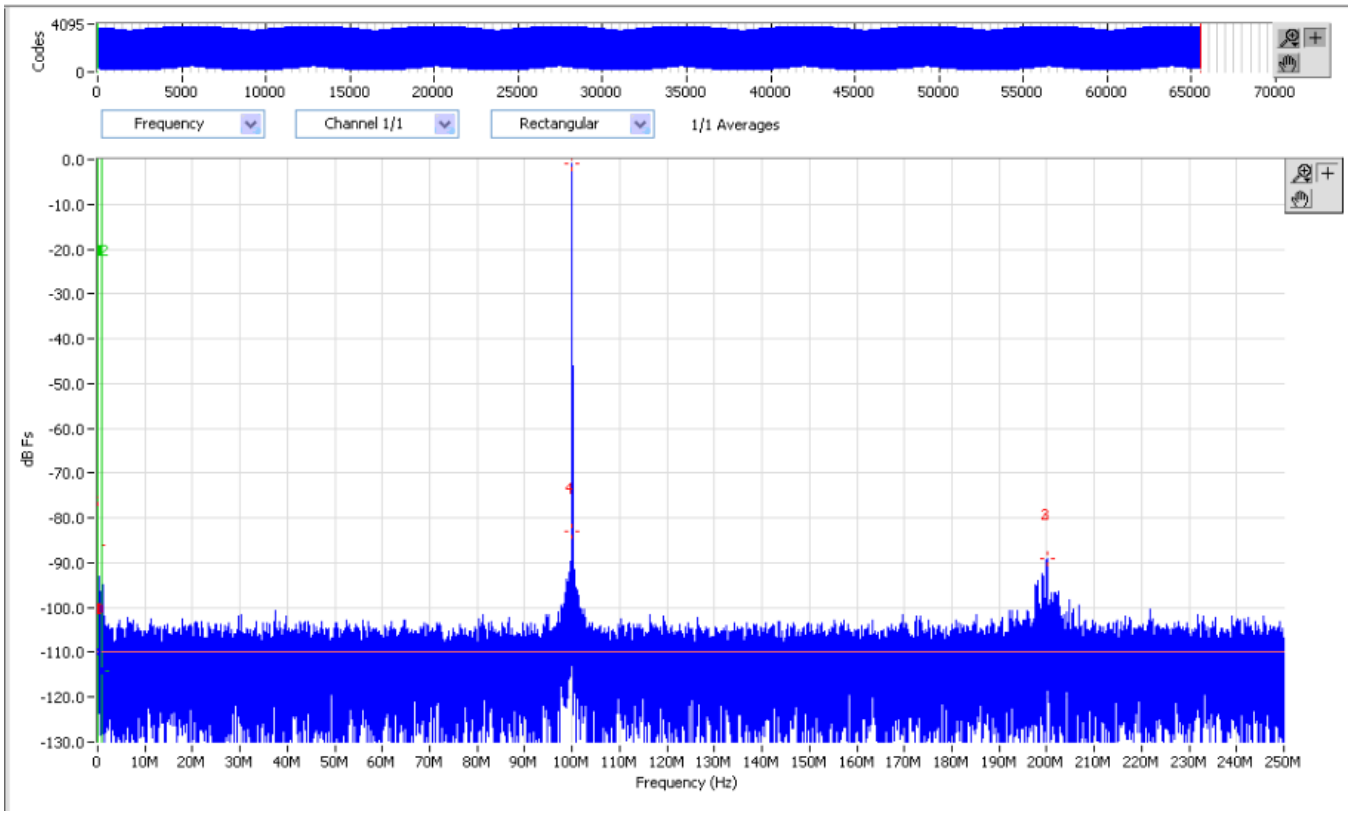


Figure 21. Typical Performance

9 Power Supply Recommendations

The ADS5463 uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies tend to generate more noise components that can be coupled to the ADS5463. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems.

The power consumption of the ADS5463 does not change substantially over clock rate or input frequency as a result of the architecture and process.

Because there are two diodes connected in reverse between AVDD3 and DVDD3 internally, a power-up sequence is recommended. When there is a delay in power up between these two supplies, the one that lags could have current sinking through an internal diode before it powers up. The sink current can be large or small depending on the impedance of the external supply and could damage the device or affect the supply source.

The best power up sequence is one of the following options (regardless of when AVDD5 powers up):

- Power up both AVDD3 and DVDD3 at the same time (best scenario), OR
- Keep the voltage difference less than 0.8 V between AVDD3 and DVDD3 during the power up (0.8 V is not a hard specification - a smaller delta between supplies is safer).

If the above sequences are not practical then the sink current from the supply needs to be controlled or protection added externally. The max transient current (on the order of msec) for the DVDD3 or AVDD3 pin is 500 mA to avoid potential damage to the device or reduce its lifetime.

The values for the analog and clock inputs given in the Absolute Maximum Ratings are valid when the supplies are on. When the power supplies are off and the clock or analog inputs are still being actively driven, the input voltage and current need to be limited to avoid device damage. If the ADC supplies are off, max/min continuous dc voltage is ±0.95 V and max dc current is 20 mA for each input pin (clock or analog), relative to ground.

10 Layout

10.1 Layout Guidelines

The evaluation board represents a good guideline of how to lay out the board to obtain the maximum performance from the ADS5463. General design rules, such as the use of multilayer boards, single ground plane for ADC ground connections, and local decoupling ceramic chip capacitors, should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces also should be isolated from other signals, especially in applications where low jitter is required like high IF sampling. Besides performance-oriented rules, care must be taken when considering the heat dissipation of the device.

10.2 Layout Example

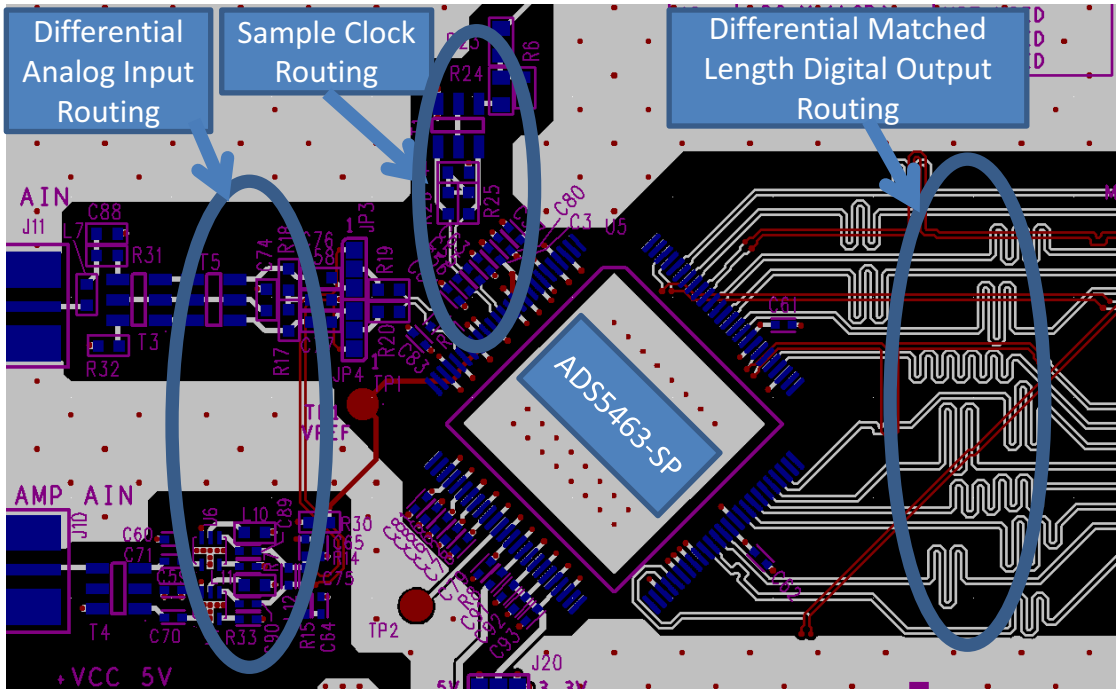


Figure 22. Typical Layout of ADS5463-SP

11 Device and Documentation Support

11.1 Device Support

11.1.1 Definition of Specifications

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay

Clock Pulse Duration/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Differential Nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Effective Resolution Bandwidth The highest input frequency where the SNR (dB) is dropped by 3 dB for a full-scale input amplitude.

Gain Error Gain error is the deviation of the ADC actual input full-scale range from its ideal value. Gain error is given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL) INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Maximum Conversion Rate The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions

Offset Error Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10} \frac{P_S}{P_N + P_D} \quad (1)$$

Signal-to-Noise Ratio (SNR) SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

SNR is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

$$SNR = 10\log_{10} \frac{P_S}{P_N} \quad (2)$$

SINAD is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to Full Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Temperature Drift Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by T_{MIN}

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10} \frac{P_S}{P_D} \quad (3)$$

THD is typically given in units of dBc (dB to carrier).

Device Support (continued)

Two-Tone Intermodulation Distortion IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0720801VXC	ACTIVE	CFP	HFG	84	1	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	5962- 0720801VXC ADS5463MHFG-V	Samples
5962R0720802VXC	ACTIVE	CFP	HFG	84	1	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	5962R 0720802VXC ADS5463MHFG-RHA	Samples
ADS5463HFG/EM	ACTIVE	CFP	HFG	84	1	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25	ADS5463HFG/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

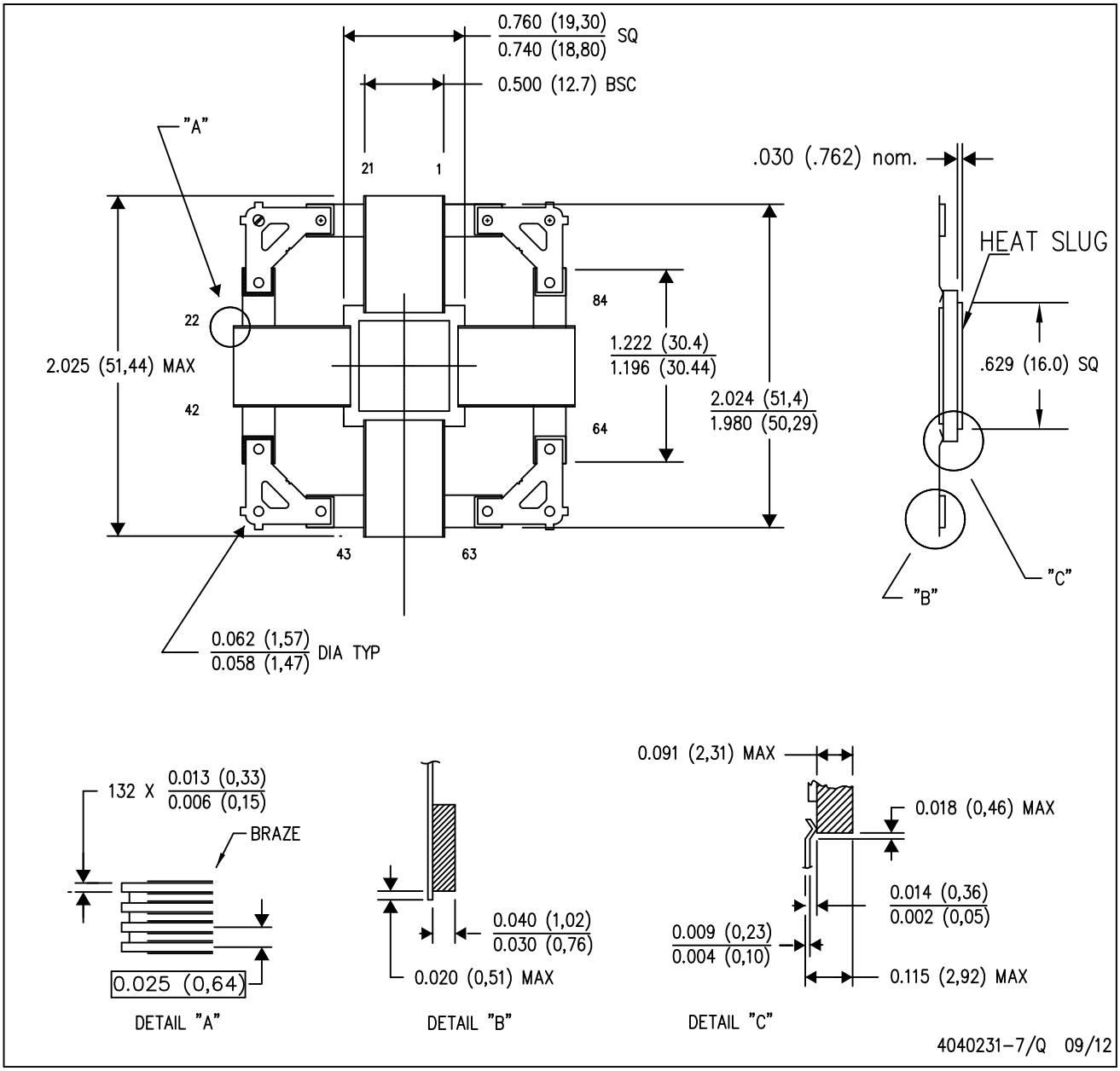
OTHER QUALIFIED VERSIONS OF ADS5463-SP :

- Catalog: ADS5463
- Enhanced Product: ADS5463-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

HFG (S–CQFP–F84) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.

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