ADS8555
16-Bit, Six-Channel, Simultaneous Sampling Analog-to-Digital Converter

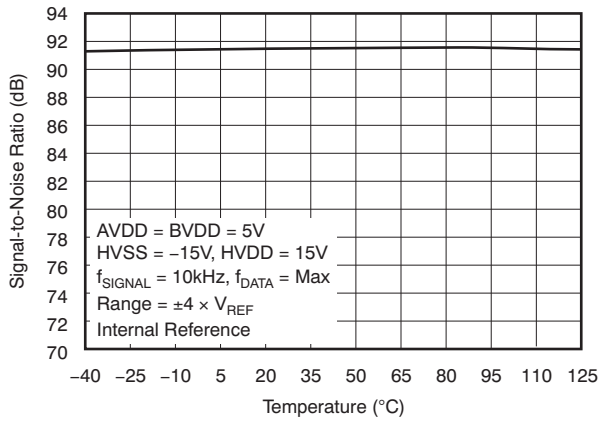
1 Features

- Six SAR ADCs Grouped in Three Pairs
- Maximum Data Rate Per Channel With Internal Clock and Reference:
  630 kSPS (Parallel) or 450 kSPS (Serial)
- Maximum Data Rate Per Channel With External Clock and Reference:
  800 kSPS (Parallel) or 500 kSPS (Serial)
- Pin-Selectable or Programmable Input Voltage Ranges: Up to ±12 V
- Excellent AC Performance:
  91.5-dB SNR, –94-dB THD
- Programmable and Buffered Internal Reference:
  0.5 V to 2.5 V and 0.5 V to 3 V
- Comprehensive Power-Down Modes:
  - Deep Power Down (Standby Mode)
  - Auto-Nap Power Down
- Selectable Parallel or Serial Interface
- Operating Temperature Range: –40°C to 125°C
- LQFP-64 Package

2 Applications

- Power Quality Measurements
- Protection Relays
- Multi-Axis Motor Controls
- Programmable Logic Controllers
- Industrial Data Acquisition

SNR vs Temperature



3 Description

The ADS8555 device contains six low-power, 16-bit, successive approximation register (SAR)-based analog-to-digital converters (ADCs) with true bipolar inputs. Each channel contains a sample-and-hold circuit that allows simultaneous high-speed multi-channel signal acquisition.

The ADS8555 device supports data rates of up to 630 kSPS in parallel interface mode or up to 450 kSPS if the serial interface is used. The bus width of the parallel interface can be set to eight or 16 bits. In serial mode, up to three output channels can be activated.

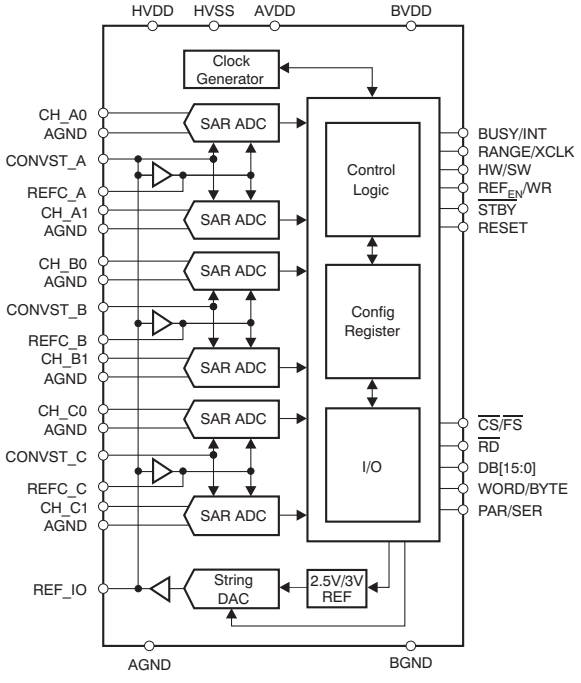
The ADS8555 device is specified over the extended industrial temperature range of –40°C to 125°C and is available in an LQFP-64 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS8555	LQFP (64)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2015) to Revision D — **Page**

- Changed Figure 36: changed capacitor values from 820 nF to 820 pF ... 32

Changes from Revision B (February 2011) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (January 2011) to Revision B — **Page**

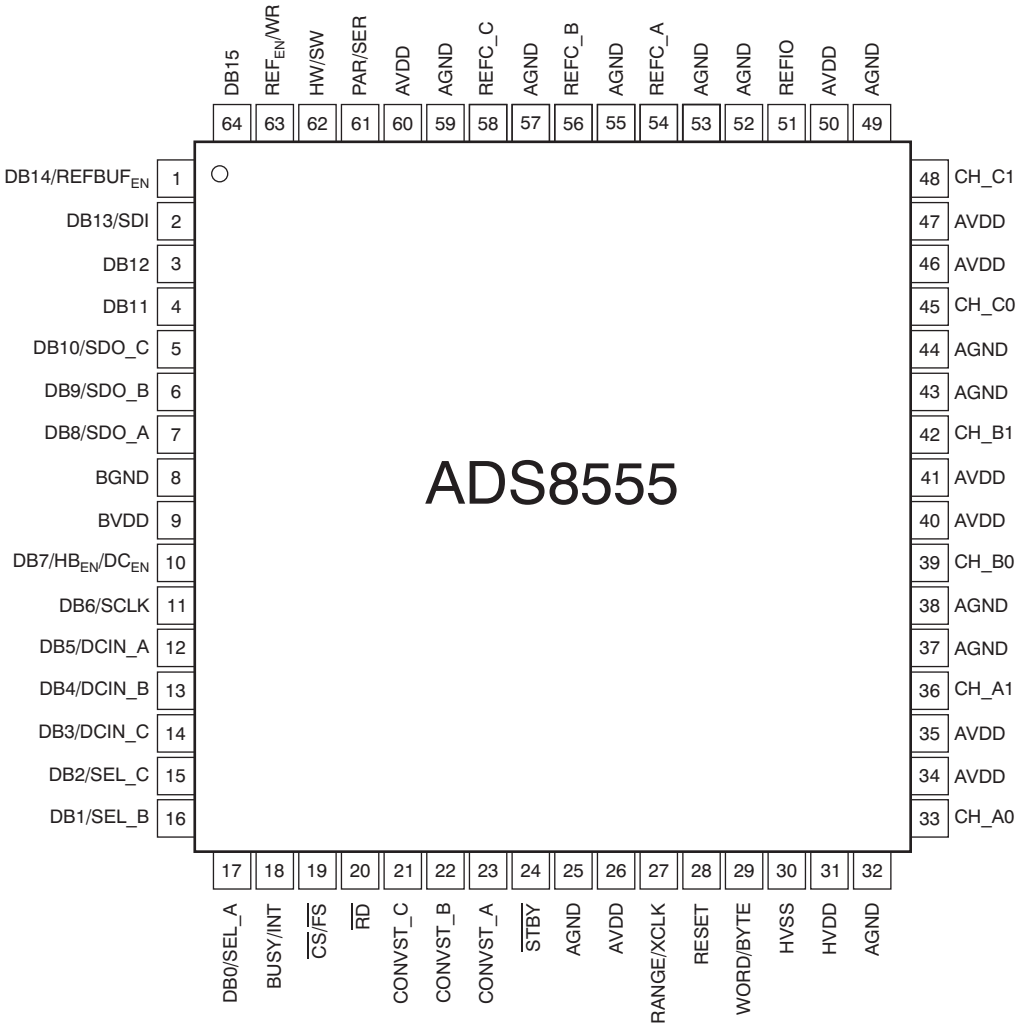
- Changed description of pin 18 in Pin Descriptions table ... 5
- Added clarification of INT in *BUSY/INT* section ... 23
- Updated Table 4 ... 28
- Changed bit C20 in Table 5 ... 30

Changes from Original (December 2010) to Revision A — **Page**

- Changed description of CONVST_C, CONVST_B, and CONVST_A pins in Pin Descriptions table ... 5
- Changed description of *CONVST_x* section ... 22
- Changed first paragraph of *BUSY/INT* section ... 23

5 Pin Configuration and Functions

PM Package
64-Pin LQFP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	
NAME	NO.		PARALLEL INTERFACE (PAR/SER = 0)	SERIAL INTERFACE (PAR/SER = 1)
DB14/REFBUF$_{EN}$	1	DIO/DI	Data bit 14 input/output	Hardware mode (HW/SW = 0): Reference buffers enable input. When low, all reference buffers are enabled (mandatory if internal reference is used). When high, all reference buffers are disabled.
				Software mode (HW/SW = 1):Connect to BGND or BVDD. The reference buffers are controlled by bit C24 (REFBUF) in control register (CR).
DB13/SDI	2	DIO/DI	Data bit 13 input/output	Hardware mode (HW/SW = 0): Connect to BGND
				Software mode (HW/SW = 1): Serial data input
DB12	3	DIO	Data bit 12 input/output	Connect to BGND
DB11	4	DIO	Data bit 11 input/output	Connect to BGND
DB10/SDO_C	5	DIO/DO	Data bit 10 input/output	When SEL_C = 1, data output for channel C When SEL_C = 0, tie this pin to BGND
DB9/SDO_B	6	DIO/DO	Data bit 9 input/output	When SEL_B = 1, data output for channel B When SEL_B = 0, tie this pin to BGND When SEL_C = 0, data from channel C1 are also available on this output
DB8/SDO_A	7	DIO/DO	Data bit 8 input/output	Data output for channel A When SEL_C = 0, data from channel C0 are also available on this output When SEL_C = 0 and SEL_B = 0, SDO_A acts as the single data output for all channels
BGND	8	P	Buffer I/O ground, connect to digital ground plane	
BVDD	9	P	Buffer I/O supply, connect to digital supply (2.7 V to 5.5 V). Decouple with a 1-µF ceramic capacitor or a combination of 100-nF and 10-µF ceramic capacitors to BGND.	
DB7/HB$_{EN}$/DC$_{EN}$	10	DIO/DI/DI	Word mode (WORD/BYTE = 0): Data bit 7 input/output	Daisy-chain enable input. When high, DB[5:3] serve as daisy-chain inputs DCIN[A:C]. If daisy-chain mode is not used, connect to BGND.
			Byte mode (WORD/BYTE = 1): High byte enable input. When high, the high byte is output first on DB[15:8]. When low, the low byte is output first on DB[15:8].	
DB6/SCLK	11	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 6 input/output	Serial interface clock input (36 MHz, max)
			Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	
DB5/DCIN_A	12	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 5 input/output	When DC$_{EN}$ = 1, daisy-chain data input for channel A When DC$_{EN}$ = 0, connect to BGND
			Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	
DB4/DCIN_B	13	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 4 input/output	When SEL_B = 1 and DC$_{EN}$ = 1, daisy-chain data input for channel B When DC$_{EN}$ = 0, connect to BGND
			Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	
DB3/DCIN_C	14	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 3 input/output	When SEL_C = 1 and DC$_{EN}$ = 1, daisy-chain data input for channel C When DC$_{EN}$ = 0, connect to BGND
			Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	
DB2/SEL_C	15	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 2 input/output	Select SDO_C input. When high, SDO_C is active. When low, SDO_C is disabled.
			Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	
DB1/SEL_B	16	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 1 input/output	Select SDO_B input. When high, SDO_B is active. When low, SDO_B is disabled.
			Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	

(1) AI = analog input; AIO = analog input/output; DI = digital input; DO = digital output; DIO = digital input/output; and P = power supply.

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION	
NAME	NO.		PARALLEL INTERFACE (PAR/SER = 0)	SERIAL INTERFACE (PAR/SER = 1)
DB0/SEL_A	17	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 0 (LSB) input/output Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	Select SDO_A input. When high, SDO_A is active. When low, SDO_A is disabled. Must always be high.
BUSY/INT	18	DO	When CR bit C21 = 0 (BUSY/INT), converter busy status output. Transitions high when a conversion starts and remains high during the entire process. Transitions low when the conversion data of all six channels are latched to the output register and remains low thereafter. In sequential mode (SEQ = 1 in the CR), the BUSY output transitions high when a conversion starts and goes low for a single conversion clock cycle (t_{CCLK}) whenever a channel pair conversion completes. When bit C21 = 1 (BUSY/INT in CR), interrupt output. This bit transitions high after a conversion completes and goes low with the first read data access. The polarity of BUSY/INT output can be changed using bit C20 (BUSY L/H) in the control register.	
$\overline{CS}/\overline{FS}$	19	DI/DI	Chip select input. When low, the parallel interface is enabled. When high, the interface is disabled.	Frame synchronization. The falling edge of $\overline{FS}$ controls the frame transfer.
$\overline{RD}$	20	DI	Read data input. When low, the parallel data output is enabled. When high, the data output is disabled.	Connect to BGND
CONVST_C	21	DI	Hardware mode (HW/SW = 0): Conversion start of channel pair C. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_C[1:0]. Software mode (HW/SW = 1): Conversion start of channel pair C in sequential mode (CR bit C23 = 1) only; connect to BGND or BVDD otherwise	
CONVST_B	22	DI	Hardware mode (HW/SW = 0): Conversion start of channel pair B. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_B[1:0]. Software mode (HW/SW = 1): Conversion start of channel pair B in sequential mode (CR bit C23 = 1) only; connect to BGND or BVDD otherwise	
CONVST_A	23	DI	Hardware mode (HW/SW = 0): Conversion start of channel pair A. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_A[1:0]. Software mode (HW/SW = 1): Conversion start of all selected channels except in sequential mode (CR bit C23 = 1): Conversion start of channel pair A only	
$\overline{STBY}$	24	DI	Standby mode input. When low, the entire device is powered down (including the internal clock and reference). When high, the device operates in normal mode.	
AGND	25, 32, 37, 38, 43, 44, 49, 52, 53, 55, 57, 59	P	Analog ground, connect to analog ground plane Pin 25 can have a dedicated ground if the difference between its potential and AGND is always kept within ±300 mV.	
AVDD	26, 34, 35, 40, 41, 46, 47, 50, 60	P	Analog power supply (4.5 V to 5.5 V). Decouple each pin with a 100-nF ceramic capacitor to AGND. Use an additional 10-µF capacitor to AGND close to the device but without compromising the placement of the smaller capacitor. Pin 26 can have a dedicated power supply if the difference between its potential and AVDD is always kept within ±300 mV.	
RANGE/XCLK	27	DI/DIO	Hardware mode (HW/SW = 0): Input voltage range select input. When low, the analog input range is ±4 V_{REF}. When high, the analog input range is ±2 V_{REF}. Software mode (HW/SW = 1): External conversion clock input, if CR bit C11 (CLKSEL) is set high or internal conversion clock output, if CR bit C10 (CLKOUT_EN) is set high. If not used, connect to BVDD or BGND.	
RESET	28	DI	Reset input, active high. Aborts any ongoing conversions. Resets the internal control register to 0x000003FF. The RESET pulse must be at least 50 ns long.	
WORD/BYTE	29	DI	Output mode selection input. When low, data are transferred in word mode using DB[15:0]. When high, data are transferred in byte mode using DB[15:8] with the byte order controlled by HB_{EN} pin when two accesses are required for a complete 16-bit transfer.	Connect to BGND
HVSS	30	P	Negative supply voltage for the analog inputs (–16.5 V to –5 V). Decouple with a 10-0nF ceramic capacitor to AGND placed next to the device and a 10-µF capacitor to AGND close to the device but without compromising the placement of the smaller capacitor.	
HVDD	31	P	Positive supply voltage for the analog inputs (5 V to 16.5 V). Decouple with a 100-nF ceramic capacitor to AGND placed next to the device and a 10-µF capacitor to AGND close to the device but without compromising the placement of the smaller capacitor.	
CH_A0	33	AI	Analog input of channel A0. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C26 (RANGE_A) in software mode.	
CH_A1	36	AI	Analog input of channel A1. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C26 (RANGE_A) in software mode.	

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION	
NAME	NO.		PARALLEL INTERFACE (PAR/SER = 0)	SERIAL INTERFACE (PAR/SER = 1)
CH_B0	39	AI	Analog input of channel B0. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C27 (RANGE_B) in software mode.	
CH_B1	42	AI	Analog input of channel B1. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C27 (RANGE_B) in software mode.	
CH_C0	45	AI	Analog input of channel C0. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C28 (RANGE_C) in software mode.	
CH_C1	48	AI	Analog input of channel C1. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C28 (RANGE_C) in software mode.	
REFIO	51	AIO	Reference voltage input/output (0.5 V to 3.025 V). The internal reference is enabled through REF_{EN}/WR pin in hardware mode or CR bit C25 (REF_{EN}) in software mode. The output value is controlled by the internal DAC (CR bits C[9:0]). Connect a 470-nF ceramic decoupling capacitor between this pin and pin 52.	
REFC_A	54	AI	Decoupling capacitor for reference of channels A. Connect a 10-µF ceramic decoupling capacitor between this pin and pin 53.	
REFC_B	56	AI	Decoupling capacitor for reference of channels B. Connect a 10-µF ceramic decoupling capacitor between this pin and pin 55.	
REFC_C	58	AI	Decoupling capacitor for reference of channels C. Connect a 10-µF ceramic decoupling capacitor between this pin and pin 57.	
PAR/SER	61	DI	Interface mode selection input. When low, the parallel interface is selected. When high, the serial interface is enabled.	
HW/SW	62	DI	Mode selection input. When low, the hardware mode is selected and the device works according to the settings of external pins. When high, the software mode is selected in which the device is configured by writing into the control register.	
REF_{EN}/WR	63	DI	Hardware mode (HW/SW = 0): Internal reference enable input. When high, the internal reference is enabled (the reference buffers are to be enabled). When low, the internal reference is disabled and an external reference is applied at REFIO.	Hardware mode (HW/SW = 0): Internal reference enable input. When high, the internal reference is enabled (the reference buffers are to be enabled). When low, the internal reference is disabled and an external reference must be applied at REFIO.
			Software mode (HW/SW = 1): Write input. The parallel data input is enabled when $\overline{CS}$ and WR are low. The internal reference is enabled by the CR bit C25 (REF_{EN}).	Software mode (HW/SW = 1): Connect to BGND or BVDD. The internal reference is enabled by CR bit C25 (REF_{EN}).
DB15	64	DIO	Data bit 15 (MSB) input/output	Connect to BGND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, HVDD to AGND	–0.3	18	V
Supply voltage, HVSS to AGND	–18	0.3	V
Supply voltage, AVDD to AGND	–0.3	6	V
Supply voltage, BVDD to BGND	–0.3	6	V
Analog input voltage	HVSS – 0.3	HVDD + 0.3	V
Reference input voltage with respect to AGND	AGND – 0.3	AVDD + 0.3	V
Digital input voltage with respect to BGND	BGND – 0.3	BVDD + 0.3	V
Ground voltage difference AGND to BGND		±0.3	V
Input current to all pins except supply	–10	10	mA
Maximum virtual junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AVDD to AGND		4.5	5	5.5	V
Supply voltage, BVDD to BGND	Low-voltage levels	2.7	3	3.6	V
	5-V logic levels	4.5	5	5.5	
Input supply voltage, HVDD to AGND	Input range = ±2 × V_{REF}	2 × V_{REF}		16.5	V
	Input range = ±4 × V_{REF}	4 × V_{REF}		16.5	
Input supply voltage, HVSS to AGND	Input range = ±2 × V_{REF}	–16.5		–2 × V_{REF}	V
	Input range = ±4 × V_{REF}	–16.5		–4 × V_{REF}	
Reference input voltage (V_{REF})		0.5	2.5	3	V
Analog inputs (also see the *Analog Inputs* section)	Input range = ±2 × V_{REF}	–2 × V_{REF}		2 × V_{REF}	V
	Input range = ±4 × V_{REF}	–4 × V_{REF}		4 × V_{REF}	
Operating ambient temperature, T_A		–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		ADS8555 PM (LQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range of –40°C to 125°C, AVDD = 4.5 V to 5.5 V, BVDD = 2.7 V to 5.5 V, HVDD = 10 V to 15 V, HVSS = –15 V to –10 V, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DC ACCURACY						
Resolution				16		Bits
No missing codes			16			Bits
Integral linearity error	INL	At T_A = –40°C to 85°C	–3	±1.5	3	LSB
		At T_A = –40°C to 125°C	–4	±1.5	4	
Differential linearity error	DNL	At T_A = –40°C to 85°C	–1	±0.75	1.5	LSB
		At T_A = –40°C to 125°C	–1	±0.75	2	
Offset error			–4	±0.8	4	mV
Offset error drift				±3.5		µV/°C
Gain error		Referenced to voltage at REFIO	–0.75	±0.25	0.75	%FSR
Gain error drift		Referenced to voltage at REFIO		±6		ppm/°C
Power-supply rejection ratio	PSRR	At output code FFFFh, related to AVDD		60		dB
SAMPLING DYNAMICS						
Acquisition time	t_{ACQ}		280			ns
Conversion time per ADC	t_{CONV}				1.26	µs
Internal conversion clock period	t_{CCLK}				18.5	t_{CCLK}
					68	ns
Throughput rate	f_{DATA}	Parallel interface, internal clock and reference			630	kSPS
		Serial interface, internal clock and reference			450	
AC ACCURACY						
Signal-to-noise ratio	SNR	At f_{IN} = 10 kHz, T_A = –40°C to 85°C	90	91.5		dB
		At f_{IN} = 10 kHz, T_A = –40°C to 125°C	89	91.5		
Signal-to-noise ratio + distortion	SINAD	At f_{IN} = 10 kHz, T_A = –40°C to 85°C	87	89.5		dB
		At f_{IN} = 10 kHz, T_A = –40°C to 125°C	86.5	89.5		
Total harmonic distortion(2)	THD	At f_{IN} = 10 kHz, T_A = –40°C to 85°C		–94	–90	dB
		At f_{IN} = 10 kHz, T_A = –40°C to 125°C		–94	–89.5	
Spurious-free dynamic range	SFDR	At f_{IN} = 10 kHz, T_A = –40°C to 85°C	90	95		dB
		At f_{IN} = 10 kHz, T_A = –40°C to 125°C	89.5	95		
Channel-to-channel isolation		At f_{IN} = 10 kHz		100		dB
–3-dB small-signal bandwidth		Input range = ±4 × V_{REF}		48		MHz
		Input range = ±2 × V_{REF}		24		
ANALOG INPUT						
Bipolar full-scale range	CHXX	RANGE pin, RANGE bit = 0	–4 × V_{REF}		4 × V_{REF}	V
		RANGE pin, RANGE bit = 1	–2 × V_{REF}		2 × V_{REF}	
Input capacitance		Input range = ±4 × V_{REF}		10		pF
		Input range = ±2 × V_{REF}		20		
Input leakage current		No ongoing conversion			±1	µA
Aperture delay				5		ns
Aperture delay matching		Common CONVST for all channels		250		ps
Aperture jitter				50		ps
EXTERNAL CLOCK INPUT (XCLK)						
External clock frequency	f_{XCLK}	An external reference must be used for $f_{XCLK} > f_{CCLK}$	1	18	20	MHz
External clock duty cycle			45%		55%	

(1) All values are at T_A = 25°C.
(2) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics (continued)

over recommended operating free-air temperature range of –40°C to 125°C, AVDD = 4.5 V to 5.5 V, BVDD = 2.7 V to 5.5 V, HVDD = 10 V to 15 V, HVSS = –15 V to –10 V, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
REFERENCE VOLTAGE OUTPUT (REF_{OUT})						
Reference voltage	V_{REF}	2.5-V operation, REFDAC = 0x3FF	2.485	2.5	2.515	V
		2.5-V operation, REFDAC = 0x3FF at 25°C	2.496	2.5	2.504	
		3-V operation, REFDAC = 0x3FF	2.985	3	3.015	
		3-V operation, REFDAC = 0x3FF at 25°C	2.995	3	3.005	
Reference voltage drift	dV_{REF}/dT			±10		ppm/°C
Power-supply rejection ratio	PSRR			73		dB
Output current	I_{REFOUT}	With dc current	–2		2	mA
Short circuit current(3)	I_{REFSC}			50		mA
Turnon settling time	t_{REFON}			10		ms
External load capacitance		At CREF_x pins	4.7	10		µF
		At REFIO pins	100	470		nF
Tuning range	REFDAC	Internal reference output voltage range	0.2 × V_{REF}		V_{REF}	V
REFDAC resolution			10			Bits
REFDAC differential nonlinearity	DNL_{DAC}		–1	±0.1	1	LSB
REFDAC integral nonlinearity	INL_{DAC}		–2	±0.1	2	LSB
REFDAC offset error	V_{OSDAC}	V_{REF} = 0.5 V (DAC = 0x0CC)	–4	±0.65	4	LSB
REFERENCE VOLTAGE INPUT (REF_{IN})						
Reference input voltage	V_{REFIN}		0.5	2.5	3.025	V
Input resistance				100		MΩ
Input capacitance				5		pF
Reference input current					1	µA
SERIAL CLOCK INPUT (SCLK)						
Serial clock input frequency	f_{SCLK}		0.1		36	MHz
Serial clock period	t_{SCLK}		0.0278		10	µs
Serial clock duty cycle			40%		60%	
DIGITAL INPUTS(4)						
Logic family			CMOS with Schmitt-Trigger			
High-level input voltage			0.7 × BVDD		BVDD + 0.3	V
Low-level input voltage			BGND – 0.3		0.3 × BVDD	V
Input current		V_I = BVDD to BGND	–50		50	nA
Input capacitance				5		pF
DIGITAL OUTPUTS(4)						
Logic family				CMOS		
High-level output voltage		I_{OH} = 100 µA	BVDD – 0.6		BVDD	V
Low-level output voltage		I_{OH} = –100 µA	BGND		BGND + 0.4	V
High-impedance-state output current			–50		50	nA
Output capacitance				5		pF
Load capacitance					30	pF

(3) Reference output current is not limited internally.
(4) Specified by design.

Electrical Characteristics (continued)

over recommended operating free-air temperature range of –40°C to 125°C, AVDD = 4.5 V to 5.5 V, BVDD = 2.7 V to 5.5 V, HVDD = 10 V to 15 V, HVSS = –15 V to –10 V, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
Analog supply voltage	AVDD		4.5	5	5.5	V
Buffer I/O supply voltage	BVDD		2.7	3	5.5	V
Input positive supply voltage	HVDD		5	10	16.5	V
Input negative supply voltage	HVSS		–16.5	–10	–5	V
Analog supply current(5)	IAVDD	f_{DATA} = maximum		30	36	mA
		f_{DATA} = 250 kSPS (auto-NAP mode)		14	16.5	
		Auto-NAP mode, no ongoing conversion, internal conversion clock		4	6	
		Power-down mode		0.1	50	µA
Buffer I/O supply current(6)	IBVDD	f_{DATA} = maximum		0.9	2	mA
		f_{DATA} = 250 kSPS (auto-NAP mode)		0.5	1.5	
		Auto-NAP mode, no ongoing conversion, internal conversion clock		0.1	10	µA
		Power-down mode		0.1	10	
Input positive supply current(7)	IHVDD	f_{DATA} = maximum		3	3.5	mA
		f_{DATA} = 250 kSPS (auto-NAP mode)		1.6	2	
		Auto-NAP mode, no ongoing conversion, internal conversion clock		0.2	0.3	µA
		Power-down mode		0.1	10	
Input negative supply current(8)	IHVSS	f_{DATA} = maximum		3.6	4	mA
		f_{DATA} = 250 kSPS (auto-NAP mode)		1.8	2.2	
		Auto-NAP mode, no ongoing conversion, internal conversion clock		0.2	0.25	µA
		Power-down mode		0.1	10	
Power dissipation(9)		f_{DATA} = maximum		251.7	298.5	mW
		f_{DATA} = 250 kSPS (auto-NAP mode)		122.5	150	
		Auto-NAP mode, no ongoing conversion, internal conversion clock		26	38.3	
		Power-down mode		3.8	580	µW

(5) At AVDD = 5 V.
(6) At BVDD = 3 V, parallel mode, load capacitance = 6 pF per pin.
(7) At HVDD = 15 V.
(8) At HVSS = –15 V.
(9) At AVDD = 5 V, BVDD = 3 V, HVDD = 15 V, and HVSS = –15 V.

6.6 Serial Interface Timing Requirements

over recommended operating free-air temperature range at –40°C to 125°C, AVDD = 5 V, and BVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_{ACQ}	Acquisition time	280		ns
t_{CONV}	Conversion time		1.26	µs
t_1	CONVST_x low time	20		ns
t_2	BUSY low to $\overline{FS}$ low time	0		ns
t_3	Bus access finished to next conversion start time	40		ns
t_{D1}	CONVST_x high to BUSY high delay	5	20	ns
t_{D2}	$\overline{FS}$ low to SDO_x active delay	5	12	ns
t_{D3}	SCLK rising edge to new data valid delay		15	ns
t_{D4}	$\overline{FS}$ high to SDO_x 3-state delay		10	ns
t_{H1}	Input data to SCLK falling edge hold time	5		ns
t_{H2}	Output data to SCLK rising edge hold time	5		ns
t_{S1}	Input data to SCLK falling edge setup time	3		ns
t_{S3}	CONVST_x high to XCLK falling or rising edge setup time	6		ns
t_{SCLK}	Serial clock period	0.0278	10	µs

(1) All input signals are specified with $t_R = t_F = 1.5$ ns (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.

6.7 Parallel Interface Timing Requirements (Read Access)

over recommended operating free-air temperature range at –40°C to 125°C, AVDD = 5 V, and BVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_{ACQ}	Acquisition time	280		ns
t_{CONV}	Conversion time		1.26	µs
t_1	CONVST_x low time	20		ns
t_2	BUSY low to $\overline{CS}$ low time	0		ns
t_3	Bus access finished to next conversion start time(2)	40		ns
t_4	$\overline{CS}$ low to $\overline{RD}$ low time	0		ns
t_5	$\overline{RD}$ high to $\overline{CS}$ high time	0		ns
t_6	$\overline{RD}$ pulse width	30		ns
t_7	Minimum time between two read accesses	10		ns
t_{D1}	CONVST_x high to BUSY high delay	5	20	ns
t_{D5}	$\overline{RD}$ falling edge to output data valid delay		20	ns
t_{H3}	Output data to $\overline{RD}$ rising edge hold time	5		ns

(1) All input signals are specified with $t_R = t_F = 1.5$ ns (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.
(2) Refer to the $\overline{CS}$ signal or $\overline{RD}$, whichever occurs first.

6.8 Parallel Interface Timing Requirements (Write Access)

over recommended operating free-air temperature range at –40°C to 125°C, AVDD = 5 V, and BVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_8	$\overline{CS}$ low to WR low time	0		ns
t_9	WR low pulse duration	15		ns
t_{10}	WR high pulse duration	10		ns
t_{11}	WR high to $\overline{CS}$ high time	0		ns
t_{S2}	Output data to WR rising edge setup time	5		ns
t_{H4}	Data output to WR rising edge hold time	5		ns

(1) All input signals are specified with $t_R = t_F = 1.5$ ns (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.

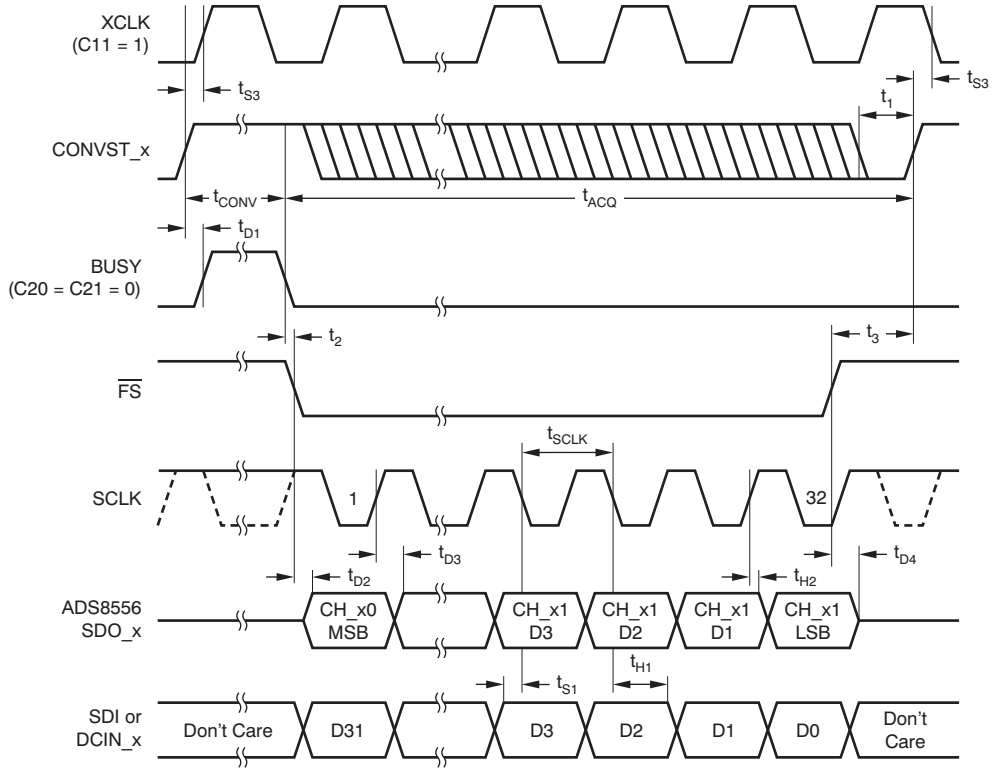


Figure 1. Serial Operation Timing Diagram (All Three SDOs Active)

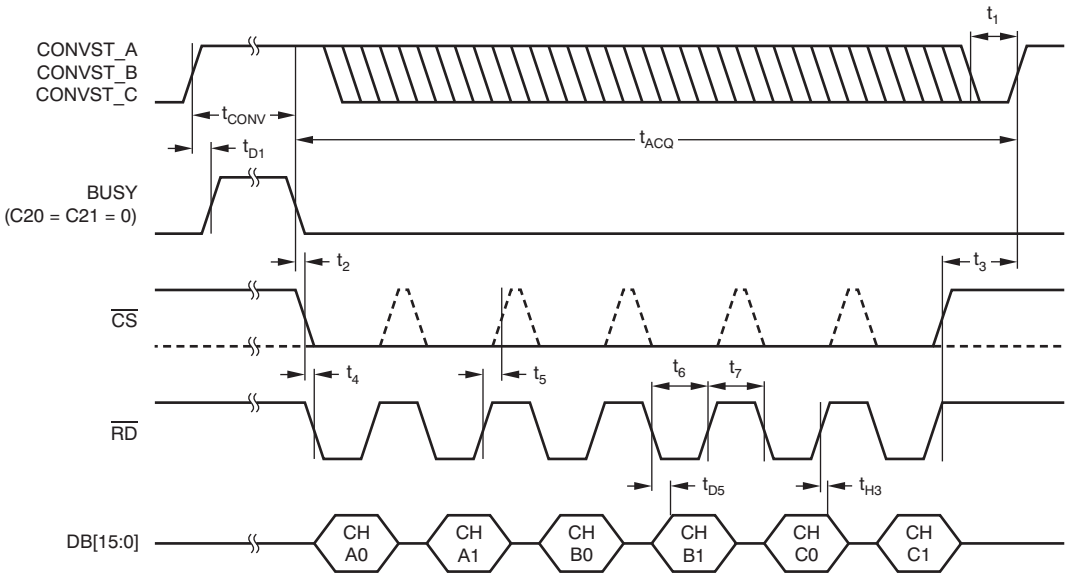


Figure 2. Parallel Read Access Timing Diagram

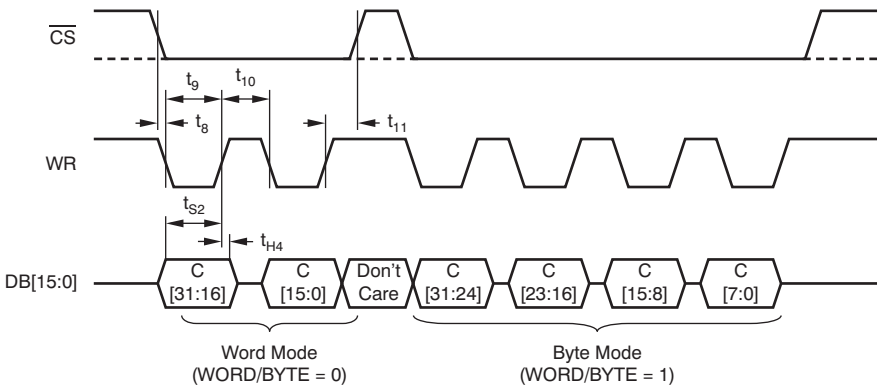


Figure 3. Parallel Write Access Timing Diagram

6.9 Typical Characteristics

at 25°C, over entire supply voltage range, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

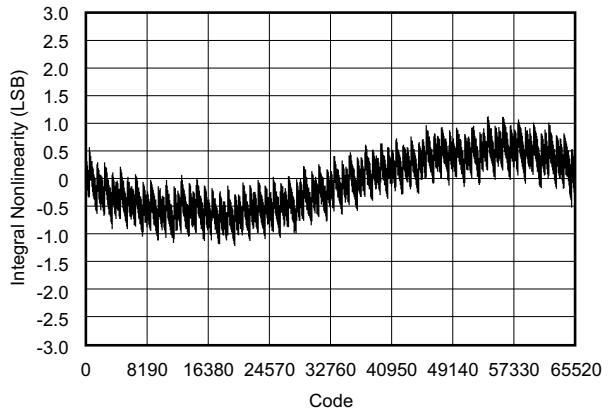


Figure 4. INL vs Code (±10-V_{IN} Range)

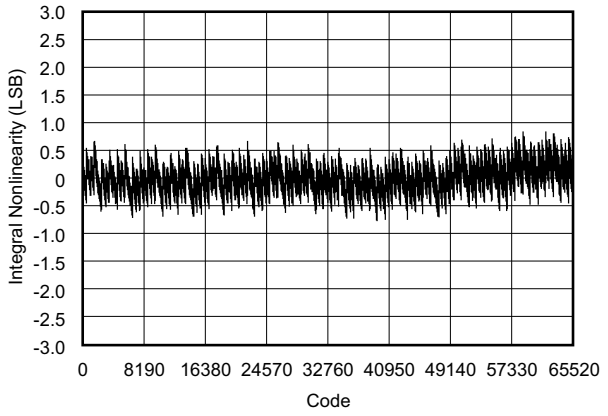


Figure 5. INL vs Code (±5-V_{IN} Range)

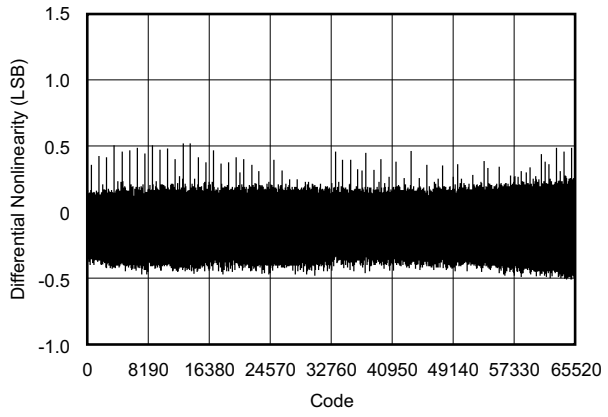


Figure 6. DNL vs Code (±10-V_{IN} Range)

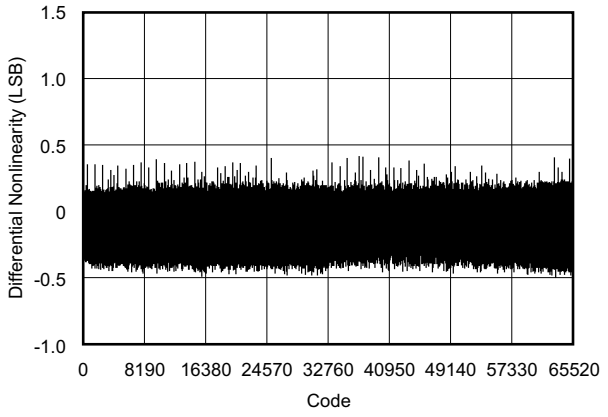


Figure 7. DNL vs Code (±5-V_{IN} Range)

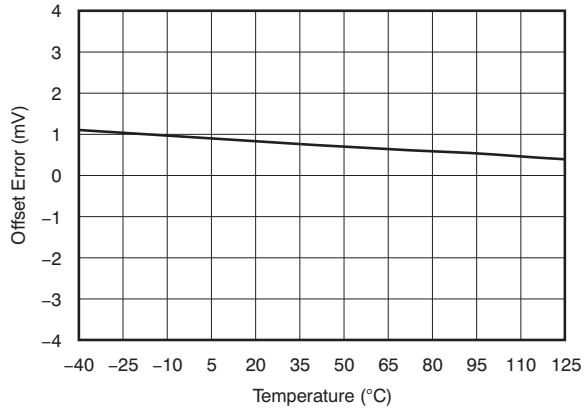


Figure 8. Offset Error vs Temperature

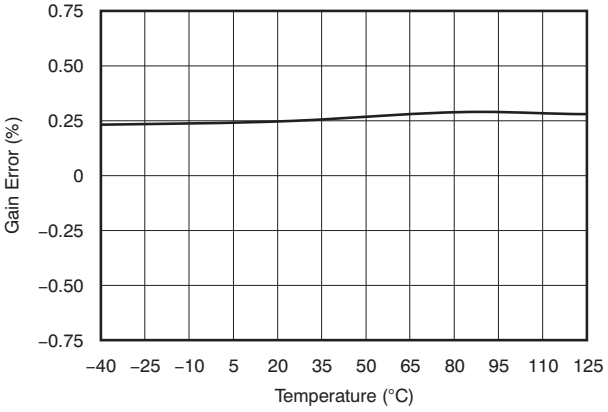


Figure 9. Gain Error vs Temperature

Typical Characteristics (continued)

at 25°C, over entire supply voltage range, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

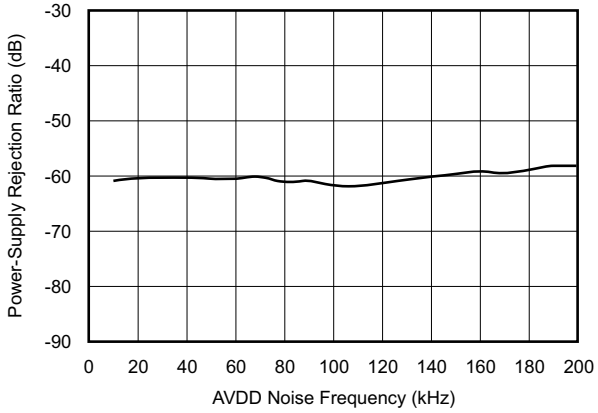


Figure 10. PSRR vs AVDD Noise Frequency

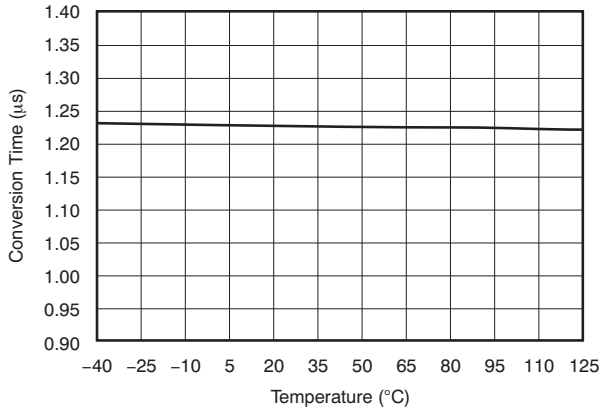


Figure 11. Conversion Time vs Temperature

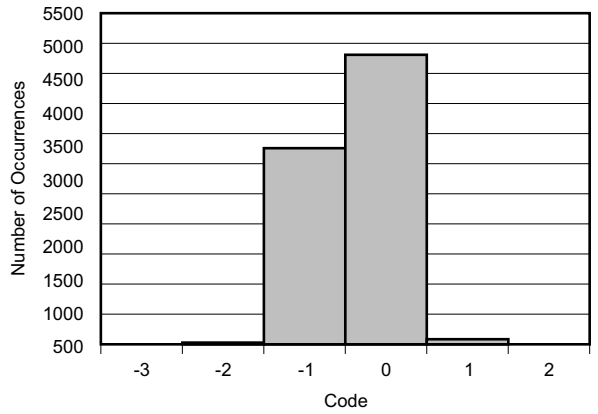


Figure 12. Code Histogram (8192 Hits)

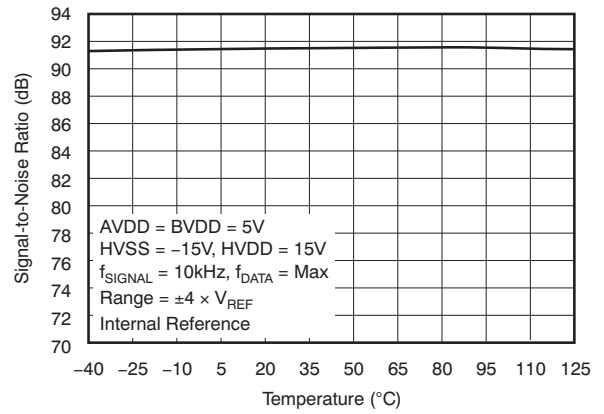


Figure 13. SNR vs Temperature

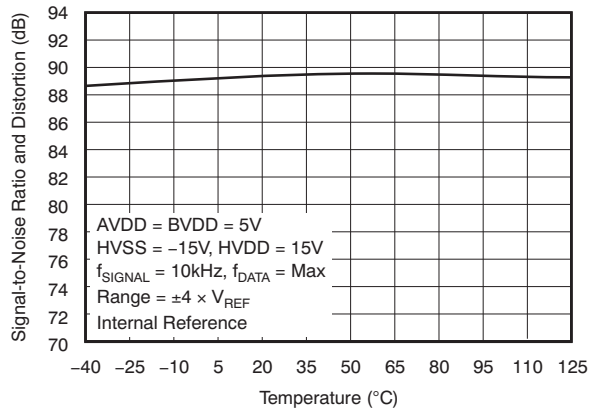


Figure 14. SINAD vs Temperature

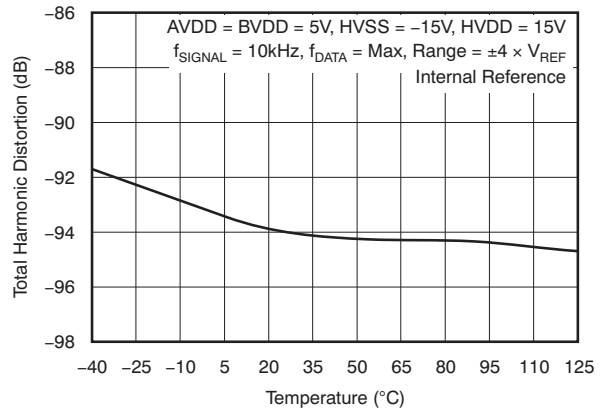


Figure 15. THD vs Temperature

Typical Characteristics (continued)

at 25°C, over entire supply voltage range, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

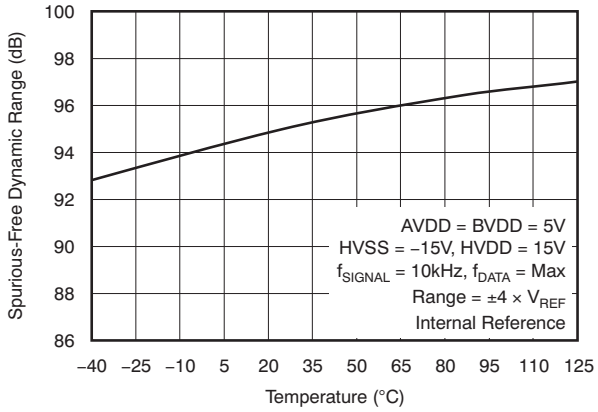


Figure 16. SFDR vs Temperature

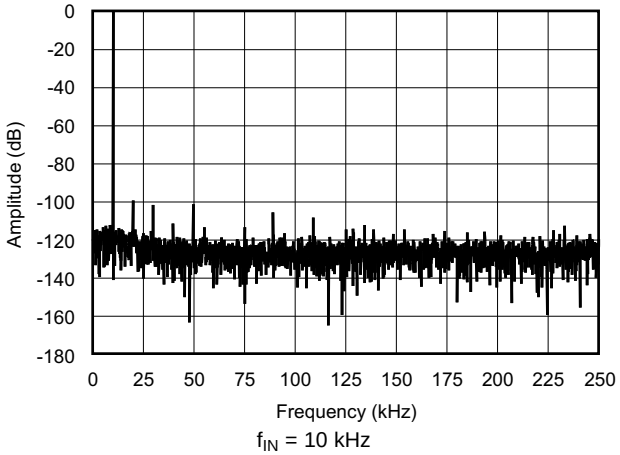


Figure 17. Frequency Spectrum (2048-Point FFT, ±10-V_{IN} Range)

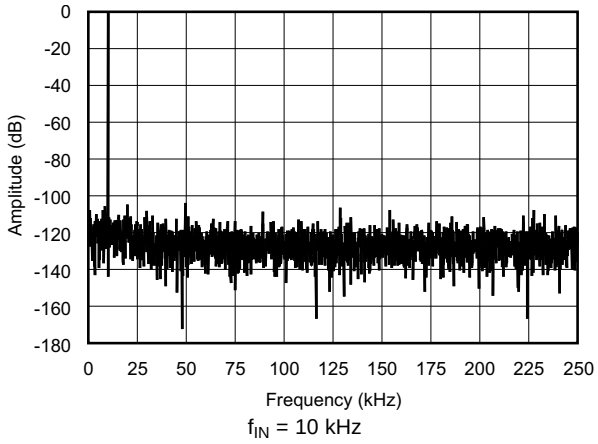


Figure 18. Frequency Spectrum (2048-Point FFT, ±5-V_{IN} Range)

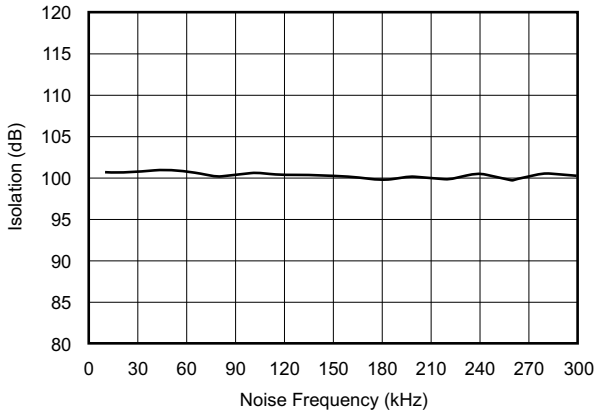


Figure 19. Channel-to-Channel Isolation vs Input Noise Frequency

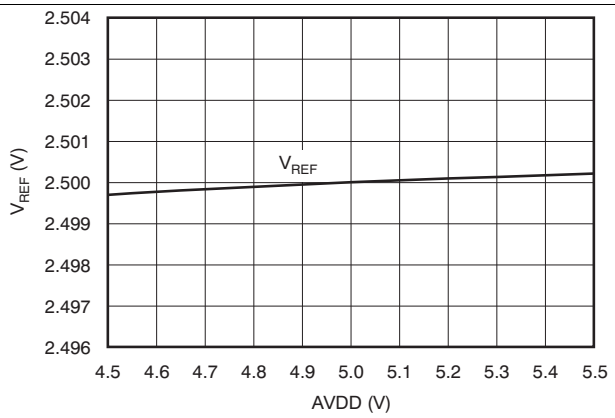


Figure 20. Internal Reference Voltage vs Analog Supply Voltage (2.5-V Mode)

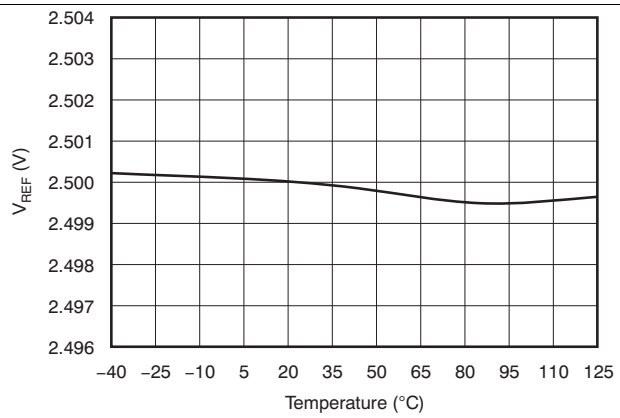


Figure 21. Internal Reference Voltage vs Temperature (2.5-V Mode)

Typical Characteristics (continued)

at 25°C, over entire supply voltage range, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

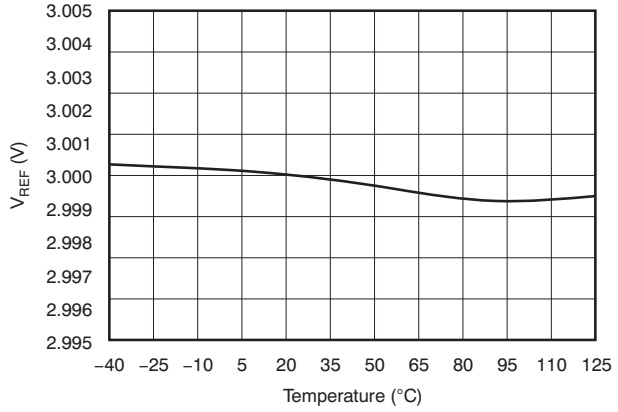


Figure 22. Internal Reference Voltage vs Temperature (3-V Mode)

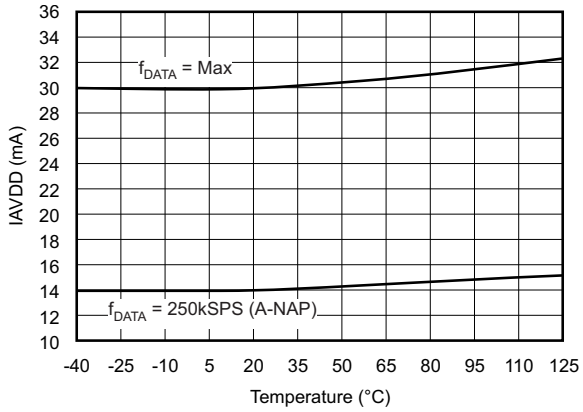


Figure 23. Analog Supply Current vs Temperature

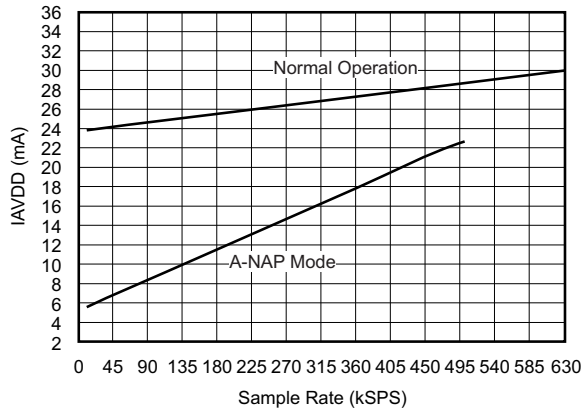


Figure 24. Analog Supply Current vs Data Rate

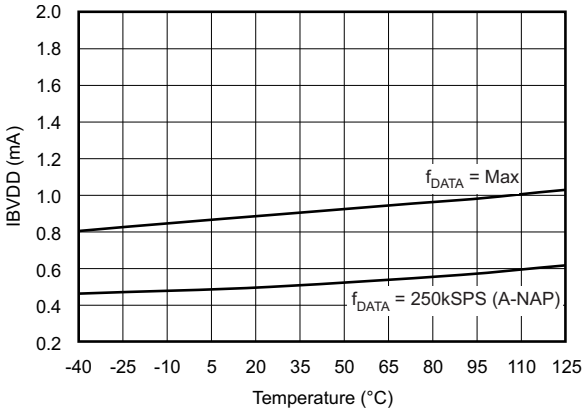


Figure 25. Buffer I/O Supply Current vs Temperature

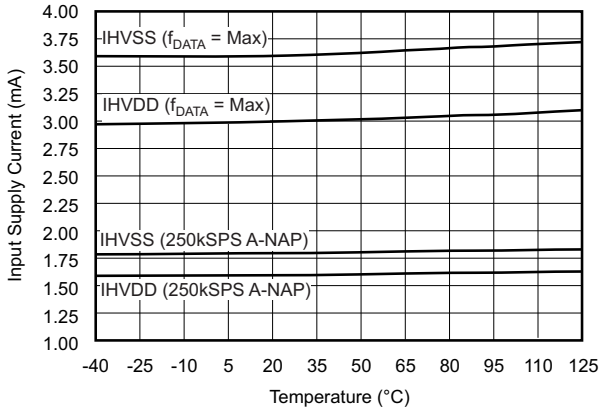


Figure 26. Input Supply Current vs Temperature

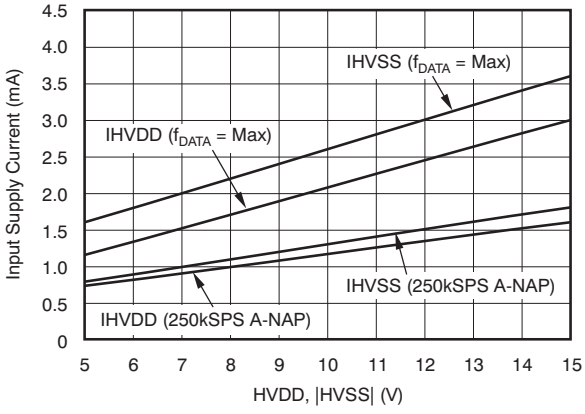


Figure 27. Input Supply Current vs Input Supply Voltage

Typical Characteristics (continued)

at 25°C, over entire supply voltage range, V_{REF} = 2.5 V (internal), and f_{DATA} = maximum (unless otherwise noted)

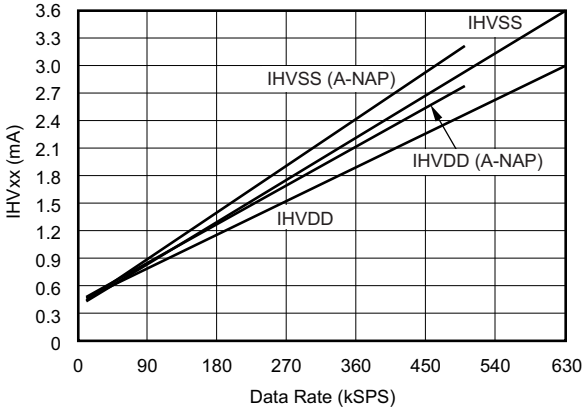


Figure 28. Input Supply Current vs Data Rate

7 Detailed Description

7.1 Overview

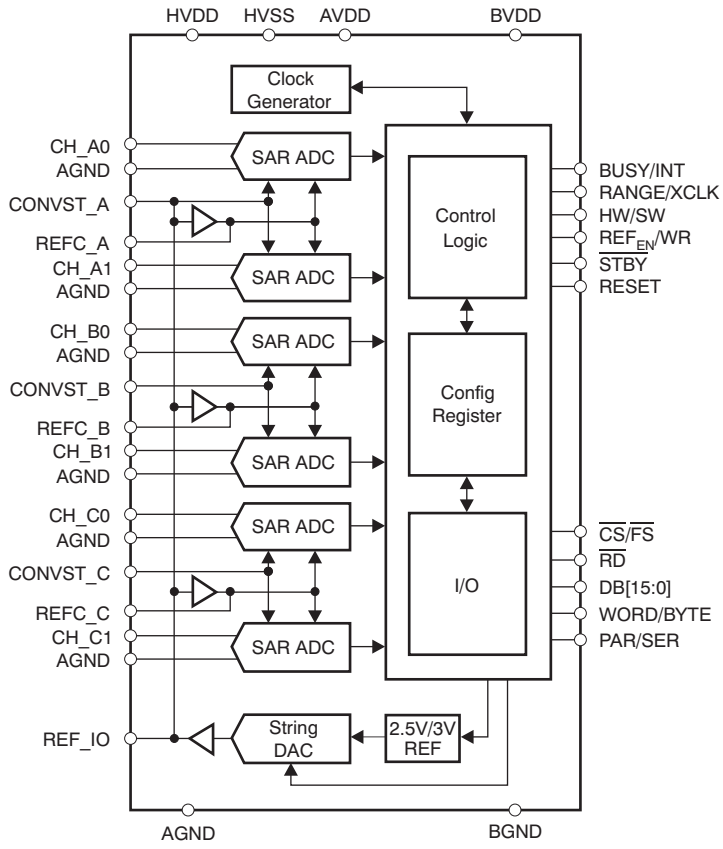
The ADS8555 device includes six 16-bit analog-to-digital converters (ADCs) that operate based on the successive approximation register (SAR) principle. The architecture is designed on the charge redistribution principle that inherently includes a sample-and-hold function. The six analog inputs are grouped into three channel pairs. These channel pairs can be sampled and converted simultaneously, preserving the relative phase information of the signals of each pair. Separate conversion start signals allow simultaneous sampling on each channel pair, on four channels or on all six channels.

These devices accept single-ended, bipolar analog input signals in the selectable ranges of ±4 V_{REF} or ±2 V_{REF} with an absolute value of up to ±12 V; see the *Analog Inputs* section for more details.

The devices offer an internal 2.5-V, 3-V reference source followed by a 10-bit, digital-to-analog converter (DAC) that allows the reference voltage V_{REF} to be adjusted in 2.44-mV or 2.93-mV steps, respectively.

The ADS8555 device also offers a selectable parallel or serial interface that can be used in hardware or software mode; see the *Device Configuration* section for details.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog

This section addresses the analog input circuit, the ADCs and control signals, and the reference design of the device.

7.3.1.1 Analog Inputs

The inputs and the converters are of the single-ended, bipolar type. The absolute voltage range can be selected using the RANGE pin (in hardware mode) or RANGE_x bits (in software mode) in the control register (CR, see Table 5) to either ±4 V_{REF} or ±2 V_{REF}. With the reference set to 2.5 V (CR bit C18 = 0), the input voltage range can be ±10 V or ±5 V. With the reference source set to 3 V (CR bit C18 = 1), an input voltage range of ±12 V or ±6 V can be configured. The logic state of the RANGE pin is latched with the falling edge of BUSY (if CR bit C20 = 0).

The input current on the analog inputs depends on the actual sample rate, input voltage, and signal source impedance. Essentially, the current into the analog inputs charges the internal capacitor array only during the sampling period (t_{ACQ}). The source of the analog input voltage must be able to charge the input capacitance of 10 pF in ±4-V_{REF} mode or 20 pF in ±2-V_{REF} mode to a 12-, 14-, 16-bit accuracy level within the acquisition time of 280 ns at maximum data rate, as shown in Figure 29.

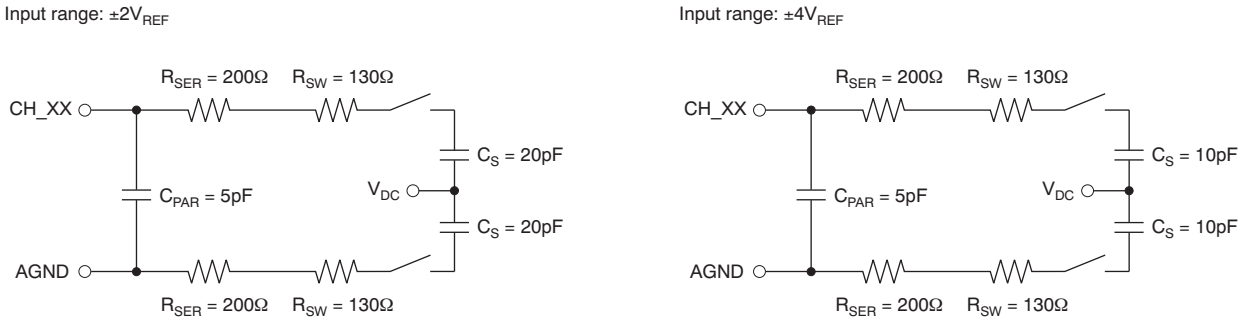


Figure 29. Equivalent Input Circuits

During the conversion period, there is no further input current flow and the input impedance is greater than 1 MΩ. To ensure a defined start condition, the sampling capacitors of the ADS8555 device are precharged to a fixed internal voltage, before switching into sampling mode.

To maintain the linearity of the converter, the inputs must always remain within the specified range of HVSS – 0.2 V to HVDD + 0.2 V.

The minimum –3-dB bandwidth of the driving operational amplifier can be calculated using Equation 1:

$$f_{-3dB} = \frac{\ln(2) \times (n + 1)}{2\pi \times t_{ACQ}} \quad (1)$$

where

- n = 16 (*n* is the resolution of the device)

With a minimum acquisition time of t_{ACQ} = 280 ns, the required minimum bandwidth of the driving amplifier is 6.7 MHz. The required bandwidth can be lower if the application allows a longer acquisition time. A gain error occurs if a given application does not fulfill the bandwidth requirement shown in Equation 1.

Feature Description (continued)

A driving operational amplifier may not be required if the impedance of the signal source (R_{SOURCE}) fulfills the requirement of Equation 2:

$$R_{SOURCE} < \frac{t_{ACQ}}{C_S \ln(2) \times (n + 1)} - (R_{SER} + R_{SW}) \quad (2)$$

where

- n = 16 (*n* is the resolution of the ADC)
- C_S = 10 pF is the sample capacitor value for V_{IN} = ±4 × V_{REF} mode
- R_{SER} = 200 Ω is the input resistor value
- R_{SW} = 130 Ω is the switch resistance value

With t_{ACQ} = 280 ns, the maximum source impedance must be less than 2 kΩ in V_{IN} = ±4-V_{REF} mode or less than 0.9 kΩ in V_{IN} = ±2-V_{REF} mode. The source impedance can be higher if the application allows longer acquisition time.

7.3.1.2 Analog-to-Digital Converter (ADC)

The devices include six ADCs that operate with either an internal or an external conversion clock. The conversion time is 1.26 µs with the internal conversion clock. When an external clock and reference are used, the minimum conversion time is 925 ns.

7.3.1.3 Conversion Clock

The device uses either an internally-generated or an external (XCLK) conversion clock signal (in software mode only). In default mode, the device generates an internal clock. When the CLKSEL bit is set high (bit C11 in *Table 5*), an external conversion clock of up to 20 MHz (maximum) can be applied on pin 27. In both cases, 18.5 clock cycles are required for a complete conversion including the precharging of the sample capacitors. The external clock can remain low between conversions.

The conversion clock duty cycle must be 50%. However, the ADS8555 device functions properly with a duty cycle from 45% to 55%.

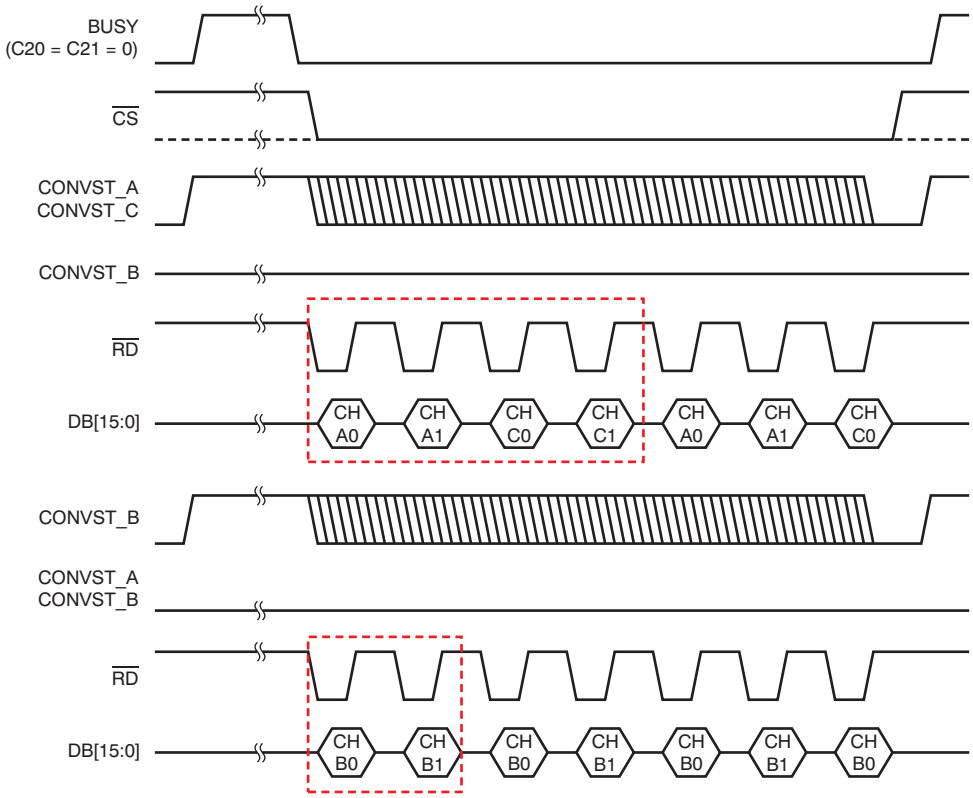
Feature Description (continued)

7.3.1.4 CONVST_x

The analog inputs of each channel pair (CH_x0, CH_x1) are held with the rising edge of the corresponding CONVST_x signal. Only in software mode (except sequential mode), CONVST_A is used for all six ADCs. The conversion automatically starts with the next edge of the conversion clock.

A conversion start must not be issued during an ongoing conversion on the same channel pair. However, conversions are allowed to be initiated on other input pairs; see the *Sequential Mode* section for more details.

If a parallel interface is used, the behavior of the output port depends on which CONVST_x signals are issued. Figure 30 shows examples of different scenarios.



NOTE: Boxed areas indicate the minimum required frame to acquire all data.

Figure 30. Data Output vs CONVST_x

Feature Description (continued)

7.3.1.5 BUSY/INT

The BUSY signal indicates if a conversion is in progress. The BUSY signal goes high with a rising edge of any CONVST_x signal and goes low when the output data of the last channel pair are available in the respective output register. The readout of the data can be initiated immediately after the falling edge of BUSY.

In sequential mode, the BUSY signal goes low only for one clock cycle; see the *Sequential Mode* section for more details.

The INT output goes high at completion of a conversion process and remains high after first read data access.

The polarity of the BUSY/INT signal can be changed using Table 5 bit C20.

7.3.1.6 Reference

The ADS8555 device provides an internal, low-drift, 2.5-V reference source. To increase the input voltage range, the reference voltage can be switched to 3-V mode using the VREF bit (bit C18 in the CR). The reference feeds a 10-bit string-DAC controlled by bits C[9:0] in the control register. The buffered DAC output is connected to the REFIO pin. In this way, the voltage at this pin is programmable in 2.44 mV (2.92 mV in 3-V mode) steps and adjustable to the application needs without additional external components. The actual output voltage can be calculated using Equation 3:

$$V_{REF} = \frac{\text{Range} \times (\text{Code} + 1)}{1024} \quad (3)$$

where

- Range = the chosen maximum reference voltage output range (2.5 V or 3 V)
- Code = the decimal value of the DAC register content

Table 1 lists some examples of internal reference DAC settings with a reference range set to 2.5 V. However, to ensure proper performance, the DAC output voltage should not be programmed below 0.5 V.

Decouple the buffered output of the DAC with a 100-nF capacitor (minimum); for best performance, TI recommends a 470-nF capacitor. If the internal reference is placed into power-down (default), an external reference voltage can drive the REFIO pin.

The voltage at the REFIO pin is buffered with three internal amplifiers, one for each ADC pair. The output of each buffer must be decoupled with a 10-µF capacitor between pin pairs 53 and 54, 55 and 56, and 57 and 58. The 10-µF capacitors are available as ceramic 0805-SMD components and in X5R quality.

The internal reference buffers can be powered down to decrease the power dissipation of the device. In this case, external reference drivers can be connected to REFC_A, REFC_B, and REFC_C pins. With 10-µF decoupling capacitors, the minimum required bandwidth can be calculated using Equation 4.

$$f_{-3dB} = \frac{\ln(2)}{2\pi \times t_{CONV}} \quad (4)$$

With the minimum t_{CONV} of 1.26 µs, the external reference buffers require a minimum bandwidth of 88 kHz.

Table 1. DAC Setting Examples (2.5-V Operation)

$V_{REF\ OUT}$ (V)	DECIMAL CODE	BINARY CODE	HEXADECIMAL CODE
0.5	204	00 1100 1100	CC
1.25	511	01 1111 1111	1FF
2.5	1023	11 1111 1111	3FF

7.3.2 Digital

This section describes the digital control and the timing of the device in detail.

7.3.2.1 Device Configuration

Depending on the desired mode of operation, the ADS8555 device can be configured using the external pins or the control register (see Table 5), as shown in Table 2.

Table 2. ADS8555 Configuration Settings

INTERFACE MODE	HARDWARE MODE (HW/SW = 0) CONVERSION START CONTROLLED BY SEPARATE CONVST_x PINS	SOFTWARE MODE (HW/SW = 1) CONVERSION START CONTROLLED BY CONVST_A PIN ONLY, EXCEPT IN SEQUENTIAL MODE
Parallel (PAR/SER = 0)	Configuration using pins, optionally, control bits C[22:18], C[15:13], and C[9:0]	Configuration using control register bits C[31:0] only; status of pins 27 (only if used as RANGE input) and 63 is disregarded
Serial (PAR/SER = 1)	Configuration using pins, optionally, control bits C[22:18], C[15:13], and C[9:0]; bits C[31:24] are disregarded	Configuration using control register bits C[31:0] only; status of pins 1, 27 (only if used as RANGE input), and 63 is disregarded; each access requires a control register update through SDI (see the *Serial Interface* section for details)

7.3.2.2 Parallel Interface

To use the device with the parallel interface, hold the PAR/SER pin low. The maximum achievable data throughput rate using the internal clock is 630 kSPS in this case.

Access to the ADS8555 device is controlled as illustrated in Figure 2 and Figure 3.

The device can either operate with a 16-bit (WORD/BYTE pin set low) or an 8-bit (WORD/BYTE pin set high) parallel interface. If 8-bit operation is used, the HB_{EN} pin selects if the low-byte (DB7 low) or the high-byte (DB7 high) is available on the data output DB[15:8] first.

7.3.2.3 Serial Interface

The serial interface mode is selected by setting the PAR/SER pin high. In this case, each data transfer starts with the falling edge of the frame synchronization input ($\overline{FS}$). The conversion results are presented on the serial data output pins SDO_A, SDO_B, and SDO_C depending on the selections made using the SEL_x pins. Starting with the most significant bit (MSB), the output data are changed at the rising edge of SCLK, so that the host processor can read it at the following falling edge.

Serial data input SDI are latched at the falling edge of SCLK.

The serial interface can be used with one, two, or three output ports. These ports are enabled with pins SEL_A, SEL_B, and SEL_C. If all three serial data output ports (SDO_A, SDO_B, and SDO_C) are selected, the data can be read with either two 16-bit data transfers or with one 32-bit data transfer. The data of channels CH_x0 are available first, followed by data from channels CH_x1. The maximum achievable data throughput rate is 450 kSPS in this case.

If the application allows a data transfer using two ports only, SDO_A and SDO_B outputs are used. The device outputs data from channel CH_A0 followed by CH_A1 and CH_C0 on SDO_A, and data from channel CH_B0 followed by CH_B1 and CH_C1 occurs on SDO_B. In this case, a data transfer of three consecutive 16-bit words or one continuous 48-bit word is supported. The maximum achievable data throughput rate is 375 kSPS.

The output SDO_A is selected if only one serial data port is used in the application. The data are available in the following order: CH_A0, CH_A1, CH_B0, CH_B1, CH_C0, and, finally CH_C1. Data can be read using six 16-bit transfers, three 32-bit transfers, or a single 96-bit transfer. The maximum achievable data throughput rate is 250 kSPS in this case.

Figure 1 (the serial operation timing diagram) and Figure 31 illustrate all possible scenarios in more detail.

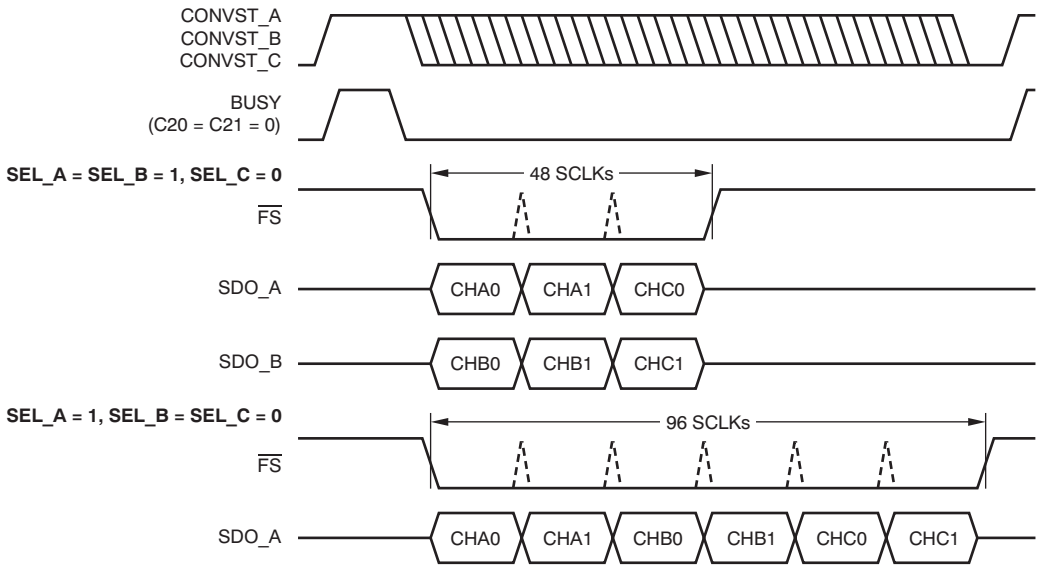


Figure 31. Serial Interface: Data Output With One or Two Active SDOs

7.3.2.4 Output Data Format

The data output format of the ADS8555 is binary twos complement, as shown in Table 3.

Table 3. Output Data Format

DESCRIPTION	INPUT VOLTAGE VALUE	BINARY CODE (HEXADECIMAL CODE)
Positive full-scale	4 V_{REF} or 2 V_{REF}	0111 1111 1111 1111 (7FFF)
Midscale + 0.5 LSB	V_{REF} / (2 × resolution)	0000 0000 0000 0000 (0000)
Midscale – 0.5 LSB	$–V_{REF}$ / (2 × resolution)	1111 1111 1111 1111 (FFFF)
Negative full-scale	–4 V_{REF} or –2 V_{REF}	1000 0000 0000 0000 (8000)

7.4 Device Functional Modes

7.4.1 Hardware Mode

With the HW/SW input (pin 62) set low, the device functions are controlled through the pins and, optionally, control register bits C[22:18], C[15:13], and C[9:0].

Generally, the device can be used in hardware mode and switched into software mode to initialize or adjust the control register settings (for example, the internal reference DAC) and then switched back to hardware mode thereafter.

7.4.2 Software Mode

When the HW/SW input is set high, the device operates in software mode with functionality set only by the control register bits (corresponding pin settings are ignored).

If parallel interface is used, an update of all control register settings is performed by issuing two 16-bit write accesses on pins DB[15:0] in word mode or four 8-bit accesses on pins DB[15:8] in byte mode (to avoid losing data, the entire sequence must be finished before starting a new conversion). Hold $\overline{CS}$ low during the two or four write accesses to completely update the configuration register. Updating only the upper eight bits (C[31:24]) is possible using a single write access and pins DB[15:8] in both word and byte modes. In word mode, the first write access updates only the upper eight bits and stores the lower eight bits (C[23:16]) for an update that takes place with the second write access along with C[15:0].

Device Functional Modes (continued)

If the serial interface is used, input data containing control register contents are required with each read access to the device in this mode (combined read/write access). For initialization purposes, all 32 bits of the register must be set (bit C16 must be set to 1 during that access to allow the update of the entire register content). To minimize switching noise on the interface, an update of the first eight bits (C[31:24]) with the remaining bits held low can be performed thereafter.

Figure 35 illustrates the different control register update options.

7.4.3 Daisy-Chain Mode (In Serial Mode Only)

The serial interface of the ADS8555 device supports a daisy-chain feature that allows cascading of multiple devices to minimize the board space requirements and simplify routing of the data and control lines. In this case, pins DB5/DCIN_A, DB4/DCIN_B, and DB3/DCIN_C are used as serial data inputs for channels A, B, and C, respectively. Figure 32 shows an example of a daisy-chain connection of three devices sharing a common CONVST line to allow simultaneous sampling of 18 analog channels along with the corresponding timing diagram. To activate the daisy-chain mode, the DC_{EN} pin must be pulled high. As a result of the time specifications t_{S1}, t_{H1}, and t_{D3}, the maximum SCLK frequency that may be used in daisy-chain mode is 27.78 MHz (assuming 50% duty cycle).

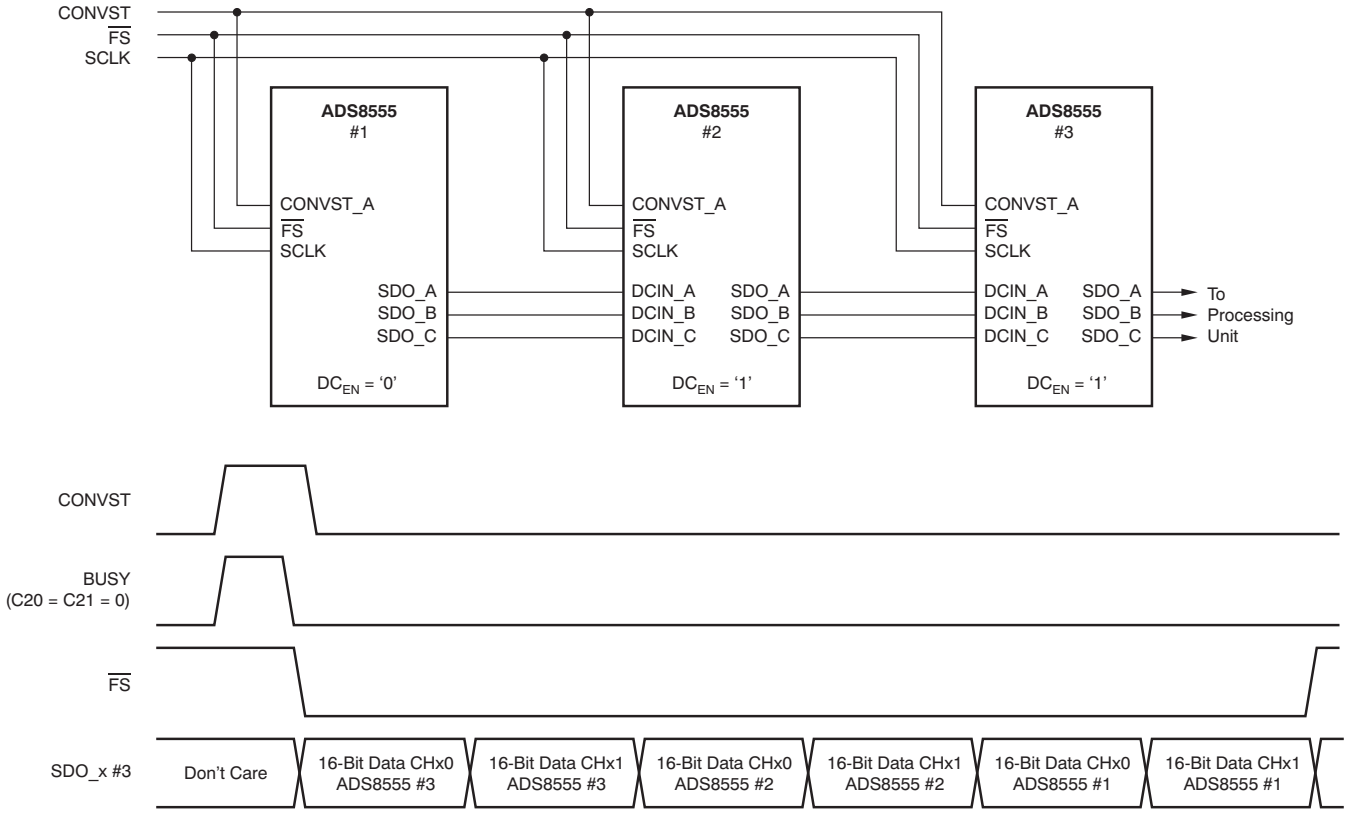
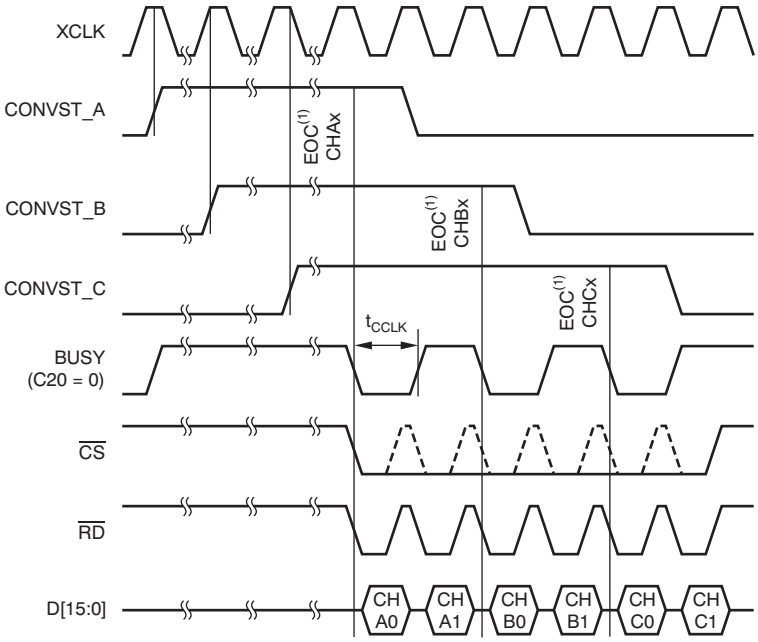


Figure 32. Example of Daisy-Chaining Three ADS8555 Devices

Device Functional Modes (continued)

7.4.4 Sequential Mode (In Software Mode With External Conversion Clock Only)

The three channel pairs of the ADS8555 device can be run in sequential mode, with the corresponding CONVST_x signals interleaved, when an external clock is used. To activate the device in sequential mode, CR bits C11 (CLKSEL) and C23 (SEQ) must be asserted. In this case, the BUSY output indicates a finished conversion by going low (when C20 = 0) or high (when C20 = 1) for only a single conversion clock cycle in case of ongoing conversions of any other channel pairs. Figure 33 shows the behavior of the BUSY output in this mode. Initiate each conversion start during the high phase of the external clock, as shown in Figure 33. The minimum time required between two CONVST_x pulses is the time required to read the conversion result of a channel (pair).



(1) EOC = end of conversion (internal signal).

Figure 33. Sequential Mode Timing

7.4.5 Reset and Power-Down Modes

The device supports two reset mechanisms: a power-on reset (POR) and a pin-controlled reset (RESET) that can be issued using pin 28. Both the POR and RESET act as a master reset that causes any ongoing conversion to be interrupted, the control register content to be set to the default value, and all channels to be switched into sample mode.

When the device is powered up, the POR sets the device in default mode when AVDD reaches 1.5 V. When the device is powered down, the POR circuit requires AVDD to remain below 125 mV at least 350 ms to ensure proper discharging of internal capacitors and to ensure correct behavior of the device when powered up again. If the AVDD drops below 400 mV but remains above 125 mV (see the *undefined zone* in Figure 34), the internal POR capacitor does not discharge fully and the device requires a pin-controlled reset to perform correctly after the recovery of AVDD.

Device Functional Modes (continued)

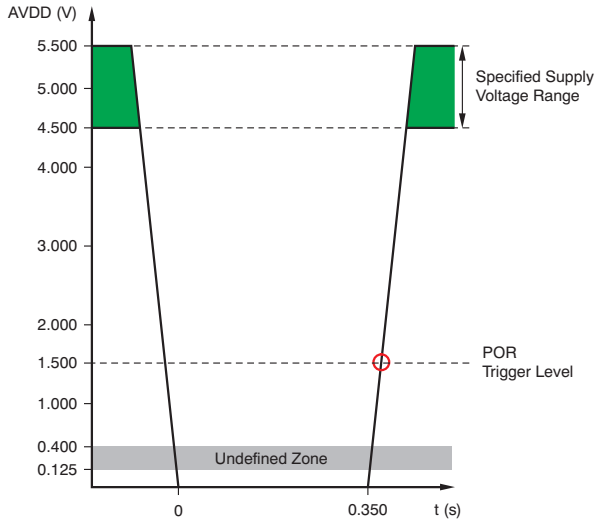


Figure 34. POR: Relevant Voltage Levels

The entire device, except the digital interface, can be powered down by pulling the $\overline{\text{STBY}}$ pin low (pin 24). Because the digital interface section remains active, data can be retrieved when in stand-by mode. To power the device on again, the $\overline{\text{STBY}}$ pin must be brought high. The device is ready to start a new conversion after the 10 ms required to activate and settle the internal circuitry. This user-controlled approach can be used in applications that require lower data throughput rates and lowest power dissipation. The content of CR is not changed during standby mode. A pin-controlled reset is not required after returning to normal operation.

Although the standby mode affects the entire device, each device channel pair can also be individually switched off by setting control register bits C[15:13] (PD_x). When reactivated, the relevant channel pair requires 10 ms to fully settle before starting a new conversion. The internal reference remains active, except all channels are powered down at the same time.

The auto-NAP power-down mode is enabled by asserting the A-NAP bit (C22) in the control register. If the auto-NAP mode is enabled, the ADS8555 device automatically reduces the current requirement to 6 mA after finishing a conversion; thus, the end of conversion actually activates the power-down mode. Triggering a new conversion by applying a positive CONVST_x edge puts the device back into normal operation, starts the acquisition of the analog input, and automatically starts a new conversion six conversion clock cycles later. Therefore, a complete conversion cycle takes 24.5 conversion clock cycles; thus, the maximum throughput rate in auto-NAP power-down mode is reduced to a maximum of 380 kSPS in serial mode, and 500 kSPS in parallel mode. The internal reference remains active during the auto-NAP mode. Table 4 compares the analog current requirements of the device in the different modes.

Table 4. Maximum Analog Current (I_{AVDD}) Demand of the ADS8555

OPERATIONAL MODE	ANALOG CURRENT (I_{AVDD})	ENABLED BY	ACTIVATED BY	NORMAL OPERATION TO POWER-DOWN DELAY	RESUMED BY	POWER UP TO NORMAL OPERATION DELAY	POWER UP TO NEXT CONVERSION START TIME	DISABLED BY
Normal operation	12mA/channel pair (maximum data rate)	Power on	CONVST_x	—	—	—	—	Power off
Auto-NAP	6mA	A-NAP = 1 (CR bit)	Each end of conversion	At falling edge of BUSY	CONVST_x	Immediate	6 × t_{CCLK}	A-NAP = 0 (CR bit)
Power down of channel pair x	16µA (channel pair x)	HW/SW = 1	PD_x = 1 (CR bit)	Immediate	PD_x = 0 (CR bit)	Immediate after completing register update	10ms	HW/SW = 0
Stand-by	50µA	Power on	$\overline{\text{STBY}}$ = 0	Immediate	$\overline{\text{STBY}}$ = 1	Immediate	10ms	Power off

7.5 Register Maps

7.5.1 Control Register (CR); Default Value = 0x000003FF

The control register settings can only be changed in software mode and are not affected when switching to hardware mode thereafter. The register values are independent from input pin settings. Changes are active with the rising edge of $\overline{WR}$ in parallel interface mode or with the 32nd falling SCLK edge of the access in which the register content has been updated in serial mode. Optionally, the register can also be partially updated by writing only the upper eight bits (C[31:24]). The CR content is defined in Table 5.

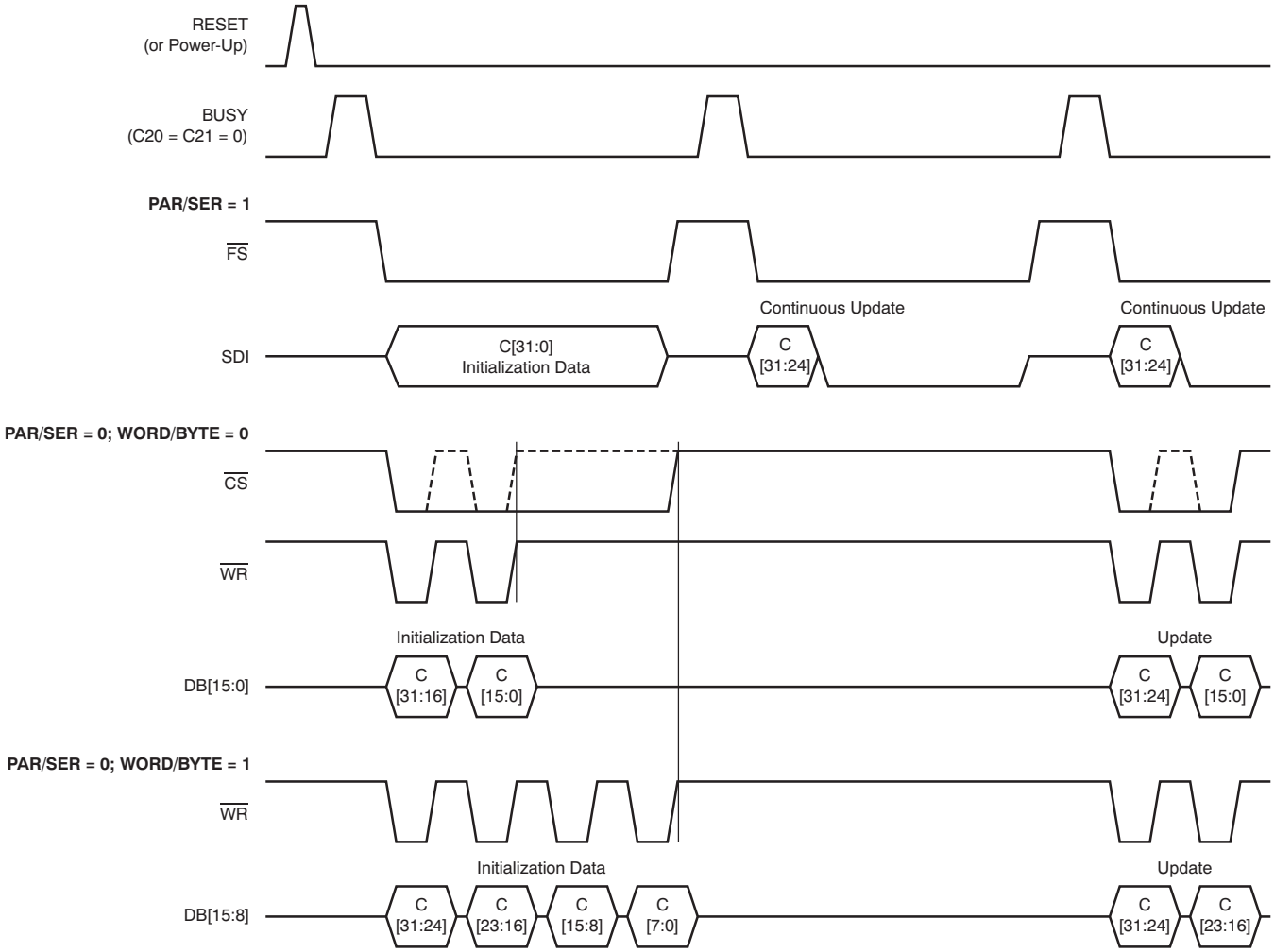


Figure 35. Control Register Update Options

Register Maps (continued)

Table 5. Control Register (CR) Map

BIT	NAME	DESCRIPTION	ACTIVE IN HARDWARE MODE
C31	CH_C	0 = Channel pair C disabled for next conversion (default) 1 = Channel pair C enabled	No
C30	CH_B	0 = Channel pair B disabled for next conversion (default) 1 = Channel pair B enabled	No
C29	CH_A	0 = Channel pair A disabled for next conversion (default) 1 = Channel pair A enabled	No
C28	RANGE_C	0 = Input voltage range selection for channel pair C: 4 V_{REF} (default) 1 = Input voltage range selection for channel pair C: 2 V_{REF}	No
C27	RANGE_B	0 = Input voltage range selection for channel pair B: 4 V_{REF} (default) 1 = Input voltage range selection for channel pair B: 2 V_{REF}	No
C26	RANGE_A	0 = Input voltage range selection for channel pair A: 4 V_{REF} (default) 1 = Input voltage range selection for channel pair A: 2 V_{REF}	No
C25	REF_{EN}	0 = Internal reference source disabled (default) 1 = Internal reference source enabled	No
C24	REFBUF	0 = Internal reference buffers enabled (default) 1 = Internal reference buffers disabled	No
C23	SEQ	0 = Sequential convert start mode disabled (default) 1 = Sequential convert start mode enabled (bit 11 must be 1 in this case)	No
C22	A-NAP	0 = Normal operation (default) 1 = Auto-NAP feature enabled	Yes
C21	BUSY/INT	0 = BUSY/INT pin in normal mode (BUSY) (default) 1 = BUSY/INT pin in interrupt mode (INT)	Yes
C20	BUSY L/H	0 = BUSY/INT active high (default) 1 = BUSY/INT active low	Yes
C19	Don't use	This bit is always set to 0	—
C18	VREF	0 = Internal reference voltage: 2.5 V (default) 1 = Internal reference voltage: 3 V	Yes
C17	READ_EN	0 = Normal operation (conversion results available on SDO_x) (default) 1 = Control register contents output on SDO_x with next access	Yes
C16	C23:0_EN	0 = Control register bits C[31:24] update only (serial mode only) (default) 1 = Entire control register update enabled (serial mode only)	Yes
C15	PD_C	0 = Normal operation (default) 1 = Power down for channel pair *C* enabled (bit 31 must be 0 in this case)	Yes
C14	PD_B	0 = Normal operation (default) 1 = Power down for channel pair *B* enabled (bit 30 must be 0 in this case)	Yes
C13	PD_A	0 = Normal operation (default) 1 = Power down for channel pair *A* enabled (bit 29 must be 0 in this case)	Yes
C12	Don't use	This bit is always 0	—
C11	CLKSEL	0 = Normal operation with internal conversion clock (mandatory in hardware mode) (default) 1 = External conversion clock (applied through pin 27) used	No
C10	CLKOUT_EN	0 = Normal operation (default) 1 = Internal conversion clock available at pin 27	No
C9	REFDAC[9]	Bit 9 (MSB) of reference DAC value; default = 1	Yes
C8	REFDAC[8]	Bit 8 of reference DAC value; default = 1	Yes
C7	REFDAC[7]	Bit 7 of reference DAC value; default = 1	Yes
C6	REFDAC[6]	Bit 6 of reference DAC value; default = 1	Yes
C5	REFDAC[5]	Bit 5 of reference DAC value; default = 1	Yes
C4	REFDAC[4]	Bit 4 of reference DAC value; default = 1	Yes
C3	REFDAC[3]	Bit 3 of reference DAC value; default = 1	Yes
C2	REFDAC[2]	Bit 2 of reference DAC value; default = 1	Yes
C1	REFDAC[1]	Bit 1 of reference DAC value; default = 1	Yes
C0	REFDAC[0]	Bit 0 (LSB) of reference DAC value; default = 1	Yes

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADS8555 device enables high-precision measurement of up to six analog signals simultaneously. The following sections summarize some of the typical use cases for the ADS8555 device and the main steps and components used around the analog-to-digital converter.

8.2 Typical Application

8.2.1 Measurement of Electrical Variables in a 3-Phase Power System

The accurate measurement of electrical variables in a power grid is extremely critical because it helps determine the operating status and running quality of the grid. Such accurate measurements also help diagnose problems with the power network thereby enabling prompt solutions and minimizing down time. The key electrical variables measured in 3-phase power systems are the three line voltages and the three line currents; see Figure 36. These variables enable metrology and power automation systems to determine the amplitude, frequency and phase information to perform harmonic analysis, power factor calculation and power quality assessment among others.

Typical Application (continued)

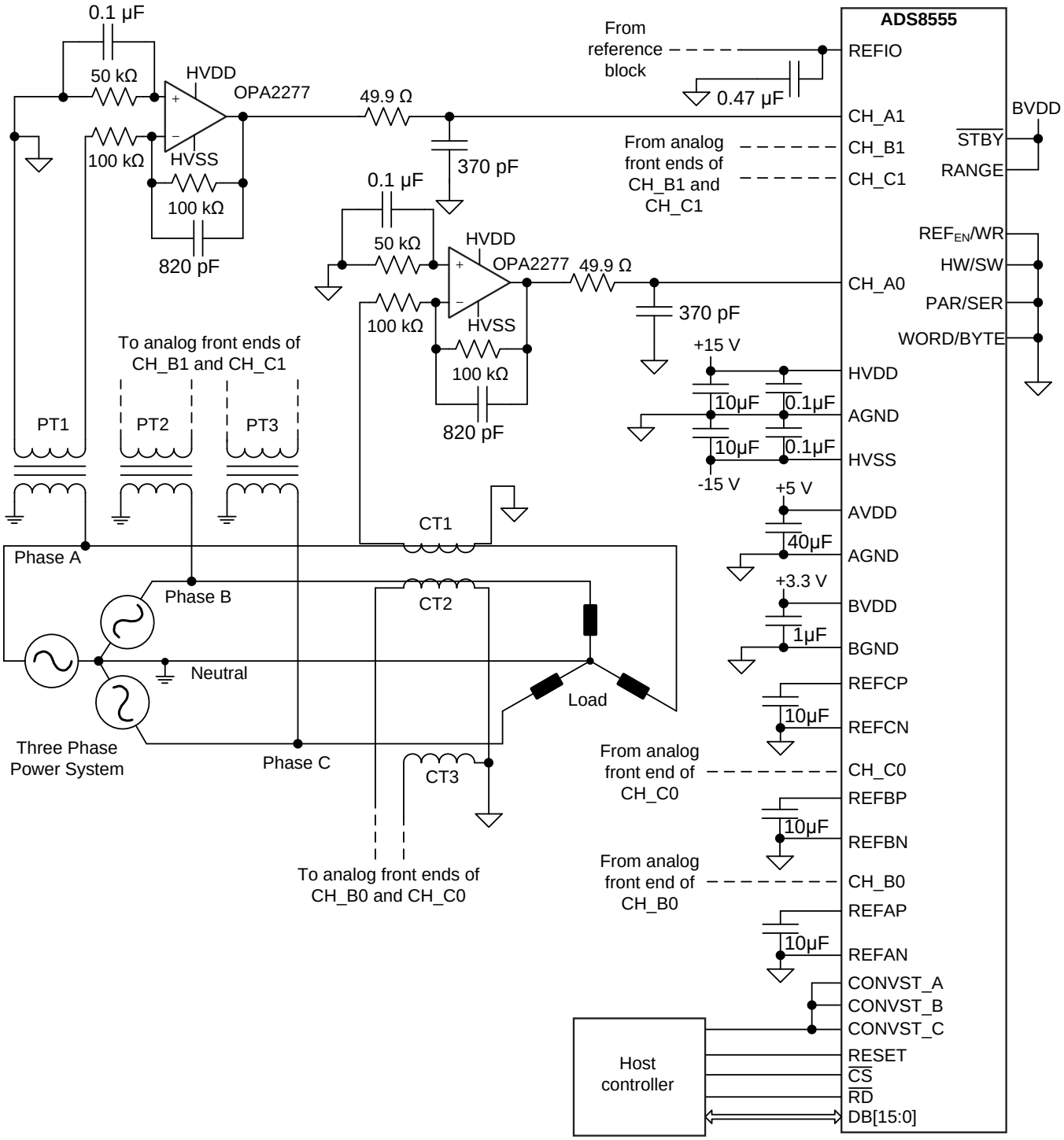


Figure 36. Simultaneous Acquisition of Voltage and Current in a 3-Phase Power System

Typical Application (continued)

8.2.1.1 Design Requirements

To begin the design process, a few parameters must be decided upon. The designer must know the following:

- Output range of the potential transformers (elements labeled PT1, PT2, and PT3 in Figure 36)
- Output range of the current transformers (elements labeled CT1, CT2, and CT3 in Figure 36)
- Input impedance required from the analog front end for each channel
- Fundamental frequency of the power system
- Number of harmonics that must be acquired
- Type of signal conditioning required from the analog front end for each channel

8.2.1.2 Detailed Design Procedure

Figure 37 shows the topology chosen to meet the design requirements. A feedback capacitor C_F is included to provide a low-pass filter characteristic and attenuate signals outside the band of interest.

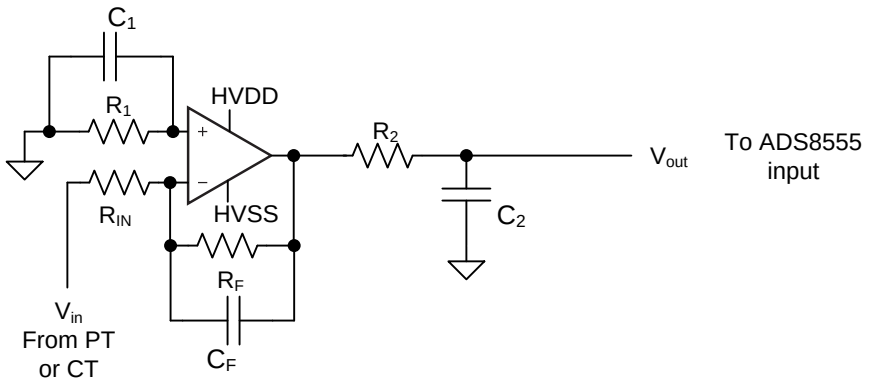


Figure 37. Op Amp in an Inverting Configuration

The potential transformers (PTs) and current transformers (CTs) used in the system depicted in Figure 36 provide the six input variables required. These transformers have a ±10-V output range. Although the PTs and CTs provide isolation from the power system, the value of R_{IN} is selected as 100 kΩ to provide an additional, high-impedance safety element to the input of the ADC. Moreover, selecting a low-frequency gain of –1 V/V (as shown in Equation 5) provides a ±10-V output that can be fed into the ADS8555 device; therefore, the value of R_F is selected as 100 kΩ.

$$V_{out}\big|_{Low\ f} = -\frac{R_F}{R_{IN}}V_{in} = -\frac{100\ k\Omega}{100\ k\Omega}V_{in} = -V_{in} \tag{5}$$

The primary goal of the acquisition system depicted in Figure 36 is to measure up to 20 harmonics in a 60-Hz power network. Thus, the analog front-end must have sufficient bandwidth to detect signals up to 1260 Hz, as shown in Equation 6.

$$f_{MAX} = (20+1)60\,Hz = 1260\,Hz \tag{6}$$

Based on the bandwidth found in Equation 6 the ADS8555 device is set to simultaneously sample all six channels at 15.36 kSPS, which provides enough samples to clearly resolve even the highest harmonic required.

The passband of the configuration shown in Figure 37 is determined by the –3-dB frequency according to Equation 7. The value of C_F is selected as 820 pF, which is a standard capacitance value available in 0603 size (surface-mount component) and such values, combined with that of R_F, result in sufficient bandwidth to accommodate the required 20 harmonics (at 60 Hz).

$$f_{-3dB} = \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi(100\ k\Omega)(820\ pF)} = 1940\ Hz \tag{7}$$

The value of R_1 is selected as the parallel combination of R_{IN} and R_F to prevent the input bias current of the operational amplifier from generating an offset error.

Typical Application (continued)

The value of component C_1 is chosen as 0.1 µF to provide a low-impedance path for noise signals that can be picked up by R_1; the 0.1-µF capacitance value improves the EMI robustness and noise performance of the system.

The OPA2277 device is chosen for its low input offset voltage, low drift, bipolar swing, sufficient gain-bandwidth product and low quiescent current. For additional information on the procedure to select SAR ADC input drivers, see reference guide TIDU181.

The charge injection damping circuit is composed of R_2 (49.9 Ω) and C_2 (370 pF); these components reject high-frequency noise and meet the settling requirements of the ADS8555 device input.

Figure 38 shows the reference block used in this design.

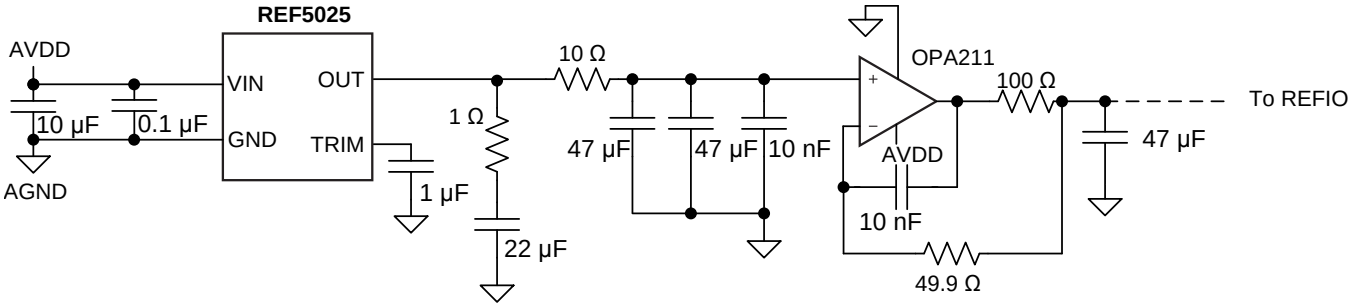


Figure 38. Op Amp in an Inverting Configuration

For more information on the design of charge injection damping circuits and reference driving circuits for SAR ADCs, consult reference guide TIDU014.

8.2.1.3 Application Curve

Figure 39 shows the frequency spectrum of the data acquired by the ADS8555 device for a sinusoidal, 20-V_{PP} input at 60 Hz.

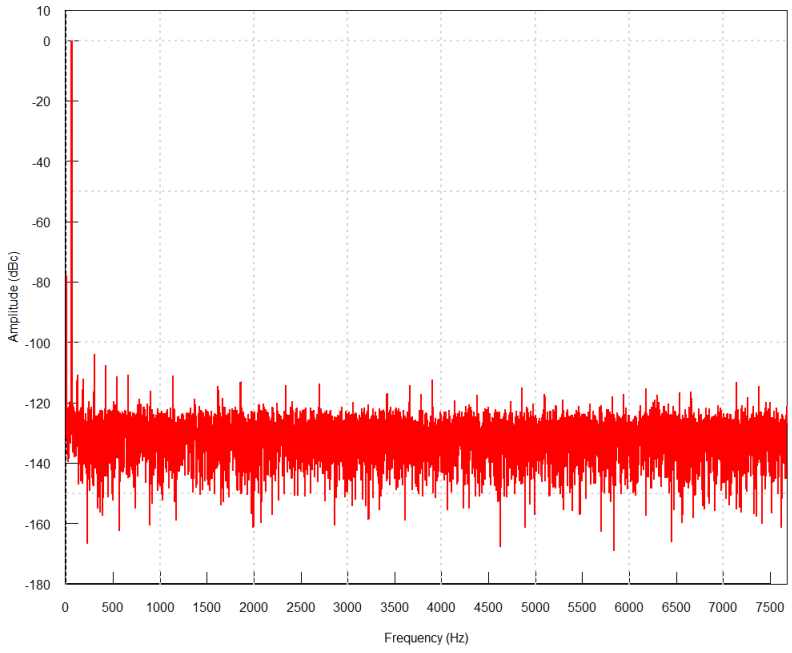


Figure 39. Frequency Spectrum for a Sinusoidal 20-V_{PP} Signal at 60 Hz

The ac performance parameters are:

Typical Application (continued)

- SNR: 91.9 dB
- THD: –99.68 dB
- SNDR: 91.23 dB
- SFDR: 103.65 dB

9 Power Supply Recommendations

The ADS8555 device requires four separate supplies: the analog supply for the ADC (AVDD), the buffer I/O supply for the digital interface (BVDD), and the two high-voltage supplies driving the analog input circuitry (HVDD and HVSS). Generally, there are no specific requirements with regard to the power sequencing of the device. However, when HVDD is supplied before AVDD, the internal ESD structure conducts, increasing IHVDD beyond the specified value.

The AVDD supply provides power to the internal circuitry of the ADC. AVDD can be set in the range of 4.5 V to 5.5 V. Because the supply current of the device is typically 30 mA, a passive filter cannot be used between the digital board supply of the application and the AVDD pin. TI recommends a linear regulator to generate the analog supply voltage. Decouple each AVDD pin to AGND with a 100-nF capacitor. In addition, place a single 10-µF capacitor close to the device but without compromising the placement of the smaller capacitor. Optionally, each supply pin can be decoupled using a 1-µF ceramic capacitor without the requirement for a 10-µF capacitor.

The BVDD supply is only used to drive the digital I/O buffers and can be set in the range of 2.7 V to 5.5 V. This range allows the device to interface with most state-of-the-art processors and controllers. To limit the noise energy from the external digital circuitry to the device, filter BVDD. A 10-Ω resistor can be placed between the external digital circuitry and the device because the current drawn is typically below 2 mA (depending on the external loads). Place a bypass ceramic capacitor of 1 µF (or alternatively, a pair of 100-nF and 10-µF capacitors) between the BVDD pin and pin 8.

The high-voltage supplies (HVSS and HVDD) are connected to the analog inputs. Noise and glitches on these supplies directly couple into the input signals. Place a 100-nF ceramic decoupling capacitor, located as close to the device as possible, between each of pins 30, 31, and AGND. An additional 10-µF capacitor is used that must be placed close to the device but without compromising the placement of the smaller capacitor.

10 Layout

10.1 Layout Guidelines

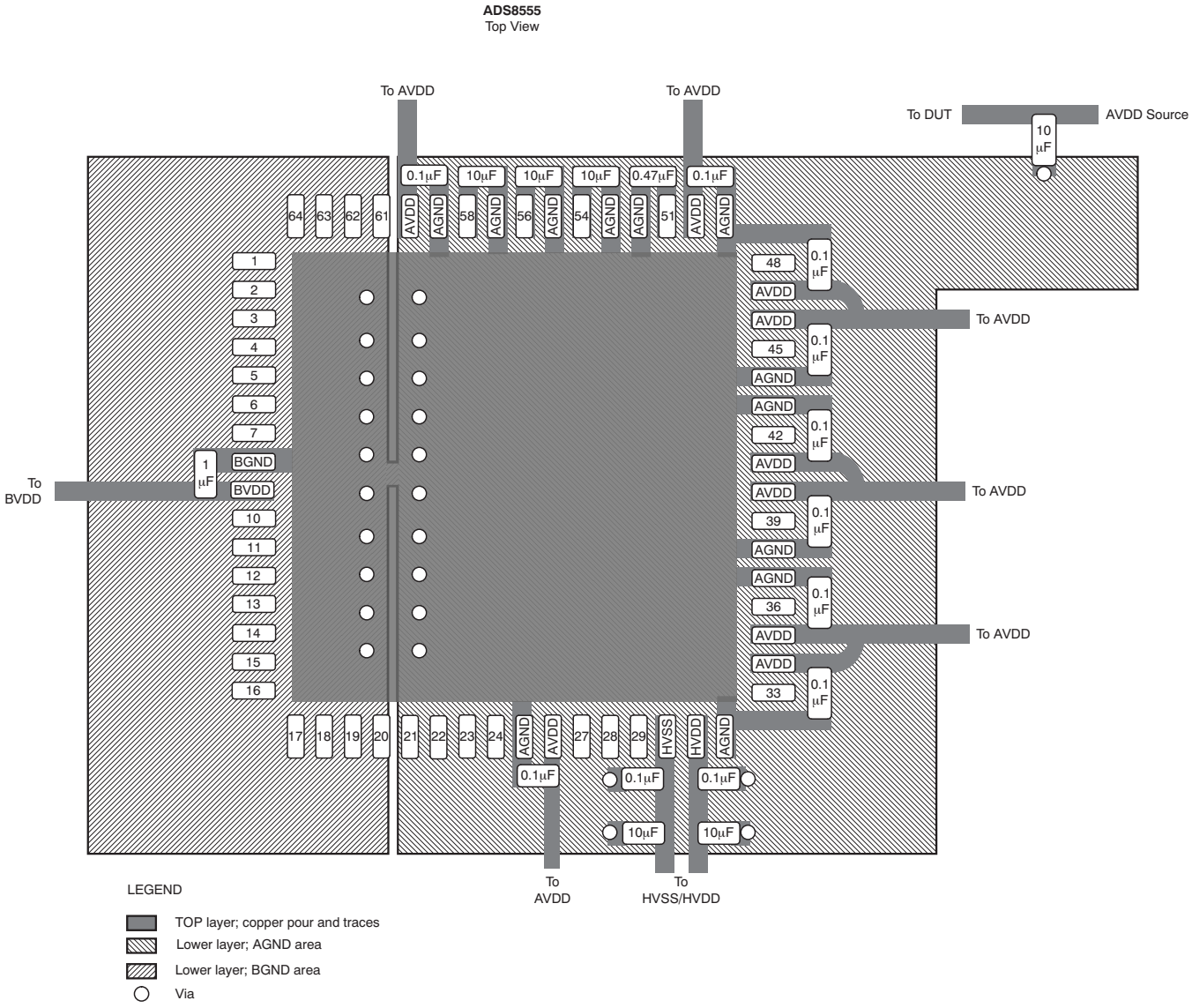
All GND pins must be connected to a clean ground reference. This connection must be kept as short as possible to minimize the inductance of this path. TI recommends using vias connecting the pads directly to the ground plane. In designs without ground planes, keep the ground trace as wide as possible. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density on the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed-circuit-board (PCB) or a dedicated analog ground area can be used. In case of a separated analog ground area, ensure a low-impedance connection between the analog and digital ground of the ADC by placing a bridge underneath (or next) to the ADC. Otherwise, even short undershoots on the digital interface lower than –300 mV lead to the conduction of ESD diodes causing current flow through the substrate and degrading the analog performance.

During PCB layout, take care to avoid any return currents crossing sensitive analog areas or signals.

Figure 40 illustrates a layout recommendation for the ADS8555 device along with the proper decoupling and reference capacitor placement and connections.

10.2 Layout Example



(1) All 0.1-µF, 0.47-µF, and 1-µF capacitors must be placed as close to the ADS8555 device as possible.

(2) All 10-µF capacitors must be close to the device but without compromising the placement of the smaller capacitors.

Figure 40. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- OPA2277 Data Sheet, SBOS079
- REF5025 Data Sheet, SBOS410
- *Power-Optimized 16-Bit 1-MSPS Data Acquisition Block Design Guide*, TIDU014
- *16-Bit 400-KSPS 4-Channel Multiplexed Data Acquisition System Design Guide*, TIDU181

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8555SPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 8555	Samples
ADS8555SPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 8555	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

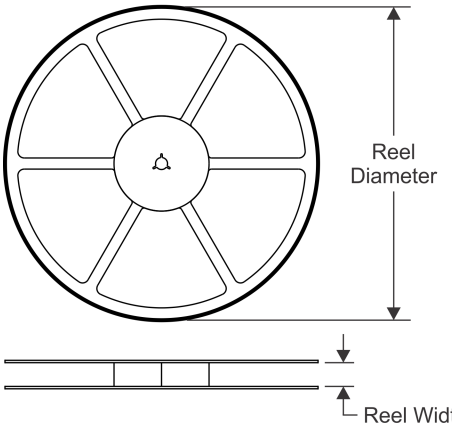
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

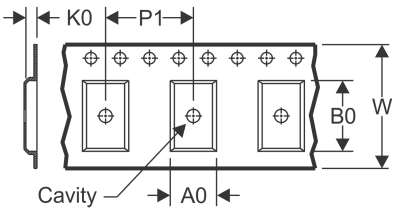
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

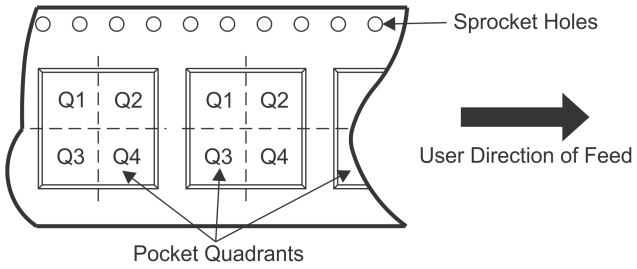


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

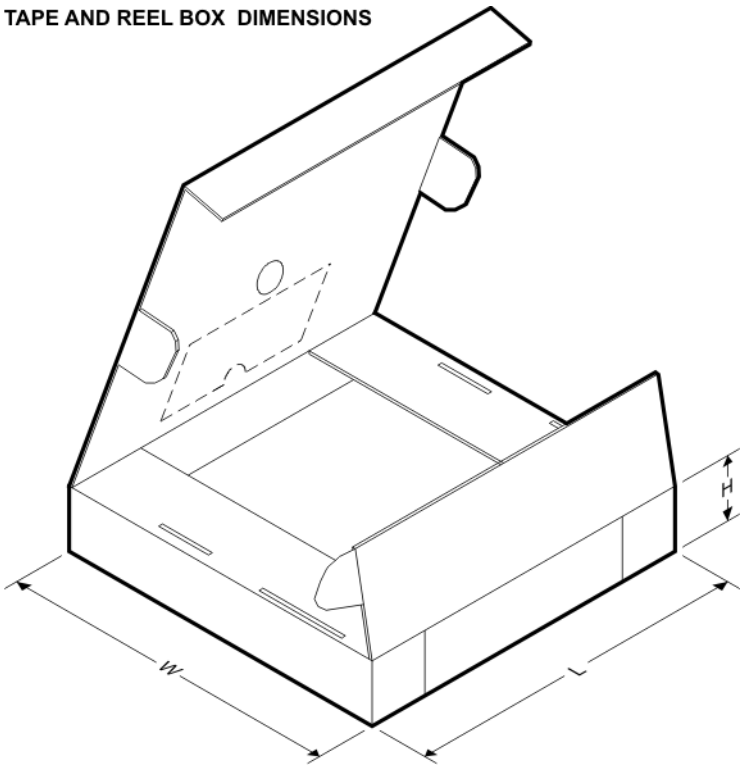
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8555SPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

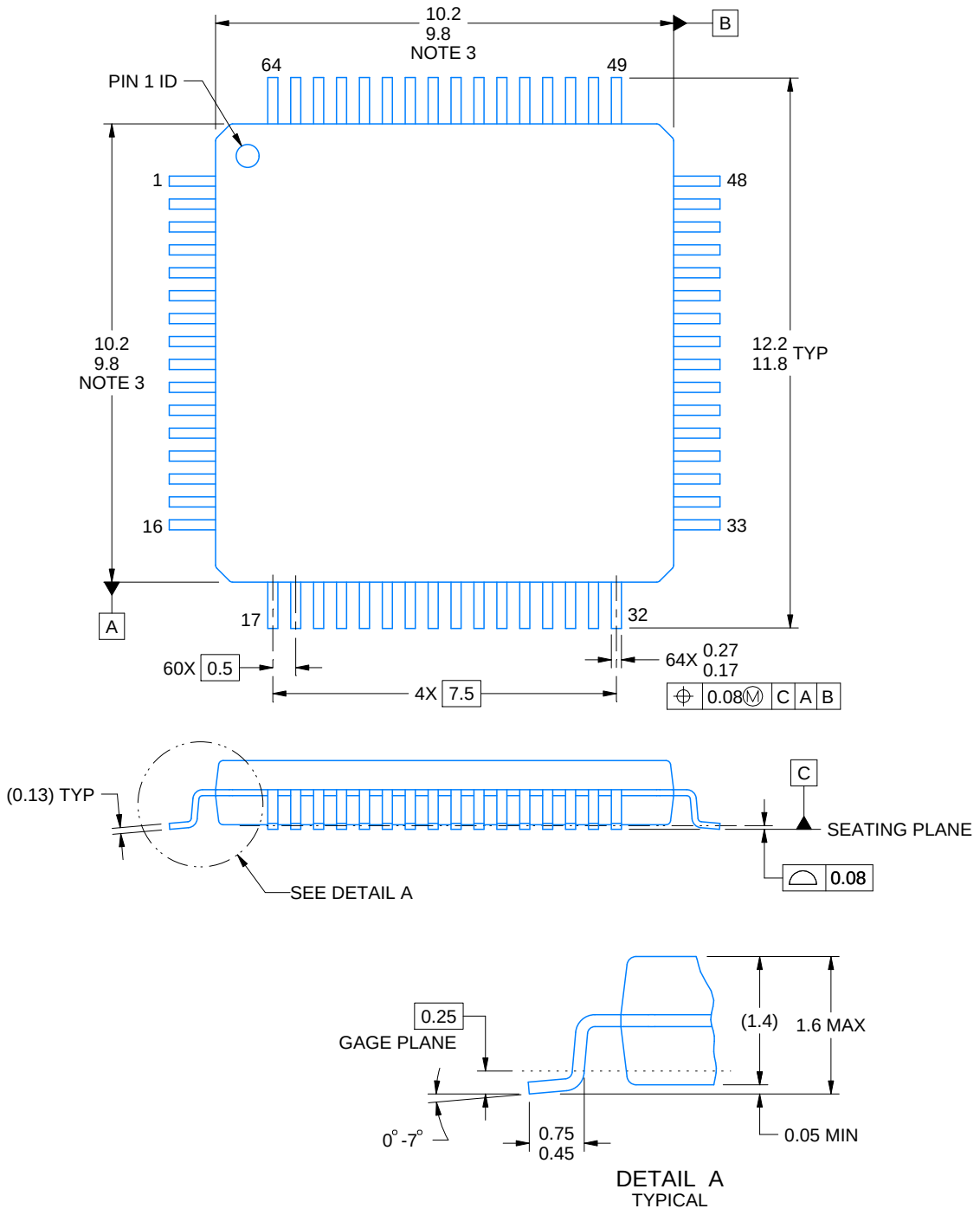
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8555SPMR	LQFP	PM	64	1000	350.0	350.0	43.0

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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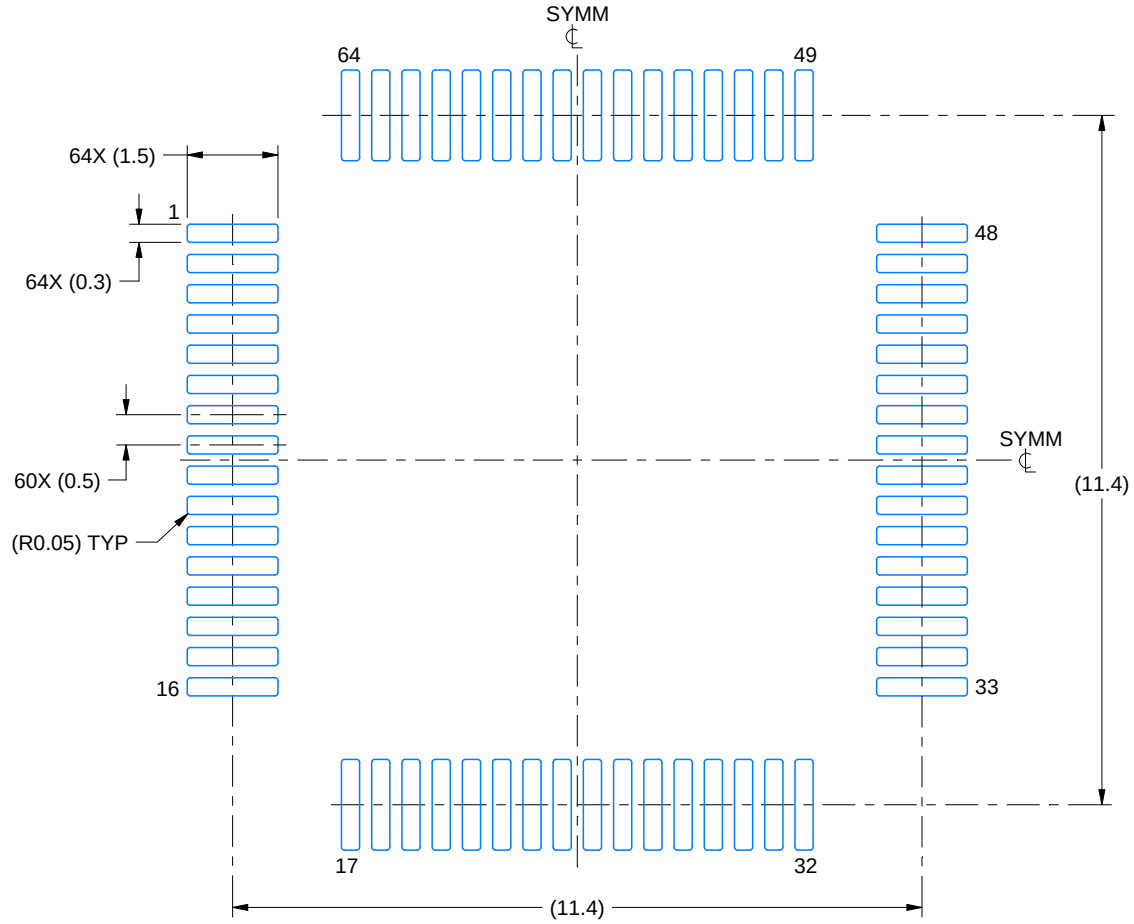
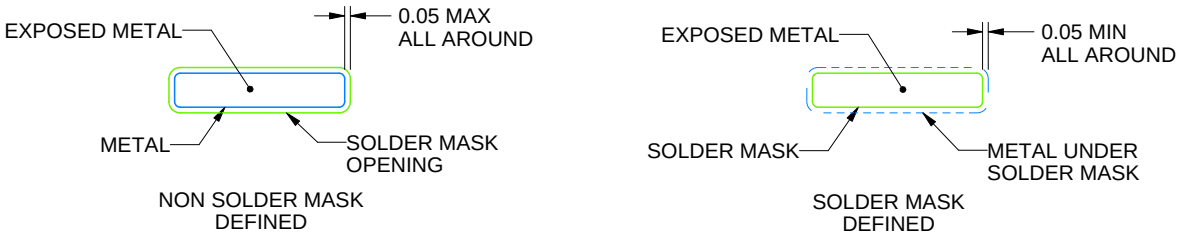
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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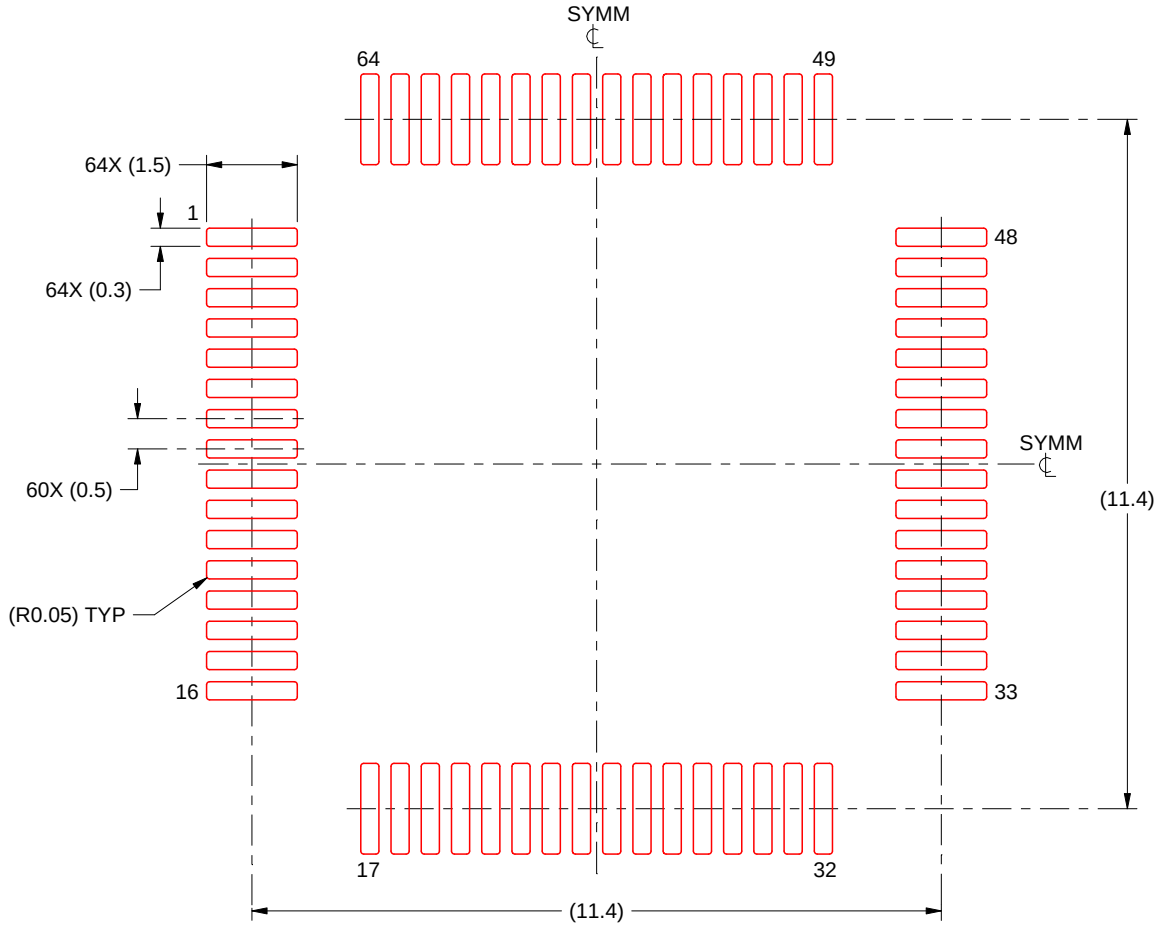
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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