



ADS7x51 12 位, 2MSPS 和 14 位, 1.5MSPS, 双路, 差分输入, 同步采样模数转换器, 具有内部基准

1 特性

- 12 和 14 位引脚兼容系列
- 两个通道同时采样
- 支持全差分模拟输入
- 独立内部基准 (每个 ADC 一个)
- 高速:
 - 使用 ADS7251 (12 位) 时高达 2MSPS
 - 使用 ADS7851 (14 位) 时高达 1.5MSPS
- 出色的性能:
 - ADS7251:
 - 信噪比 (SNR): 73dB
 - 积分非线性 (INL): ± 1 最低有效位 (LSB)
 - ADS7851:
 - 信噪比 (SNR): 83.5dB
 - 积分非线性 (INL): ± 2 LSB
- 在 -40°C 至 $+125^{\circ}\text{C}$ 的扩展工业用温度范围内完全额定运行
- 小型封装: 超薄四方扁平无引线 (WQFN)-16 (3mm x 3mm)

2 应用范围

- 电机控制: 与 SinCos 编码器的直接对接
- 光网络互连: 掺铒光纤放大器 (EDFA) 增益控制环路
- 保护中继器
- 电源质量测量
- 三相电源控制
- 可编程逻辑控制器
- 工业自动化

3 说明

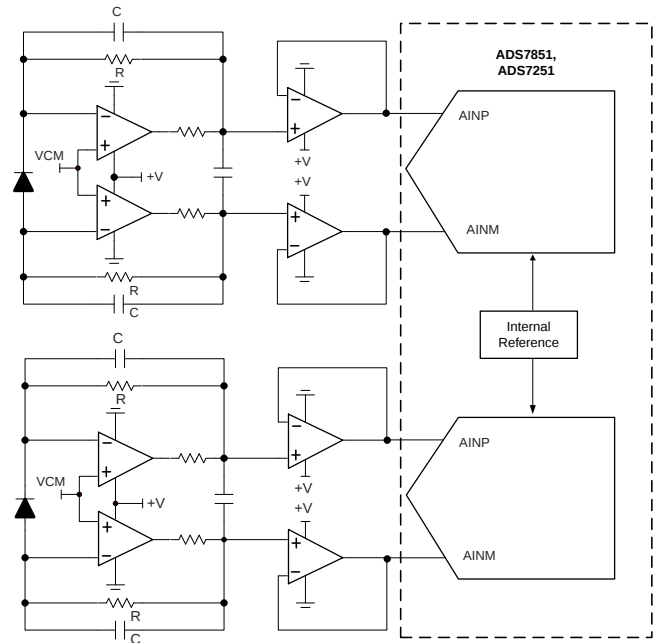
ADS7251 和 ADS7851 属于引脚兼容、双路、高速、同步采样模数转换器 (ADC) 产品系列, 此系列产品支持全差分模拟输入, 并且特有 2 个单独的内部电压基准。ADS7251 提供 12 位分辨率以及高达 2MSPS 的采样速度。ADS7851 提供 14 位分辨率以及高达 1.5MSPS 的采样速度。

此器件支持宽数字电源电压范围, 从而通过一个简单串口轻松实现与多种数字主机控制器的通信。两个器件都在扩展工业用温度范围 (-40°C 至 $+125^{\circ}\text{C}$) 内完全额定运行, 并且采用引脚兼容、节省空间的 WQFN-16 (3mm x 3mm) 封装。

器件信息

订货编号	封装	封装尺寸
ADS7251RTE	WQFN (16)	3mm x 3mm
ADS7851RTE	WQFN (16)	3mm x 3mm

典型应用图



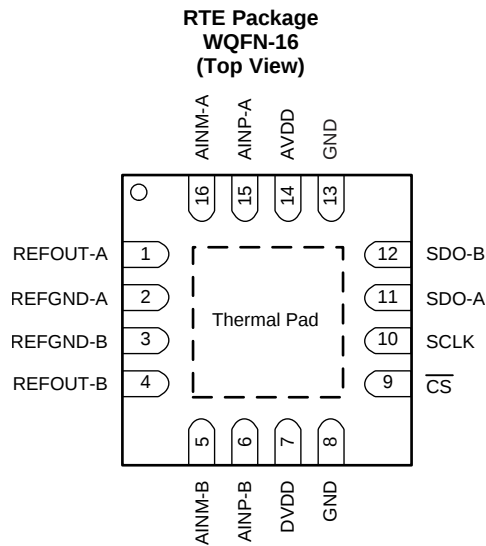
目录

1	特性	1	7.1	Overview	17
2	应用范围	1	7.2	Functional Block Diagram	17
3	说明	1	7.3	Feature Description	18
4	修订历史记录	2	7.4	Device Functional Modes	21
5	Terminal Configuration and Functions	3	8	Application and Implementation	23
6	Specifications	4	8.1	Application Information	23
6.1	Absolute Maximum Ratings	4	8.2	Typical Application	23
6.2	Handling Ratings	4	9	Power Supply Recommendations	27
6.3	Recommended Operating Conditions	4	10	Layout	28
6.4	Thermal Information	4	10.1	Layout Guidelines	28
6.5	Electrical Characteristics: ADS7251	5	10.2	Layout Example	28
6.6	Electrical Characteristics: ADS7851	6	11	器件和文档支持	29
6.7	Electrical Characteristics: Common	7	11.1	文档支持	29
6.8	ADS7251 Timing Characteristics	8	11.2	相关链接	29
6.9	ADS7851 Timing Characteristics	9	11.3	Trademarks	29
6.10	Typical Characteristics: ADS7251	10	11.4	Electrostatic Discharge Caution	29
6.11	Typical Characteristics: ADS7851	13	11.5	Glossary	29
6.12	Typical Characteristics: Common	16	12	机械封装和可订购信息	29
7	Detailed Description	17			

4 修订历史记录

Changes from Original (January 2014) to Revision A	Page
• 已将格式更改为最新的数据表标准；已添加 电路板布局 部分，已移动现有部分	1
• Deleted Ordering Information table	3
• Changed Supply Current, $I_{D VDD}$ parameter typical specification in Electrical Characteristics: ADS7251 table	5
• Changed Supply Current, $I_{D VDD}$ parameter typical specification in Electrical Characteristics: ADS7851 table	6
• Changed <i>Input Voltage</i> column in Table 1	20

5 Terminal Configuration and Functions



Terminal Descriptions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AINM-A	16	Analog input	Negative analog input, channel A
AINP-A	15	Analog input	Positive analog input, channel A
AINM-B	5	Analog input	Negative analog input, channel B
AINP-B	6	Analog input	Positive analog input, channel B
AVDD	14	Supply	ADC supply voltage
$\overline{CS}$	9	Digital input	Chip-select signal; active low
DVDD	7	Supply	Digital I/O supply
GND	8, 13	Supply	Digital ground
REFGND-A	2	Supply	Reference ground potential, channel A
REFGND-B	3	Supply	Reference ground potential, channel B
REFOUT-A	1	Analog output	Reference voltage output, REF_A
REFOUT-B	4	Analog output	Reference voltage output, REF_B
SCLK	10	Digital input	Serial communication clock
SDO-A	11	Digital output	Data output for serial communication, channel A
SDO-B	12	Digital output	Data output for serial communication, channel B
Thermal pad		Supply	Exposed thermal pad. TI recommends connecting this pin to the printed circuit board (PCB) ground.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	AVDD to GND	−0.3	+7	V
	DVDD to GND	−0.3	+7	V
Analog input voltage	AINP_x to REFGND_x	REFGND_x − 0.3	AVDD + 0.3	V
	AINM_x to REFGND_x	REFGND_x − 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK to GND	GND − 0.3	DVDD + 0.3	V
Ground voltage difference	REFGND_x − GND		0.3	V
Input current	Any pin except supply pins		±10	mA
Maximum virtual junction temperature, T _J			+150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	−65	+150	°C
V _{ESD} ⁽¹⁾ , all pins	Human body model (HBM) ESD stress voltage ⁽²⁾ , JEDEC standard 22, test method A114-C.01		±2000	V
	Charged device model (CDM) ESD stress voltage ⁽³⁾ , JEDEC standard 22, test method C101		±500	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that ±2000-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that ±500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage		5		V
DVDD	Digital supply voltage		3.3		V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ADS7251, ADS7851	UNIT
		RTE (WQFN)	
		16 TERMINALS	
R _{θJA}	Junction-to-ambient thermal resistance	33.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	29.5	
R _{θJB}	Junction-to-board thermal resistance	7.3	
Ψ _{JT}	Junction-to-top characterization parameter	0.2	
Ψ _{JB}	Junction-to-board characterization parameter	7.4	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	0.9	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics: ADS7251

All minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $\text{AVDD} = 5\text{ V}$, $V_{\text{REF}_A} = V_{\text{REF}_B} = 2.5\text{ V}$, and $f_{\text{DATA}} = 2\text{ MSPS}$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$, $\text{AVDD} = 5\text{ V}$, and $\text{DVDD} = 3.3\text{ V}$.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	
RESOLUTION								
Resolution				12			Bits	
SAMPLING DYNAMICS								
t _{CONV}	Conversion time			t _{SU_CSCK} + 12 t _{CLK}			ns	
t _{ACQ}	Acquisition time			75			ns	
f _{DATA}	Data rate			2			MSPS	
f _{CLK}	Clock frequency			32			MHz	
DC ACCURACY								
NMC	No missing codes			12			Bits	
DNL	Differential nonlinearity			−0.99	±0.3	1	LSB	
INL	Integral nonlinearity			−1	±0.5	1	LSB	
V _{OS}	Input offset error			−1	±0.2	1	mV	
	V _{OS} match		ADC_A to ADC_B	−1	±0.2	1	mV	
dV _{OS} /dT	Input offset thermal drift			4			μV/°C	
G _E	Gain error		Referenced to the voltage at REFOUT_x	−0.1%	±0.05%	0.1%		
	G _{ERR} match		ADC_A to ADC_B	−0.1%	±0.05%	0.1%		
G _E /dT	Gain error thermal drift		Referenced to the voltage at REFOUT_x	1			ppm/°C	
CMRR	Common-mode rejection ratio		Both ADCs, dc to 20 kHz	72			dB	
AC ACCURACY								
SINAD	Signal-to-noise + distortion		For 20-kHz input frequency, at −0.5 dBFS	72.7	72.9		dB	
SNR	Signal-to-noise ratio			72.8	73		dB	
THD	Total harmonic distortion				−90		dB	
SFDR	Spurious-free dynamic range				90		dB	
	Isolation between ADC_A and ADC_B		f _{IN} = 15 kHz, f _{NOISE} = 25 kHz	−105			dB	
SUPPLY CURRENT								
I _{AVDD-DYNAMIC}	Supply current	Analog, during conversion	Throughput = 2 MSPS, AVDD = 5 V	11			12	mA
I _{AVDD-STATIC}		Analog, static		5.5				mA
I _{DVDD}		Digital, for code 800		0.15				mA
POWER DISSIPATION								
P _{D-ACTIVE}	Power dissipation	During conversion	Throughput = 2 MSPS, AVDD = 5 V	55			60	mW
P _{D-STATIC}		Static mode		27.5				mW

6.6 Electrical Characteristics: ADS7851

All minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $AVDD = 5\text{ V}$, $V_{REF_A} = V_{REF_B} = 2.5\text{ V}$, and $f_{DATA} = 1.5\text{ MSPS}$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION							
Resolution				14			Bits
SAMPLING DYNAMICS							
t _{CONV}	Conversion time			t _{SU_CSCK} + 14 t _{CLK}			ns
t _{ACQ}	Acquisition time			90			ns
f _{DATA}	Data rate			1500			kSPS
f _{CLK}	Clock frequency			27			MHz
DC ACCURACY							
NMC	No missing codes			13			Bits
DNL	Differential nonlinearity			−1	±0.75	2	LSB
INL	Integral nonlinearity			−2	±1	2	LSB
V _{OS}	Input offset error			−1	±0.2	1	mV
	V _{OS} match		ADC_A to ADC_B	−1	±0.2	1	mV
dV _{OS} /dT	Input offset thermal drift			1			μV/°C
G _E	Gain error		Referenced to the voltage at REFOUT_x	−0.1%	±0.05%	0.1%	
	G _{ERR} match		ADC_A to ADC_B	−0.1%	±0.05%	0.1%	
G _E /dT	Gain error thermal drift		Referenced to the voltage at REFOUT_x	1			ppm/°C
CMRR	Common-mode rejection ratio		Both ADCs, dc to 20 kHz	72			dB
AC ACCURACY							
SINAD	Signal-to-noise + distortion		For 20-kHz input frequency, at −0.5 dBFS	81.4	82.6		dB
SNR	Signal-to-noise ratio			82	83.5		dB
THD	Total harmonic distortion			−90			dB
SFDR	Spurious-free dynamic range			90			dB
Isolation between ADC_A and ADC_B			f _{IN} = 15 kHz, f _{NOISE} = 25 kHz	−120			dB
SUPPLY CURRENT							
I _{AVDD-DYNAMIC}	Supply current	Analog, during conversion	Throughput = 1.5 MSPS, AVDD = 5 V	10		12	mA
I _{AVDD-STATIC}		Analog, static		5.5			mA
I _{DVDD}		Digital, for code 2000		0.15			mA
POWER DISSIPATION							
P _{D-ACTIVE}	Power dissipation	During conversion	Throughput = 1.5 MSPS, AVDD = 5 V	50		60	mW
P _{D-STATIC}		Static mode		27.5			mW

6.7 Electrical Characteristics: Common

All minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $\text{AVDD} = 5\text{ V}$, $V_{\text{REF_A}} = V_{\text{REF_B}} = 2.5\text{ V}$, and $f_{\text{DATA}} = 2\text{ MSPS}$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$, $\text{AVDD} = 5\text{ V}$, and $\text{DVDD} = 3.3\text{ V}$.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
FSR	Full-scale input range (AINP_x – AINM_x)		For AVDD ≥ 5 V	–2 V _{REF}	2 V _{REF}		V
			For AVDD < 5 V	–AVDD	AVDD		V
V _{IN}	Absolute input voltage (AINP_x or AIM_x to REFGND_x)		For AVDD ≥ 5 V	0	2 V _{REF}		V
			For AVDD < 5 V	0	AVDD		V
V _{CM}	Input common-mode voltage range		V _{REF_A} = V _{REF_B} = V _{REF}	V _{REF} – 0.1	V _{REF}	V _{REF} + 0.1	V
C _{IN}	Input capacitance		In sample mode	40			pF
			In hold mode	4			pF
SAMPLING DYNAMICS							
t _A	Aperture delay			8			ns
	t _A match		ADC_A to ADC_B	40			ps
BW	Full-power bandwidth	At 3 dB		25			MHz
		At 0.1 dB		5			MHz
INTERNAL VOLTAGE REFERENCE							
V _{REFOUT}	Internal reference output voltage		At +25°C	2.495	2.500	2.505	V
V _{REFOUT-match}	V _{REFOUT} matching		REFOUT_A – REFOUT_B	±1			mV
dV _{REFOUT} /dt	Long-term voltage drift		1000 hours	150			ppm
dV _{REFOUT} /dT	Reference voltage drift with temperature			±10			ppm/°C
R _O	Internal reference output impedance			1			Ω
C _{OUT}	External output capacitor			22			μF
	Internal reference output settling time		C _{OUT} = 22 μF	10			ms
DIGITAL INPUTS ⁽¹⁾							
V _{IH}	Input voltage, high			0.7 DVDD	DVDD + 0.3		V
V _{IL}	Input voltage, low			–0.3	0.3 DVDD		V
C _{IN}	Input capacitance			5			pF
I _{IN}	Input leakage current		0 ≤ V _{digital-input} ≤ DVDD	±0.1			1 μA
DIGITAL OUTPUTS ⁽¹⁾							
V _{OH}	Output voltage, high		I _{OH} = 500-μA source	0.8 DVDD	DVDD		V
V _{OL}	Output voltage, low		I _{OH} = 500-μA sink	0	0.2 DVDD		V
POWER SUPPLY							
AVDD	Supply voltage	Analog (AVDD to GND)		4.75 ⁽²⁾	5.0	5.25	V
DVDD		Digital (DVDD to GND)	Operational range	1.65	3.3	5.25	V
			For specified performance	1.65	3	3.6	V
TEMPERATURE RANGE							
T _A	Operating free-air temperature			–40	+125		°C

(1) Specified by design; not production tested.

(2) The AVDD supply voltage defines the permissible voltage swing on the analog input pins. Refer to the [Power Supply Recommendations](#) section for more details.

6.8 ADS7251 Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{THROUGHPUT}}$	Throughput	$f_{\text{CLK}} = \text{max}$			2000	kSPS
f_{CLK}	CLOCK frequency	$f_{\text{THROUGHPUT}} = \text{max}$			32	MHz
t_{CLK}	CLOCK period	$f_{\text{THROUGHPUT}} = \text{max}$	31.25			ns
$t_{\text{PH_CK}}$	CLOCK high time		0.45		0.55	t_{CLK}
$t_{\text{PL_CK}}$	CLOCK low time		0.45		0.55	t_{CLK}
t_{CONV}	Conversion time			$t_{\text{SU_CSCK}} + 12 t_{\text{CLK}}$		ns
t_{ACQ}	Acquisition time	$f_{\text{CLK}} = \text{max}$	75			ns
$t_{\text{PH_CS}}$	$\overline{\text{CS}}$ high time		30			ns
$t_{\text{D_CKDO}}$	Delay time	SCLK rising edge to (next) data valid			15	ns
$t_{\text{DV_CSDO}}$		$\overline{\text{CS}}$ falling to data enable			10	ns
$t_{\text{D_CKCS}}$		Last SCLK rising to $\overline{\text{CS}}$ rising	5			ns
$t_{\text{DZ_CSDO}}$		$\overline{\text{CS}}$ rising to DOUT going to 3-state			10	ns
$t_{\text{SU_CSCK}}$	Setup time	$\overline{\text{CS}}$ falling to SCLK falling	15			ns

Figure 1 shows the details of the serial interface between the ADS7251 and the digital host controller.

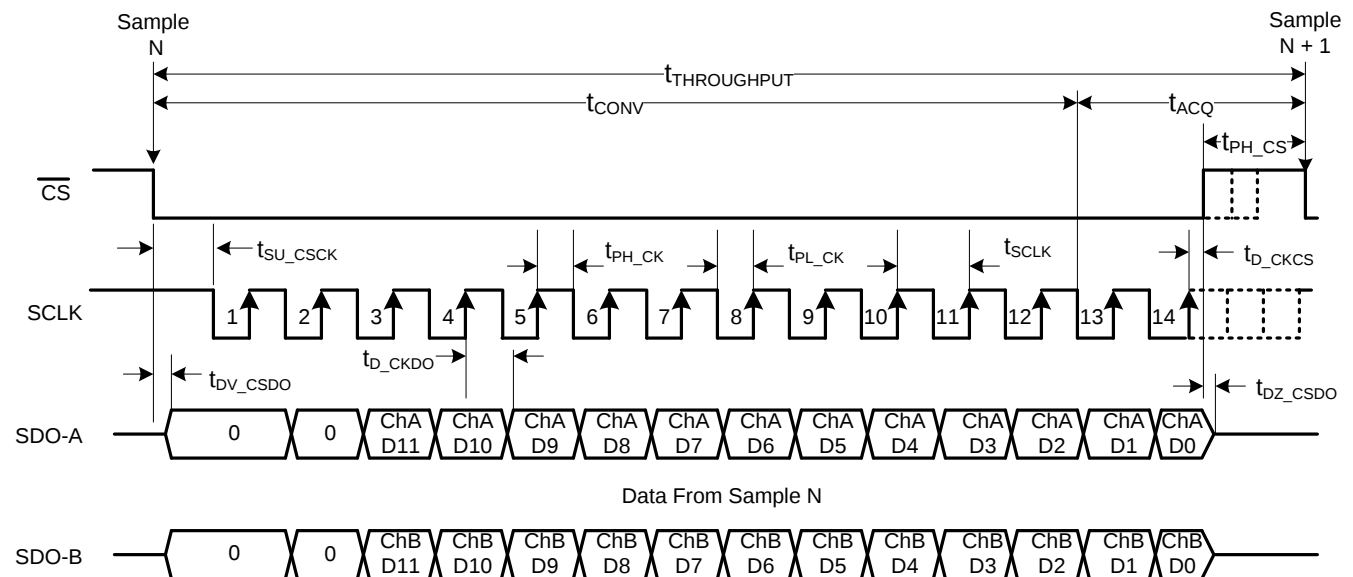


Figure 1. ADS7251 Serial Interface Timing Diagram

6.9 ADS7851 Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{THROUGHPUT}}$	Sample taken to data read	$f_{\text{CLK}} = \text{max}$			1500	kSPS
f_{CLK}	CLOCK frequency	$f_{\text{THROUGHPUT}} = \text{max}$			27	MHz
t_{CLK}	CLOCK period	$f_{\text{THROUGHPUT}} = \text{max}$	37			ns
$t_{\text{PH_CK}}$	CLOCK high time		0.45		0.55	t_{CLK}
$t_{\text{PL_CK}}$	CLOCK low time		0.45		0.55	t_{CLK}
t_{CONV}	Conversion time			$t_{\text{SU_CSCK}} + 14 t_{\text{CLK}}$		ns
t_{ACQ}	Acquisition time	$f_{\text{CLK}} = \text{max}$	90			ns
$t_{\text{PH_CS}}$	$\overline{\text{CS}}$ high time		30			ns
$t_{\text{D_CKDO}}$	Delay time	SCLK rising edge to (next) data valid			15	ns
$t_{\text{DV_CSDO}}$		$\overline{\text{CS}}$ falling to data enable			10	ns
$t_{\text{D_CKCS}}$		Last SCLK rising to $\overline{\text{CS}}$ rising	5			ns
$t_{\text{DZ_CSDO}}$		$\overline{\text{CS}}$ rising to DOUT going to 3-state			10	ns
$t_{\text{SU_CSCK}}$	Setup time	$\overline{\text{CS}}$ falling to SCLK falling	15			ns

Figure 2 shows the details of the serial interface between the ADS7851 and the digital host controller.

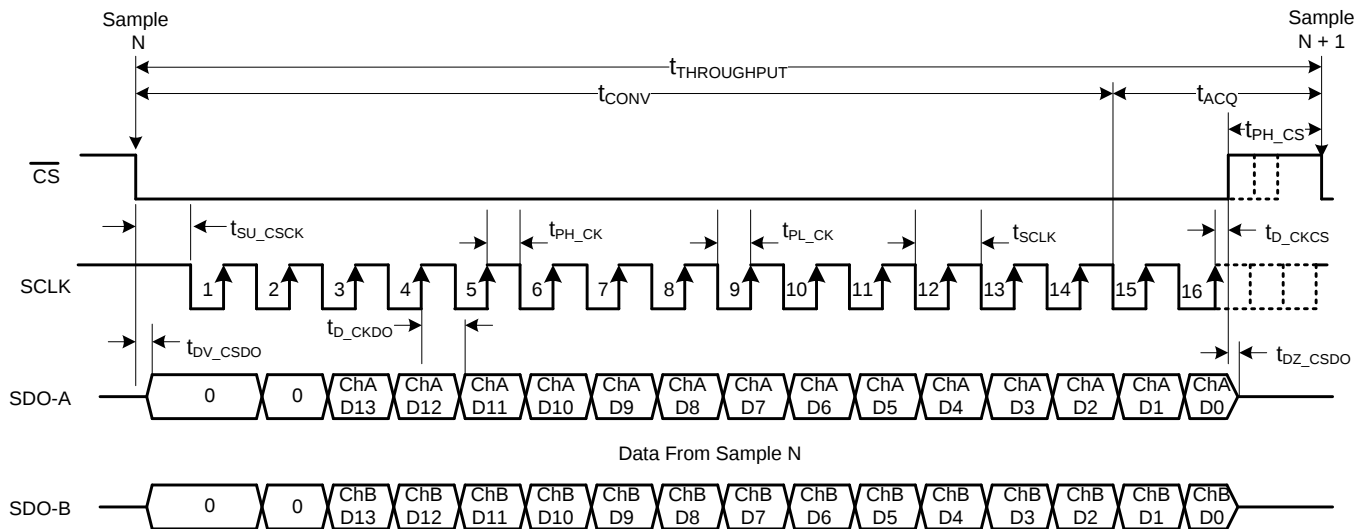


Figure 2. ADS7851 Serial Interface Timing Diagram

6.10 Typical Characteristics: ADS7251

At $T_A = +25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$ (internal), and $f_{DATA} = 1\text{ MSPS}$, unless otherwise noted.

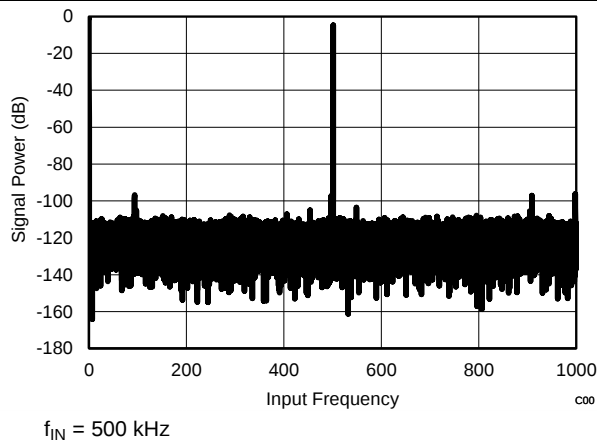


Figure 3. Typical FFT for 500-kHz Input

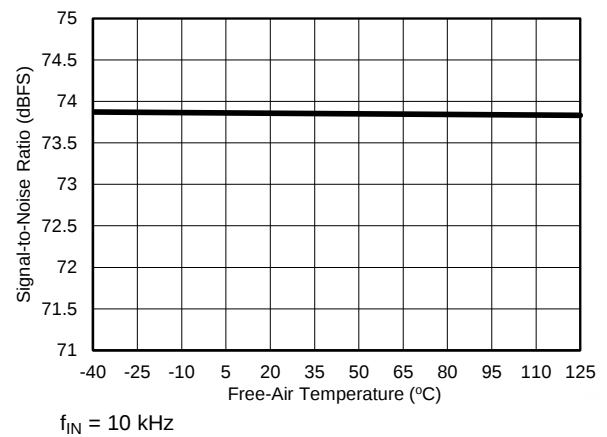


Figure 4. SNR vs Device Temperature

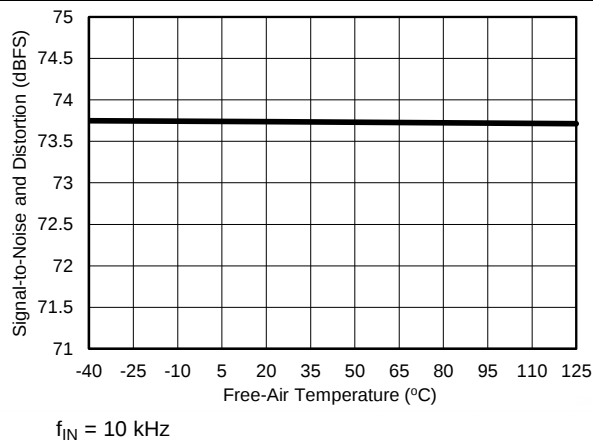


Figure 5. SINAD vs Device Temperature

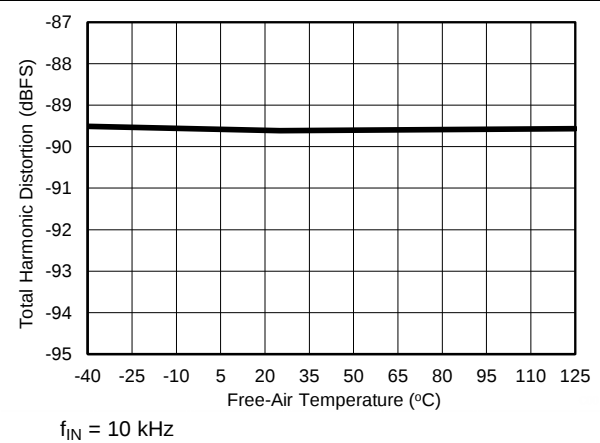


Figure 6. THD vs Device Temperature

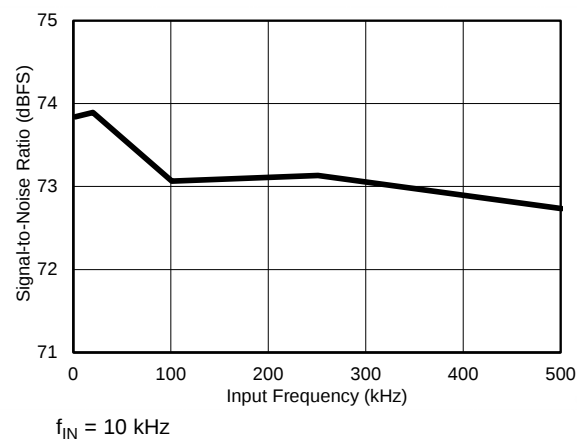


Figure 7. SNR vs Input Frequency

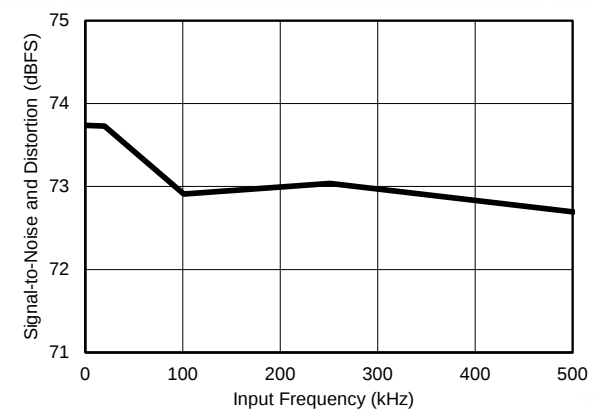


Figure 8. SINAD vs Input Frequency

Typical Characteristics: ADS7251 (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$ (internal), and $f_{DATA} = 1\text{ MSPS}$, unless otherwise noted.

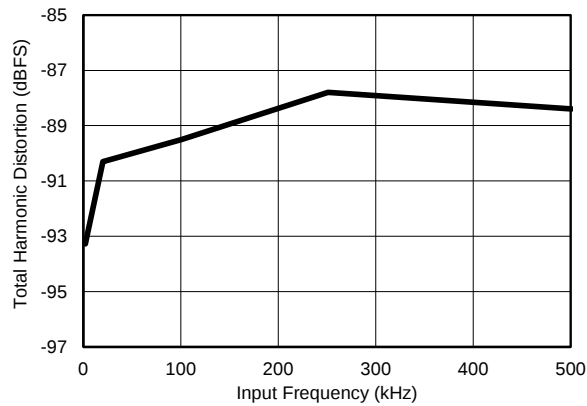


Figure 9. THD vs Input Frequency

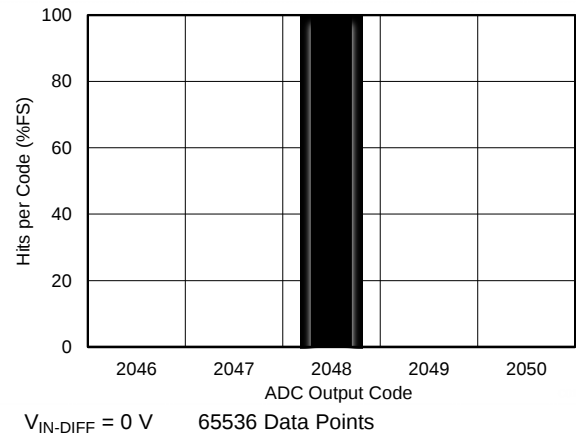


Figure 10. DC Histogram

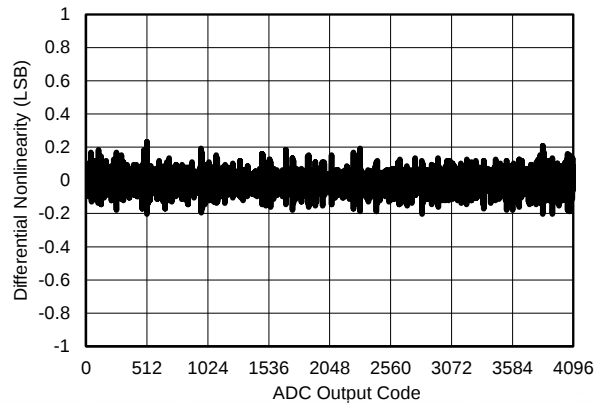


Figure 11. Typical DNL

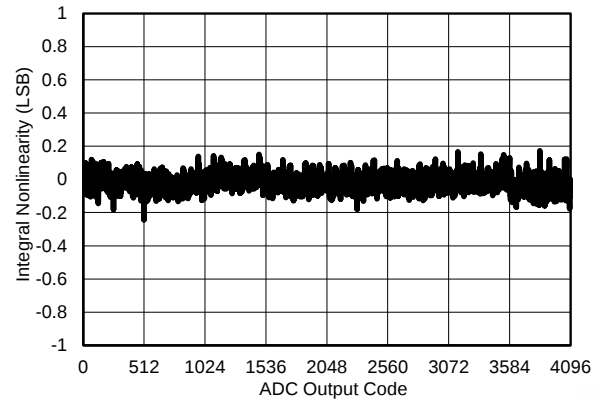


Figure 12. Typical INL

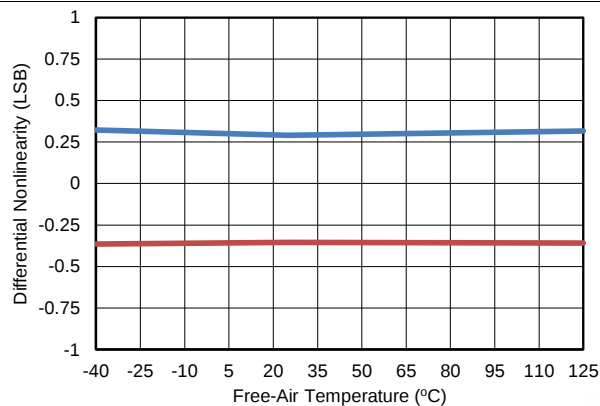


Figure 13. DNL vs Device Temperature

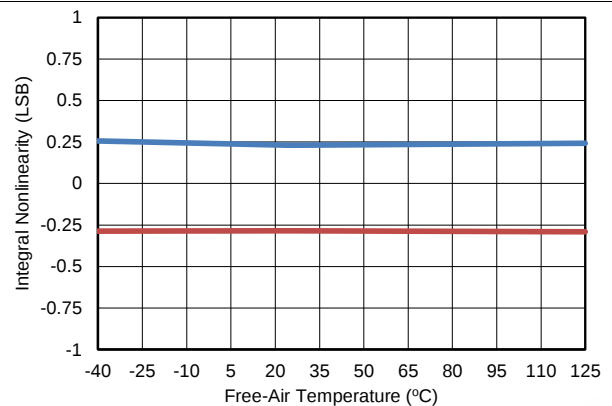


Figure 14. INL vs Device Temperature

Typical Characteristics: ADS7251 (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$ (internal), and $f_{DATA} = 1\text{ MSPS}$, unless otherwise noted.

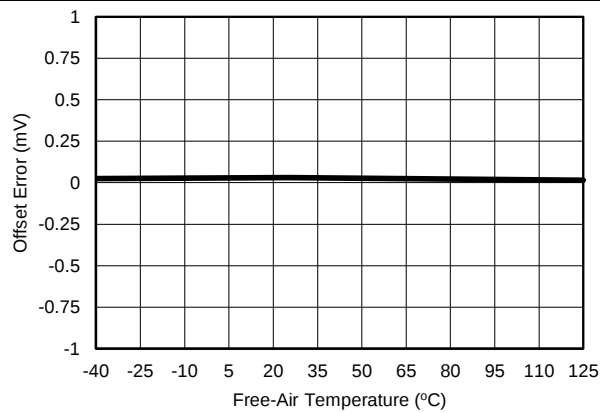


Figure 15. Offset Error vs Device Temperature

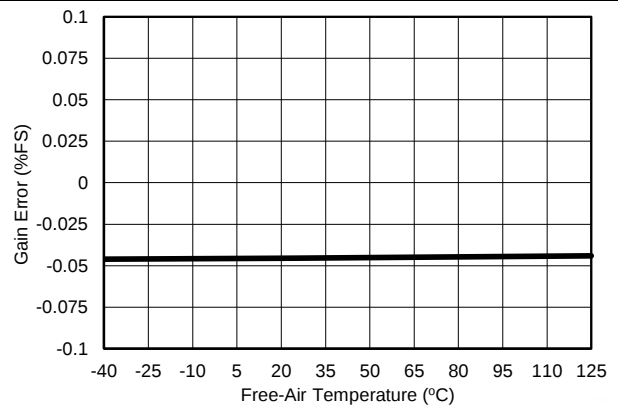


Figure 16. Gain Error vs Device Temperature

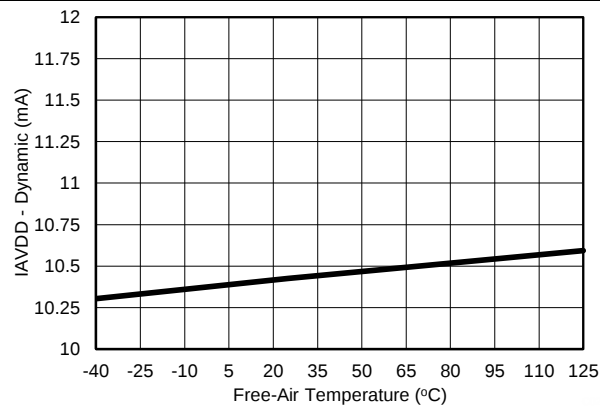


Figure 17. I_{AVDD} vs Device Temperature

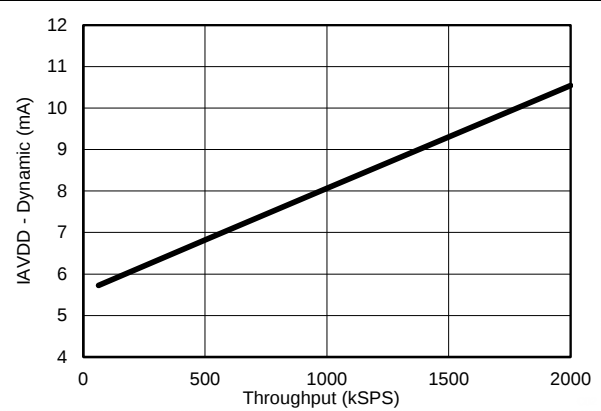


Figure 18. I_{AVDD} vs Throughput

6.11 Typical Characteristics: ADS7851

At $T_A = +25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$ (internal), and $f_{DATA} = 1\text{ MSPS}$, unless otherwise noted.

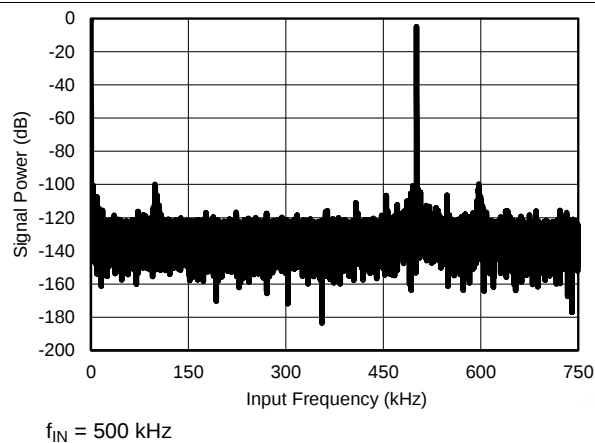


Figure 19. Typical FFT for 500-kHz Input

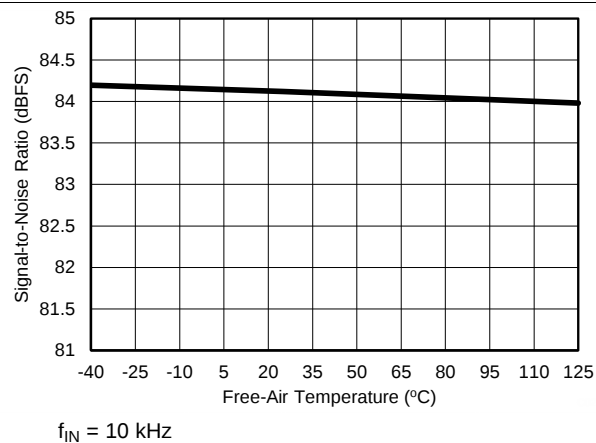


Figure 20. SNR vs Device Temperature

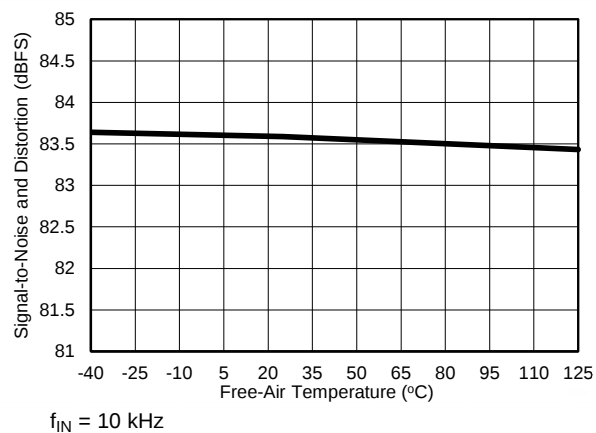


Figure 21. SINAD vs Device Temperature

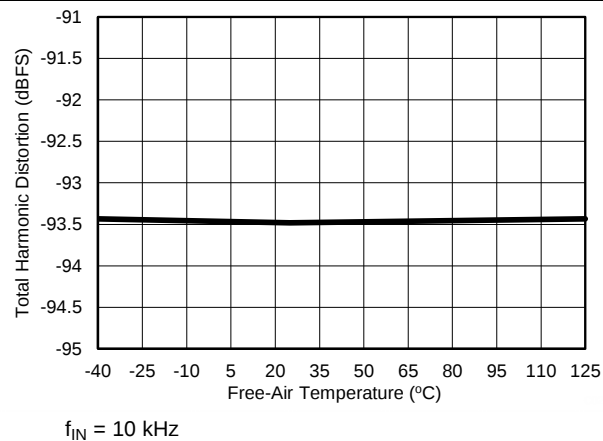


Figure 22. THD vs Device Temperature

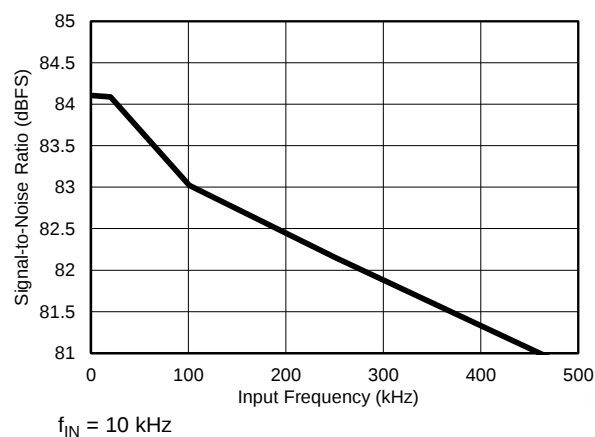


Figure 23. SNR vs Input Frequency

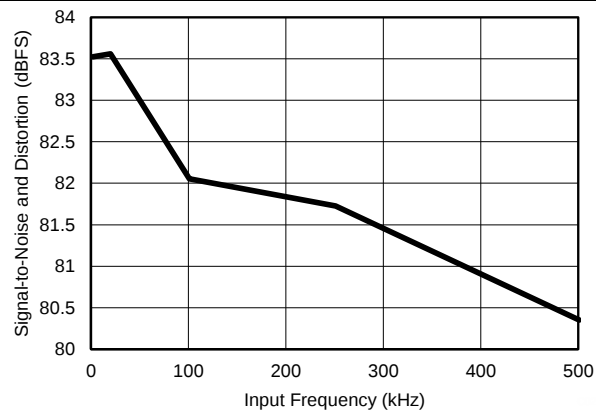


Figure 24. SINAD vs Input Frequency

Typical Characteristics: ADS7851 (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = 5\text{ V}$, $DV_{DD} = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$ (internal), and $f_{DATA} = 1\text{ MSPS}$, unless otherwise noted.

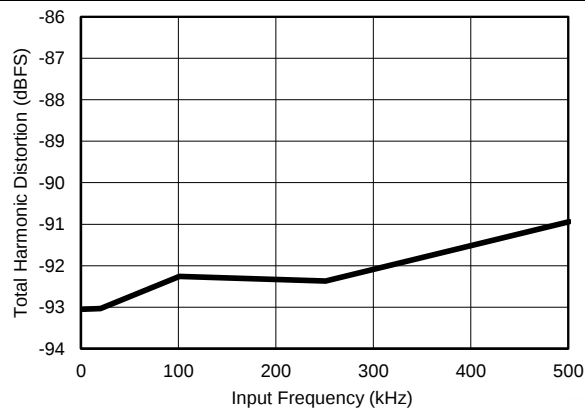


Figure 25. THD vs Input Frequency

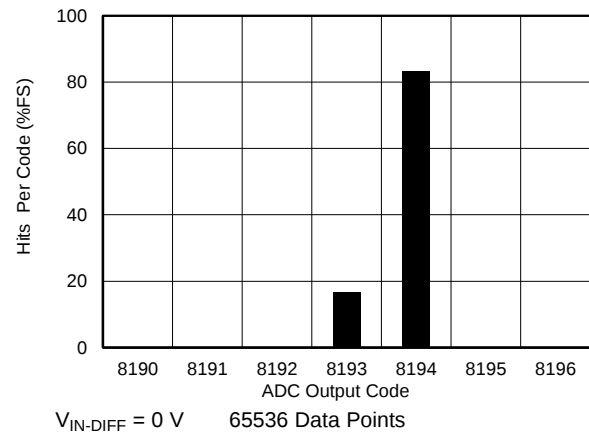


Figure 26. DC Histogram

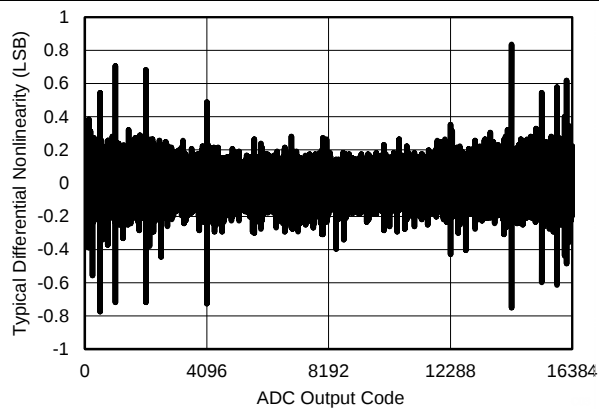


Figure 27. Typical DNL

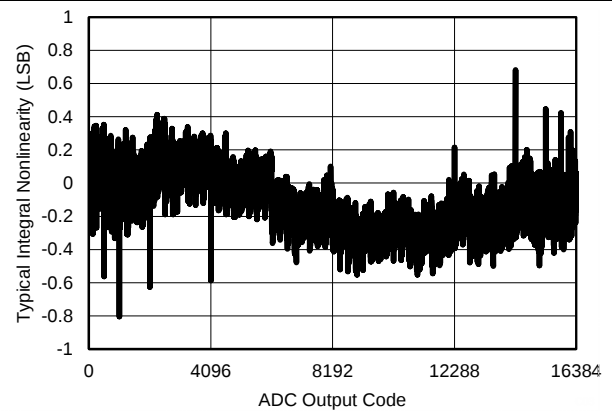


Figure 28. Typical INL

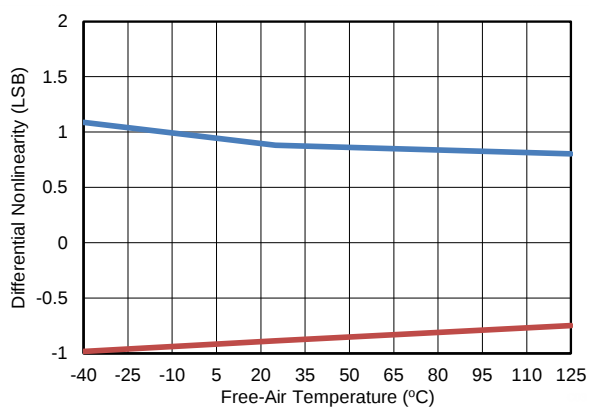


Figure 29. DNL vs Device Temperature

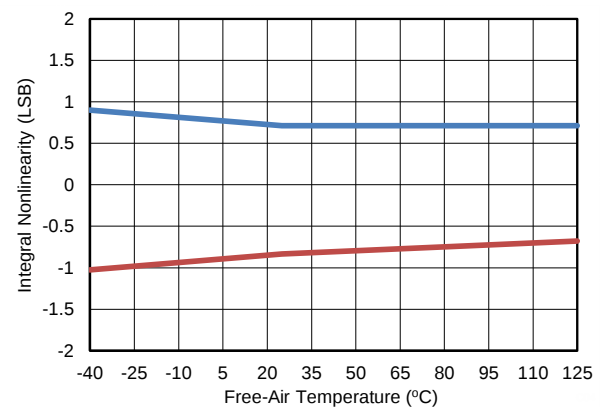


Figure 30. INL vs Device Temperature

Typical Characteristics: ADS7851 (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$ (internal), and $f_{DATA} = 1\text{ MSPS}$, unless otherwise noted.

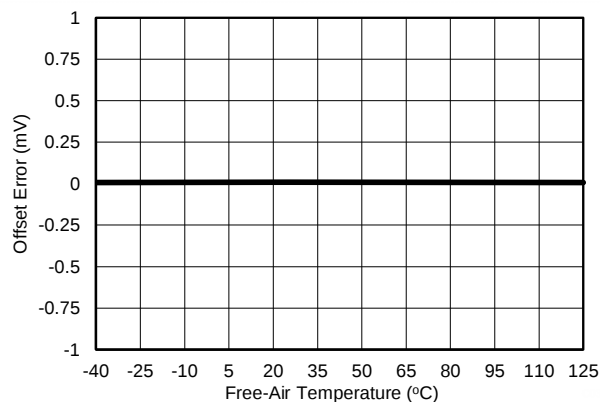


Figure 31. Offset Error vs Device Temperature

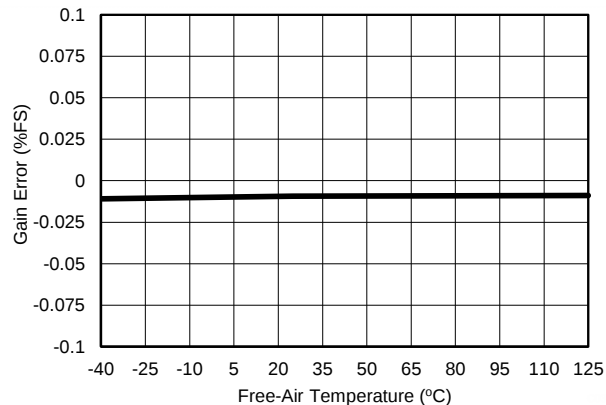


Figure 32. Gain Error vs Device Temperature

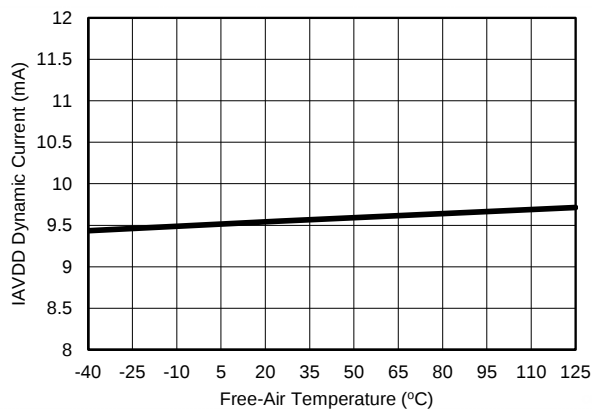


Figure 33. I_{AVDD} vs Device Temperature

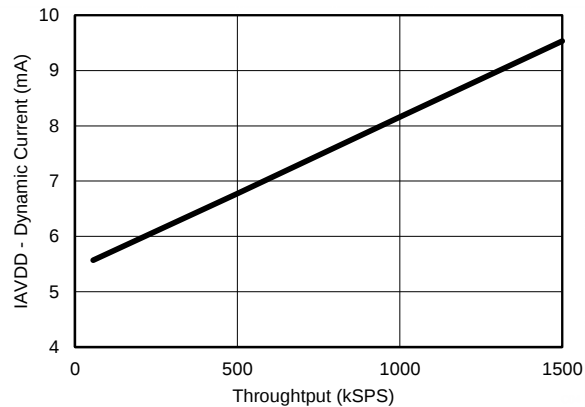


Figure 34. I_{AVDD} vs Throughput

6.12 Typical Characteristics: Common

At $T_A = +25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, and $V_{REF} = 2.5\text{ V}$ (internal), unless otherwise noted.

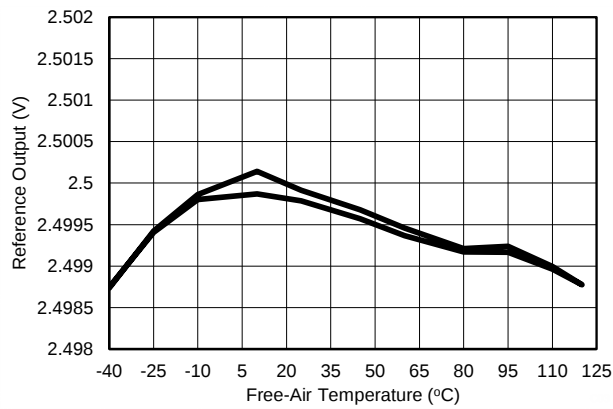
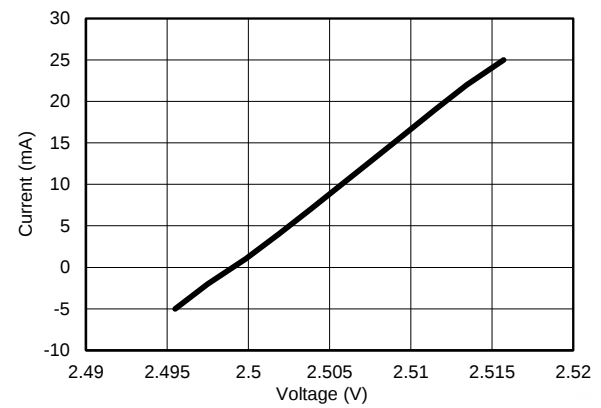


Figure 35. Reference Output vs Device Temperature



$R_{out} = 0.75\ \Omega$ Typ

Figure 36. Internal Reference: Output Current vs Output Voltage

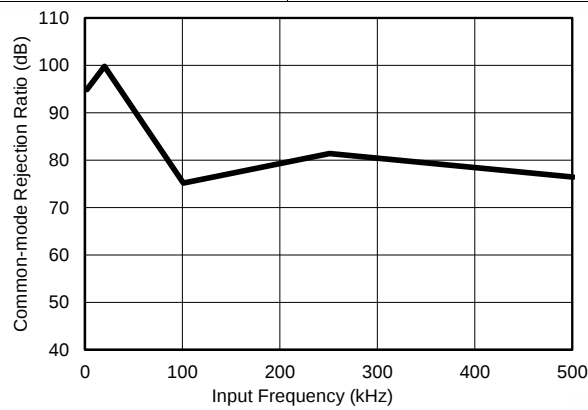


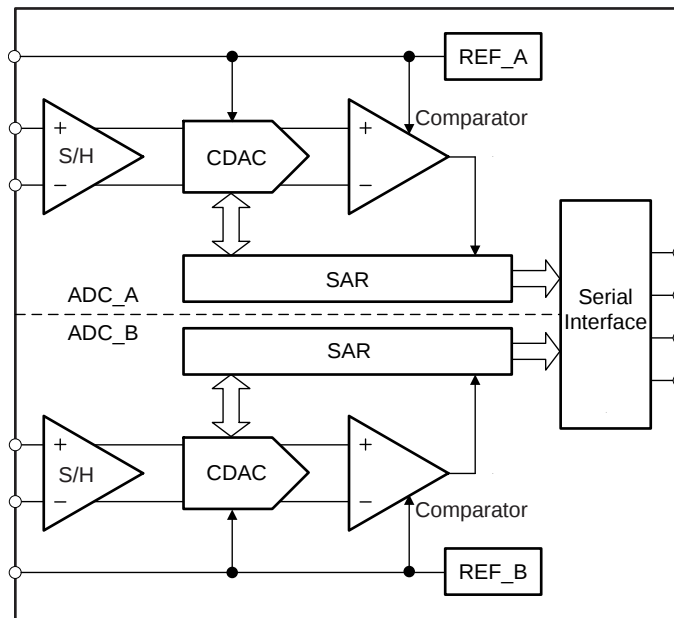
Figure 37. CMRR vs Input Frequency

7 Detailed Description

7.1 Overview

The ADS7251 and ADS7851 are pin-compatible, dual, simultaneous-sampling, analog-to-digital converters (ADCs). Each device features two independent internal voltage references and supports fully-differential input signals with the input common-mode on each input pin equal to the reference voltage. The full-scale input signal on each input pin is equal to twice the reference voltage. The devices provide a simple, serial interface to the host controller and operate over a wide range of digital power supplies.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference

The device has two simultaneous sampling ADCs (ADC_A and ADC_B) and two independent internal reference sources (INTREF_A and INTREF_B). INTREF_A outputs voltage V_{REF_A} on pin REFOUT_A and INTREF_B outputs voltage V_{REF_B} on pin REFOUT_B. As shown in Figure 38, the REFOUT_A and REFOUT_B pins must be decoupled with the REFGND_A and REFGND_B pins, respectively, with individual 22- μ F decoupling capacitors. ADC_A operates with reference voltage V_{REF_A} and ADC_B operates with reference voltage V_{REF_B} .

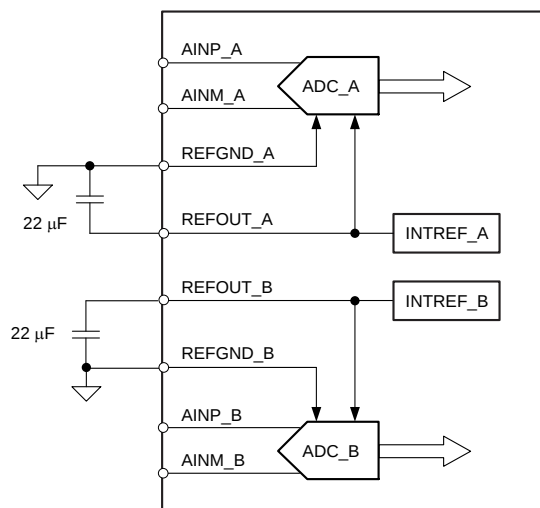


Figure 38. Reference Block Diagram

Feature Description (continued)

7.3.2 Analog Input

The devices support fully-differential analog input signals. These inputs are sampled and converted simultaneously by the two ADCs, ADC_A and ADC_B. [Figure 39a](#) and [Figure 39b](#) show equivalent circuits for the ADC_A and ADC_B analog input pins, respectively.

Series resistance (R_S) represents the on-state sampling switch resistance (typically 50 Ω) and C_{SAMPLE} is the device sampling capacitor (typically 40 pF). ADC_A samples V_{AINP_A} and V_{AINM_A} and converts for the difference voltage ($V_{AINP_A} - V_{AINM_A}$). ADC_B samples V_{AINP_B} and V_{AINM_B} and converts for the difference voltage ($V_{AINP_B} - V_{AINM_B}$).

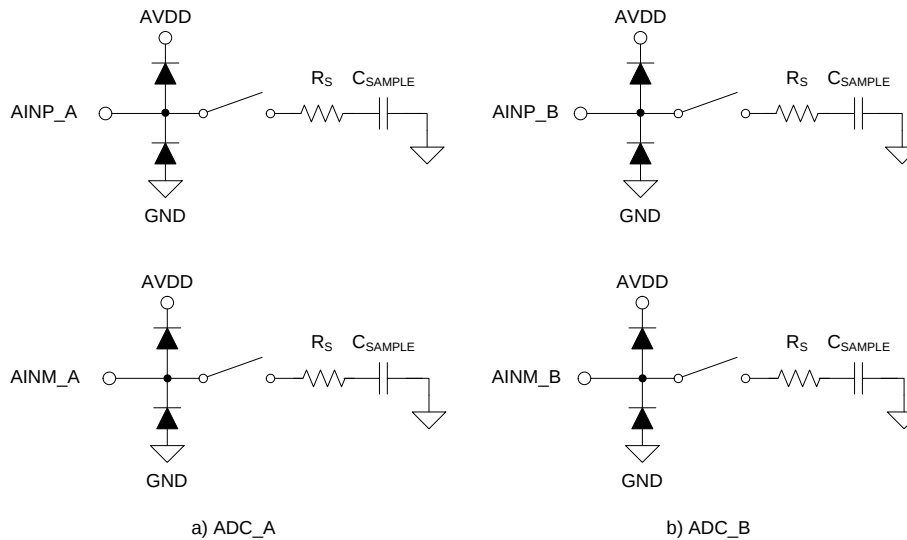


Figure 39. Equivalent Circuit for the Analog Input Pins

7.3.2.1 Analog Input Full-Scale Range

The analog input full-scale range (FSR) for ADC_A and ADC_B is twice the reference voltage provided to the particular ADC. Therefore, the FSR for ADC_A and ADC_B can be determined by [Equation 1](#) and [Equation 2](#), respectively:

$$FSR_ADC_A = 2 \times V_{REF_A}, \quad (1)$$

$$V_{AINP_A} \text{ and } V_{AINM_A} = 0 \text{ to } 2 \times V_{REF_A},$$

$$FSR_ADC_B = 2 \times V_{REF_B}, \quad (2)$$

$$V_{AINP_B} \text{ and } V_{AINM_B} = 0 \text{ to } 2 \times V_{REF_B}$$

To use the full dynamic input range on the analog input pins, AVDD must be as shown in [Equation 3](#), [Equation 4](#), and [Equation 5](#):

$$AVDD \geq 2 \times V_{REF_A} \quad (3)$$

$$AVDD \geq 2 \times V_{REF_B} \quad (4)$$

$$4.5 \text{ V} \leq AVDD \leq 5.5 \text{ V} \quad (5)$$

7.3.2.2 Common-Mode Voltage Range

For the analog input, the devices support a common-mode voltage equal to the reference voltage provided to the ADC. Therefore, the common-mode voltage for the ADC_A and ADC_B must be as shown in [Equation 6](#) and [Equation 7](#), respectively.

$$V_{CM_A} = V_{REF_A} \quad (6)$$

$$V_{CM_B} = V_{REF_B} \quad (7)$$

Feature Description (continued)

7.3.3 ADC Transfer Function

The device output is in twos complement format. Device resolution for the fully-differential input can be computed by [Equation 8](#):

$$1 \text{ LSB} = (4 \times V_{\text{REF}}) / (2^N)$$

where:

- $V_{\text{REF}} = V_{\text{REF_A}} = V_{\text{REF_B}}$, and
 - $N = 12$ (ADS7251), or 14 (ADS7851).
- (8)

[Table 1](#) shows the different input voltages and the corresponding device output codes. [Figure 40](#) shows the ideal transfer characteristics for the device.

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINP_x – AINM_x)	OUTPUT CODE (Hex)		
	CODE	ADS7251	ADS7851
$< -2 \times V_{\text{REF}}$	NFSC	800	2000
$-2 \times V_{\text{REF}} + 1 \text{ LSB}$	NFSC + 1	801	2001
-1 LSB	MC	FFF	3FFF
0	PLC	000	0000
$> 2 \times V_{\text{REF}} - 1 \text{ LSB}$	PFSC	7FF	1FFF

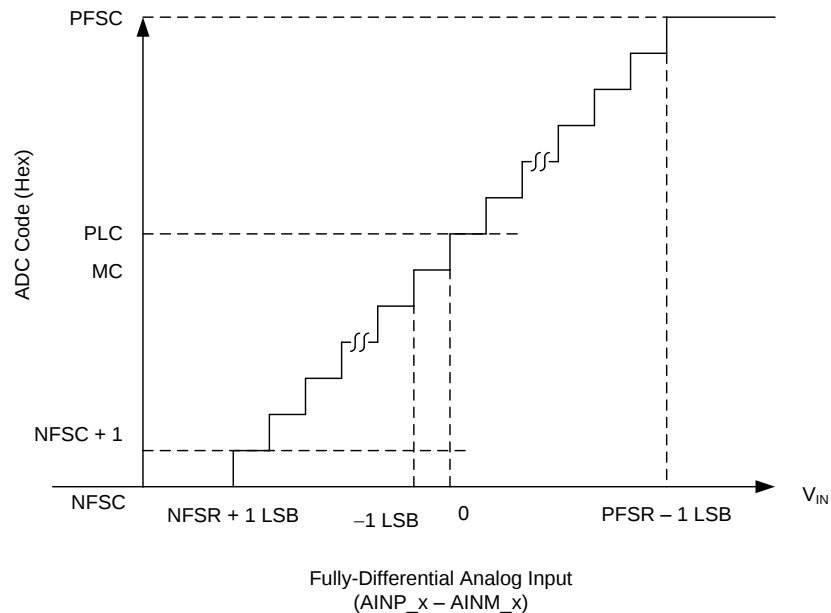


Figure 40. Ideal Transfer Characteristics

7.4 Device Functional Modes

7.4.1 Serial Interface

The devices support a simple, SPI-compatible interface to the external digital host. The $\overline{\text{CS}}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{\text{CS}}$ falling edge and ends with a $\overline{\text{CS}}$ rising edge. The SDO_A and SDO_B pins output the ADC_A and ADC_B conversion results, respectively. Figure 41 shows a detailed timing diagram for the ADS7251.

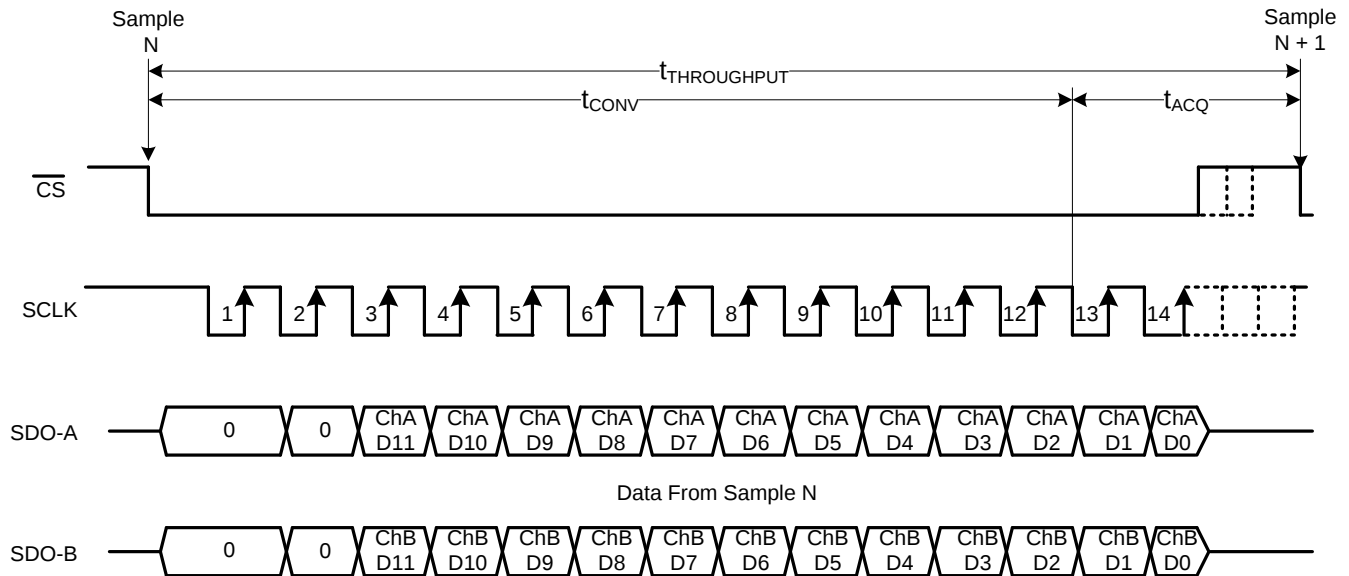


Figure 41. ADS7251 Serial Interface Timing Diagram

Figure 42 shows a detailed timing diagram for the ADS7851.

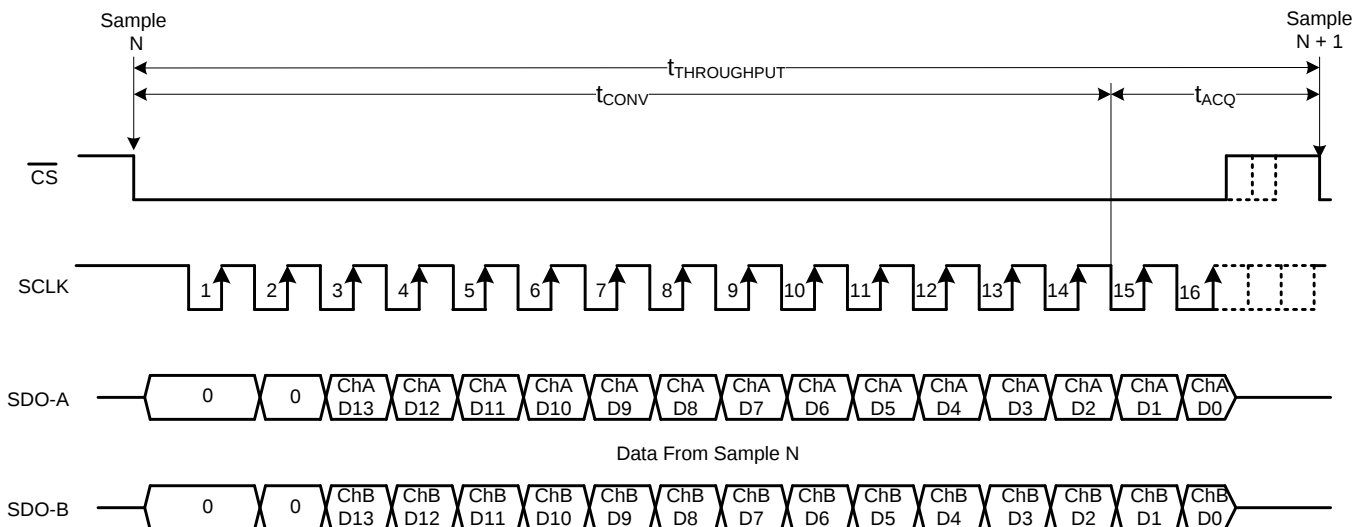


Figure 42. ADS7851 Serial Interface Timing Diagram

Device Functional Modes (continued)

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs '0' on the SDO_A and SDO_B pins. A minimum delay of t_{SU_CCLK} must elapse between the $\overline{CS}$ falling edge and the first SCLK falling edge. The subsequent clock edges are used to shift out the conversion result using the serial interface, as shown in Table 2. The sample-and-hold circuit returns to sample mode as soon as the conversion process is over. Any extra clock edges output a '0' on the SDO pins. A $\overline{CS}$ rising edge ends the frame and brings the serial data bus to 3-state.

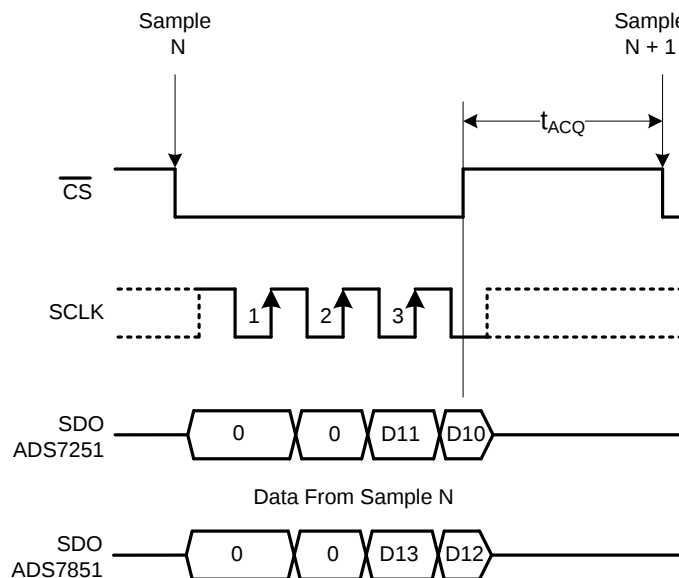
Table 2. Data Launch Edge

DEVICE	PIN	LAUNCH EDGE									
		$\overline{CS}\downarrow$	SCLK								$\overline{CS}\uparrow$
			$\downarrow 1$	$\downarrow 2$	...	$\downarrow 13$	$\downarrow 14$	$\downarrow 15$	$\downarrow 16$	...	
ADS7851	SDO-A	0	0	D13_A	...	D2_A	D1_A	D0_A	0	...	Hi-Z
	SDO-B	0	0	D13_B	...	D2_B	D1_B	D0_B	0	...	Hi-Z
ADS7251	SDO-A	0	0	D11_A	...	D0_A	0	0	0	...	Hi-Z
	SDO-B	0	0	D11_B	...	D0_B	0	0	0	...	Hi-Z

7.4.2 Short-Cycling Feature

For the ADS7851, a minimum of 16 SCLK rising edges must be provided between the beginning and end of the frame to complete the 14-bit data transfer. For the ADS7251, a minimum of 14 SCLK rising edges must be provided between the beginning and end of the frame to complete the 12-bit data transfer. As shown in Figure 43, if $\overline{CS}$ is brought high before the expected number of SCLK rising edges are provided, the current frame is aborted and the device starts sampling the new analog input signal. However, the output data bits latched into the digital host before this $\overline{CS}$ rising edge are still valid data corresponding to sample N.

After aborting the current frame, $\overline{CS}$ must be kept high for t_{ACQ} to ensure minimum acquisition time is provided for the next conversion.


Figure 43. Short-Cycling Feature

8 Application and Implementation

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. The ADS7851 and ADS7251 feature an internal reference designed to support device requirements. This section details some general principles for designing the input driver circuit and provides some application circuits designed using these devices.

8.2 Typical Application

The application circuit shown in Figure 44 is optimized for using the ADS7251 at a 2-MSPS throughput to achieve lowest distortion and lowest noise for input signal frequencies up to 100 kHz.

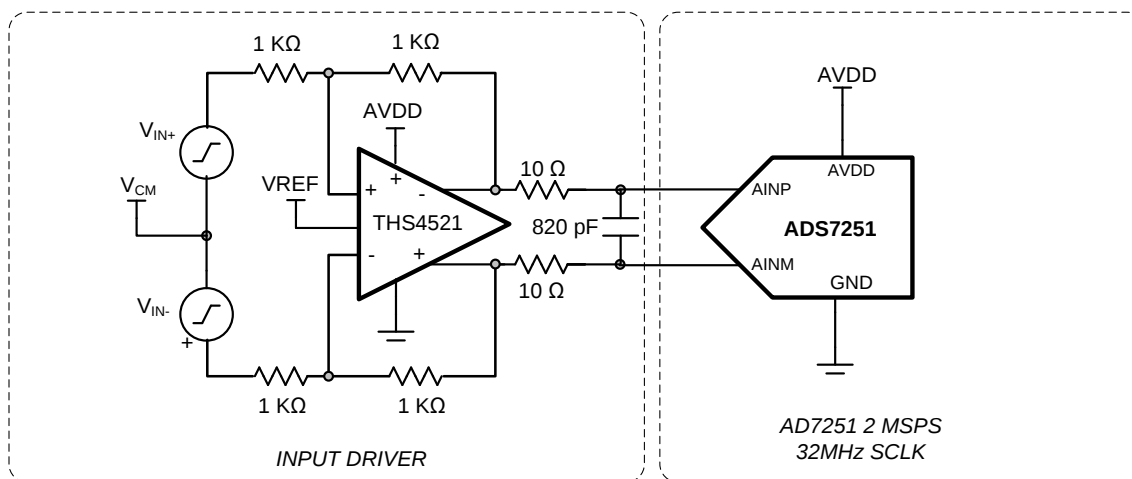


Figure 44. ADS7251 DAQ Circuit: Maximum SINAD for Input Signal Frequencies up to 100 kHz

The application circuit shown in Figure 45 is optimized for using the ADS7851 at a 1.5-MSPS throughput to achieve lowest distortion and lowest noise for input signal frequencies up to 100 kHz.

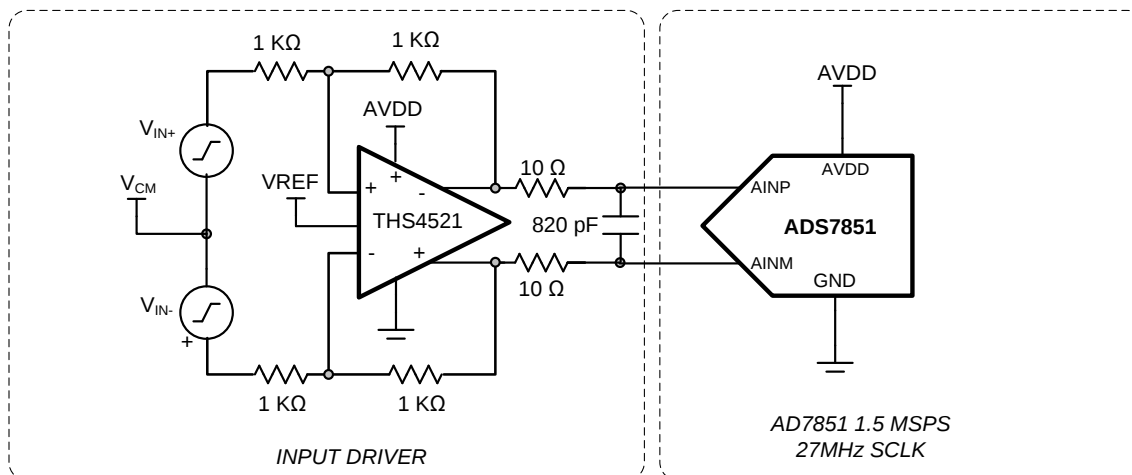


Figure 45. ADS7851 DAQ Circuit: Maximum SINAD for Input Signal Frequencies up to 100 kHz

Typical Application (continued)

8.2.1 Design Requirements

For the ADS7251, design an input driver and reference driver circuit to achieve > 71-dB SNR and < –90-dB THD at input frequencies of 10 kHz and 100 kHz.

For the ADS7851, design an input driver and reference driver circuit to achieve > 81-dB SNR and < –90-dB THD at input frequencies of 10 kHz and 100 kHz.

8.2.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and an antialiasing filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

8.2.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth.** Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in [Equation 9](#):

$$\text{Unity – Gain Bandwidth} \geq 4 \times \left(\frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \quad (9)$$

- **Noise.** Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is bandlimited by designing a low cutoff frequency RC filter, as explained in [Equation 10](#).

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6} \right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{\left(\frac{SNR(dB)}{20} \right)}$$

where:

- V_{1/f_AMP_PP} is the peak-to-peak flicker noise in μV_{RMS} ,
- e_{n_RMS} is the amplifier broadband noise density in $nV/\sqrt{Hz}$,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to '1' in a buffer configuration. (10)
- **Distortion.** Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in [Equation 11](#).

$$THD_{AMP} \leq THD_{ADC} - 10 \text{ (dB)} \quad (11)$$

- **Settling Time.** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

Typical Application (continued)

The distortion resulting from variation in the common-mode signal is eliminated by using a fully-differential amplifier (FDA) in an inverting gain configuration that establishes a fixed common-mode level at the ADC input. This configuration also eliminates the requirement of rail-to-rail swing at the amplifier input. The low-power [THS4521](#), used as an input driver, provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications. The device REFOUT_x pin can be directly connected to the V_{OCM} pin of the THS4521 to set the output common-mode voltage to 2.5 V, as required by the ADC.

8.2.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements (as shown in [Figure 46](#)). For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of C_{FLT} should be greater than 400 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

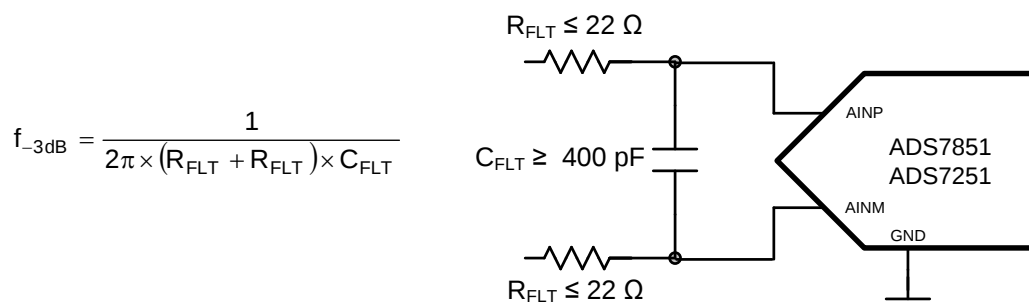


Figure 46. Antialiasing Filter

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22-Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

Typical Application (continued)

8.2.3 Application Curves

Figure 47 shows an FFT plot for the ADS7251 with the circuit shown in Figure 44 and an input frequency of 10 kHz. Figure 48 shows an FFT plot for the ADS7251 with the same circuit configuration but for an input frequency of 100 kHz.

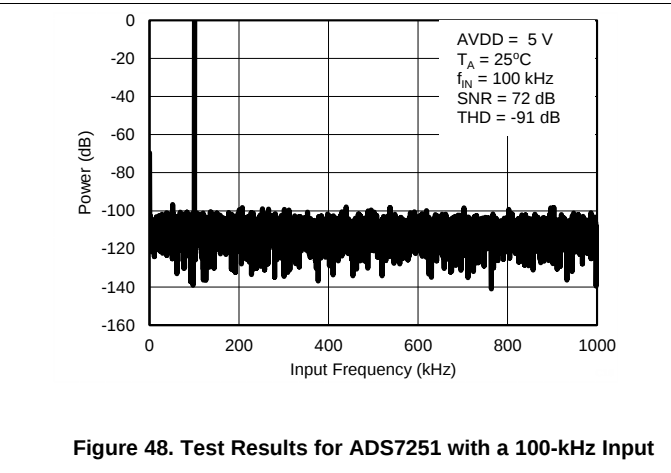
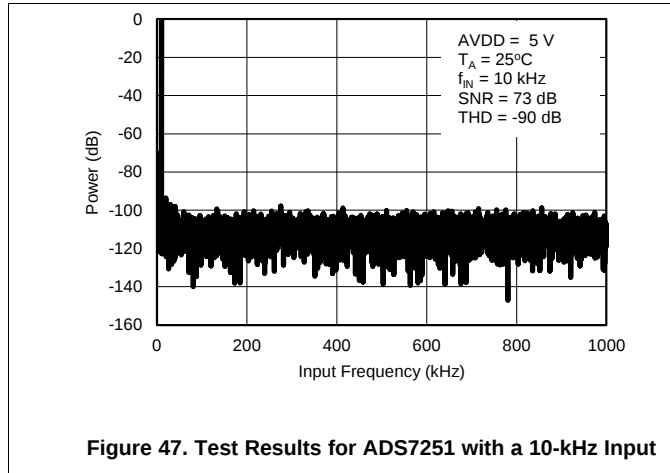
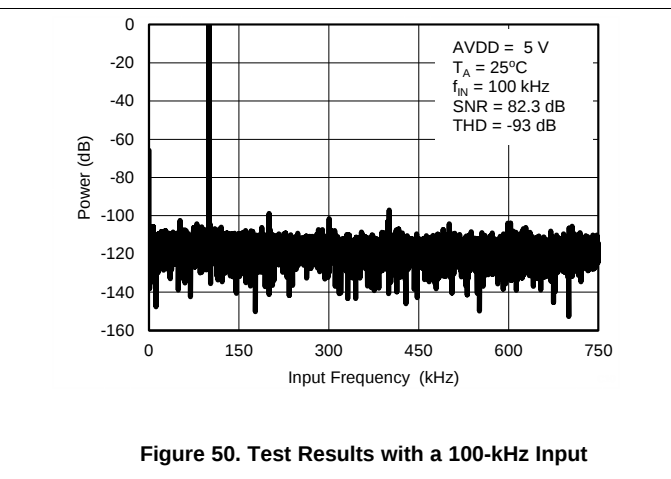
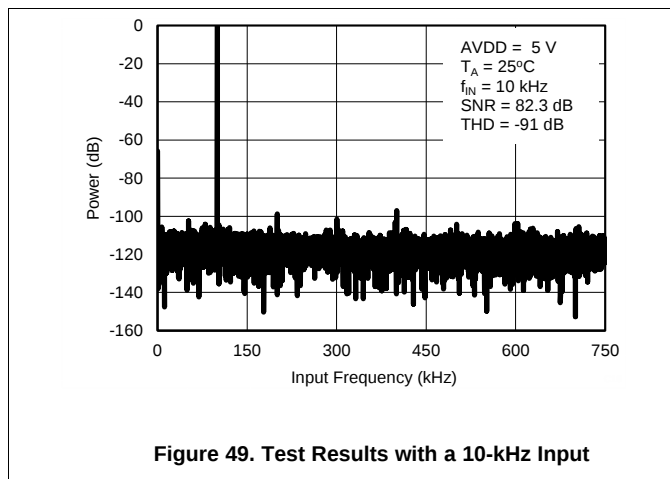


Figure 49 shows an FFT plot for the ADS7851 with the circuit shown in Figure 45 and an input frequency of 10 kHz. Figure 50 shows an FFT plot for the ADS7251 with the same circuit configuration but for an input frequency of 100 kHz.



9 Power Supply Recommendations

The devices have two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges.

The AVDD supply voltage value defines the permissible voltage swing on the analog input pins. To avoid saturation of output codes, and to use the full dynamic range on the analog input pins, AVDD must be set as shown in [Equation 12](#), [Equation 13](#), and [Equation 14](#):

$$AVDD \geq 2 \times V_{REF_A} \quad (12)$$

$$AVDD \geq 2 \times V_{REF_B} \quad (13)$$

$$4.75 \text{ V} \leq AVDD \leq 5.25 \text{ V} \quad (14)$$

Decouple the AVDD and DVDD pins with the GND pin using individual 10-μF decoupling capacitors, as shown in [Figure 51](#).

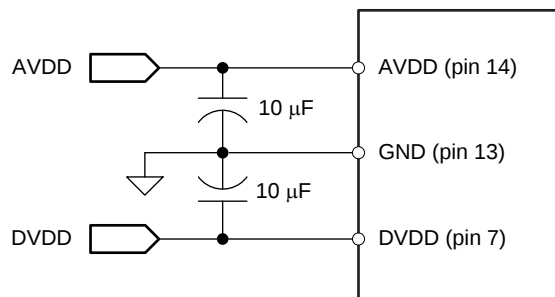


Figure 51. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

Figure 52 shows a board layout example for the ADS7251 and ADS7851. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 52, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the device must be clean and well-bypassed. Use 10- μ F, ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths.

The REFOUT-A and REFOUT-B reference outputs are bypassed with 10- μ F, X7R-grade ceramic capacitors (C_{REF-x}). Place the reference bypass capacitors as close as possible to the reference REFOUT-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFOUT-x pins and the bypass capacitors. Small 0.1- Ω to 0.2- Ω resistors (R_{REF-x}) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 52 shows C_{IN-A} and C_{IN-B} filter capacitors placed across the analog input pins of the device.

10.2 Layout Example

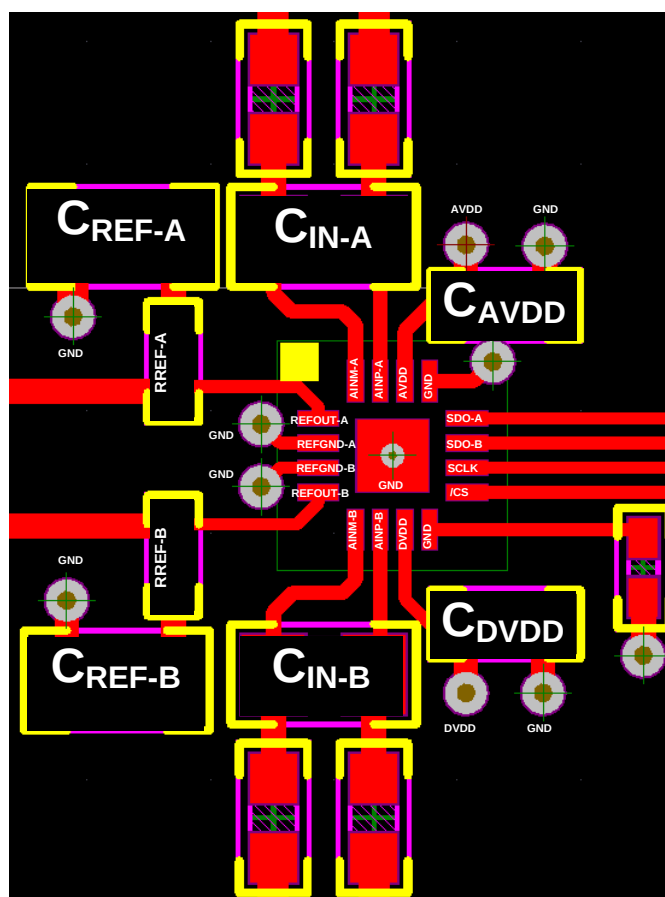


Figure 52. Example Layout for the ADS7251 and ADS7851

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- THS4521 数据表，[SBOS458](#)

11.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片与购买的快速访问。

Table 3. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ADS7251	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS7851	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 Trademarks

TINA is a trademark of Texas Instruments Inc..

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务 的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件 或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独力负责满足与其产品及其应用中使用的 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122
Copyright © 2014, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7251IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7251	Samples
ADS7251IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7251	Samples
ADS7851IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7851	Samples
ADS7851IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7851	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

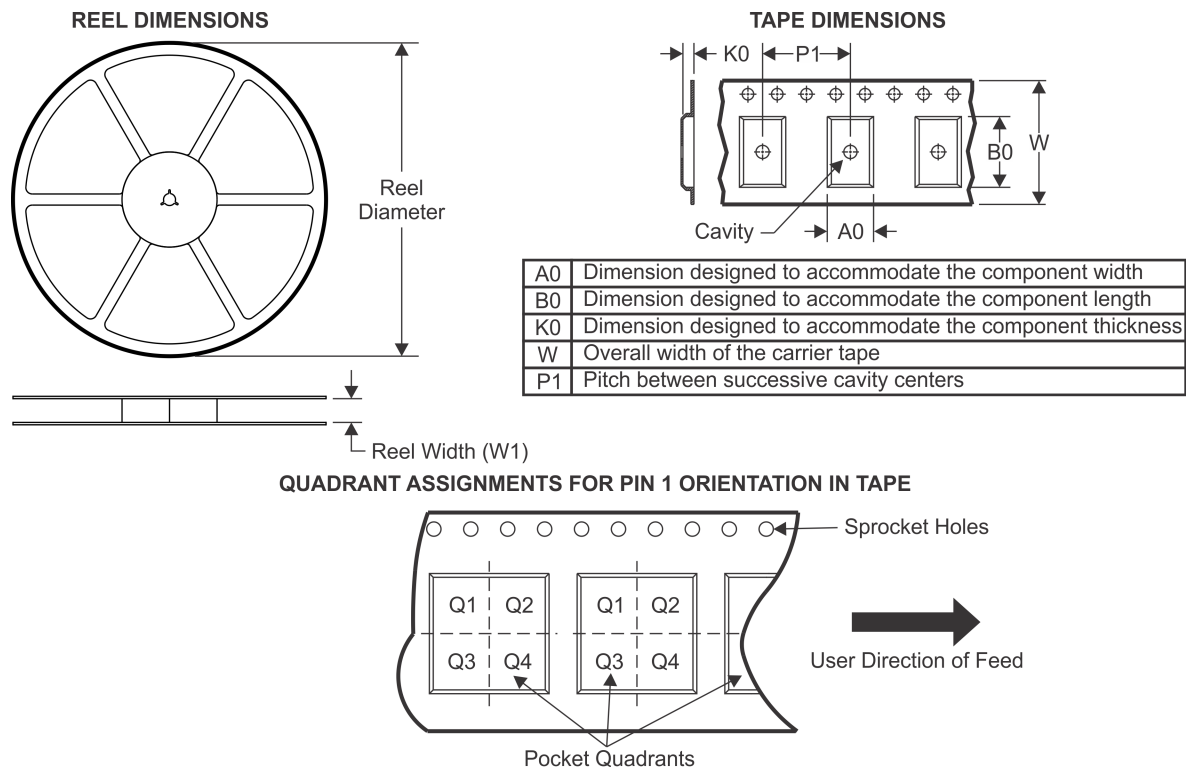
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

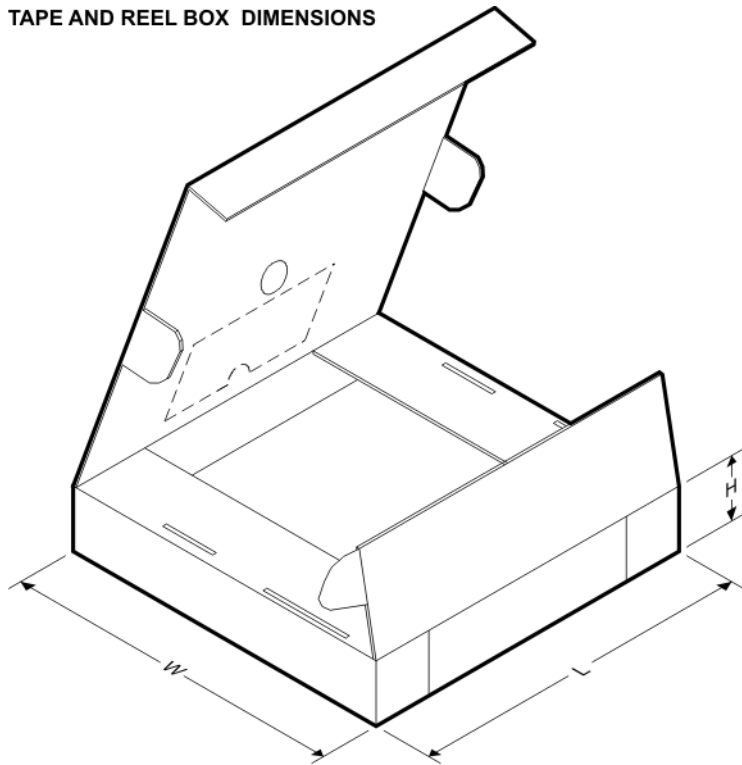
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7251IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7251IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7851IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7851IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



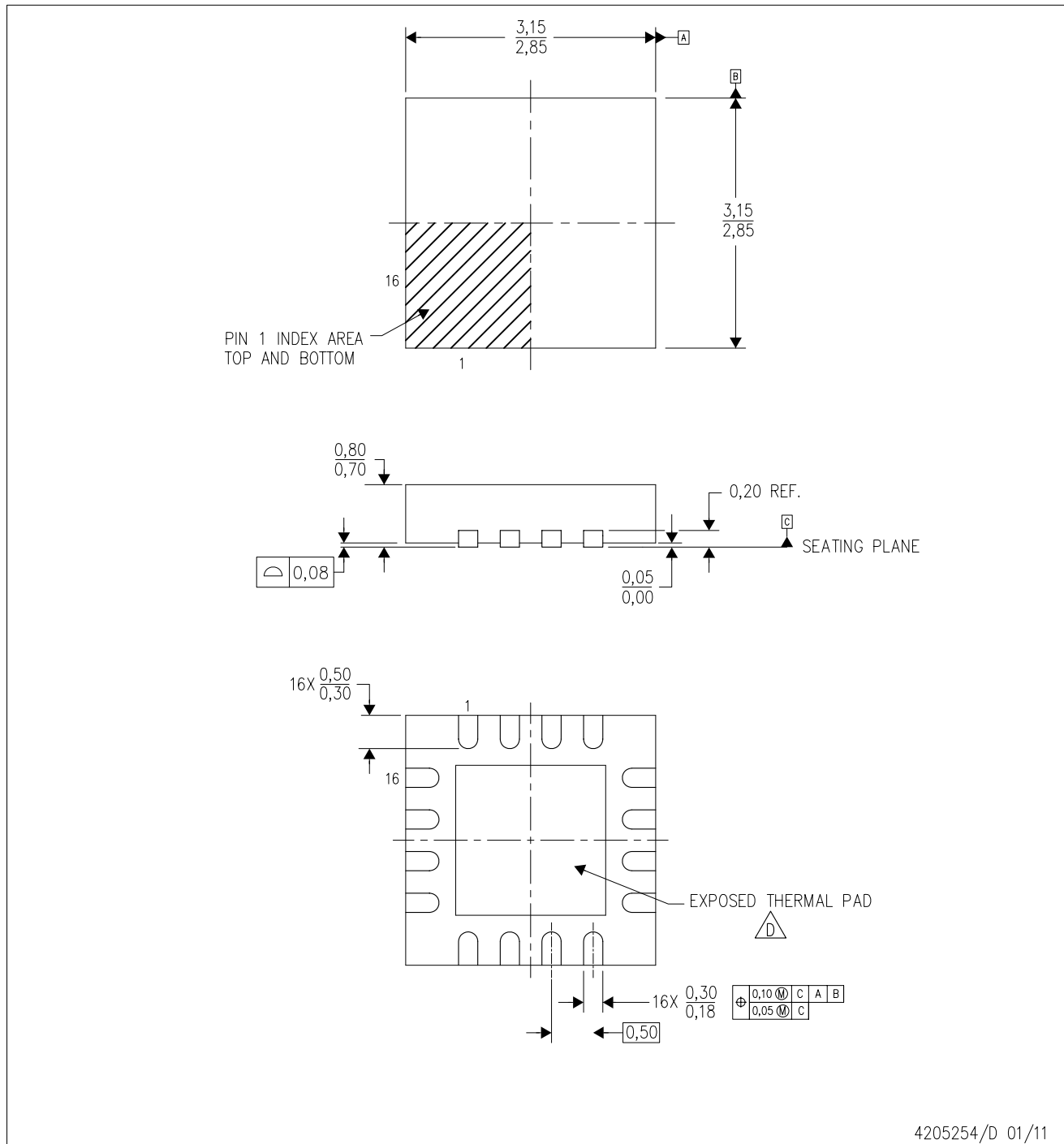
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7251IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7251IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7851IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7851IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

MECHANICAL DATA

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

RTE (S-PWQFN-N16)

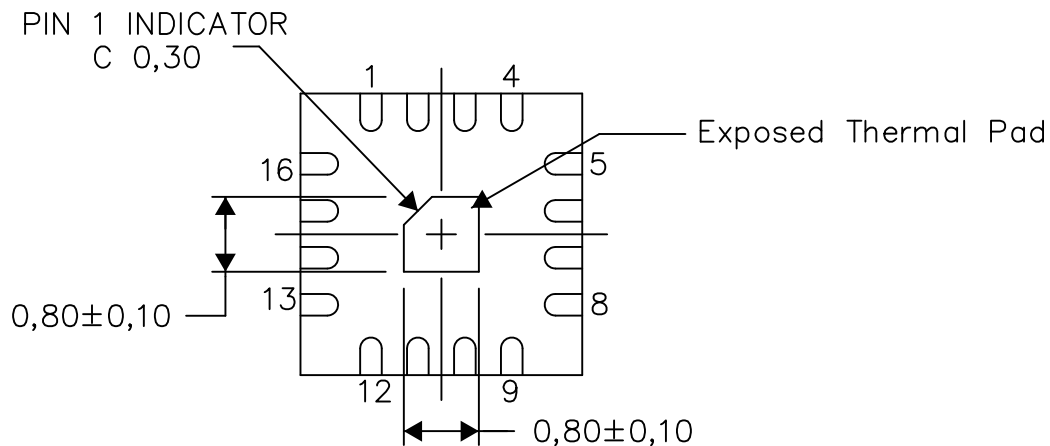
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

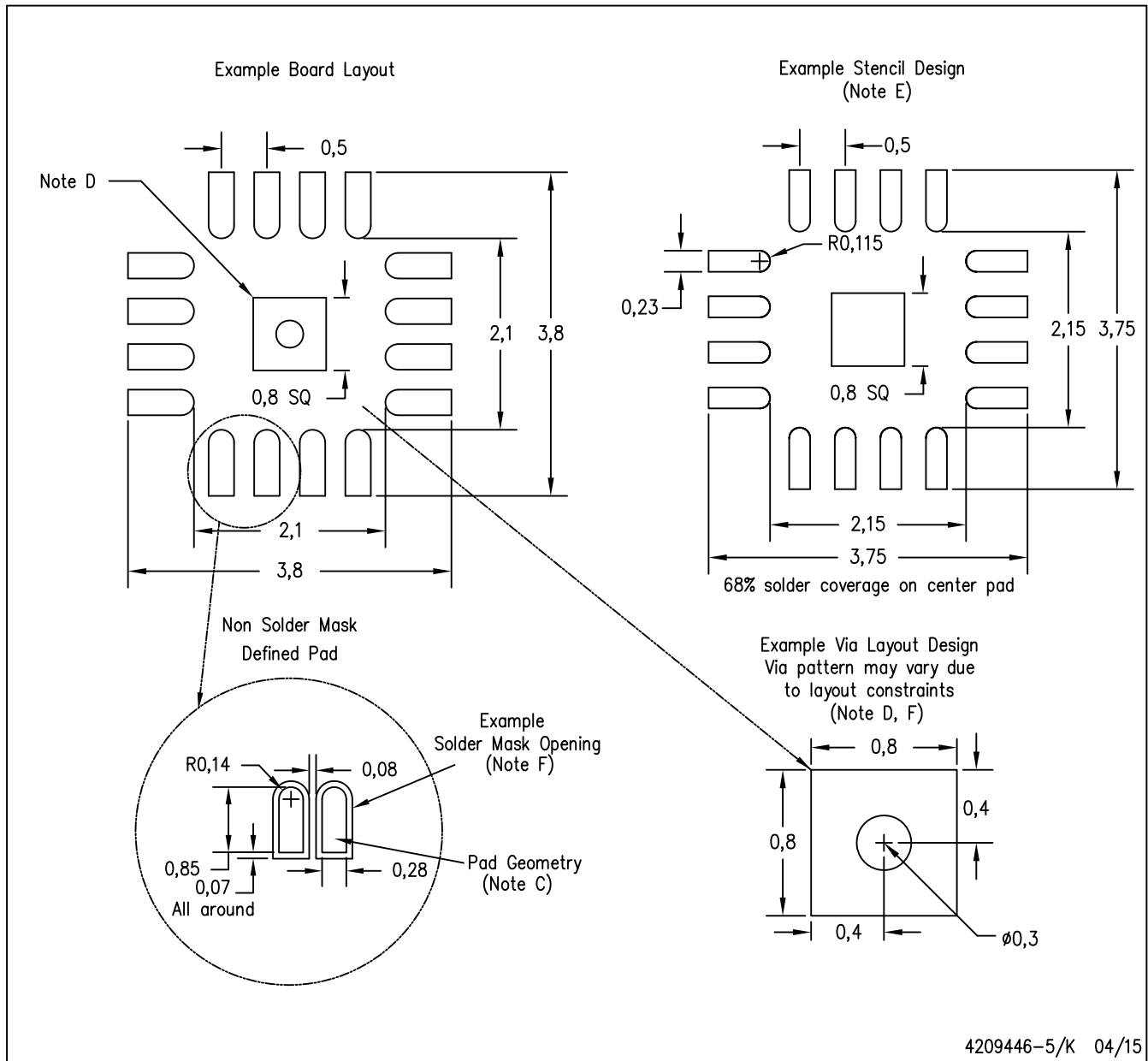
Exposed Thermal Pad Dimensions

4206446-5/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司