ADC12081 12-Bit, 5 MHz Self-Calibrating, Pipelined A/D Converter with Internal Sample & Hold

Check for Samples: ADC12081

FEATURES

- **Single 5V Power Supply**
- **Simple Analog Input Interface**
- **Internal Sample-and-Hold**
- **Internal Reference Buffer Amplifier**
- **Low Power Consumption**

APPLICATIONS

- **Image Processing Front End**
- **PC-Based Data Acquisition**
- **Scanners**
- **Fax Machines**
- **Waveform Digitizer**

DESCRIPTION

The ADC12081 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 5 megasamples per second (MSPS). The ADC12081 utilizes an innovative pipeline architecture to minimize die size and power consumption. The ADC12081 uses self-calibration and error correction to maintain accuracy and performance over temperature.

The ADC12081 converter operates on a 5V power supply and can digitize analog input signals in the range of 0 to 2V. A single convert clock controls the conversion operation. All digital I/O is TTL compatible.

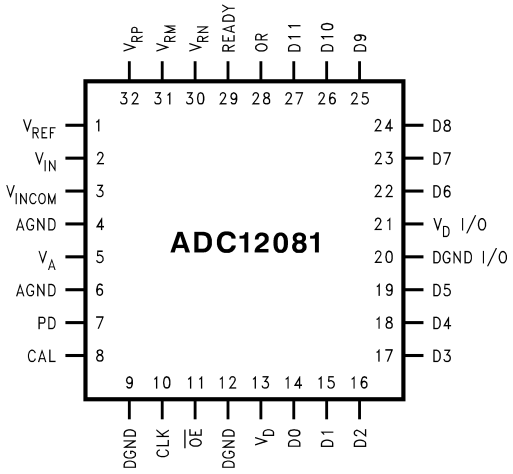
The ADC12081 is designed to minimize external components necessary for the analog input interface. An internal sample-and-hold circuit samples the analog input and an internal amplifier buffers the reference voltage input.

The ADC12081 is available in the 32-lead LQFP package and is designed to operate over the extended commercial temperature range of -40°C to +85°C.

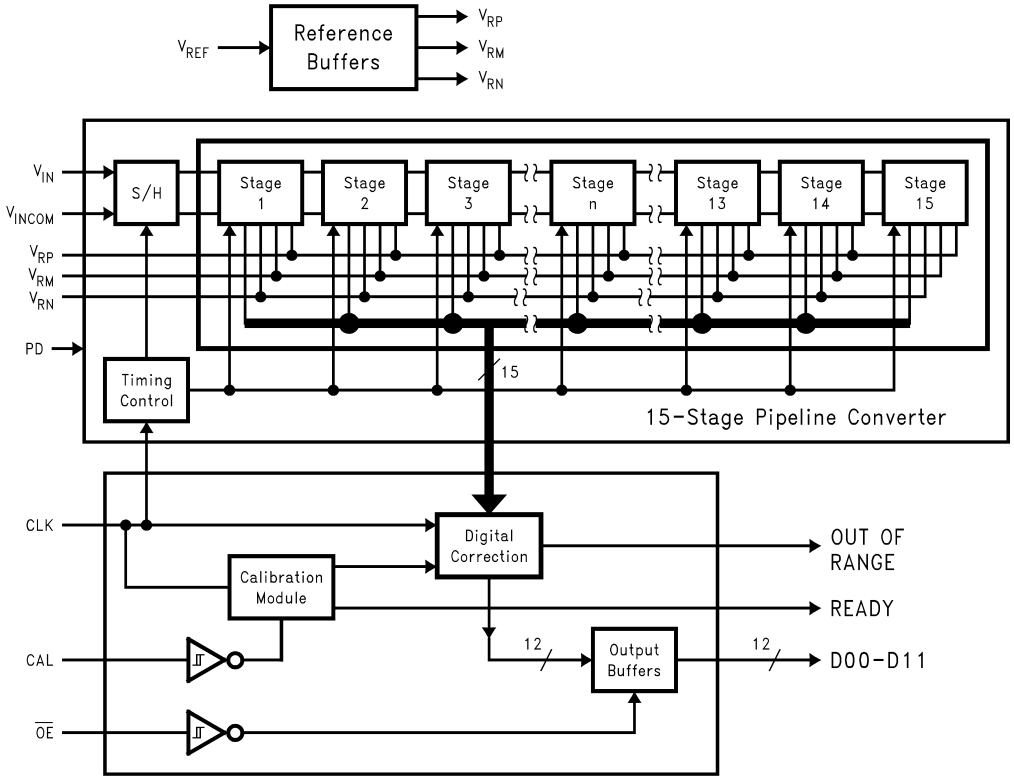
Table 1. Key Specifications

	VALUE	UNIT
Resolution	12	Bits
Conversion Rate	5	Msps (min)
DNL	±0.35	LSB (typ)
SNR	68	dB (typ)
ENOB	10.9	Bits (typ)
Analog Input Range	2	Vpp (min)
Supply Voltage	+5 ±5%	V
Power Consumption, 5 MHz	105	mW (typ)

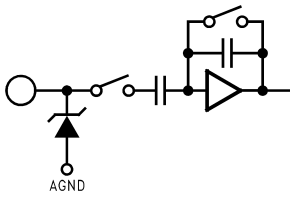
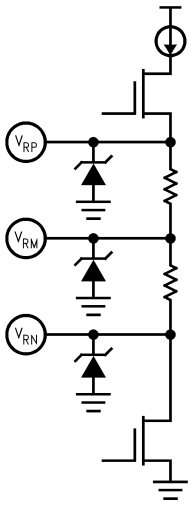
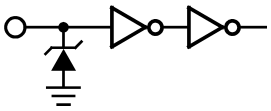
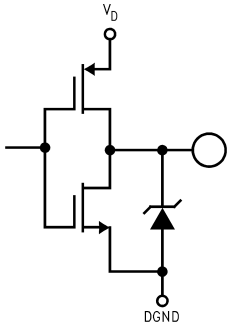
Connection Diagram



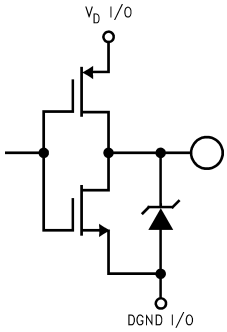
Simplified Block Diagram



PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS #2

No.	Symbol	Equivalent Circuit	Description
2	V_{IN}		Analog signal input. With a 2.0V reference voltage, input signal voltages in the range of 0 to 2.0 Volts will be converted. See Analog Inputs.
1	V_{REF}		Reference voltage input. This pin should be driven from an accurate, stable reference source in the range of 1.8 to 2.2V and bypassed to a low-noise analog ground with a monolithic ceramic capacitor, nominally 0.01µF. See Reference Input.
32	V_{RP}		Positive reference bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See Reference Output Voltages
31	V_{RM}		Reference midpoint bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See Reference Output Voltages
30	V_{RN}		Negative reverence bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. SeeReference Output Voltages
10	CLOCK		Sample Clock input, TTL compatible. Maximum amplitude should not exceed 3V.
8	CAL		Calibration request, active High. Calibration cycle starts when CAL returns to logic low. CAL is ignored during power-down mode. See CAL.
7	PD		Power-down, active High, ignored during calibration cycle. See PD Pin
11	$\overline{OE}$		Output enable control, active low. When this pin is high the data outputs are in Tri-state (high-impedance) mode.
28	OR		Over range indicator. This pin is at a logic High for $V_{IN} < 0$ or for $V_{IN} > V_{REF}$.
29	READY		Device ready indicator, active High. This pin is at a logic Low during a calibration cycle and while the device is in the power down mode.

PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS #2 (continued)

No.	Symbol	Equivalent Circuit	Description
14-19, 22-27	D0 - D11		Digital output word, CMOS compatible. D0 (pin 14) is LSB, D11 (pin 27) is MSB. Load with no more than 50pF.
3	$V_{IN\ com}$		Analog input common. Connect to a quiet point in analog ground near the driving device. See Layout and Grounding.
5	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1µF chip capacitor.
4, 6	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12081 package. See Layout and Grounding.
13	V_D		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1 µF chip capacitor.
9, 12	DGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12081 package. See Layout and Grounding
21	V_D I/O		The digital output driver supply pin. This pin can be operated from a supply voltage of 3V to 5V, but the voltage on this pin should never exceed the V_D supply pin voltage.
20	DGND I/O		The ground return for the output drivers. This pin should be returned to a point in the digital ground that is removed from the other ground pins of the ADC12081.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage		6.5V
Voltage on Any Output		−0.3V to V^+ +0.3V
Input Current at Any Pin(4)		±25mA
Package Input Current(4)		±50mA
Package Dissipation		See(5)
ESD Susceptibility(6)	Human Body Model	1500V
	Machine Model	150V
Soldering Temp., Infrared, 10 sec.(7)		300°C
Storage Temp.		−65°C to +150°C
Maximum Junction Temp.		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A, V_D or V_D I/O), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperatures ($T_J$max) for this device is 150°C. The maximum allowable power consumption is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula P_DMAX = ($T_J$max - T_A)/θ_{JA}. In the 32-pin TQFP, θ_{JA} is 74°C/W, so P_DMAX = 1,689 mW at 25°C and 1,013 mW at the maximum operating ambient temperature of 75°C. Note that the power consumption of this device under normal operation will typically be about 125 mW (typical power consumption + 20 mW TTL output loading). The values for maximum power consumption listed above will be reached only when the ADC12081 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220 pf discharged through ZERO Ohms.
(7) See AN450, "Surface Mounting Methods and Their Effect on Product Reliability", or the section entitled "Surface Mount" found in any post 1986 Texas Instruments Linear Data Book, for other methods of soldering surface mount devices.

Operating Ratings

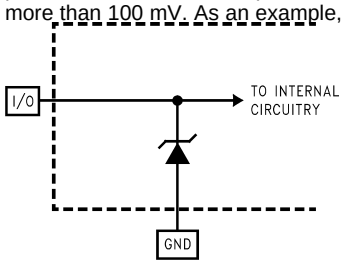
Operating Temp. Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage	+4.75V to +5.25V
V_D I/O	+2.7V to V_D
V_{REF} Input	1.8V to 2.2V
CLOCK, CAL, PD, OE	−0.05V to V_D + 0.05V
|AGND −DGND|	≤100mV

Converter Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, $V_A = V_D = V_D$ I/O = +5V, PD = +5V, V_{REF} = +2.0V, f_{CLK} = 5MHz, C_L = 50 pF/pin. After Auto-Cal at Temperature. **Boldface limits apply for $T_A = T_J$ to T_{MIN} to T_{MAX}:** all other limits $T_A = T_J$ = 25°C(1)(2)(3)

Symbol	Parameter	Conditions		Typical(4)	Limits(5)	Units (Limits)
Static Converter Characteristics						
	Resolution with No Missing Codes				**12**	Bits(min)
INL	Integral Non Linearity(6)			±0.6	**±1.7**	LSB(max)
DNL	Differential Non Linearity			±0.35	**±0.75**	LSB(max)
	Full-Scale Error			±0.05	**±0.1**	%FS(max)
	Zero Error			±0.15	**±0.24**	%FS(max)
Dynamic Converter Characteristics						
BW	Full Power Bandwidth			100		MHz
SNR	Signal-to-Noise Ratio	f_{in} = 2.5 MHz, $V_{IN} = 2.0V_{P-P}$		68	65	dB
SINAD	Signal-to-Noise & Distortion	f_{in} = 2.5 MHz, $V_{IN} = 2.0V_{P-P}$		67.6	64.5	dB
ENOB	Effective Number of Bits	f_{in} = 2.5 MHz, $V_{IN} = 2.0V_{P-P}$		10.9	10.4	Bits
THD	Total Hamonic Distortion	f_{in} = 2.5 MHz, $V_{IN} = 2.0V_{P-P}$		79		dB
SFDR	Spurious Free Dynamic Range	f_{in} = 2.5 MHz, $V_{IN} = 2.0V_{P-P}$		79		dB
Reference and Analog Input Characteristics						
V_{IN}	Input Voltage Range	V_{REF} = 2.0V			**0** **V_{REF}**	V(min) V(max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 1.0Vdc + 0.7Vrms	(CLK LOW)	10		pF
			(CLK HIGH)	15		pF
V_{REF}	Reference Voltage(7)			2.00	**1.8** **2.2**	V(min) V(max)
	Reference Input Leakage Current			10		µA
	Reference Input Resistance			1		MΩ(min)

(1) The inputs are protected as shown below. Input voltage magnitudes up to 5V above V_A or to 5V below GND will not damage this device, provided current is limited per Note 3. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤4.85V to ensure accurate conversions.



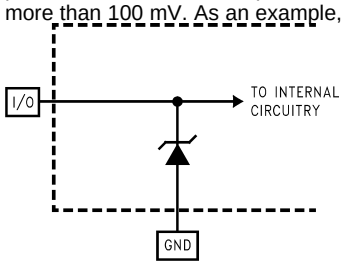
(2) To guarantee accuracy, it is required that $|V_A - V_D| \leq 100mV$ and separate bypassed capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +2.0V, the 12-bit LSB is 488µV.
(4) Typical figures are at $T_A = T_J$ = 25°C, and represent most likely parametric norms.
(5) Tested limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(6) Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scall and zero.
(7) Optimum SNR performance will be obtained by keeping the reference input in the 1.8V to 2.2V range. The LM4041CIM3-ADJ (SOT-23 package), the LM4041CIZ-ADJ (TO-92 package), or the LM4041CIM-ADJ (SOT-8 package) bandgap voltage reference is recommended for this application.

DC and Logic Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V_A = V_D = V_D I/O = +5V, PD = +5V, V_{REF} = +2.0V, f_{CLK} = 50MHz, C_L = 50 pF/pin. After Auto-Cal at Temperature. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C(1)(2)(3)

Symbol	Parameter	Conditions	Typical(4)	Limits(5)	Units (Limits)
CLK, $\overline{OE}$ Digital Input Characteristics					
V_{IH}	Logical "1" Input Voltage	V+ = 5.25V		**2.0**	V(min)
V_{IL}	Logical "0" Input Voltage	V+ = 4.75V		**0.8**	V(min)
I_{IH}	Logical "1" Input Current	V_{IN} = 5.0V	5		µA
I_{IL}	Logical "0" Input Current	V_{IN} = 0V	−5		µA
C_{IN}	V_{IN} Input Capacitance		8		pF
D0 - D11 Digital Output Characteristics(6)					
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −1mA		**4**	V (min)
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6mA		**0.4**	V (max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 3V or 5V	10		µA
		V_{OUT} = 0V	−10		µA
$+I_{SC}$	Output Short Circuit Source Current	VDDO= 3V, V_{OUT} = 0V	−14		mA(min)
$-I_{SC}$	Output Short Circuit Sink Current	VDDO= 3V, V_{OUT} = V_O	16		mA(min)
Power Supply Characteristics					
I_A	Analog Supply Current	PD = VDDO PD = DGND	2.5 20	**4** **26**	mA(max) mA(max)
I_D	Digital Supply Current	PD = VDDO PD = DGND	0.5 1	**2** **2**	mA(max) mA(max)
	Total Power Consumption	PD = VDDO PD = DGND	15 105	**30** **140**	mW(max) mW(max)

(1) The inputs are protected as shown below. Input voltage magnitudes up to 5V above V_A or to 5V below GND will not damage this device, provided current is limited per Note 3. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤4.85V to ensure accurate conversions.



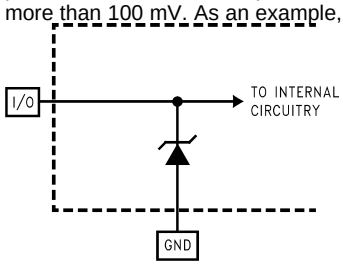
(2) To guarantee accuracy, it is required that $|V_A - V_D|$ ≤ 100mV and separate bypassed capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +2.0V, the 12-bit LSB is 488µV.
(4) Typical figures are at T_A = T_J = 25°C, and represent most likely parametric norms.
(5) Tested limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(6) Timing specifications are tested at the TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

AC Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V_A = V_D = V_D I/O = +5V, PD = +5V, V_{REF} = +2.0V, f_{CLK} = 5 MHz, C_L = 50 pF/pin. After Auto-Cal at Temperature. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C(1)(2)(3)

Symbol	Parameter	Conditions	Typical(3)	Limits(4)	Units (Limits)
f_{CLK}	Clock Frequency		**0.5**		MHz(min)
				5	MHz(max)
	Clock Duty Cycle		50		%
t_{CONV}	Conversion Latency		10.25		Clock Cycles
t_{AD}	Aperture Delay Time		3.5		ns
t_{OD}	Data output delay after rising clk edge	V_D I/O = 3V	44		ns
		V_D I/O = 5V	40		
t_{DIS}	Data outputs into Tristate mode		21		nA (max)
t_{EN}	Data outputs active after Tristate		21		ns (max)
t_{WCAL}	Calibration request pulse width			3	Tclk(min)
t_{RDYC}	Ready Low after CAL request			3	Tclk
t_{CAL}	Calibration cycle			4000	Tclk
t_{WPD}	Power-down pulse width			3	Tclk(min)
t_{RDYPD}	Ready Low after PD request			3	Tclk
t_{PD}	Power down mode exit cycle			4000	Tclk

(1) The inputs are protected as shown below. Input voltage magnitudes up to 5V above V_A or to 5V below GND will not damage this device, provided current is limited per Note 3. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤4.85V to ensure accurate conversions.



(2) To guarantee accuracy, it is required that $|V_A - V_D| \leq 100$mV and separate bypassed capacitors are used at each power supply pin.
(3) Typical figures are at T_A = T_J = 25°C, and represent most likely parametric norms.
(4) Tested limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

Transfer Characteristic

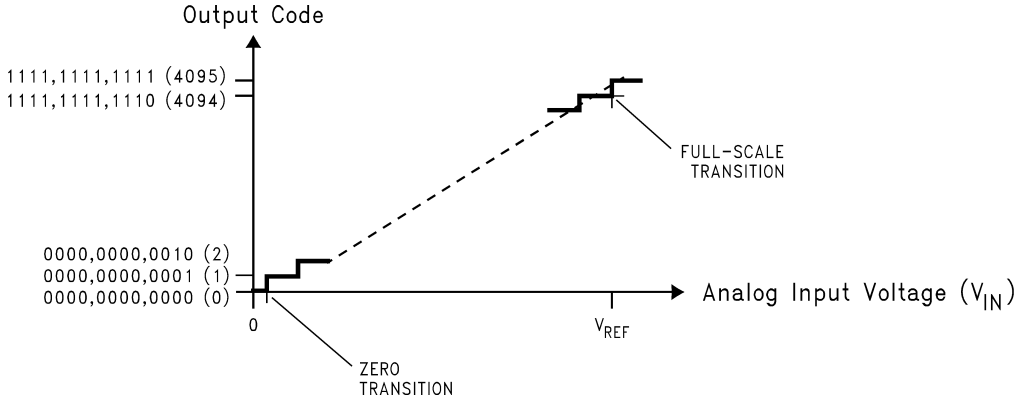


Figure 1. Transfer Characteristic

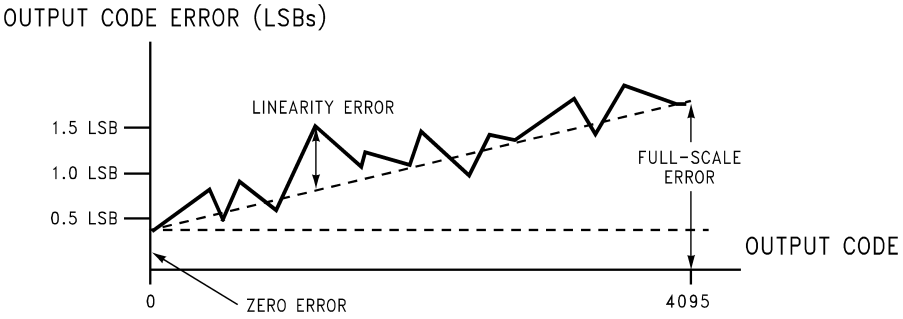


Figure 2. Errors Minimized by the Auto-Cal Cycle

Typical Performance Characteristics

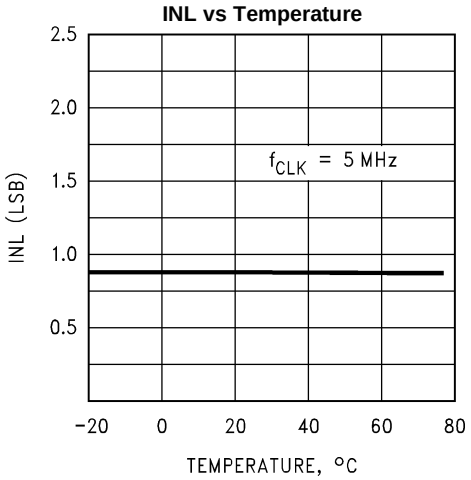


Figure 3.

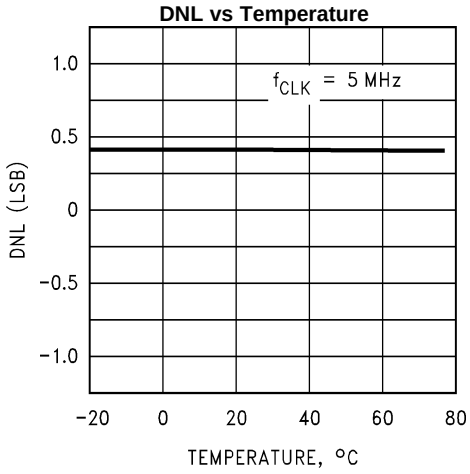


Figure 4.

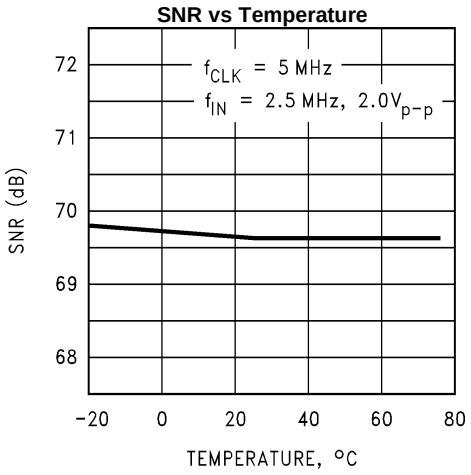


Figure 5.

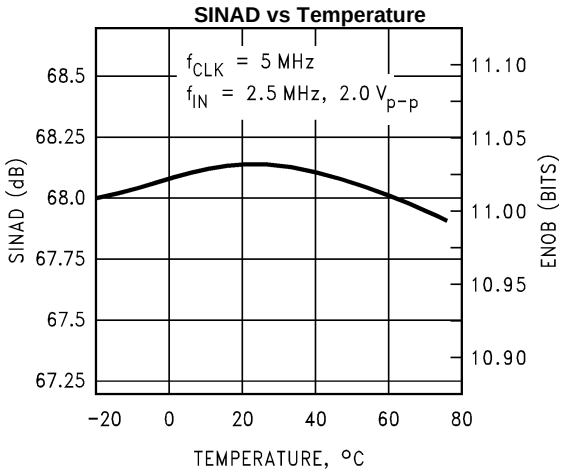


Figure 6.

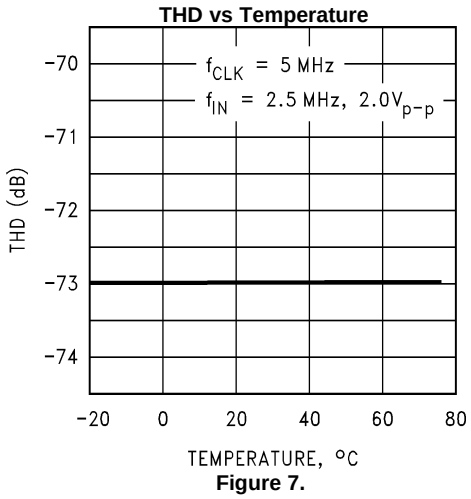


Figure 7.

Specification Definitions

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

APERTURE DELAY See Sampling Delay.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is high to the total time for one clock cycle.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE ERROR is the difference between the input voltage just causing a transition to positive full scale and V_{REF} -1.5 LSB.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (1½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. INL is commonly measured at rated clock frequency with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dB.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and the availability of that conversion result at the output. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay plus the Output Delay.

SAMPLING (APERTURE) DELAY is the time after the edge of the clock to when the input signal is acquired or held for conversion.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SIGNAL TO NOISE RATIO (SNR) is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency, not including harmonics or dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first six harmonic components, to the rms value of the input signal.

ZERO SCALE OFFSET ERROR is the difference between the ideal input voltage (½ LSB) and the actual input voltage that just causes a transition from an output code of zero to an output code of one.

ZERO ERROR see Zero Scale Offset Error.

TEST CIRCUIT DIAGRAMS

Timing Diagrams

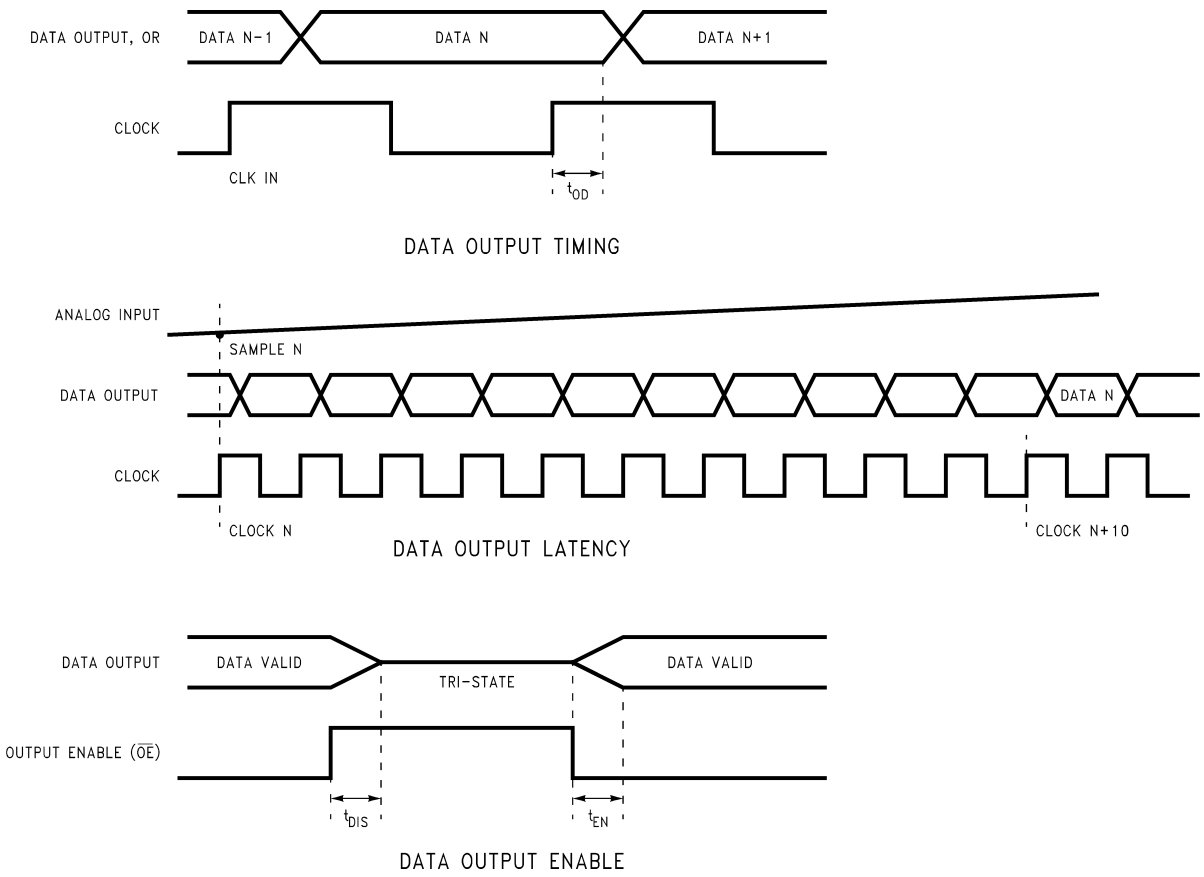


Figure 8. Data Output Timing

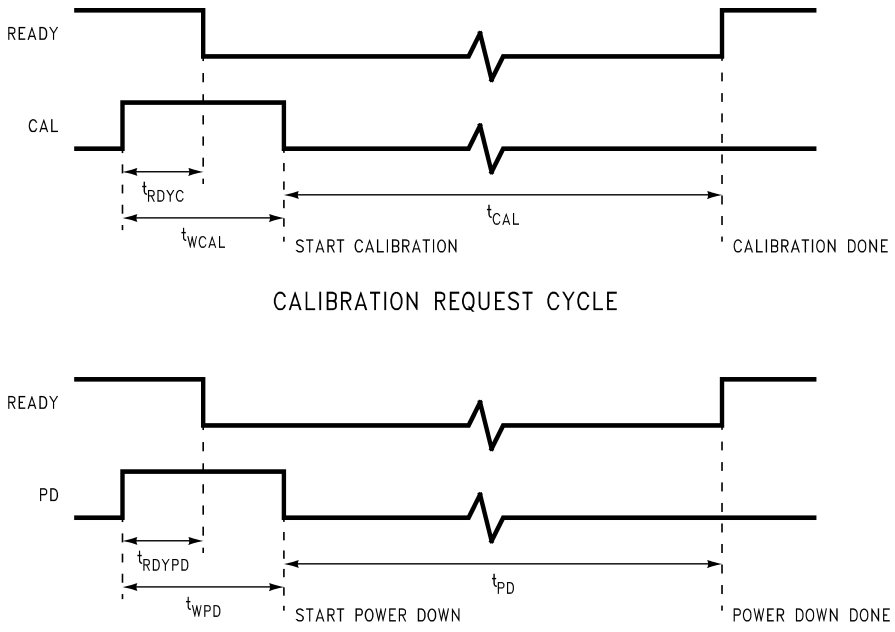


Figure 9. Reset and Calibration Timing

FUNCTIONAL DESCRIPTION

The ADC12081 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 5 megasamples per second (MSPS). This device utilizes a proprietary pipeline architecture and algorithm to minimize die size and power consumption. The ADC12081 uses self-calibration and digital error correction to maintain accuracy and performance over temperature. The ADC12081 has an input sample-and-hold amplifier and internal reference buffer. The analog input and the reference voltage are converted to differential signals for internal use. Using differential signals in the analog conversion core reduces crosstalk and noise pickup from the digital section and power supply.

The pipeline conversion core has 15 sequential signal processing stages. Each stage receives an analog signal from the previous stage (called “residue”) and produces a 1-bit digital output that is sent to the digital correction module. At each stage the analog signal received from the previous stage is compared to an internally generated reference level. It is then amplified by a factor of 2, and, depending on the output of the comparator, the internal reference signal may be subtracted from the amplifier output. This produces the residue that is passed to the next stage.

The calibration module is activated at power-on or by user request. During calibration the conversion core is put into a special mode of operation in order to determine inherent errors in the analog conversion blocks and to determine correction coefficients for each digital output bit from the conversion core and stores these coefficients in RAM. The digital correction module uses the coefficients in RAM to convert the raw data bits from the conversion core into the 12-bit digital output code.

Applications Information

ANALOG INPUTS

The ADC12081 has two single-ended analog inputs. V_{REF} is the reference input and V_{IN} is the signal input.

Reference Input

The V_{REF} input must be driven from an accurate, stable reference voltage source. of 1.8V to 2.2V, and bypassed to a clean, quiet point in analog ground.

Analog Signal Input

The V_{IN} input must be driven with a low impedance signal source that does not add any distortion to the input signal. The ground reference for the V_{IN} input is the V_{INCOM} pin. The V_{INCOM} pin must be connected to a clean, quiet point in analog ground.

DIGITAL INPUTS

The ADC12081 has four digital inputs. They are CLOCK, CAL, $\overline{OE}$ and PD.

CLOCK

The CLOCK signal drives an internal phase delay loop to create timing for the ADC. The clock input should be driven with a stable, low phase jitter TTL level clock signal in the range of 0.5 to 5 MHz. The trace carrying the clock signal should be as short as possible. This trace should not cross any other signal line, analog or digital, not even at 90°. A 100 Ohm resistor should be placed in series with the CLOCK pin, as close to the pin as possible.

CAL

The level sensitive CAL input must be pulsed high for at least three clock cycles to begin ADC calibration. For best performance, calibration should be performed about ten seconds after power up, after resetting the ADC, and after the temperature has changed by more than 50°C since the last calibration was performed.

Calibration should be performed at the same clock frequency that the ADC12081 will be used for conversions to minimize offset errors. Calibration takes 4000 clock cycles. **Irrelevant data may appear during CAL.**

$\overline{OE}$ Pin

The $\overline{OE}$ pin is used to control the state of the outputs. When the $\overline{OE}$ pin is low, the output buffers go into the active state. When the $\overline{OE}$ input is high, the output buffers are in the high impedance state.

PD Pin

The PD pin, when high, holds the ADC12081 in a power-down mode where power consumption is typically less than 15 mW to conserve power when the converter is not being used. The ADC12081 will begin normal operation within t_{PD} after this pin is brought low, provided a valid CLOCK input is present. The data in the pipeline is corrupted while in the power down mode. The ADC12081 should be re-calibrated after a power-down cycle to ensure optimum performance.

OUTPUTS

The ADC12081 has three analog outputs: reference output voltages V_{RN}, V_{RM} , and V_{RP}. There are 14 digital outputs: 12 Data Output pins, Ready and OR (Out of range).

Reference Output Voltages

The reference output voltages are made available only for the purpose of bypassing with capacitors to a clean analog ground. The recommended bypass capacitors are 0.1µF ceramic chip capacitors. Do not load these pins.

Ready Output

The Ready output goes high to indicate that the converter is ready for operation. This signal will go low when the converter is Calibration or Power Down made.

OR (Out of Range) Output

The OR output goes high when the analog input is below GND or above V_{REF}. This output is low when the input signal is in the valid range of operation ($0V \le V_{IN} \le V_{REF}$).

Data Outputs

The Data Outputs are TTL/CMOS compatible. The output data format is 12 bits straight binary.

Minimizing the digital output currents will help to minimize noise due to output switching. This can be done by connecting buffers between the ADC outputs and any other circuitry. Only one buffer input should be connected to each output. Additionally, inserting series resistors of 47 to 56 Ohms right at the digital outputs, close to the ADC pins, will isolate the outputs from other circuitry and limit output currents.

POWER SUPPLY CONSIDERATIONS

Each power pin should be bypassed with a parallel combination of a 10µF capacitor and a 0.1µF ceramic chip capacitor. The chip capacitors should be within 1/2 centimeter of the power pins. Leadless chip capacitors are preferred because they provide low lead inductance.

The converter's digital logic supply (V_D) should be well isolated from the supply that is used for other digital circuitry on the board. A common power supply should be used for both V_A (analog supply) and V_D (digital supply), and each of these supply pins should be separately bypassed with a 0.1µF ceramic capacitor and a low ESR 10µF electrolytic capacitor. A ferrite bead or inductor should be used between V_A and V_D to prevent noise coupling from the digital supply into the analog circuit.

V_D I/O is the power pin for the output driver. This pin may be supplied with a potential between 2.7V and V_D. This makes it easy to interface the ADC12081 with 3V or 5V logic families. Powering the V_D I/O from 3 Volts will also reduce power consumption and noise generation due to output switching. **DO NOT operate the V_D I/O at a voltage higher than V_D or V_A!** All power supplies connected to the device should be applied simultaneously.

As is the case with all high speed converters, the ADC12081 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be minimized, keeping it below 100mV P-P.

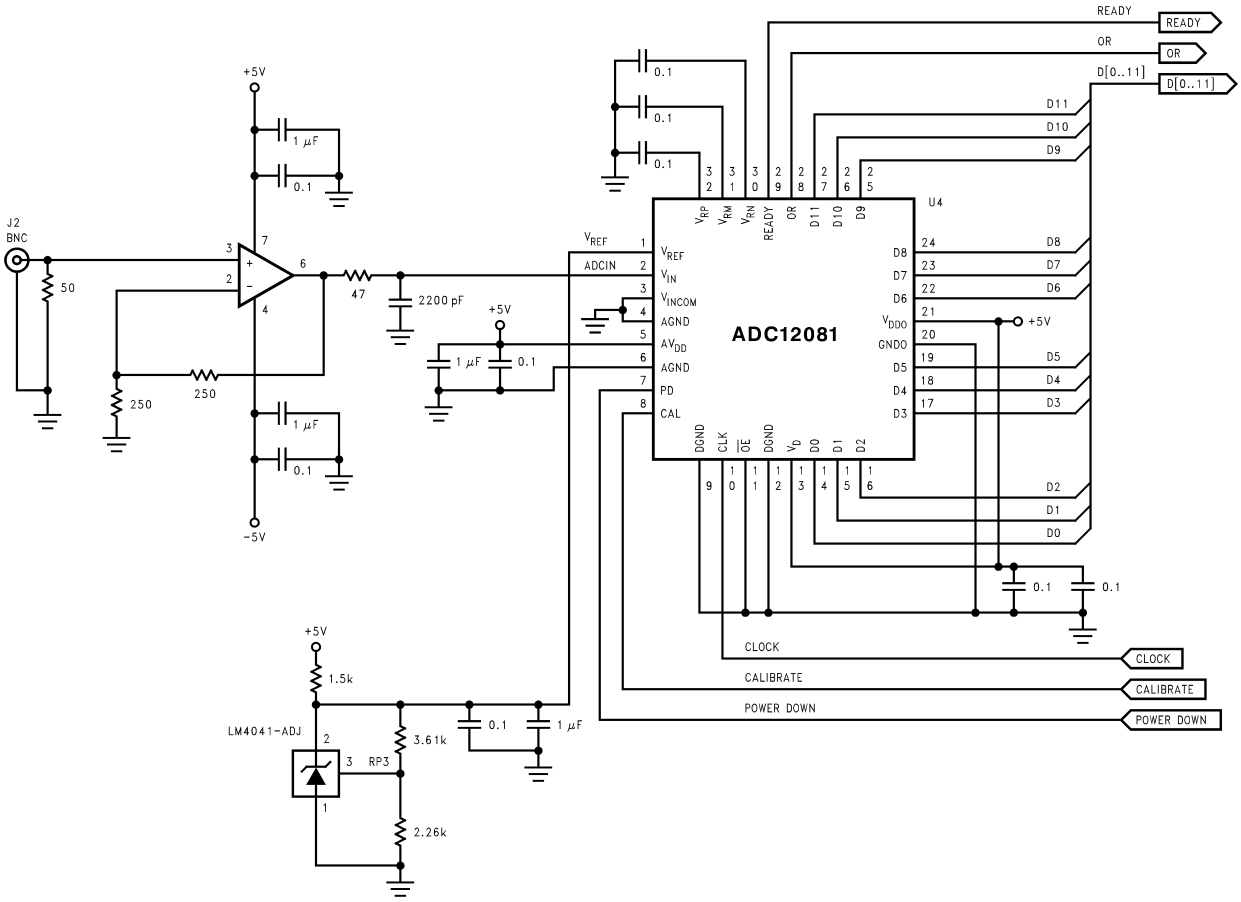


Figure 10. Basic Connections Diagram

LAYOUT AND GROUNDING

Proper grounding and routing of all signals is essential to ensure accurate conversion. Separate analog and digital ground planes that are connected beneath the ADC12081 are required to achieve specified performance. The analog and digital grounds may be in the same layer, but should be separated from each other and should never overlap each other. Separation should be at least 1/8 inch, where possible.

The ground return for the output buffer digital supply (DGND I/O) carries the ground current for the output drivers. This pin should be connected to the system digital ground. The current on this pin can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DGND I/O pin should NOT be connected in close proximity to any of the ADC12081's other ground pins. See Figure 11.

Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry separated from the digital circuitry and from the digital ground plane.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74 AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by connecting the analog and digital ground planes together beneath the ADC with a copper trace that is very narrow compared with the rest of the ground plane. This narrowing beneath the converter provides a fairly high impedance to the high frequency components of the digital switching currents, directing them away from the analog pins. The relatively lower frequency analog ground currents do not create a significant voltage drop across the impedance of this narrow ground connection.

To maximize accuracy in high speed, high resolution systems, avoid crossing analog and digital signal traces. It is important to keep any clock lines isolated from ALL other lines. Even the generally accepted 90 degree crossing should be avoided as even a little coupling can cause problems at high frequencies. This is because other lines can introduce phase noise (jitter) into the clock line, which can lead to degradation of SNR.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane.

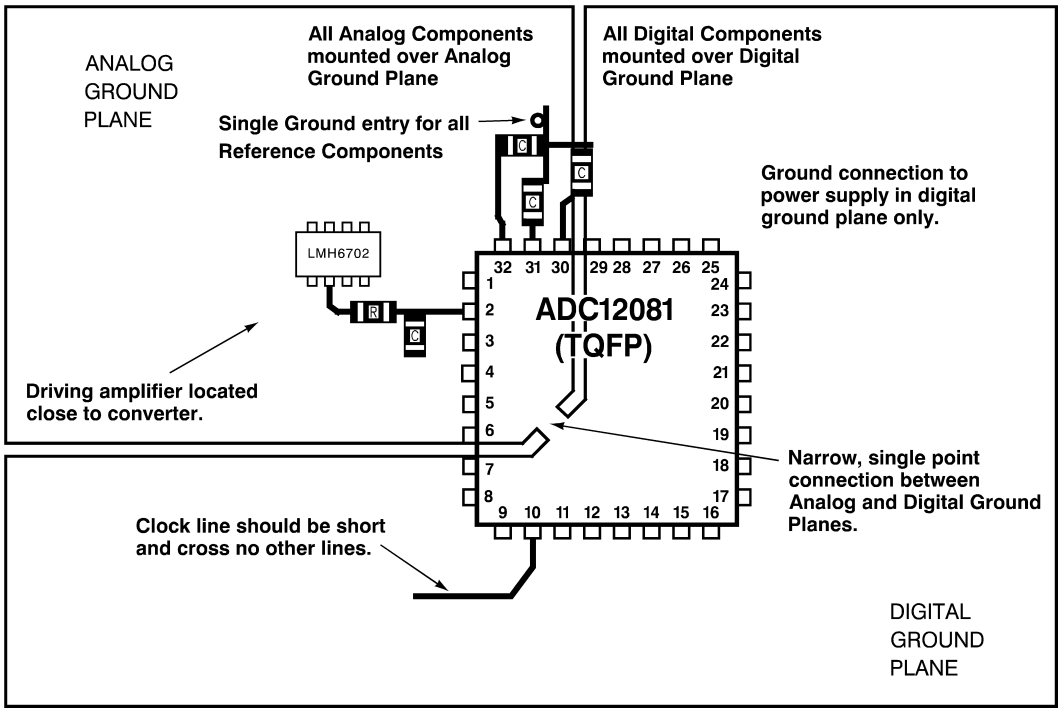


Figure 11. Layout example

Figure 11 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed on or over the analog ground plane. All digital circuitry and I/O lines should be placed over the digital ground plane.

All ground connections should have a low inductance path to ground.

LAYOUT AND GROUNDING

The ADC12081 can achieve impressive dynamic performance. To achieve the best dynamic performance with the ADC12081, the clock source driving the CLK input must be free of jitter. For best ac performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 12.

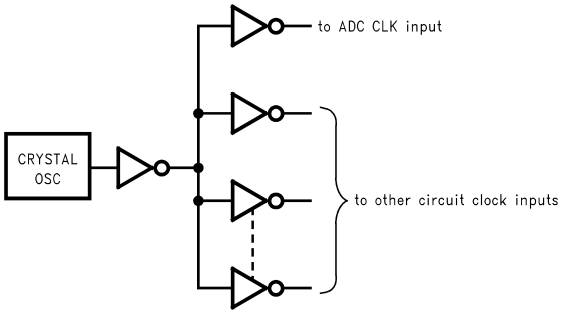


Figure 12. Isolating the ADC clock from other circuitry with a clock tree.

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce phase noise (jitter) into the clock signal, which can lead to increased distortion. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300mV beyond the supply rails (more than 300mV below the ground pins or 300mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground above the power supply. A resistor of about 50 to 100Ω in series with the offending digital input will eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC12081 with a device that is powered from supplies outside the range of the ADC12081 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. Capacitive loading on the digital outputs causes instantaneous digital currents to flow from the V_D I/O supply into the DGND I/O ground plane. These large charging current spikes can couple into the analog section, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem. The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12081, reducing the energy coupled back into the converter output pins by limiting the output slew rate. A reasonable value for these resistors is 47Ω.

Using an inadequate amplifier to drive the analog input. The analog input circuits of the ADC12081 place a switched capacitor load on the input signal source. Therefore the amplifier used to drive the ADC12081 must have a low impedance output and adequate bandwidth to avoid distortion of the input signal.

Operating with the reference pins outside of the specified range. As mentioned in Analog Inputs, V_{REF} should be in the range of $1.8V \le V_{REF} \le 2.2V$. Operating outside of these limits could lead to signal distortion.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC12081CIVT/NOPB	ACTIVE	LQFP	NEY	32	250	RoHS & Green	SN	Level-3-260C-168 HR	-20 to 75	ADC12081 CIVT	Samples
ADC12081CIVTX/NOPB	ACTIVE	LQFP	NEY	32	1000	RoHS & Green	SN	Level-3-260C-168 HR	-20 to 75	ADC12081 CIVT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

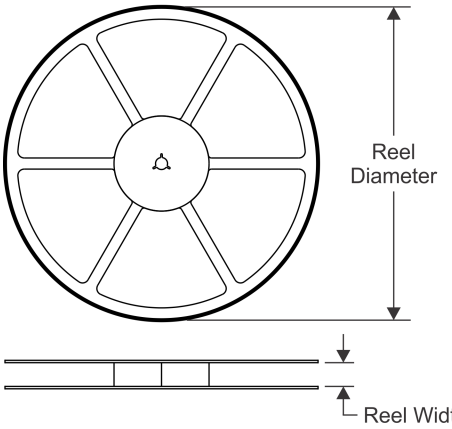
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

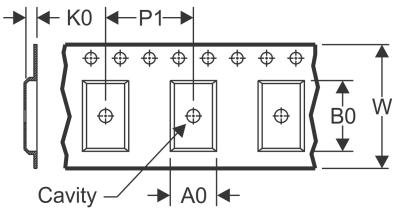
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

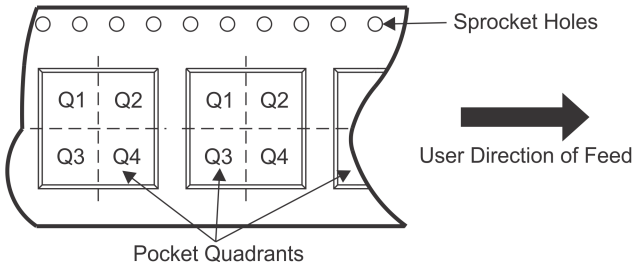


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

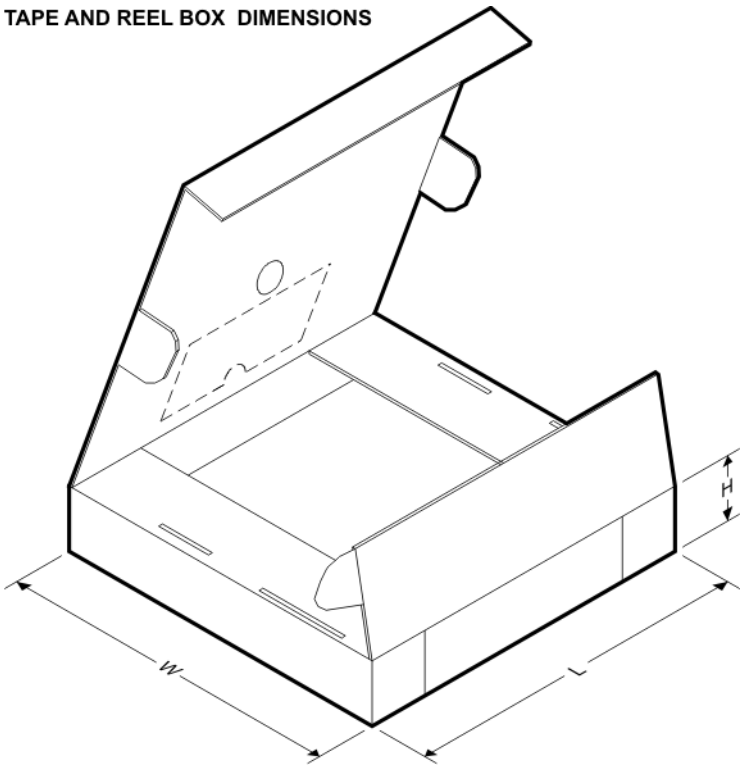
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

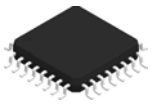
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC12081CIVTX/NOPB	LQFP	NEY	32	1000	330.0	16.4	9.3	9.3	2.2	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC12081CIVTX/NOPB	LQFP	NEY	32	1000	367.0	367.0	38.0

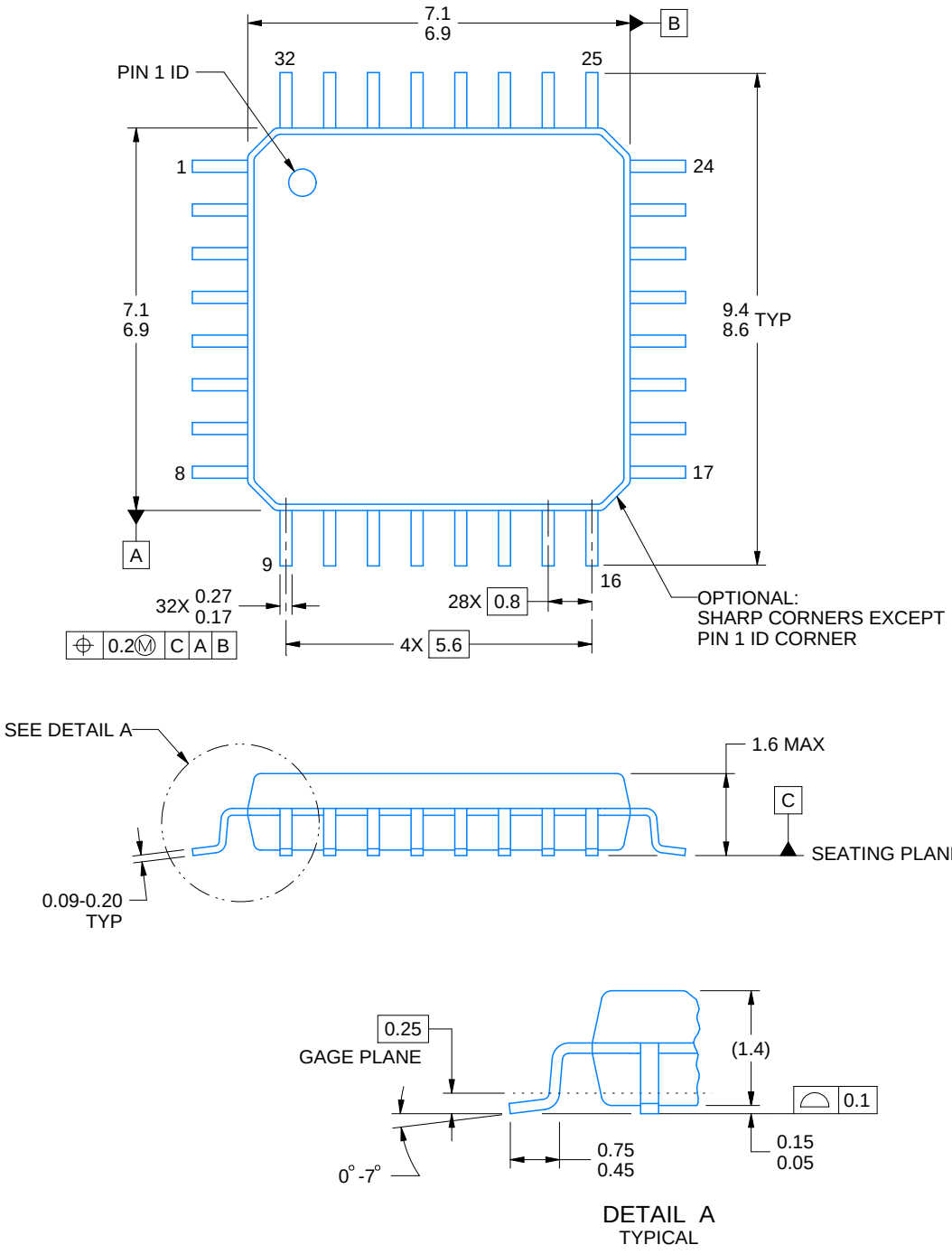


PACKAGE OUTLINE

NEY0032A

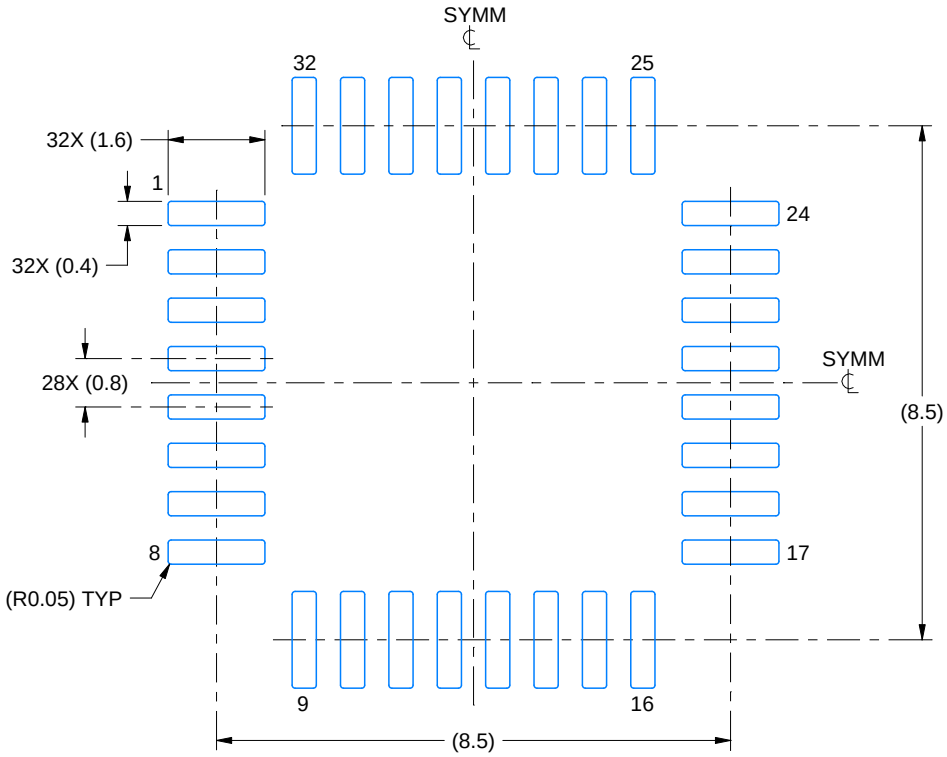
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

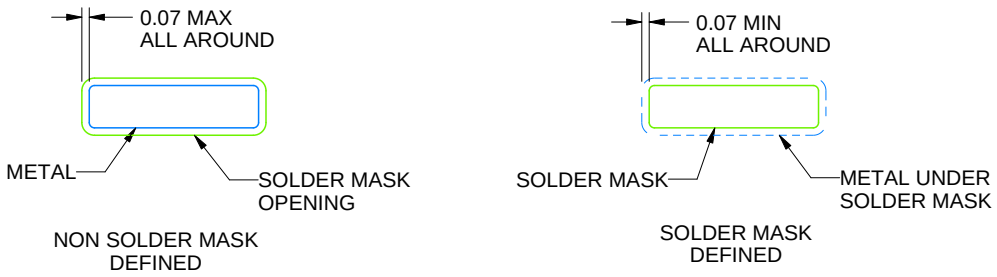


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4219901/A 10/2016

NOTES: (continued)

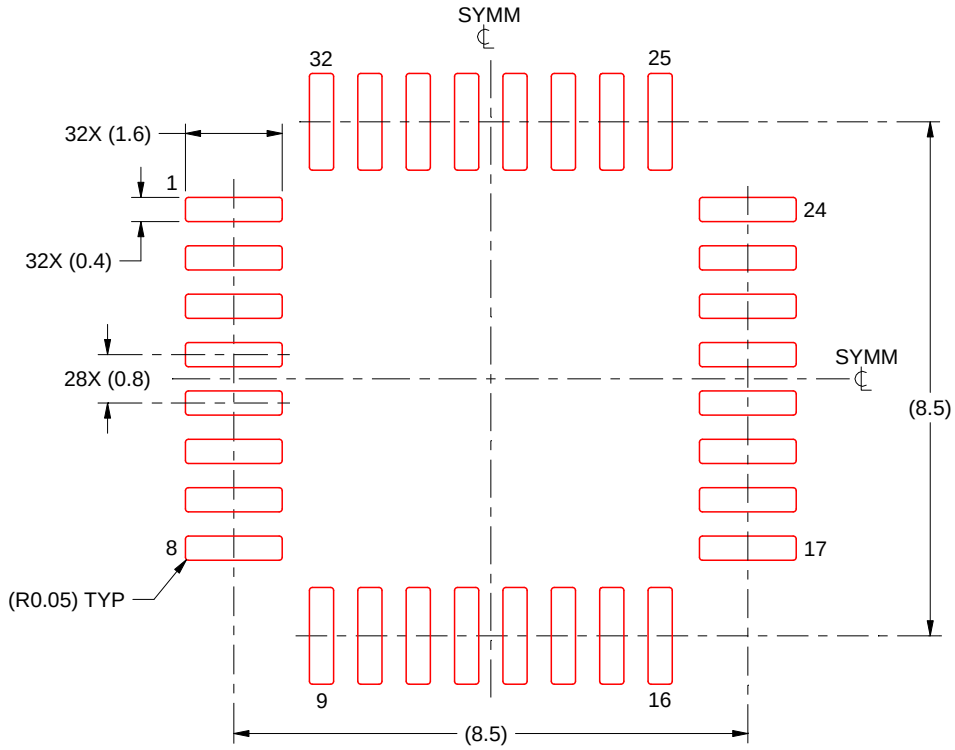
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE 8X

4219901/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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