适用于 **4-20mA** 电流回路应用的 **DACx750** 单通道、**12** 位和 **16** 位可编程电流输出 数模 转换器

1 特性

- 电流输出选项：
  - 0mA 至 24mA
  - 4mA 至 20mA
  - 0mA 至 20mA
- ±0.1% 满量程范围 (FSR) 典型总体非调整误差 (TUE)
- 微分非线性 (DNL)：±1 最低有效位 (LSB)（最大值）
- 最大环路合规电压：AVDD - 2V
- 内部 5V 基准电压：10ppm/°C（最大值）
- 内部 4.6V 电源输出
- 循环冗余校验 (CRC) 帧错误校验
- 看门狗定时器
- 过热警报
- 开路警报
- 监控输出电流的端子
- 片上故障警报
- 针对偏移和增益的用户校准
- 宽温度范围：-40°C 至 125°C
- 6mm × 6mm 40 引脚超薄四方扁平无引线 (VQFN) 封装和 24 引脚散热薄型小外形尺寸封装 (HTSSOP)

2 应用

- 4mA 至 20mA 电流环路
- 模拟输出模块
- 楼宇自动化
- 环境监视
- 可编程逻辑控制器 (PLC)
- 场传感器和过程发射器

3 说明

DAC7750 和 DAC8750 为低成本、高精度、全集成 12 位和 16 位数模转换器 (DAC)，设计用于满足工业过程控制应用 的要求。这些器件经编程可提供范围介于 4mA 至 20mA、0mA 至 20mA 或 0mA 至 24mA 的电流输出。DAC7750 和 DAC8750 包含可靠 功能， 例如串行外设接口 （SPI™) 数据帧的 CRC 错误校验、一个看门狗定时器、一个开路、依从电压和过热警报。此外，可通过访问一个内部高精度电阻器来监控输出电流。

这些器件包括一个加电复位功能，以确保器件在已知状态中加电（IOUT 被禁用并且处于高阻抗 (Hi-Z) 状态）。如果输出被启用，CLR 端子将电流输出设定在范围的低端限度。对零和增益寄存器进行编程，以便对终端系统内的器件进行数字校准。输出转换率也由寄存器设定。这些器件可在电流输出上添加一个外部 HART®信号，可通过 10V 至 36V 电源供电。

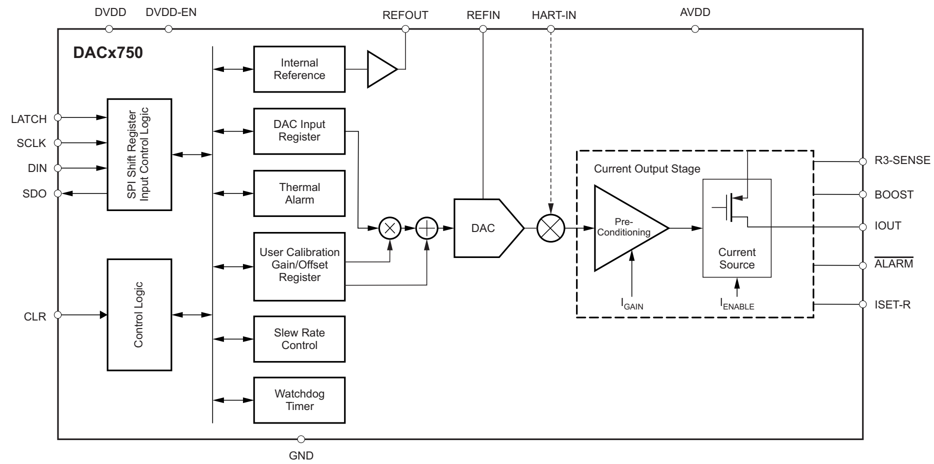
所有版本都提供 40 引脚 VQFN 封装和 24 引脚薄型小外形尺寸 (TSSOP) 封装。

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DACx750	带散热片薄型小外形尺寸封装 (HTSSOP) (24)	7.80mm × 4.40mm
	VQFN (40)	6.00mm × 6.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

框图


DVDD
DVDD-EN
REFOUT
REFIN
HART-IN
AVDD
DACx750
Internal Reference
DAC Input Register
Thermal Alarm
User Calibration Gain/Offset Register
Slew Rate Control
Watchdog Timer
SPI Shift Register Input Control Logic
Control Logic
LATCH
SCLK
DIN
SDO
CLR
DAC
Current Output Stage
Pre-Conditioning
Current Source
I_GAIN
I_ENABLE
R3-SENSE
BOOST
IOUT
ALARM
ISET-R
GND

目录

4 修订历史记录

Changes from Revision B (June 2016) to Revision C — **Page**

- Changed description of *Power-Supply Sequence* section 23
- Added *The DACx750 Shares the SPI Bus With Other Devices* section 25
- Added first sentence to second paragraph and added last paragraph to *Frame Error Checking* section 26
- Added *The DACx750 Shares the SPI Bus With Other Devices* section 27
- Added last paragraph to *User Calibration* section 28
- Added last paragraph to *Programmable Slew Rate* section 30

Changes from Revision A (March 2012) to Revision B — **Page**

- 已添加 *ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* 1
- Added I/O column to *Pin Functions* table 5
- Moved *Thermal Considerations* from *Power Supply Recommendations* to *Layout* 44

Changes from Original (December 2013) to Revision A — **Page**

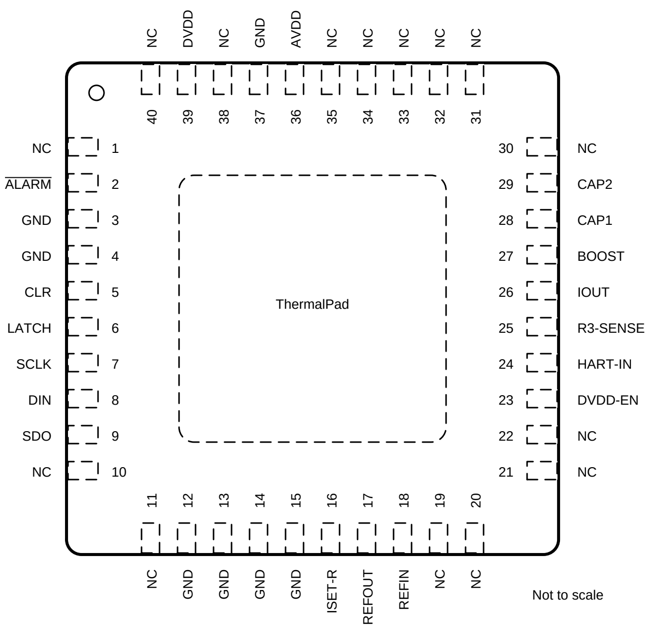
- 已将格式更改为符合最新的数据表标准；已添加新部分并移动现有部分 1
- 已将数据表从 1 页产品预览更改为完整生产数据 1
- Updated Layout Schematic 43

5 Device Comparison Table

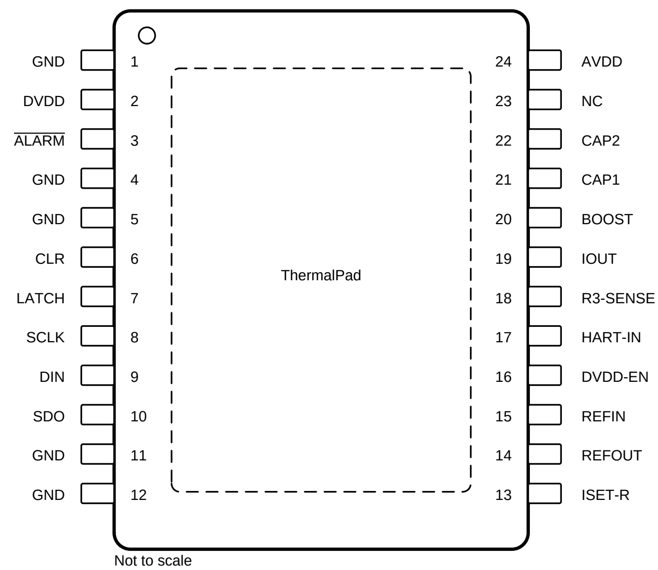
PRODUCT	RESOLUTION	TUE (FSR)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE
DAC8750	16	0.2%	±1	–40°C to 125°C
DAC7750	12	0.2%	±1	–40°C to 125°C

6 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



PWP Package
24-Pin HTSSOP
Top View



NOTE: Thermal pad is connected to ground.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	VQFN	HTSSOP		
$\overline{\text{ALARM}}$	2	3	Digital output	Alarm terminal. Open drain output. External pull-up resistor required (10 kΩ). The terminal goes low (active) when the $\overline{\text{ALARM}}$ condition is detected (open circuit/over temperature/timeout, and so forth).
AVDD	36	24	Supply input	Positive analog power supply.
BOOST	27	20	Analog output	Boost terminal. External transistor connection (optional).
CAP1	28	21	Analog input	Connection for output filtering capacitor (optional).
CAP2	29	22	Analog input	Connection for output filtering capacitor (optional).
CLR	5	6	Digital input	Clear input. Logic high on this terminal causes the part to enter CLEAR state. Active high.
DIN	8	9	Digital input	Serial data input. Data are clocked into the 24-bit input shift register on the rising edge of the serial clock input. Schmitt-Trigger logic input.
DVDD	39	2	Supply input or output	Digital power supply. Can be input or output, depending on DVDD-EN terminal.
DVDD-EN	23	16	Digital input	Internal power-supply enable terminal. Connect this terminal to GND to disable the internal supply, or leave this terminal unconnected to enable the internal supply. When this terminal is connected to GND, an external supply must be connected to the DVDD terminal.
GND	12, 13, 14, 15, 37	1, 11, 12	Supply input	Ground reference point for all analog circuitry of the device.
GND	3, 4	4, 5	Supply input	Ground reference point for all digital circuitry of the device.
HART-IN	24	17	Analog input	Input terminal for HART modulation.
IOUT	26	19	Analog output	Current output terminal
ISET-R	16	13	Analog input	Connection terminal for external precision resistor (15 kΩ). See *Detailed Description* of this data sheet.
LATCH	6	7	Digital input	Load DAC registers input. A rising edge on this terminal loads the input shift register data into the DAC data and control registers and updates the DAC output.
NC	1, 10, 11, 19, 20, 21, 22, 30, 31, 32, 33, 34, 35, 38, 40	23	—	No connection.
R3-SENSE	25	18	Analog output	This terminal is used as a monitoring feature for the output current. The voltage measured between the R3-SENSE terminal and the BOOST terminal is directly proportional to the output current.
REFOUT	17	14	Analog output	Internal reference output. Connects to REFIN when using internal reference.
REFIN	18	15	Analog input	Reference input
SCLK	7	8	Digital input	Serial clock input of the SPI. Data can be transferred at rates up to 30 MHz. Schmitt-Trigger logic input.
SDO	9	10	Digital output	Serial data output. Data are valid on the rising edge of SCLK.
Thermal Pad	—	—	Supply input	The thermal pad is internally connected to GND. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance. The pad can be electrically connected to the same potential as the GND terminal or left electrically unconnected provided a supply connection is made at the GND terminal.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	40	V
DVDD to GND	–0.3	6	V
IOUT to GND	–0.3	AVDD	V
REFIN to GND	–0.3	6	V
REFOUT to GND	–0.3	6	V
$\overline{\text{ALARM}}$ to GND	–0.3	6	V
Digital input voltage to GND	–0.3	DVDD + 0.3	V
SDO to GND	–0.3	DVDD + 0.3	V
Current into REFOUT		10	mA
Operating temperature	–40	125	°C
Junction temperature, T_J max		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge(1)	Human body model (HBM) ESD stress voltage(2)	±3000	V
		Charged device model (CDM) ESD stress voltage(3)	±1000	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AVDD		10		36	V
DVDD		2.7		5.5	V
Loop compliance voltage		4.95		5.05	V
Reference input voltage			30		µA
Loop compliance voltage (output = 24 mA)(1)				AVDD – 2	V
VIH, Digital input high voltage		2			V
VIL, Digital Input low voltage	3.6 V < AVDD < 5.5 V			0.8	V
	2.7 V < AVDD < 2.6 V			0.6	
Specified performance temperature		–40		125	°C

(1) Loop compliance voltage is defined as the voltage at the IOUT pin

7.4 Thermal Information

THERMAL METRIC[(1)]		DAC7750, DAC8750		UNIT
		RHA (VQFN)	PWP (HTSSOP)	
		40 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	32.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.2	14.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	12	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	0.63	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

At AVDD = 10 V to 36 V, GND = 0 V, REFIN = 5 V external, DVDD = 2.7 V to 5.5 V, and all specifications are from –40°C to 125°C (unless otherwise noted). For IOUT, R_L = 300 Ω. Typical specifications are at 25°C.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT OUTPUT						
Current output			0		24	mA
			0		20	
			4		20	
Resolution	DAC8750		16			Bits
	DAC7750		12			
CURRENT OUTPUT ACCURACY (0 mA TO 20 mA AND 0 mA TO 24 mA)[(1)]						
Total unadjusted error, TUE	T_A = –40°C to 125°C		–0.2%		0.2%	FSR
	T_A = –40°C to 85°C		–0.16%		0.16%	
	T_A = 25°C		–0.08%	±0.02%	0.08%	
Differential nonlinearity, DNL	Monotonic				±1	LSB
Relative accuracy, INL[(2)]	T_A = –40°C to 125°C				±0.08%	FSR
	T_A = –40°C to 85°C				±0.024%	
Offset error	T_A = –40°C to 125°C		–0.17%		0.17%	FSR
	T_A = –40°C to 85°C		–0.1%		0.1%	
	T_A = 25°C		–0.07%	±0.01%	0.07%	
Offset error temperature coefficient				±5		ppm FSR/°C
Full-scale error	T_A = –40°C to 125°C		–0.2%		0.2%	FSR
	T_A = –40°C to 85°C		–0.16%		0.16%	
	T_A = 25°C		–0.08%	±0.015%	0.08%	
Full-scale error temperature coefficient	Internal R_{SET}			±5		ppm FSR/°C
	External R_{SET}			±10		
Gain error	Internal R_{SET}	T_A = –40°C to 125°C	–0.2%		0.2%	FSR
		T_A = –40°C to 85°C	–0.15%		0.15%	
		T_A = 25°C	–0.08%	±0.01%	0.08%	
	External R_{SET}	T_A = –40°C to 125°C	–0.17%		0.17%	
		T_A = –40°C to 85°C	–0.12%		0.12%	
		T_A = 25°C	–0.05%	±0.01%	0.05%	
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		
Output current drift vs time	T_A = 125°C, 1000 hrs	Internal R_{SET}		±50		ppm FSR
		External R_{SET}		±25		

(1) DAC8750 and DAC7750 current output range is set by writing to RANGE bits in control register at address 0x55.
(2) For 0-mA to 20-mA and 0-mA to 24-mA ranges, INL is calculated beginning from code 0x0100 for DAC8750 and from code 0x0010 for DAC7750.

Electrical Characteristics (continued)

At AVDD = 10 V to 36 V, GND = 0 V, REFIN = 5 V external, DVDD = 2.7 V to 5.5 V, and all specifications are from –40°C to 125°C (unless otherwise noted). For IOUT, R_L = 300 Ω. Typical specifications are at 25°C.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT OUTPUT ACCURACY (4 mA TO 20 mA)(1)						
Total unadjusted error, TUE	Internal R_{SET}	T_A = –40°C to 125°C	–0.25%		0.25%	FSR
		T_A = 25°C	–0.08%	±0.02%	0.08%	
	External R_{SET}	T_A = –40°C to 125°C	–0.29%		0.29%	
		T_A = –40°C to 85°C	–0.25%		0.25%	
		T_A = 25°C	–0.1%	±0.02%	0.1%	
Differential nonlinearity, DNL	Monotonic				±1	LSB
Relative accuracy, INL(2)	T_A = –40°C to 125°C				±0.08%	FSR
	T_A = –40°C to 85°C				±0.024%	
Offset error	Internal R_{SET}	T_A = –40°C to 125°C	–0.22%		0.22%	FSR
		T_A = –40°C to 85°C	–0.2%		0.2%	
	External R_{SET}	T_A = –40°C to 125°C	–0.2%		0.2%	
		T_A = –40°C to 85°C	–0.18%		0.18%	
	Internal and external R_{SET}, T_A = 25°C		–0.07%	±0.01%	0.07%	
Offset error temperature coefficient				±3		ppm FSR/°C
Full-scale error	Internal R_{SET}	T_A = –40°C to 125°C	–0.25%		0.25%	FSR
		T_A = 25°C	–0 .08%	±0.015%	0.08%	
	External R_{SET}	T_A = –40°C to 125°C	–0.29%		0.29%	
		T_A = –40°C to 85°C	–0.25%		0.25%	
		T_A = 25°C	–0 .1%	±0.015%	0.1%	
Full-scale error temperature coefficient	Internal R_{SET}			±5		ppm FSR/°C
	External R_{SET}			±10		
Gain error	Internal R_{SET}	T_A = –40°C to 125°C	–0.2%		0.2%	FSR
		T_A = –40°C to 85°C	–0.15%		0.15%	
		T_A = 25°C	–0.08%	±0.01%	0.08%	
	External R_{SET}	T_A = –40°C to 125°C	–0.16%		0.16%	
		T_A = –40°C to 85°C	–0.12%		0.12%	
		T_A = 25°C	–0.05%	±0.01%	0.05%	
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		
Output current drift vs time	T_A = 125°C, 1000 hrs	Internal R_{SET}		±50		ppm FSR
		External R_{SET}		±75		
CURRENT OUTPUT STAGE(3)						
Loop compliance voltage(4)	Output = 24 mA				AVDD – 2	V
Inductive load(5)				50		mH
DC PSRR					1	μA/V
Output impedance	Code = 0x8000			50		MΩ
R3 RESISTOR						
R3 resistor value			36	40	44	Ω
R3 resistor temperature coefficient				40		ppm/°C
EXTERNAL REFERENCE INPUT						
Reference input voltage			4.95	5	5.05	V
External reference current	REFIN = 5.0 V			30		μA
Reference input capacitance				10		pF

(3) Specified by design and characterization; not production tested.
(4) Loop compliance voltage is defined as the voltage at the IOUT terminal.
(5) For stability, use slew rate limit feature or add a capacitor between IOUT and GND

Electrical Characteristics (continued)

At AVDD = 10 V to 36 V, GND = 0 V, REFIN = 5 V external, DVDD = 2.7 V to 5.5 V, and all specifications are from –40°C to 125°C (unless otherwise noted). For IOUT, R_L = 300 Ω. Typical specifications are at 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE OUTPUT					
Reference output	T_A = 25°C	4.995		5.005	V
Reference temperature coefficient[3]	T_A = –40°C to 85°C			±10	ppm/°C
Output noise (0.1 Hz to 10 Hz)	T_A = 25°C		14		μV_{PP}
Noise spectral density	T_A = 25°C, 10 kHz		185		nV/√Hz
Capacitive load			600		nF
Load current			±5		mA
Short-circuit current	REFOUT shorted to GND		25		mA
Load regulation	AVDD = 24 V, T_A = 25°C, sourcing		55		µV/mA
	AVDD = 24 V, T_A = 25°C, sinking		120		
Line regulation			±1.2		µV/V
DVDD INTERNAL REGULATOR					
Output voltage	AVDD = 24 V		4.6		V
Output load current[3]				10	mA
Load regulation			3.5		mV/mA
Line regulation			1		mV/V
Short-circuit current	AVDD = 24 V, to GND		35		mA
Capacitive load stability[3]				2.5	µF
DIGITAL INPUTS					
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}	3.6 V < AVDD < 5.5 V			0.8	V
	2.7 V < AVDD < 3.6 V			0.6	
Hysteresis voltage			0.4		V
Input current	DVDD-EN, V_{IN} ≤ 5 V	–2.7			µA
	All terminals other than DVDD-EN			±1	
Terminal capacitance	Per terminal		10		pF
DIGITAL OUTPUTS					
SDO	Low-level output voltage, V_{OL}, sinking 200 µA			0.4	V
	HIigh-level output voltage, V_{OH}, sourcing 200 µA	DVDD – 0.5			
	High-impedance leakage			±1	µA
$\overline{ALARM}$	Low-level output voltage, V_{OL}: 10-kΩ pullup resistor to DVDD			0.4	V
	Low-level output voltage, V_{OL}: 2.5 mA			0.6	
	High-impedance leakage			±1	µA
High-impedance output capacitance			10		pF
POWER SUPPLY					
AVDD		10		36	V
DVDD	Internal regulator disabled	2.7		5.5	V
AIDD	Outputs disabled, external DVDD			3	mA
	Outputs disabled, internal DVDD			4	
	Code = 0x0000, IOUT enabled			3	
DIDD	V_{IH} = DVDD, V_{IL} = GND, interface idle			1	mA
Power dissipation	AVDD = 36 V, IOUT = 0 mA, DVDD = 5 V		95	115	mW
TEMPERATURE					
Thermal alarm			142		°C
Thermal alarm hysteresis			18		°C

7.6 Electrical Characteristics: AC

At AVDD = 10 V to 36 V, GND = 0 V, REFIN= 5 V external and DVDD = 2.7 V to 5.5 V. For IOUT, R_L = 300 Ω. All specifications –40°C to 125°C (unless otherwise noted). Typical specifications are at 25°C.

PARAMETER(1)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE					
Output current settling time	16-mA step, to 0.1% FSR, no L (inductance)		10		µs
	16-mA step, to 0.1% FSR, L < 1 mH		25		µs
AC PSRR	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage		–75		dB

(1) Specified by characterization, not production tested.

7.7 Timing Requirements: Write Mode

at T_A = –40°C to 125°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_1	SCLK cycle time	33		ns
t_2	SCLK low time	13		ns
t_3	SCLK high time	13		ns
t_4	LATCH delay time	13		ns
t_5	LATCH high time(2)	40		ns
t_6	Data setup time	5		ns
t_7	Data hold time	7		ns
t_8	LATCH low time	40		ns
t_9	CLR pulse duration	20		ns
t_{10}	CLR activation time		5	µs

(1) Specified by design, not production tested.
(2) Based on digital interface circuitry only. When writing to DAC control and configuration registers, consider the analog output specifications in *Electrical Characteristics: AC*.

7.8 Timing Requirements: Readback Mode

at T_A = –40°C to 125°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_{11}	SCLK cycle time	60		ns
t_{12}	SCLK low time	25		ns
t_{13}	SCLK high time	25		ns
t_{14}	LATCH delay time	13		ns
t_{15}	LATCH high time	40		ns
t_{16}	Data setup time	5		ns
t_{17}	Data hold time	7		ns
t_{18}	LATCH low time	40		ns
t_{19}	Serial output delay time ($C_{L, SDO}$ = 15 pF)		35	ns
t_{20}	LATCH rising edge to SDO 3-state ($C_{L, SDO}$ = 15 pF)		35	ns

(1) Specified by design, not production tested.

7.9 Timing Requirements: Daisy-Chain Mode

at T_A = –40°C to 125°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_{21}	SCLK cycle time	60		ns
t_{22}	SCLK low time	25		ns
t_{23}	SCLK high time	25		ns
t_{24}	LATCH delay time	13		ns
t_{25}	LATCH high time	40		ns
t_{26}	Data setup time	5		ns
t_{27}	Data hold time	7		ns
t_{28}	LATCH low time	40		ns
t_{29}	Serial output delay time ($C_{L, SDO}$ = 15 pF)		35	ns

(1) Specified by design, not production tested.

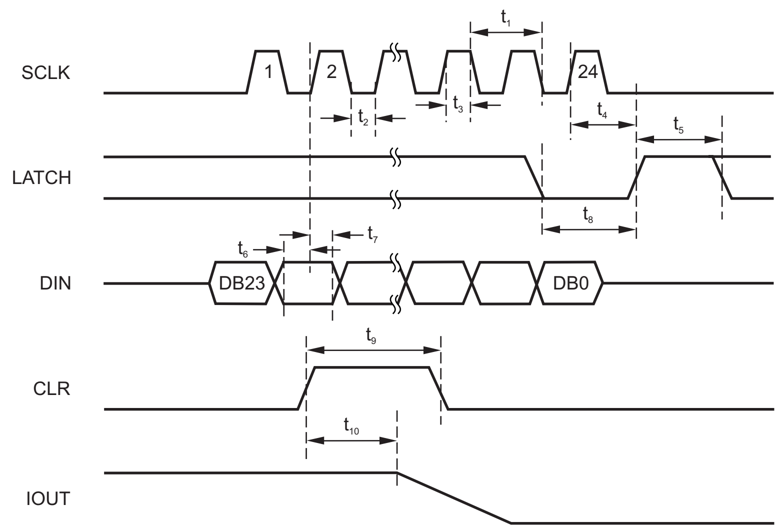


Figure 1. Write Mode Timing

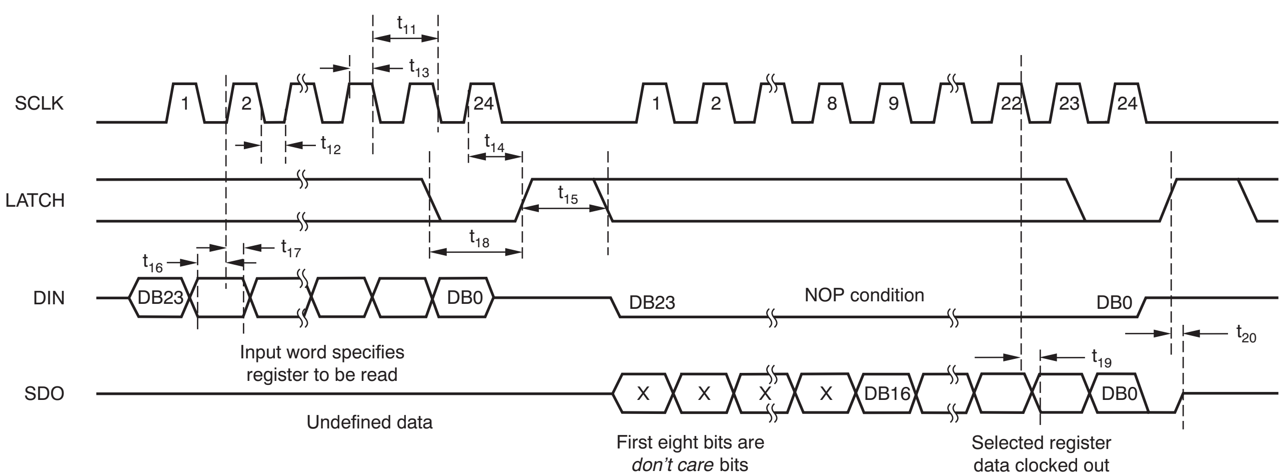


Figure 2. Readback Mode Timing

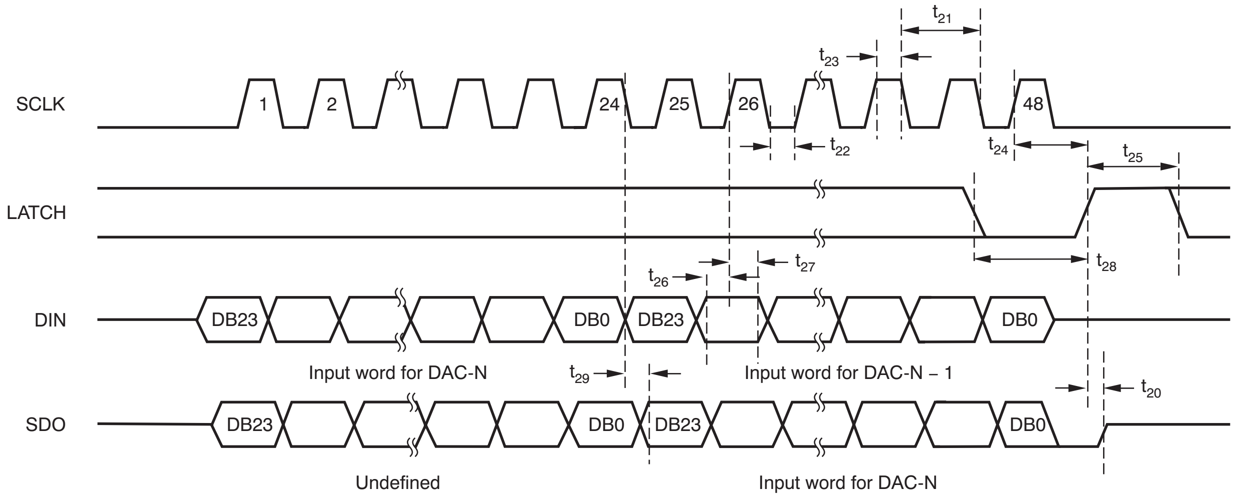
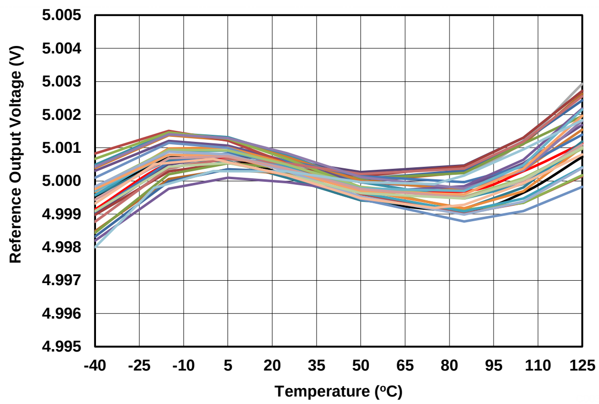


Figure 3. Daisy-Chain Mode Timing

7.10 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



30 units shown AVDD = 24 V

Figure 4. REFOUT vs Temperature

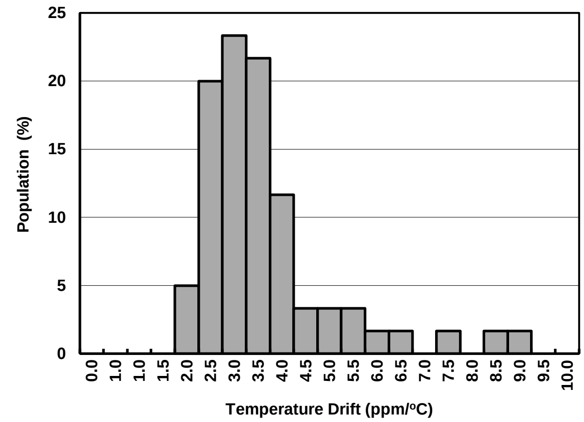
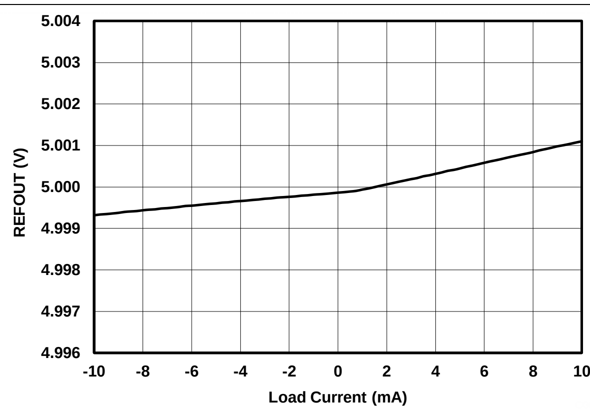
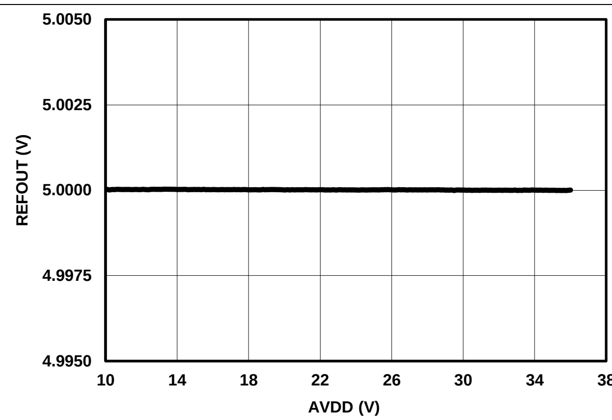


Figure 5. Internal Reference Temperature Drift Histogram



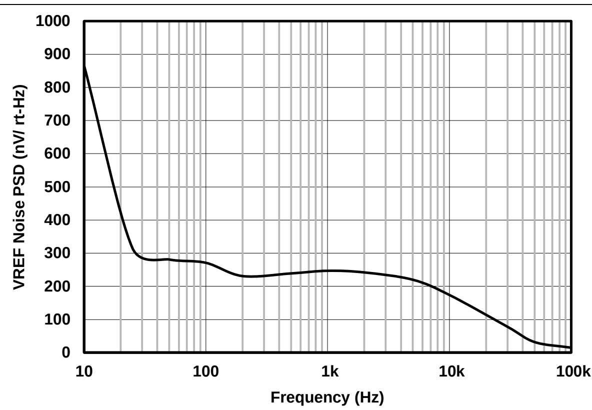
AVDD = 24 V

Figure 6. REFOUT vs Load Current



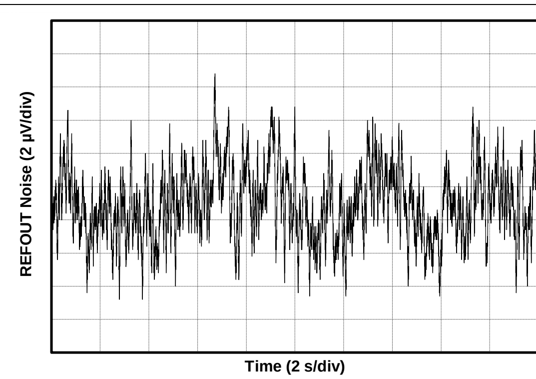
T_A = 25°C

Figure 7. REFOUT vs AVDD



AVDD = 24 V

Figure 8. REFOUT Noise PSD vs Frequency

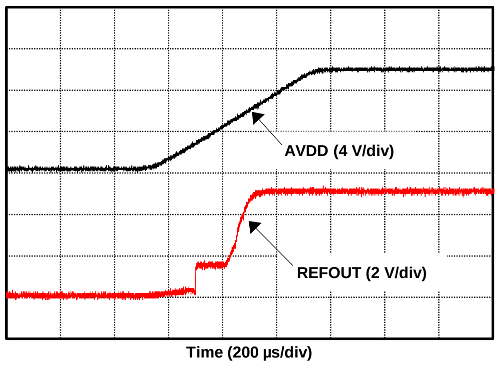


AVDD = 24 V

Figure 9. Internal Reference, Peak-to-Peak Noise (0.1 Hz to 10 Hz)

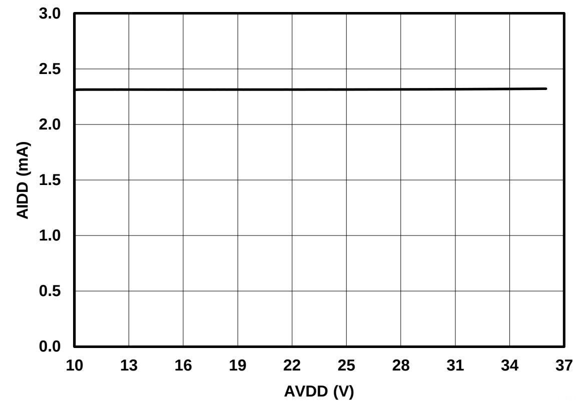
Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



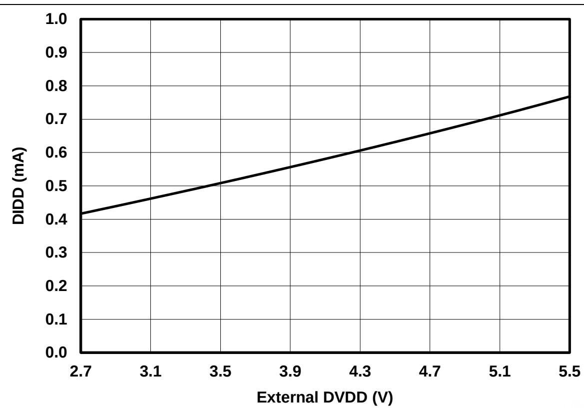
AVDD = 10 V

Figure 10. REFOUT Transient vs Time



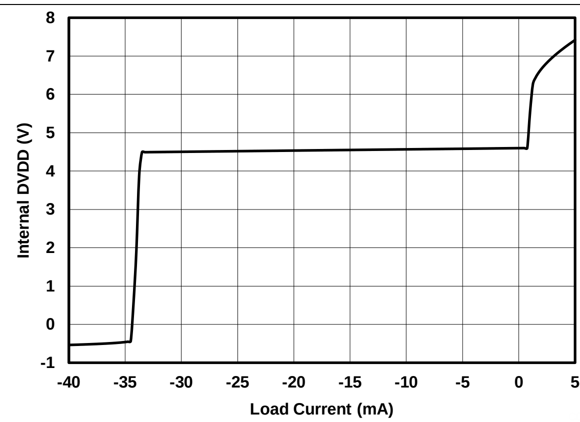
External DVDD IOUT = 0 mA

Figure 11. AIDD vs AVDD



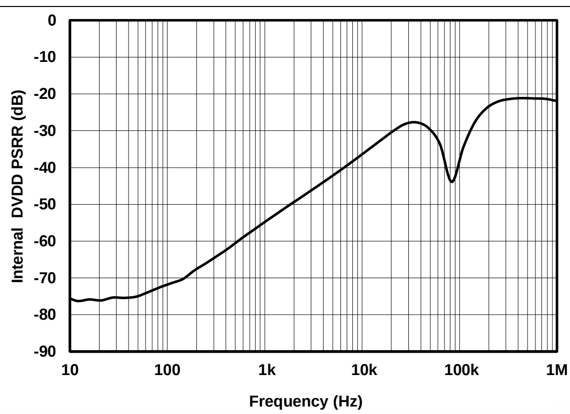
T_A = 25°C External DVDD

Figure 12. DIDD vs External DVDD



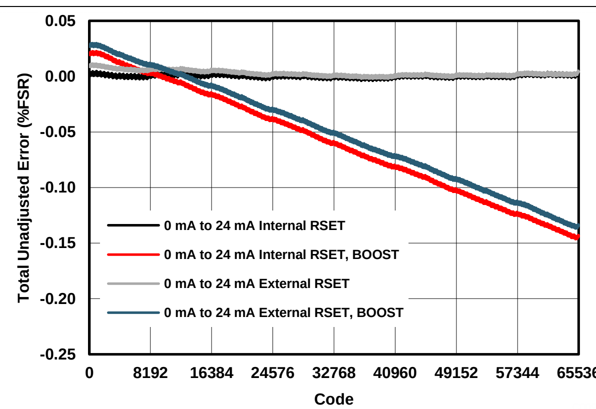
T_A = 25°C Internal DVDD

Figure 13. Internal DVDD vs Load Current



AVDD = 18 V C_{LOAD} = 100 nF

Figure 14. Internal DVDD PSRR vs Frequency

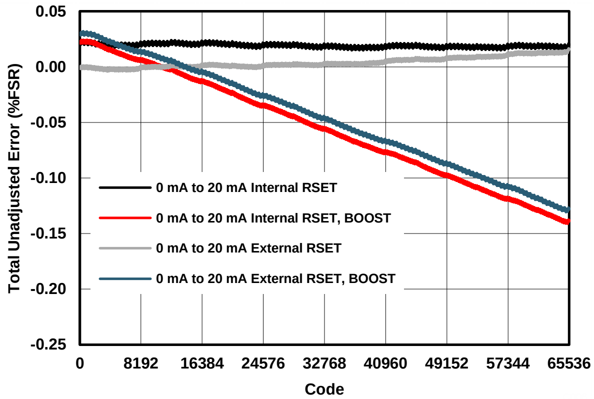


AVDD = 24 V R_{LOAD} = 300 Ω

Figure 15. IOUT TUE vs Code (0 mA to 24 mA)

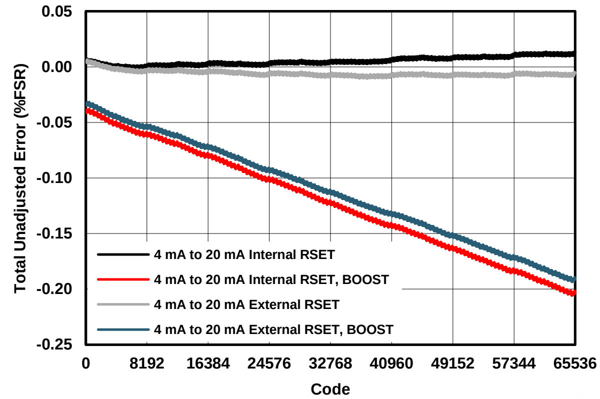
Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



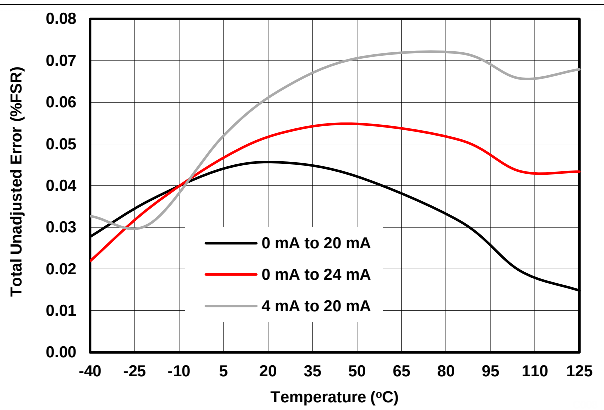
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 16. IOUT TUE vs Code (0 mA to 20 mA)



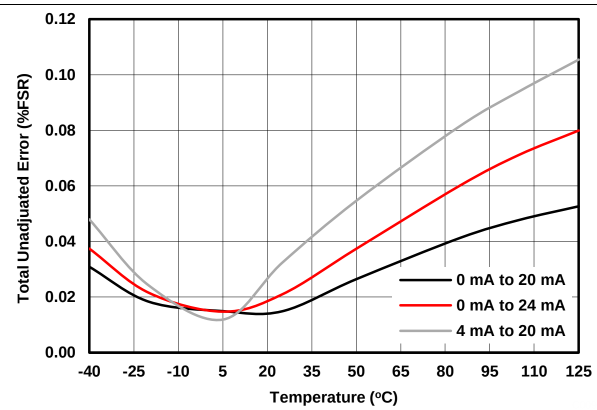
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 17. IOUT TUE vs Code (4 mA to 20 mA)



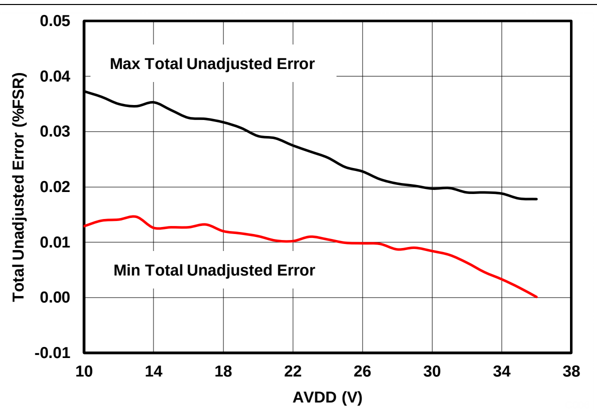
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 18. IOUT TUE vs Temperature (Internal R_{SET})



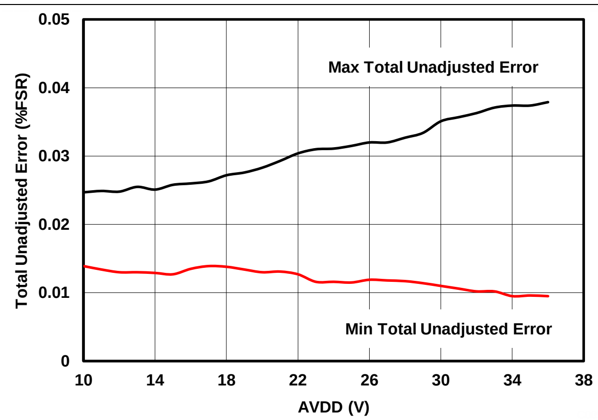
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 19. IOUT TUE vs Temperature (External R_{SET})



R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 20. IOUT TUE vs Supply (Internal R_{SET})

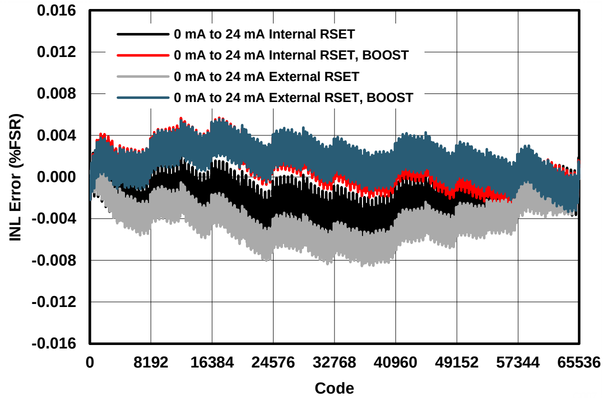


R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 21. IOUT TUE vs Supply (External R_{SET})

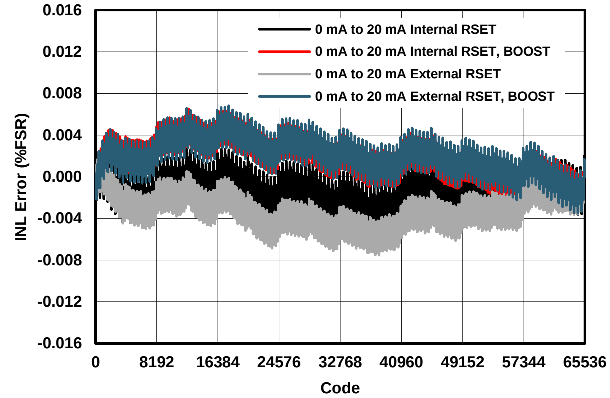
Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



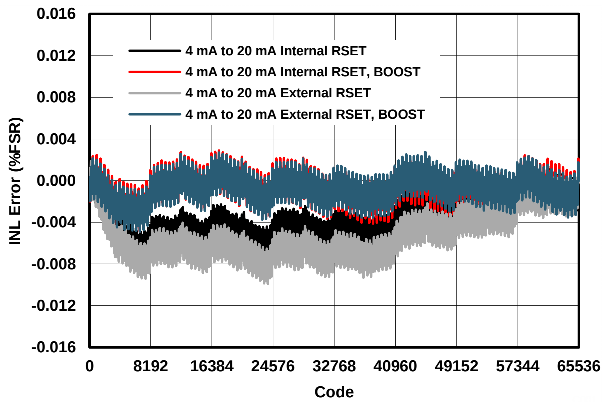
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 22. IOUT INL vs Code (0 mA to 24 mA)



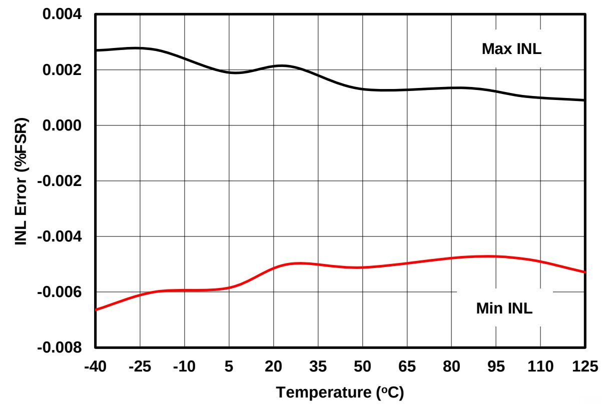
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 23. IOUT INL vs Code (0 mA to 20 mA)



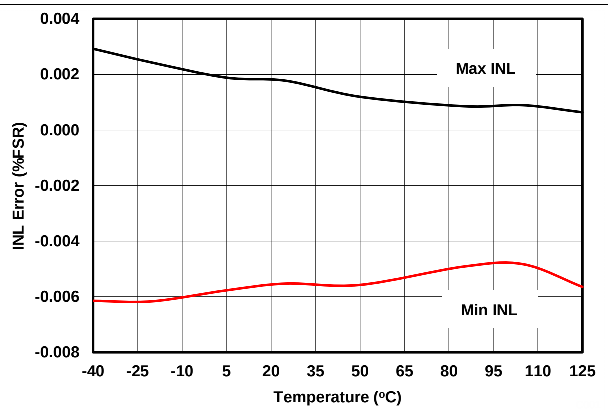
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 24. IOUT INL vs Code (4 mA to 20 mA)



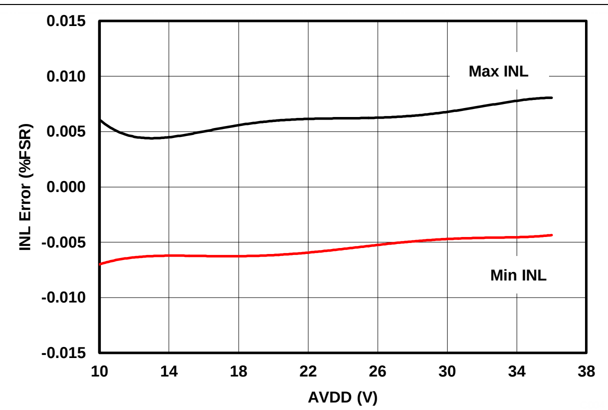
AVDD = 10 V R_{LOAD} = 300 Ω   All IOUT ranges

Figure 25. IOUT INL vs Temperature (Internal R_{SET})



AVDD = 10 V R_{LOAD} = 300 Ω   All IOUT ranges

Figure 26. IOUT INL vs Temperature (External R_{SET})

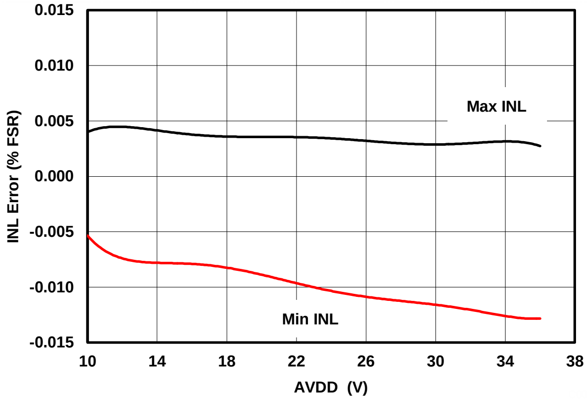


R_{LOAD} = 300 Ω   0-mA to 24-mA range

Figure 27. IOUT INL vs Supply (Internal R_{SET})

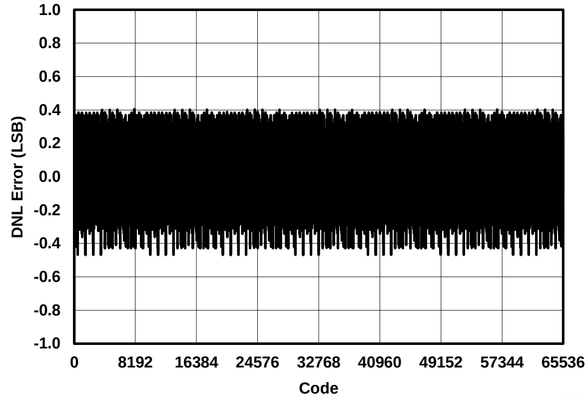
Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



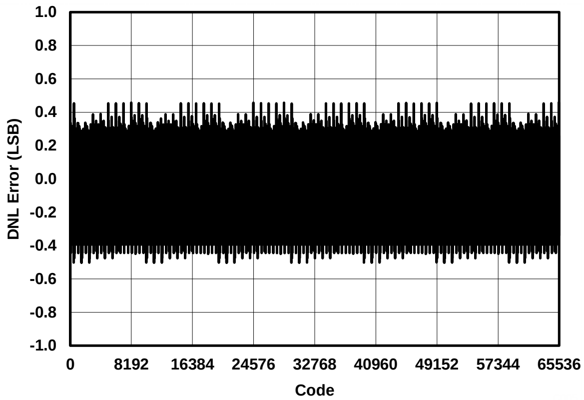
R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 28. IOUT INL vs Supply (External R_{SET})



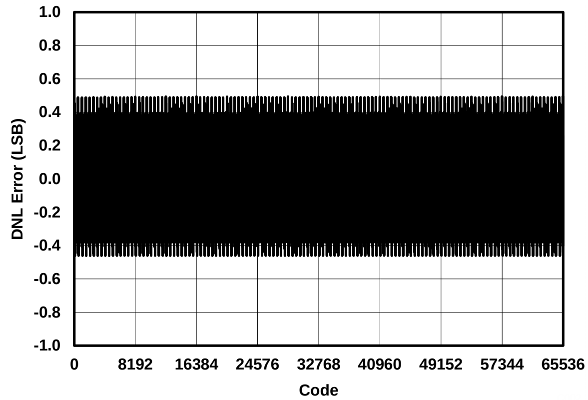
AVDD = 24 V 0-mA to 24-mA range
R_{LOAD} = 300 Ω

Figure 29. IOUT DNL vs Code (0 mA to 24 mA)



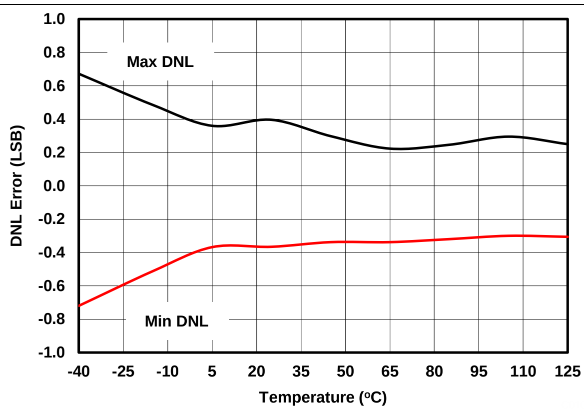
AVDD = 24 V 0-mA to 24-mA range
R_{LOAD} = 300 Ω

Figure 30. IOUT DNL vs Code (0 mA to 20 mA)



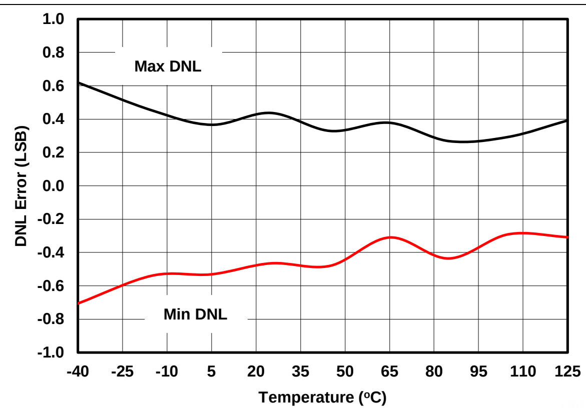
AVDD = 24 V 4-mA to 24-mA range
R_{LOAD} = 300 Ω

Figure 31. IOUT DNL vs Code (4 mA to 20 mA)



AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

Figure 32. IOUT DNL vs Temperature (Internal R_{SET})

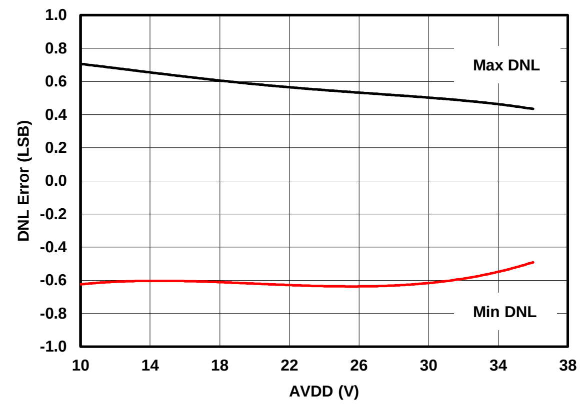


AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

Figure 33. IOUT DNL vs Temperature (External R_{SET})

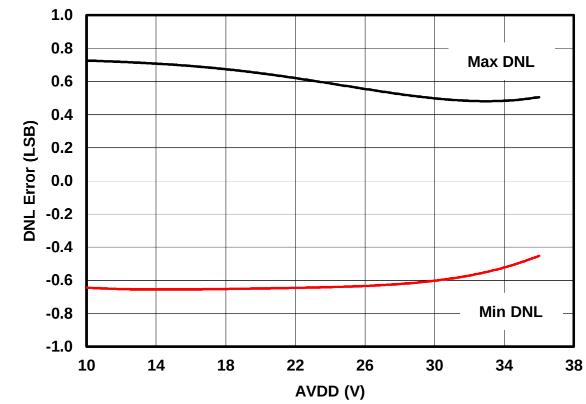
Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



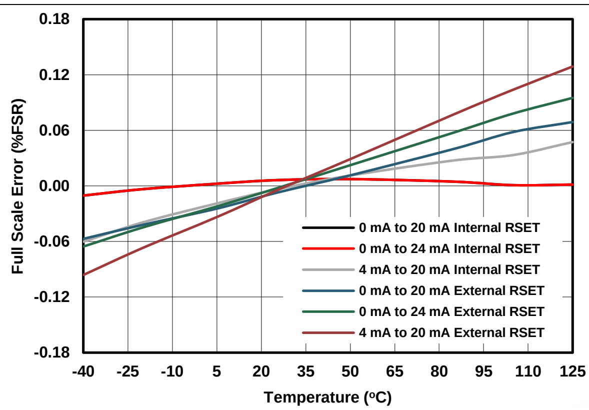
R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 34. IOUT DNL vs Supply (Internal R_{SET})



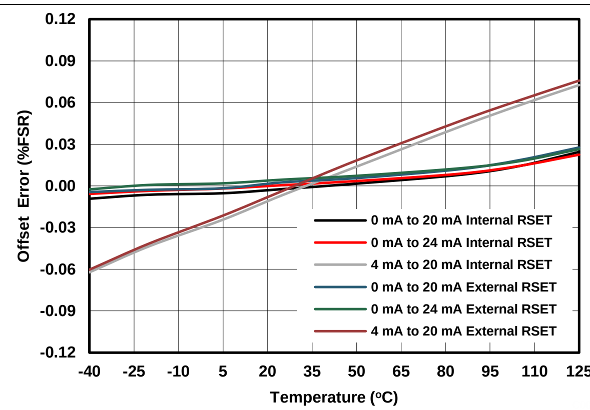
R_{LOAD} = 300 Ω 0-mA to 24-mA range

Figure 35. IOUT DNL vs Supply (External R_{SET})



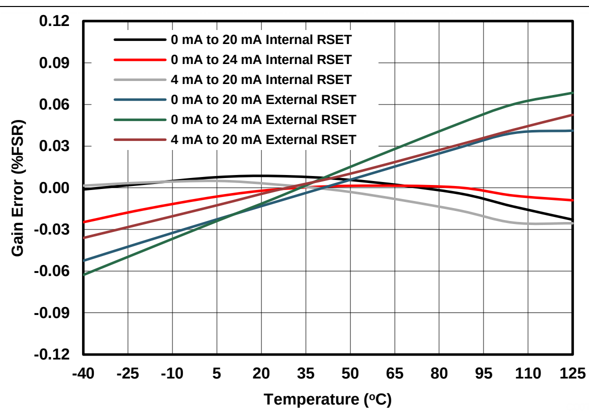
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 36. IOUT Full-Scale Error vs Temperature



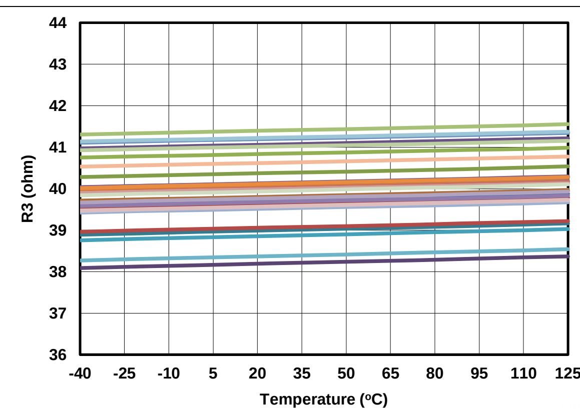
AVDD = 10 V R_{LOAD} = 300 Ω

Figure 37. IOUT Offset Error vs Temperature



AVDD = 10 V R_{LOAD} = 300 Ω

Figure 38. IOUT Gain Error vs Temperature



33 units shown

Figure 39. R3 Resistance vs Temperature

1. Compliance voltage headroom is defined as the drop from AVDD terminal to the IOUT terminal.

Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

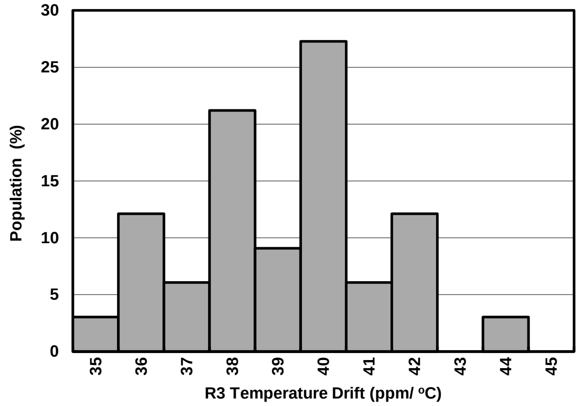
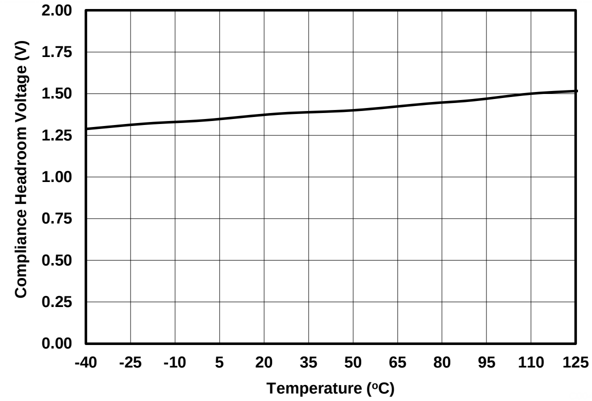
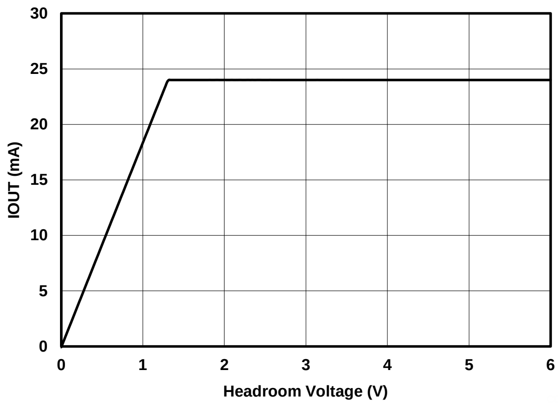


Figure 40. R3 Resistance Temperature Drift Histogram



AVDD = 36 V IOUT = 24 mA R_{LOAD} = 300 Ω

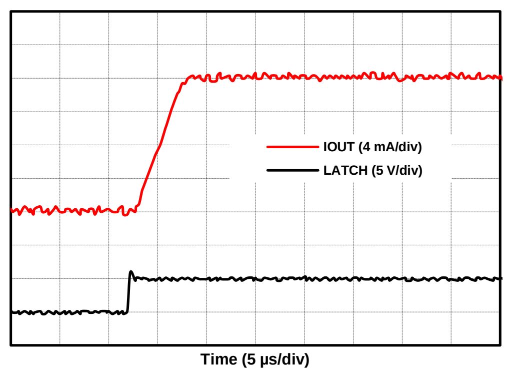
Figure 41. Compliance Headroom Voltage(1) vs Temperature



AVDD = 36 V DAC configured to deliver 24 mA

R_{LOAD} = 300 Ω

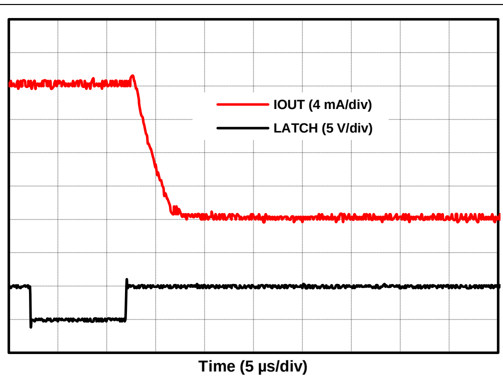
Figure 42. IOUT vs Compliance Headroom Voltage(1)



AVDD = 24 V 4-mA to 20-mA range

R_{LOAD} = 300 Ω From code: 0x0000 To code: 0xFFFF

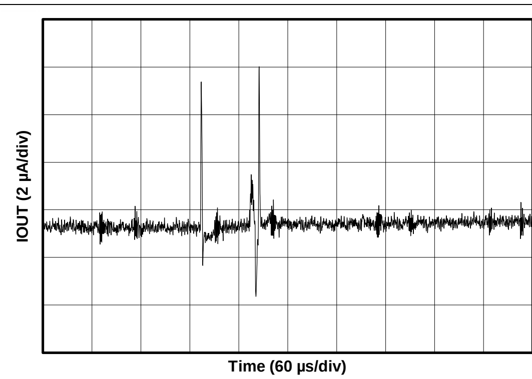
Figure 43. 4-mA to 20-mA Rising



AVDD = 24 V 4-mA to 20-mA range

R_{LOAD} = 300 Ω From code: 0x0000 To code: 0xFFFF

Figure 44. 4-mA to 20-mA Falling

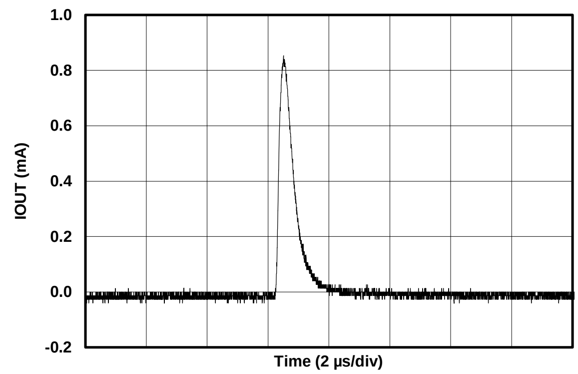


AVDD = 24 V R_{LOAD} = 300 Ω

Figure 45. IOUT Power-On Glitch

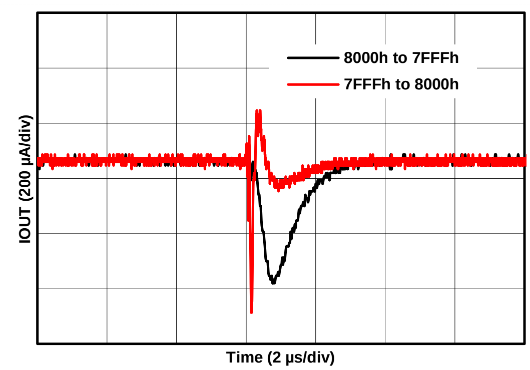
Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



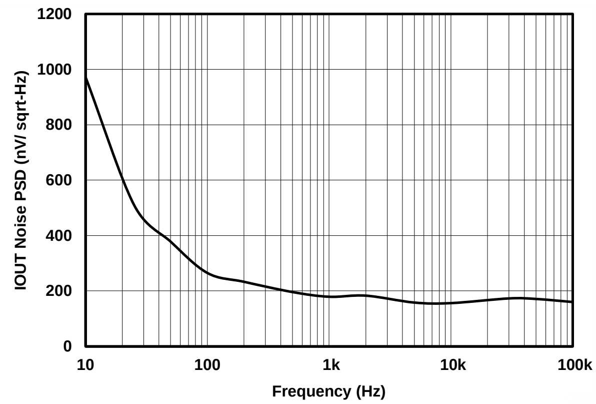
AVDD = 24 V R_{LOAD} = 300 Ω

Figure 46. IOUT Output Enable Glitch



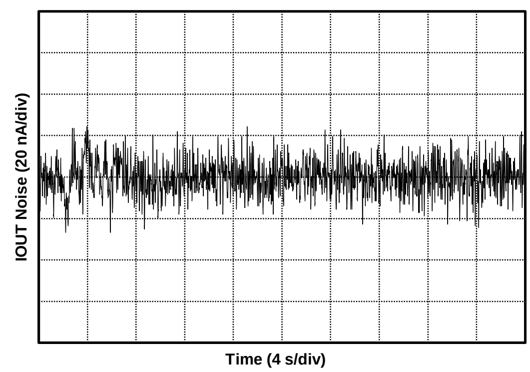
AVDD = 24 V R_{LOAD} = 250 Ω

Figure 47. IOUT Digital-to-Analog Glitch



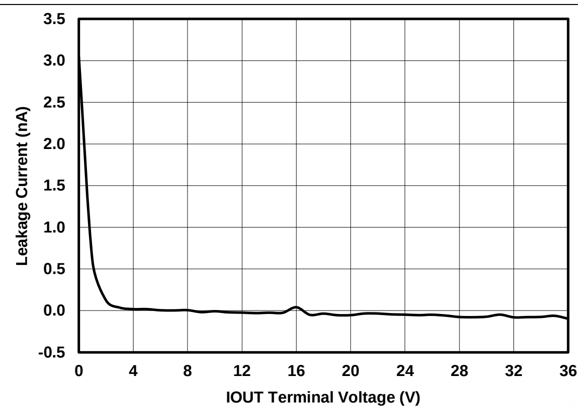
AVDD = 24 V R_{LOAD} = 300 Ω   All IOUT ranges

Figure 48. IOUT Noise PSD vs Frequency



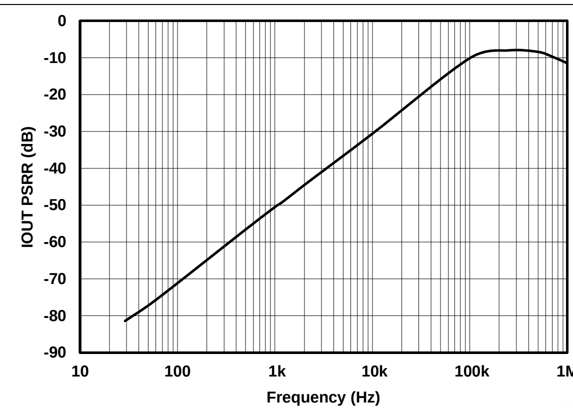
AVDD = 24 V   0-mA to 20-mA range
DAC = midscale

Figure 49. IOUT Peak-to-Peak Noise vs Time (0.1 Hz to 10 Hz)



AVDD = 36 V   Output disabled

Figure 50. IOUT Hi-Z Leakage Current vs Voltage



AVDD = 24 V R_{LOAD} = 250 Ω   All IOUT ranges

Figure 51. IOUT PSRR vs Frequency

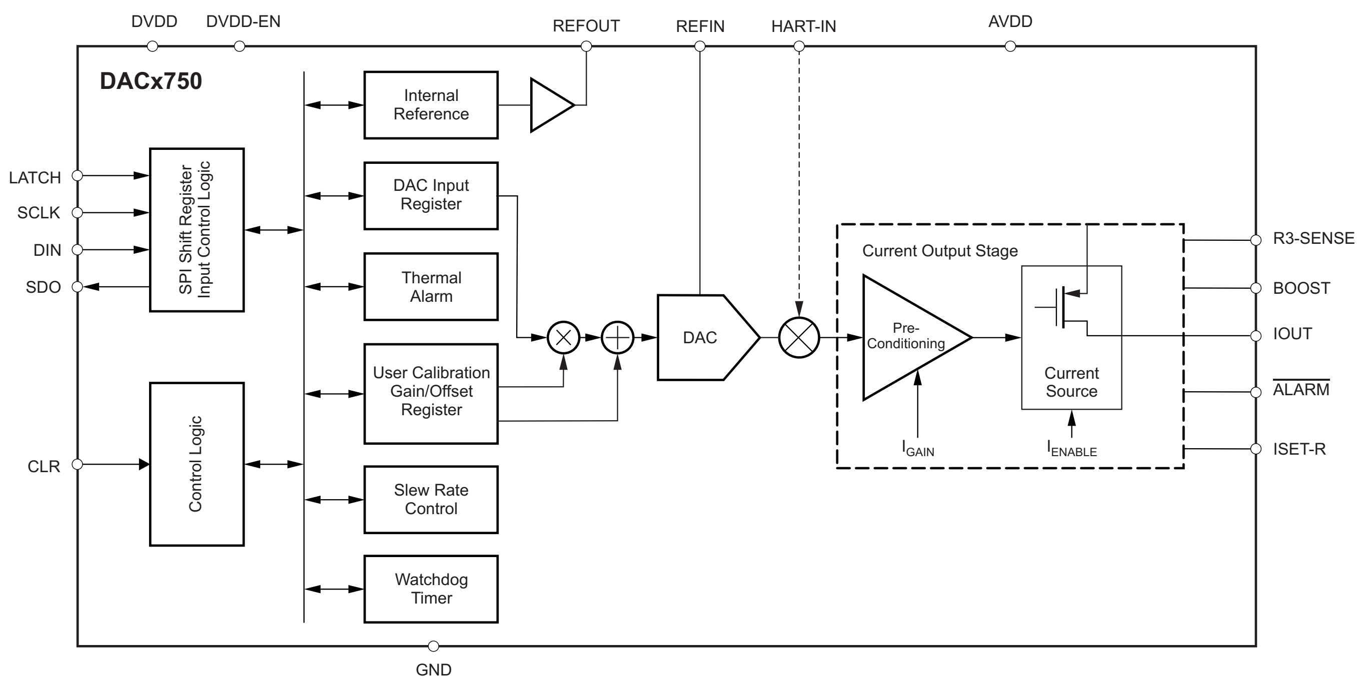
8 Detailed Description

8.1 Overview

The DAC8750 and DAC7750 are low-cost, precision, fully-integrated, 16-bit an 12-bit digital-to-analog converters (DACs) designed to meet the requirements of industrial process control applications. These devices can be programmed as a current output with a range of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA. The DAC8750 and DAC7750 include reliability features such as CRC error checking on the serial peripheral interface (SPI) frame, a watchdog timer, an open circuit, compliance voltage, and thermal alarm. In addition the output current can be monitored by accessing an internal precision resistor.

These devices include a power-on-reset function to ensure powering up in a known state (both IOUT is disabled and in a high-impedance state). The CLR pin sets the current output to the low-end of the range if the output is enabled. Zero code error and gain error calibration registers can be programmed to digitally calibrate the device in the end system. The output slew rate is also programmable. These devices can AC couple an external HART signal on the current output and can operate with either a 10-V to 36-V supply.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Architecture

The resistor-string section is simply a string of resistors, each with the same value, from REFIN to GND, as Figure 52 shows. This type of architecture makes sure the DAC is monotonic. The 16-bit (DAC8750) or 12-bit (DAC7750) binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before it is fed into the voltage-to-current conversion stage. The current-output stage converts the voltage output from the string to current. When the output is disabled, it is in a high-impedance (Hi-Z) state. After power-on, the output is disabled.

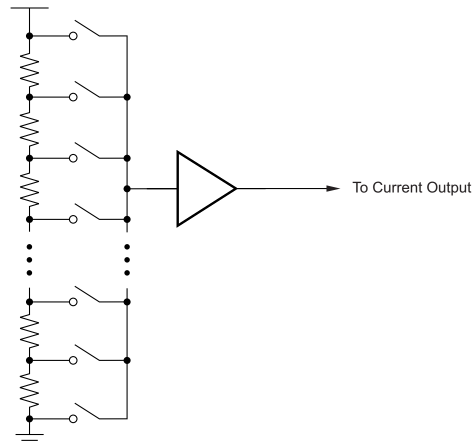


Figure 52. DAC Structure: Resistor String

8.3.2 Current Output Stage

The current output stage consists of a preconditioner and a current source, as shown in Figure 53. This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA. Use an external transistor to reduce the power dissipation of the device. The maximum compliance voltage on IOUT equals (AVDD – 2 V). In single power-supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 34 V. After power on, the IOUT terminal is in a Hi-Z state.

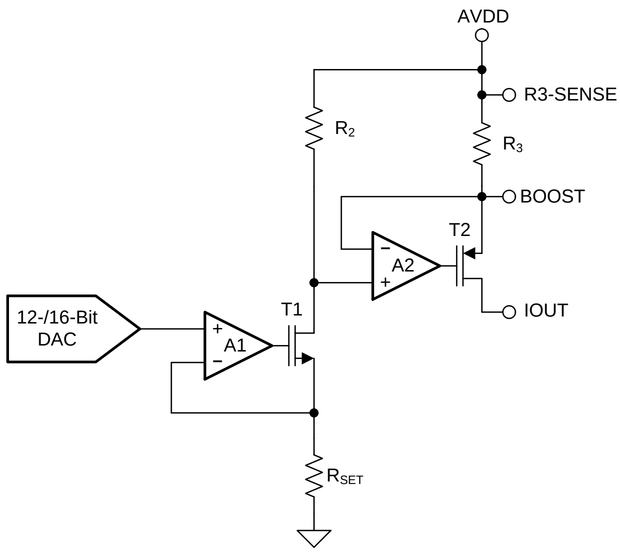


Figure 53. Current Output

Feature Description (continued)

For a 5-V reference, the output can be expressed as shown in Equation 1 through Equation 3.

For a 0-mA to 20-mA output range, use Equation 1.

$$IOUT = 20mA \bullet \frac{CODE}{2^N} \quad (1)$$

For a 0-mA to 24-mA output range, use Equation 2.

$$IOUT = 24mA \bullet \frac{CODE}{2^N} \quad (2)$$

For a 4-mA to 20-mA output range, use Equation 3.

$$IOUT = 16mA \bullet \frac{CODE}{2^N} + 4mA$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC
- *N* is the bits of resolution; 16 for DAC8750, and 12 for DAC7750 (3)

The current-output range is normally set according to the value of the RANGE bits in the *Control Register* (see *Setting Current-Output Ranges* for more details).

8.3.3 Internal Reference

The DACx750 includes an integrated 5-V reference with a buffered output (REFOUT) capable of driving up to 5 mA (source or sink) with an initial accuracy of ±5 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum.

8.3.4 Digital Power Supply

An internally generated 4.6-V supply capable of driving up to 10 mA can be output on DVDD by leaving the DVDD-EN terminal unconnected. This eases the system power supply design when an isolation barrier is required to generate the digital supply. It can be used to drive isolation components used for the digital data lines and other miscellaneous components like references and temp sensors; see Figure 62 for an example application.

If an external supply is preferred, the DVDD terminal (which can be driven up to 5.5 V in this case) can become an input by tying DVDD-EN to GND. See *Electrical Characteristics* for detailed specifications.

8.3.5 DAC Clear

The DAC has an asynchronous clear function through the CLR terminal that is active-high and allows the current output to be cleared to zero-scale code. When the CLR signal returns to low, the output remains at the cleared value. The preclear value can be restored by pulsing the LATCH signal without clocking any data. A new value cannot be programmed until the CLR terminal returns to low. To avoid glitches on the output, disable the output by writing a 0 to the OUTEN bit of the *Control Register* before changing the current range.

8.3.6 Power-Supply Sequence

The DACx750 has an internal power-on reset (POR) circuitry for both the digital DVDD and analog AVDD supplies. This circuitry makes sure that the internal logic and power-on state of the DAC power-up to the proper state independent of the supply sequence. The recommended power-supply sequence is to first have the analog AVDD supply come up, followed by the digital supply DVDD. DVDD can also come up first as long as AVDD ramps to at least 5 V within 50 µs. If neither of these conditions can be satisfied, TI recommends that a software reset command be issued via the SPI bus after both AVDD and DVDD are stable.

Feature Description (continued)

8.3.7 Power-On Reset

The DACx750 incorporates two internal POR circuits for the DVDD and AVDD supplies. The DVDD and AVDD POR signals are ANDed together so that both supplies must be at their minimal specified values for the device to *not* be in a reset condition. These POR circuits initialize internal logic and registers, as well as set the analog outputs to a known state while the device supplies are ramping. All registers are reset to their default values. Typically the POR function can be ignored, as long as the device supplies power-up and maintains the specified minimum voltage levels. However, in the case of a supply drop or brownout, the DACx750 can have an internal POR reset event or lose digital memory integrity. Figure 54 represents the threshold levels for the internal POR for both the DVDD and AVDD supplies.

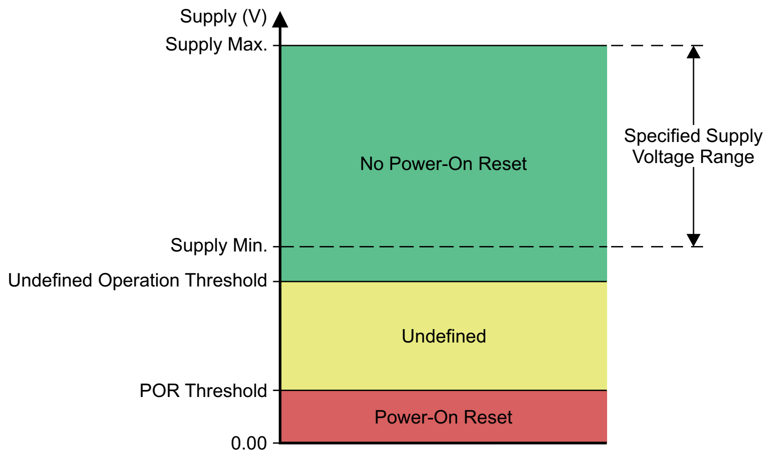


Figure 54. Relevant Voltage Levels for POR Circuit

For the DVDD supply, no internal POR occurs for nominal supply operation from 2.7 V (supply min) to 5.5 V (supply max). For the DVDD supply region between 2.4 V (undefined operation threshold) and 0.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the DVDD supply below 0.8 V (POR threshold), the internal POR resets if the supply voltage remains less than 0.8 V for approximately 1 ms.

For the AVDD supply, no internal POR occurs for nominal supply operation from 10 V (supply min) to 36 V (supply max). For AVDD supply voltages between 8 V (undefined operation threshold) and 1 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the AVDD supply below 1 V (POR threshold), the internal POR resets if the supply voltage remains less than 1 V for approximately 1 ms. In case the DVDD or AVDD supply drops to a level where the internal POR signal is indeterminate, either power cycle the device, or toggle the LATCH terminal and then perform a software reset. Both options initialize the internal circuitry to a known state and provide proper operation.

8.3.8 Alarm Detection

These devices also provide an alarm detection feature. When one or more of following events occur, the $\overline{\text{ALARM}}$ terminal goes low:

- The current output load is in open circuit,
- The voltage at IOUT reaches a level where accuracy of the output current is compromised. This condition is detected by monitoring internal voltage levels of the IOUT circuitry and is typically below the specified compliance voltage headroom (defined as the voltage drop between the AVDD and IOUT terminals) minimum of 2 V,
- The die temperature exceeds 142°C,
- The SPI watchdog timer exceeds the timeout period (if enabled), or
- The SPI frame error CRC check encounters an error (if enabled).

Feature Description (continued)

When the ALARM terminals of multiple DACx750 devices are connected together to form a wired-AND function, the host processor must read the status register of each device to know all the fault conditions that are present. Note that the thermal alarm has hysteresis of approximately 18°C. After being set, the alarm only resets when the die temperature drops below 124°C.

8.3.9 Watchdog Timer

This feature is useful to make sure that communication between the host processor and the DACx750 has not been lost. It can be enabled by setting the WDEN bit of the *Configuration Register* to 1. The watchdog timeout period can be set using the WDPD bits of the configuration register, as shown in Table 1. The timer period is based off an internal oscillator with a typical value of 8 MHz.

Table 1. Watchdog Timeout Period

WDPD BITS	WATCHDOG TIMEOUT PERIOD (Typical)
00	10 ms
01	51 ms
10	102 ms
11	204 ms

If the watchdog timer is enabled, these devices must have an SPI frame with 0x95 as the write address byte written to the device within the programmed timeout period. Otherwise, the ALARM terminal asserts low and the WD-FLT bit of the status register is set to 1. Note that the ALARM terminal can be asserted low for any of the different conditions as explained in *Alarm Detection*. The WD-FLT bit is reset to 0 with a software reset, by disabling the watchdog timer, or by powering down the device.

When using multiple DACx750 devices in a daisy-chain configuration, the open-drain ALARM terminals of all devices can be connected together in a wired-AND function. The watchdog timer can be enabled in any number of the devices in the chain although enabling it in one device is sufficient. The wired-AND ALARM terminal may get pulled low because of the simultaneous presence of different trigger conditions in the daisy-chained devices. The host processor reads the status register of each device to know all the fault conditions present in the chain.

8.3.9.1 The DACx750 Shares the SPI Bus With Other Devices (Non-DACx750)

This section is only applicable for applications where the DACx750 is digitally interfaced via an SPI bus that has other devices on the bus that are not DACx750 devices.

As explained in the *Serial Peripheral Interface (SPI)* section of this document, the DACx750 digital interface constantly clocks in data regardless of the status of the LATCH pin, and data are unconditionally latched on the rising edge of the LATCH pin. A rising edge on the LATCH pin is the only way the device takes action on clocked data.

The watchdog timer can also be enabled without a rising edge on the LATCH pin if a specific pattern, shown in Table 2, is present on DIN and SCLK. When this pattern enables the watchdog timer, this enabled status is not reflected in the configuration register. During this condition, the watchdog timer cannot be enabled or disabled through writes to the configuration register. Additionally, the alarm condition can only be cleared through a power-on reset event triggered either by a reset command or cycling power to the device. The ALARM pin also indicates that the watchdog timer has triggered.

Table 2. Enable Watchdog Timer Digital Interface Pattern

BIT FORMAT	BIT SETTING							
	DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB18**	**DB17**	**DB16**
Binary	0	0	1	0	1	0	1	1
Hex	0x2				0xB			
	DB25	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**
Binary	1	X	X	X	X	X	X	X
Hex	D15 = 1				X			
	DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
Binary	X	X	X	X	X	1	X	X
Hex	X				DB2 = 1			

If the watchdog timer feature is enabled as described in the *Watchdog Timer* section along with full compliance of the watchdog timer, then the pattern shown in Table 2 on DIN and SCLK does not have any effect.

8.3.10 Frame Error Checking

In noisy environments, error checking can be used to check the integrity of SPI data communication between the DACx750 and the host processor. To enable this feature, set the CRCEN bit of the *Configuration Register* to 1. The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, *100000111*). When error checking is enabled, the SPI frame width is 32 bits, as shown in Table 3. Start with the default 24-bit frame, enable frame error checking, and then switch to the 32-bit frame. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding to the device. For a register readback, the CRC polynomial is output on the SDO terminals by the device as part of the 32-bit frame.

Table 3. SPI Frame with Frame Error Checking Enabled

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

When in CRC mode the DACx750 calculates CRC words every 32 clocks, unconditional of when the LATCH pin toggles. The DACx750 decodes the 32-bit input frame data to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is non-zero (that is, the input frame has single- or multiple-bit errors), the ALARM terminal asserts low and the CRC-FLT bit of the status register is set to 1. The ALARM terminal can be asserted low for any of the different conditions as explained in *Alarm Detection*. The CRC-FLT bit is reset to 0 with a software reset, by disabling the frame error checking, or by powering down the device. In the case of a CRC error, the specific SPI frame is blocked from writing to the device.

Frame error checking can be enabled for any number of DACx750 devices connected in a daisy-chain configuration. However, it is recommended to enable error checking for either none or all devices in the chain. When connecting the ALARM terminals of multiple devices, forming a wired-AND function, the host processor reads the status register of each device to know all the fault conditions present in the chain. For proper operation, the host processor must provide the correct number of SCLK cycles in each frame, taking care to identify whether or not error checking is enabled in each device in the daisy-chain.

If the CRC mode is enabled on the first frame issued to the device after power-up, TI suggests that a no operation, or NOOP, command be issued to the device in order to reset the SPI clock and SPI frame alignment in the event that any transients on the SCLK line are interpreted as SCLK periods. A NOOP command can be issued to the device by simply toggling the LATCH pin without any SCLK periods.

8.3.10.1 The DACx750 Shares the SPI Bus With Other Devices (Non-DACx750)

This section is only applicable for applications where the DACx750 is digitally interfaced via an SPI bus that has other devices on the bus that are not DACx750 devices, and there are multiple DACx750s in a daisy-chain configuration.

As explained in the *SPI Shift Register* section of this document, the DACx750 digital interface constantly clocks in data regardless of the status of the LATCH pin, and data are unconditionally latched on the rising edge of the LATCH pin. A rising edge on the LATCH pin is the only way the device takes action on clocked data.

The frame error checking (CRC) mode can also be enabled without a rising edge on the LATCH pin if a specific pattern, shown in Table 4, is present on DIN and SCLK. When this pattern enables CRC mode, this enabled status is not reflected in the configuration register. During this condition the CRC mode cannot be enabled or disabled through writes to the configuration register. Additionally, the alarm pin and status registers do not indicate CRC alarm conditions, and frames with incorrect or missing CRC bits are not disregarded as described in the *Frame Error Checking* section. During this condition the devices in daisy-chain output data on the SDO pin on a 32-bit frame structure instead of 24 bits. The CRC mode can only be cleared through a power-on reset event triggered either by a reset command or by cycling power to the device.

Table 4. Enable CRC Mode Digital Interface Pattern

BIT FORMAT	BIT SETTING							
	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16
Binary	0	1	0	1	0	1	1	1
Hex	0x5				0x7			
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8
Binary	X	X	X	X	X	X	1	1
Hex	X				X			
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Binary	0	0	1	0	1	0	1	1
Hex	X				DB2 = 1			

If the CRC feature is enabled as described in the *Frame Error Checking* section along with full compliance of the frame error checking, then the pattern shown in Table 4 on DIN and SCLK does not have any effect.

8.3.11 User Calibration

The device implements a user-calibration function (enabled by the CALEN bit in the *Configuration Register*) to trim system gain and zero errors. The DAC output is calibrated according to the value of the gain calibration and zero calibration registers. The range of gain adjustment is typically ±50% of full-scale with 1 LSB per step. The gain register must be programmed to 0x8000 to achieve the default gain of 1 because the power-on value of the register is 0x0000, equivalent to a gain of 0.5. The zero code adjustment is typically ±32,768 LSBs with 1 LSB per step. The input data format of the gain register is unsigned straight binary, and the input data format of the zero register is twos complement. The gain and offset calibration is described by Equation 4.

$$CODE\_OUT = CODE \cdot \frac{User\_GAIN + 2^{15}}{2^{16}} + User\_ZERO \tag{4}$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC data register at address 0x01
- *N* is the bits of resolution (16 for DAC8750 and 12 for DAC7750)
- *User_ZERO* is the signed 16-bit code in the zero register
- *User_GAIN* is the unsigned 16-bit code in the gain register
- *CODE_OUT* is the decimal equivalent of the code loaded to the DAC (limited between 0x0000 to 0xFFFF for DAC8750 and 0x000 to 0xFFF for DAC7750) (4)

This is a purely digital implementation and the output is still limited by the programmed value at both ends of the current output range (set by the RANGE bits, as described in *Setting Current-Output Ranges*). In addition, the correction only makes sense for endpoints inside of the true device end points. To correct more than just the actual device error, for example a system offset, the valid range for the adjustment changes accordingly and must be taken into account.

New calibration codes are only applied to subsequent writes to the DAC data register. Updating the calibration codes does not automatically update the DAC output. Additionally, TI recommends configuring the calibration codes along with the slew rate control prior to applying new DAC data.

8.3.12 Programmable Slew Rate

The slew rate control feature controls the rate at which the output current changes. With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the slew rate control feature through bit 4 of the *Control Register*. With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [7:5] (SRSTEP) and bits [11:8] (SRCLK) of the *Control Register*. SRCLK defines the rate at which the digital slew updates; SRSTEP defines the amount by which the output value changes at each update. If the DAC data register is read while the DAC output is still changing, the instantaneous value is read. Table 5 lists the slew rate step-size options. Table 6 summarizes the slew rate update clock options.

Table 5. Slew Rate Step-Size (SRSTEP) Options

SRSTEP	STEP SIZE (LSB)	
	DAC7750	DAC8750
000	0.0625	1
001	0.125	2
010	0.125	4
011	0.5	8
100	1	16
101	2	32
110	4	64
111	8	128

Table 6. Slew Rate Update Clock (SRCLK) Options

SRCLK	DAC UPDATE FREQUENCY (Hz)
0000	258,065
0001	200,000
0010	153,845
0011	131,145
0100	115,940
0101	69,565
0110	37,560
0111	25,805
1000	20,150
1001	16,030
1010	10,295
1011	8,280
1100	6,900
1101	5,530
1110	4,240
1111	3,300

The time required for the output to slew over a given range is expressed as Equation 5.

$$\text{Slew Time} = \frac{\text{Output Change}}{\text{Step Size} \cdot \text{Update Clock Frequency} \cdot \text{LSB Size}}$$

where

- *Slew Time* is expressed in seconds
- *Output Change* is expressed in amps (A) for IOUT or volts (V) for VOUT (5)

When the slew rate control feature is enabled, all output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. If the CLR terminal is asserted, the output slews to the zero-scale value at the programmed slew rate. Bit 1 (SR-ON) of the *Status Register* can be read to verify that the slew operation has completed. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. Figure 55 shows an example of IOUT slewing at a rate set by the above described parameters. In this example for the DAC8750 (LSB size of 305 nA for the 0-mA to 20-mA range), the settings correspond to an update clock frequency of 6.9 kHz and a step size of 128 LSB. As is shown in the case with no capacitors on CAP1 or CAP2, the steps occur at the update clock frequency (6.9 kHz corresponds to a period close to 150 µs), and the size of each step is approximately 38 µA (128 × 305 nA). Calculate the slew time for a specific code change by using Equation 5.

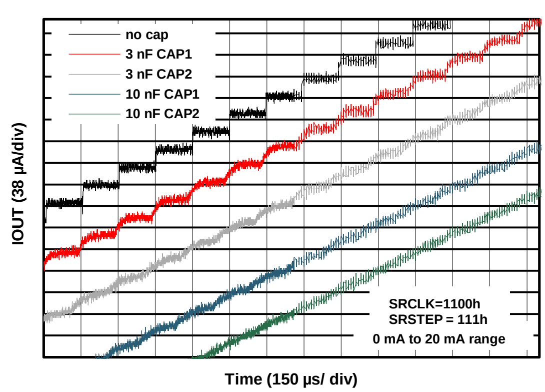


Figure 55. IOUT vs Time with Digital Slew Rate Control

Apply the desired programmable slew rate control setting prior to updating the DAC data register because updates to the DAC data register in tandem with updates to the slew rate control registers can create race conditions that may result in unexpected DAC data.

8.4 Device Functional Modes

8.4.1 Setting Current-Output Ranges

The current output range is set according to Table 7.

Table 7. RANGE Bits vs Output Range

RANGE	OUTPUT RANGE
101	4 mA to 20 mA
110	0 mA to 20 mA
111	0 mA to 24 mA

Note that changing the RANGE bits at any time causes the DAC data register to be cleared.

8.4.2 Current-Setting Resistor

Resistor R_{SET} (used to convert the DAC voltage to current) illustrated in Figure 53 determines the stability of the output current over temperature. If desired, an external, low-drift, precision 15-kΩ resistor can be connected to the ISET-R terminal and used instead of the internal R_{SET} resistor.

8.4.3 BOOST Configuration for IOUT

Figure 56 illustrates an external NPN transistor used to reduce power dissipation on the die. Most of the load current flows through the NPN transistor with a small amount flowing through the on-chip PMOS transistor based on the gain of the NPN transistor. This configuration reduces the temperature induced drift on the die and internal reference and is an option for use cases at the extreme end of the supply, load current, and ambient temperature ranges.

The inclusion of the bipolar junction transistor (BJT) adds an additional open loop gain to internal amplifier A2 (see Figure 53) and thus, can cause possible instability. Adding series emitter resistor R2 decreases the gain of the stage created by the BJT and internal R3 resistor (see Figure 53) especially for cases where R_{LOAD} is a short or a very small load, such as a multimeter. Recommended values for R_1, R_2, and C_1 in this circuit are 1 kΩ, 30 Ω and 22 nF, respectively. An equivalent solution is to place R_2 (with a recommended value of 3 kΩ instead of 30 Ω) in series with the base of the transistor instead of the configuration provided in Figure 56. Note that there is some gain error introduced by this configuration; see Figure 15, Figure 16 and Figure 17. Use the internal transistor in most cases because the values in *Electrical Characteristics* are based on the configuration with the internal on-chip PMOS transistor.

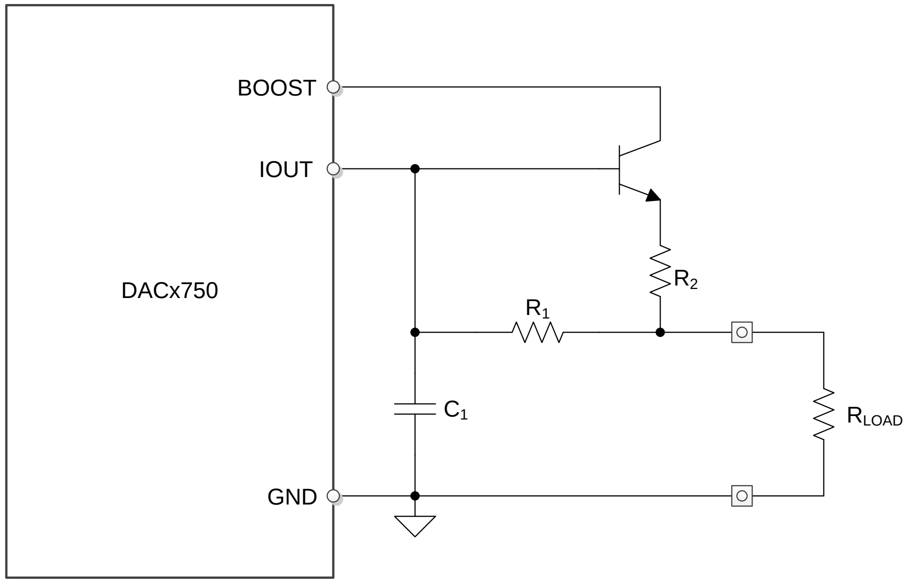


Figure 56. Boost Mode Configuration

8.4.4 Filtering The Current Output

The DACx750 provides access to internal nodes of the circuit; see Figure 61. Place capacitors on these terminals and AVDD to form a filter on the output current, reducing bandwidth and the slew rate of the output, especially useful for driving inductive loads. However, to achieve large reductions in slew rate, use the programmable slew rate to avoid having to use large capacitors. Even in that case, use the capacitors on CAP1 and CAP2 to smooth out the stairsteps caused by the digital code changes as shown in Figure 57. However, note that power supply ripple also couples into the devices through these capacitors.

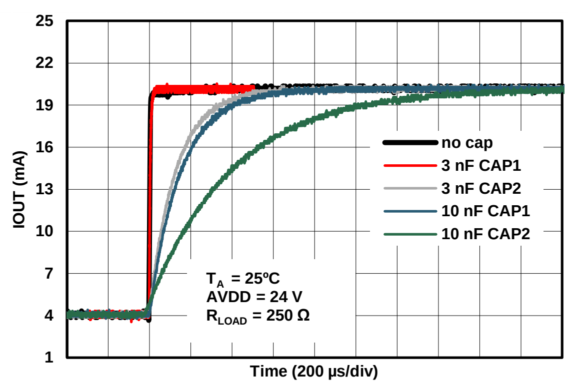


Figure 57. IOUT vs Time for Different Cap Values on CAP1 and CAP2

8.4.5 Output Current Monitoring

Many applications, especially for functional safety, require monitoring of the output current to ensure it stays close to the programmed value. Place a sense resistor in series to the output to measure the voltage across it. However, this resistor reduces the compliance voltage available for the load. The DACx750 provides access to an internal precision resistor (R3 in Figure 53) through the R3-SENSE and BOOST terminals to perform analog readback for monitoring the output current. Measure the voltage between the R3-SENSE and BOOST terminals and divide by the value of the R3 resistor to determine the magnitude of the output current. The R3 resistor has a typical value of 40 Ω (see Figure 39 for a plot of resistance versus temperature) with a temperature drift coefficient of 40 ppm/°C (see Figure 40 for a histogram of R3 resistance temperature drift). The R3 resistor is tested to stay within the minimum (36 Ω) and maximum (44 Ω) resistance values shown in the *R3 Resistor* section of *Electrical Characteristics*. To remove the tolerance error, perform a simple calibration by programming a certain value of output current, measuring the voltage across R3-SENSE and BOOST, and calculating the exact value of R3.

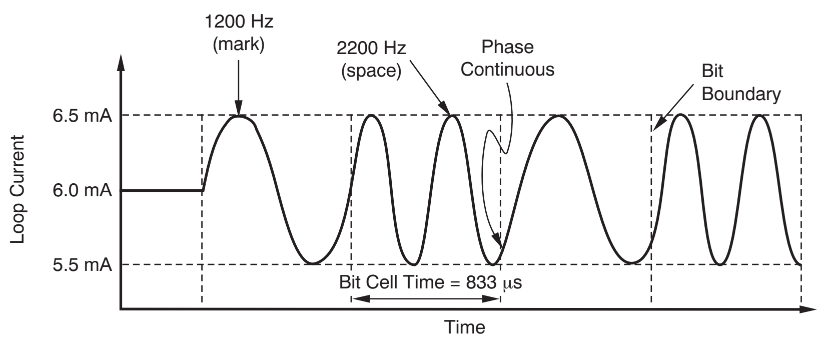
8.4.6 HART Interface

On the DACx750, HART digital communication can be modulated onto the input signal by the methods shown in the following subsections. For more detail, see *Implementing HART Communication with the DAC8760 Family*.

8.4.6.1 Implementing HART in 4-mA to 20-mA Mode

This method is limited to the case where the RANGE bits of the *Control Register* are programmed to the 4-mA to 20-mA range. Some applications require going beyond the 4-mA to 20-mA range. In those cases, refer to the methods described in the next subsection.

The external HART signal (ac voltage; 500 mV_{PP}, 1200 Hz, and 2200 Hz) can be capacitively coupled in through the HART-IN terminal and transferred to a current that is superimposed on the 4-mA to 20-mA current output. The HART-IN terminal has a typical input impedance of 35 kΩ that together with the input capacitor used to couple the external HART signal, forms a filter to attenuate frequencies beyond the HART band-pass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. Figure 58 shows the output current versus time operation for a typical HART signal. Table 8 specifies the performance of the HART-IN terminal.



NOTE: DC current = 6 mA.

Figure 58. Output Current vs Time

Table 8. HART-IN Terminal Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance	HART signal ac-coupled into terminal		35		kΩ
Output current (peak-to-peak)	Input signal of 500 mV (peak-to-peak)	0.9	1	1.1	mA

8.4.6.2 Implementing HART in All Current Output Modes

The use of the HART-IN terminal to implement HART modulation is limited to the case where the RANGE bits of the *Control Register* are set to the 4-mA to 20-mA range. If it is desirable to implement HART in all current-output modes, refer to Implementing HART In All Current Output Modes in *Application Information*.

8.5 Programming

Table 13 describes the available commands and registers on the DACx750 devices. *No operation*, *read operation*, and *watchdog timer* refer to commands and are not explicit registers. For more information on these commands, see the *Read Operation* and *Watchdog Timer* sections.

Programming (continued)

8.5.1 Serial Peripheral Interface (SPI)

The device is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, Microwire, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. The timing for the digital interface is illustrated in Figure 1, Figure 2, and Figure 3.

8.5.1.1 SPI Shift Register

The default frame is 24 bits wide (see *Frame Error Checking* for 32-bit frame mode) and begins with the rising edge of SCLK that clocks in the MSB. The subsequent bits are latched on successive rising edges of SCLK. The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word as shown in Table 9.

Table 9. Default SPI Frame

BIT 23:BIT 16	BIT 15:BIT 0
Address byte	Data word

The host processor must issue 24 bits before it issues a rising edge on the LATCH terminal. Input data bits are clocked in regardless of the LATCH terminal and are unconditionally latched on the rising edge of LATCH. By default, the SPI shift register resets to 0x000000 at power on or after a reset.

8.5.1.2 Write Operation

A write operation is accomplished when the address byte is set according to Table 10. For more information on the DACx750 registers, see the *Register Maps* section.

Table 10. Write Address Functions

ADDRESS BYTE (HEX)	FUNCTION
00	No operation (NOP)
01	Write DAC Data register
02	Register read
55	Write control register
56	Write reset register
57	Write configuration register
58	Write DAC gain calibration register
59	Write DAC zero calibration register
95	Watchdog timer reset

8.5.1.3 Read Operation

A read operation is accomplished when the address byte is 0x02. Follow the read operation with a no-operation (NOP) command to clock out an addressed register; see Figure 2. To read from a register, the address byte and data word is as shown in Table 11. The read register value is output MSB first on SDO on successive falling edges of SCLK.

Table 11. Default SPI Frame for Register Read

ADDRESS BYTE (HEX)	DATA WORD	
	BIT 15:BIT 6	BIT 5:BIT 0
02	X (*don't care*)	Register read address (see Table 12)

Table 12 shows the register read addresses available on the DACx750 devices.

Table 12. Register Read Address Functions

READ ADDRESS(1)	FUNCTION
XX XX00	Read status register
XX XX01	Read DAC data register
XX XX10	Read control register
00 1011	Read configuration register
01 0011	Read DAC gain calibration register
01 0111	Read DAC zero calibration register

(1) X denotes *don't care* bits.

8.5.1.4 Stand-Alone Operation

SCLK can operate in either continuous or burst mode, as long as the LATCH rising edge occurs after the appropriate number of SCLK cycles. Providing more than or less than 24 SCLK cycles before the rising edge of LATCH results in incorrect data being programmed into the device registers, and incorrect data sent out on SDO. The rising edge of SCLK that clocks in the MSB of the 24-bit input frame marks the beginning of the write cycle, and data are written to the addressed registers on the rising edge of LATCH.

8.5.1.5 Daisy-Chain Operation

For systems that contain multiple DACx750s, use the SDO terminal to daisy-chain several devices. This mode is useful in reducing the number of serial interface lines in applications that use multiple SPI devices. Daisy-chain mode is enabled by setting the DCEN bit of the control register to 1. By connecting the SDO of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed, as Figure 59 shows.

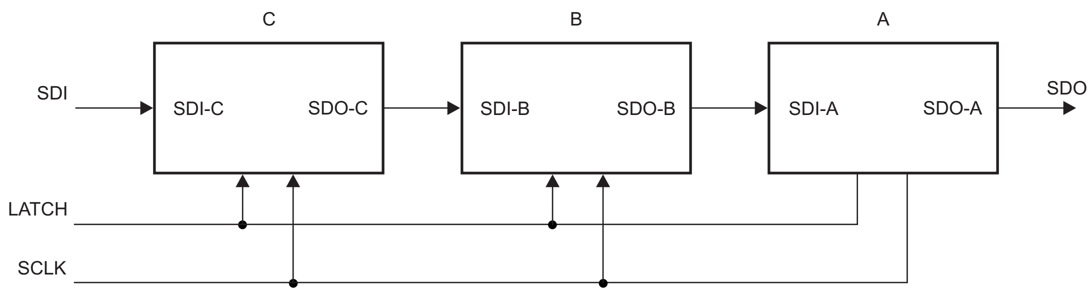


Figure 59. Three DACx750s in Daisy-Chain Mode

Like stand-alone operation, the SPI daisy-chain write operation requires one frame, and the read requires two frames. The rising edge of SCLK that clocks in the MSB of the input frame marks the beginning of the write cycle. When the serial transfer to all devices is complete, LATCH is taken high. This action transfers the data from the SPI shift registers to the device internal register of each DACx750 in the daisy-chain. However, the number of clocks in each frame in this case depends on the number of devices in the daisy chain. For two devices, each frame is 48 clocks; the first 24 clocks are for the second DAC and the next 24 bits are for the first DAC. For a readback, the data are read from the two DACs in the following 48-bit frame; the first 24 clocks are for the second DAC, and the next 24 clocks are for the first DAC. The input data to the DACs during the second frame can be another command or NOP. Similar to the two-device case described, for N devices, each frame is N × 24 clocks, where *N* is the total number of DACx750s in the chain.

The serial clock can be a continuous or gated clock. A continuous SCLK source can only be used if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data.

8.6 Register Maps

Table 13 shows the available registers on the DACx750 devices. See *DACx750 Register Descriptions* for descriptions of all DACx750 registers.

Table 13. Command and Register Map

<table>
<tr><th rowspan="2">REGISTER OR COMMAND</th><th rowspan="2">READ AND WRITE ACCESS</th><th colspan="14">DATA BITS (DB15:DB0)</th></tr>
<tr><th>15:14</th><th>13</th><th>12</th><th>11</th><th>10:9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Control</td><td>RW</td><td>X</td><td>REXT</td><td>OUTEN</td><td colspan="3">SRCLK</td><td colspan="3">SRSTEP</td><td>SREN</td><td>DCEN</td><td colspan="3">RANGE</td></tr>
<tr><td>Configuration</td><td>RW</td><td colspan="8">X(1)</td><td>CALEN</td><td>HARTEN</td><td>CRCEN</td><td>WDEN</td><td colspan="2">WDPD</td></tr>
<tr><td>DAC Data(2)</td><td>RW</td><td colspan="14">D15:D0</td></tr>
<tr><td>No operation(3)</td><td>—</td><td colspan="14">X</td></tr>
<tr><td>Read Operation(3)</td><td>—</td><td colspan="8">X</td><td colspan="6">READ ADDRESS</td></tr>
<tr><td>Reset</td><td>W</td><td colspan="13"></td><td>RESET</td></tr>
<tr><td>Status</td><td>R</td><td colspan="9">Reserved</td><td>CRC-FLT</td><td>WD-FLT</td><td>I-FLT</td><td>SR-ON</td><td>T-FLT</td></tr>
<tr><td>DAC Gain Calibration(2)</td><td>RW</td><td colspan="14">G15:G0, unsigned</td></tr>
<tr><td>DAC Zero Calibration(2)</td><td>RW</td><td colspan="14">Z15:Z0, signed</td></tr>
<tr><td>Watchdog Timer(3)</td><td>—</td><td colspan="14">X</td></tr>
</table>

(1) X denotes *don't care* bits.
(2) DAC8750 (16-bit version) shown. DAC7750 (12-bit version) contents are located in DB15:DB4. For DAC7750, DB3:DB0 are *don't care* bits when writing and zeros when reading.
(3) *No operation*, *read operation*, and *watchdog timer* are commands and not registers.

8.6.1 DACx750 Register Descriptions

8.6.1.1 Control Register

The DACx750 control register is written to at address 0x55. Table 14 shows the description for the control register bits.

Table 14. Control Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB14	Reserved	00	Reserved. Do not write any value other than zero to these bits.
DB13	REXT	0	External current setting resistor enable.
DB12	OUTEN	0	Output enable. Bit = 1: Output is determined by RANGE bits. Bit = 0: Output is disabled. IOUT is Hi-Z.
DB11:DB8	SRCLK[3:0]	0000	Slew rate clock control. Ignored when bit SREN = 0.
DB7:DB5	SRSTEP[2:0]	000	Slew rate step size control. Ignored when bit SREN = 0.
DB4	SREN	0	Slew Rate Enable. Bit = 1: Slew rate control is enabled, and the ramp speed of the output change is determined by SRCLK and SRSTEP. Bit = 0: Slew rate control is disabled. Bits SRCLK and SRSTEP are ignored. The output changes to the new level immediately.
DB3	DCEN	0	Daisy-chain enable.
DB2:DB0	RANGE[2:0]	000	Output range bits.

8.6.1.2 Configuration Register

The DACx750 configuration register is written to at address 0x57. Table 15 summarizes the description for the configuration register bits.

Table 15. Configuration Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB6	Reserved	00 0000 0000	Reserved. Do not write any value other than zero to these bits.
DB5	CALEN	0	User calibration enable. When user calibration is enabled, the DAC data are adjusted according to the contents of the gain and zero calibration registers. See the *User Calibration* section.
DB4	HARTEN	0	Enable interface through HART-IN terminal (only valid for IOUT set to 4-mA to 20-mA range through RANGE bits). Bit = 1: HART signal is connected through internal resistor and modulates output current. Bit = 0: HART interface is disabled.
DB3	CRCEN	0	Enable frame error checking.
DB2	WDEN	0	Watchdog timer enable.
DB1:DB0	WDPD[1:0]	00	Watchdog timeout period.

8.6.1.3 DAC Registers

The DAC registers consist of a DAC data register (Table 16), a DAC gain calibration register (Table 17), and a DAC zero calibration register (Table 18). User calibration as described in the *User Calibration* section is a feature that allows for trimming the system gain and zero errors. Table 16 through Table 18 show the DAC8750, 16-bit version of these registers. The DAC7750 (12-bit version) register contents are located in DB15:DB4. For DAC7750, DB3:DB0 are *don't care* bits when writing and zeros when reading.

Table 16. DAC Data Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	D15:D0	0x0000	DAC data register. Format is unsigned straight binary.

Table 17. DAC Gain Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	G15:G0	0x0000	Gain calibration register for user calibration. Format is unsigned straight binary.

Table 18. DAC Zero Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	Z15:Z0	0x0000	Zero calibration register for user calibration. Format is twos complement.

8.6.1.4 Reset Register

The DACx750 reset register is written to at address 0x56. Table 19 provides the description.

Table 19. Reset Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB1	Reserved	000 0000 0000 0000	Reserved. Writing to these bits does not cause any change.
DB0	RESET	0	Software reset bit. Writing 1 to the bit performs a software reset that resets all registers and the ALARM status to the respective power-on reset default value. After reset completes, the RESET bit clears itself.

8.6.1.5 Status Register

This read-only register consists of four $\overline{\text{ALARM}}$ status bits (CRC-FLT, WD-FLT, I-FLT, and T-FLT) and the SR-ON bit that shows the slew rate status, as shown in Table 20.

Table 20. Status Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB5	Reserved	000 0000 0000	Reserved. Reading these bits returns 0.
DB4	CRC-FLT	0	Bit = 1 indicates CRC error on SPI frame. Bit = 0 indicates normal operation.
DB3	WD-FLT	0	Bit = 1 indicates watchdog timer timeout. Bit = 0 indicates normal operation.
DB2	I-FLT	0	Bit = 1 indicates an open circuit or a compliance voltage violation in IOUT loading. Bit = 0 indicates IOUT load is at normal condition.
DB1	SR-ON	0	Bit = 1 when DAC code is slewing as determined by SRCLK and SRSTEP. Bit = 0 when DAC code is not slewing.
DB0	T-FLT	0	Bit = 1 indicates die temperature is over 142°C. Bit = 0 indicates die temperature is not over 142°C.

These devices continuously monitor the current output and die temperature. When an alarm occurs, the corresponding $\overline{\text{ALARM}}$ status bit is set (1). Whenever an $\overline{\text{ALARM}}$ status bit is set, it remains set until the event that caused it is resolved. The $\overline{\text{ALARM}}$ bit can only be cleared by performing a software reset, a power-on reset (by cycling power), or by having the error condition resolved. These bits are reasserted if the alarm condition continues to exist in the next monitoring cycle.

The $\overline{\text{ALARM}}$ bit goes to 0 when the error condition is resolved.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Implementing HART in All Current Output Modes

If it is desirable to implement HART irrespective of the RANGE bit settings, there are two ways to do this.

9.1.1.1 Using CAP2 Terminal

The first method of implementing HART is to couple the signal through the CAP2 pin, as shown in Figure 60. Note that this pin is only available in the 40-pin VQFN package

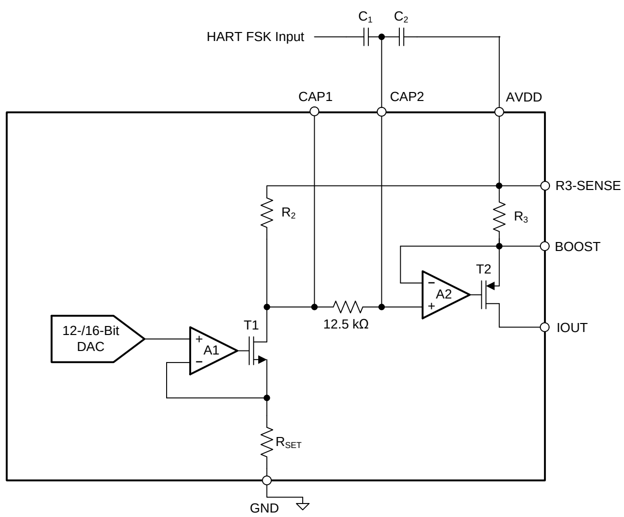


Figure 60. Implementing HART on IOUT Using the CAP2 Terminal

In Figure 60, R_3 is nominally 40 Ω, and R_2 is dependent on the current output range (set by the RANGE bits), described as follows:

- 4-mA to 20-mA range: R_2 = 2.4 kΩ (typical)
- 0-mA to 20-mA range: R_2 = 3 kΩ (typical)
- 0-mA to 24-mA range: R_2 = 3.6 kΩ (typical)

The purpose of the 12.5-kΩ resistor is to create a filter when CAP1 and CAP2 are used.

To insert the external HART signal on the CAP2 terminal, an external ac-coupling capacitor is typically connected to CAP2. The high pass filter 3-dB frequency is determined by the resistive impedance looking into CAP2 (R_2 + 12.5 kΩ) and the coupling-capacitor value. The 3-dB frequency is $1 / (2 \times \pi \times [R_2 + 12.5\ k\Omega] \times [\text{Coupling Capacitor Value}])$.

When the input HART frequency is greater than the 3-dB frequency, the ac signal is seen at the plus input of amplifier A2 and is therefore seen across the 40-Ω resistor. To generate a 1-mA signal on the output therefore requires a 40-mV peak-to-peak signal on CAP2. Because most HART modems do not output a 40-mV signal, a capacitive divider is used in Figure 60 to attenuate the FSK signal from the modem. In Figure 60, the high-pass cutoff frequency is $1 / (2 \times \pi \times [R_2 + 12.5\ k\Omega] \times [C_1 + C_2])$. There is one disadvantage to this approach: if the AVDD supply is not clean, any ripple on it could couple into the part.

Application Information (continued)

9.1.1.2 Using the ISET-R Pin

The second method to implement HART is to couple the HART signal through the ISET-R terminal when IOUT is operated using an external R_{SET} resistor. The FSK signal from the modem is ac-coupled into the terminal through a series combination of Rin and Cin as shown in Figure 61.

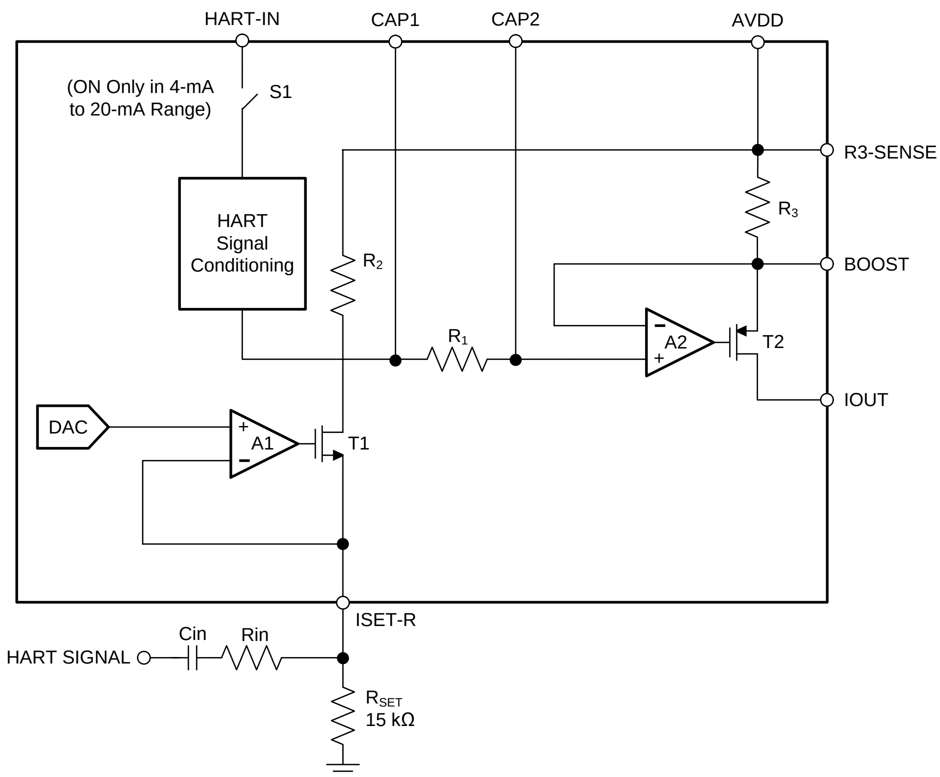


Figure 61. Implementing HART with the ISET-R Terminal

The magnitude of the ac-current output is calculated with Equation 6.

$$(V_{HART} \times k) / Rin \quad (6)$$

where

- V_{HART} is the amplitude of the HART FSK signal from the modem
- k is a constant that represents the gain transfer function from the ISET-R terminal to the IOUT terminal and depends on the selected current output range as follows:
  - k = 60 for the 4-mA to 20-mA range
  - k = 75 for the 0-mA to 20-mA range
  - k = 90 for the 0-mA to 24-mA range

The series input resistor and capacitor form a high-pass filter at the ISET-R terminal. Select Cin to make sure that all signals in the HART extended-frequency band pass through unattenuated.

9.2 Typical Application

9.2.1 Voltage and Current Output Driver for Factory Automation AND Control, EMC/EMI Protected

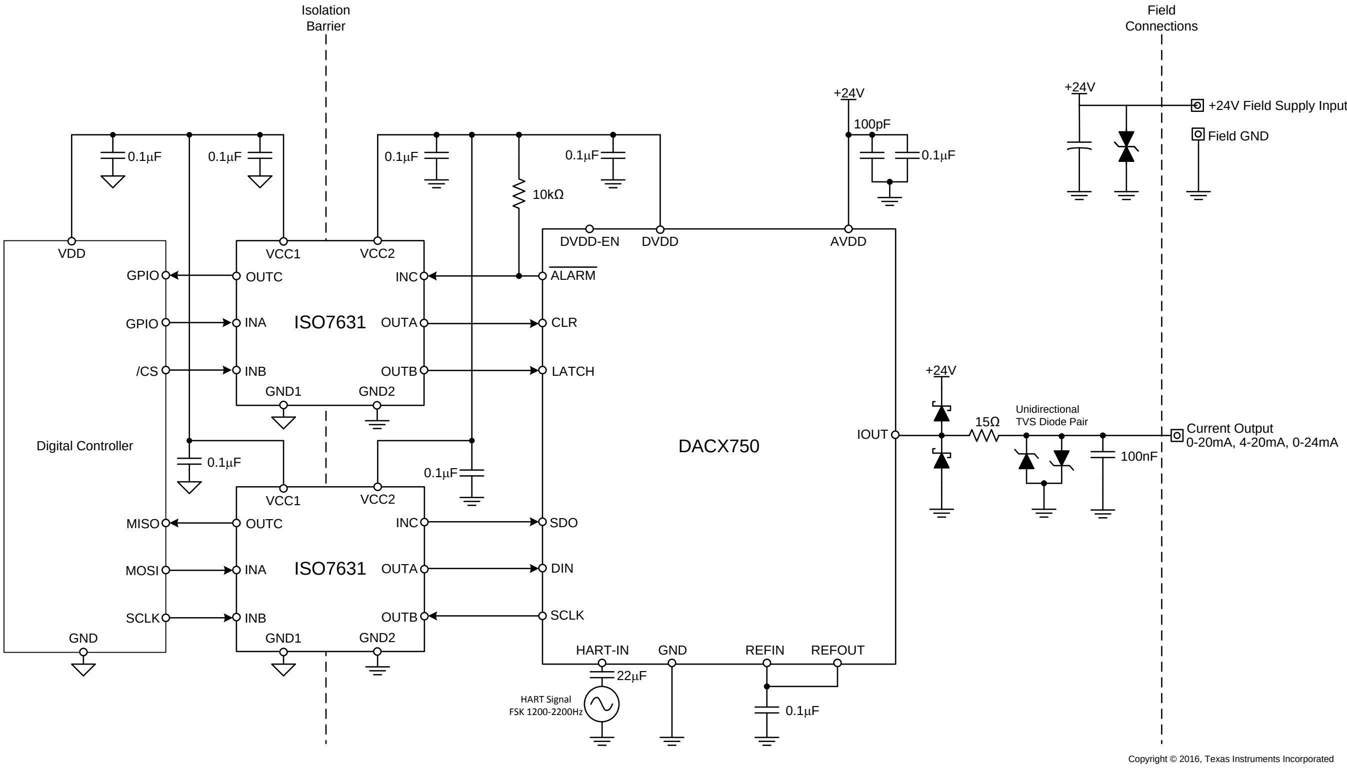


Figure 62. DACx750 in an Analog Output (AO) Module

9.2.1.1 Design Requirements

Analog I/O modules are used by programmable logic controllers (PLCs) and distributed control systems (DCSs) to interface to sensors, actuators, and other field instruments. These modules must meet stringent electrical specifications for both performance as well as protection. These outputs are typically current loops based on the 4-mA to 20-mA range. Common error budgets accommodate 0.1% full-scale range total unadjusted error (% FSR TUE) at room temperature. Designs which desire stronger accuracy over temperature frequently implement calibration. Often times the PLC back-plane provides access to a 12-V to 36-V analog supply from which a majority of supply voltages are derived.

9.2.1.2 Detailed Design Procedure

Figure 63 illustrates a common generic solution for realizing these desired voltage and current output spans.

Typical Application (continued)

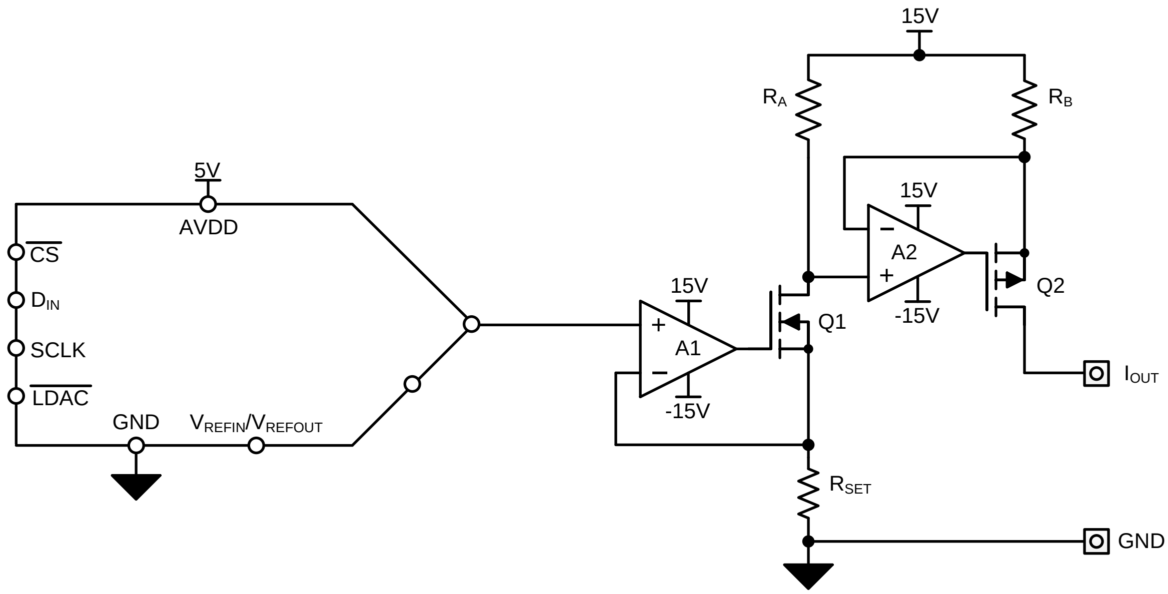


Figure 63. Generic Design for Typical PLC Current and Voltage Outputs

The current output circuit is comprised of amplifiers A1 and A2, MOSFETs Q1 and Q1, and the three resistors R_{SET}, R_A, and R_B. This two-stage current source enables the ground-referenced DAC output voltage to drive the high-side amplifier required for the current-source.

The high-level of integration of the DACx750 family lends itself very well to the design of analog output modules, offering simplicity of design and reducing solution size. The DACx750 integrates all of the components shown in Figure 63 allowing a software configurable current output driver. Figure 62 illustrates an example circuit design for such an application using the DACx750 for the current output driver.

The design uses two triple channel isolators (ISO7631FC) to provide galvanic isolation for the digital lines to communicate to the main controller. Note that these isolators can be driven by the internally-generated supply (DVDD) from the DACx750 to save components and cost. The DACx750 supplies up to 10 mA that meets the supply requirements of the two isolators running at up to 10 Mbps. Note that additional cost savings are possible if noncritical digital signals such as CLR and ALARM are tied to GND or left unconnected. Finally, a protection scheme with transient voltage suppressors and other components is placed on all pins which connect to the field.

The protection circuitry is designed to provide immunity to the IEC61000-4 test suite which includes system-level industrial transient tests. The protection circuit includes transient voltage suppressor (TVS) diodes, clamp-to-rail steering diodes, and pass elements in the form of resistors and ferrite beads. For more detail about selecting these components, refer to *Single-Channel Industrial Voltage & Current Output Driver, Isolated, EMC/EMI Tested Reference Design*.

9.2.1.3 Application Curve

The current output circuit was measured in 0-mA to 24-mA mode using an 8.5 digit digital multi-meter to measure the output while driving a 300-Ω load at 25°C. The measured results are illustrated in Figure 64. The current output remains within the data sheet specified performance.

The design was also exposed to IEC61000-4 electrostatic discharge, electrically fast transient, conducted immunity, and radiated immunity tests on both the current and voltage outputs. During each of these tests a 6.5 digit digital multi-meter, set in fast 5.5 digit acquisition mode, was used to monitor the output. Complete data sets for the voltage and current outputs during these tests are available in *Single-Channel Industrial Voltage & Current Output Driver, Isolated, EMC/EMI Tested Reference Design*.

Typical Application (continued)

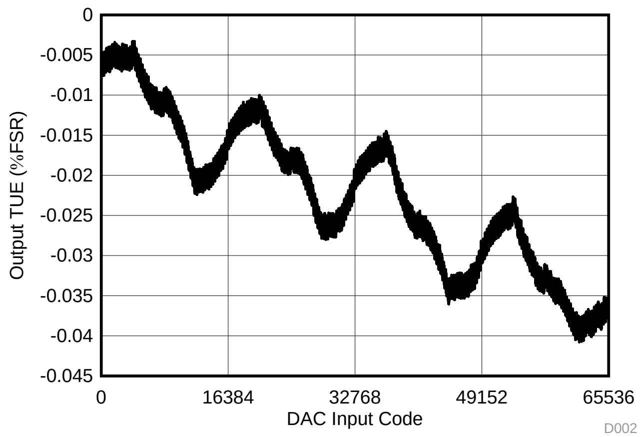


Figure 64. Current Output TUE vs Code

10 Power Supply Recommendations

The DACx750 family can operate within the specified single-supply range of 10 V to 36 V applied to the AVDD pin. The digital supply, DVDD, can operate within the specified supply range of 2.7 V to 5.5 V or be powered by the internal 4.6-V LDO. Switching power supplies and DC/DC converters often have high frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can be easily coupled into the DAC output voltage or current through various paths between the power connections and analog output. TI recommends including bulk and local decoupling capacitors to further reduce noise. The current consumption on the AVDD pin and current ranges for the current output are listed in *Electrical Characteristics*. The power supply must meet the requirements listed in the *Electrical Characteristics* table.

11 Layout

11.1 Layout Guidelines

To maximize the performance of the DACx750 in any application, good layout practices and proper circuit design must be followed. A few recommendations specific to the DACx750 are:

1. As illustrated in Figure 60, CAP2 is directly connected to the input of the final IOUT amplifier. Any noise or unwanted ac signal routed near the CAP1 and CAP2 terminals could capacitively couple onto internal nodes and affect IOUT. Therefore, it is important to avoid routing any digital or HART signal traces over the CAP1 and CAP2 traces.
2. Connect the thermal PAD to the lowest potential in the system.
3. Make sure that AVDD has decoupling capacitors local to the respective terminals.
4. Place the reference capacitor close to the reference input terminal.
5. Avoid routing switching signals near the reference input.
6. For designs that include protection circuits:
   a. Place diversion elements, such as TVS diodes or capacitors, close to off-board connectors to make sure that return current from high-energy transients does not cause damage to sensitive devices.
   b. Use large, wide traces to provide a low-impedance path to divert high-energy transients away from I/O terminals.

11.2 Layout Example

Figure 65 shows an example layout for the DAC8760 and DAC7760 devices from TIPD153. A similar layout can be used for the DACx750 with a few modifications to account for pinout differences.

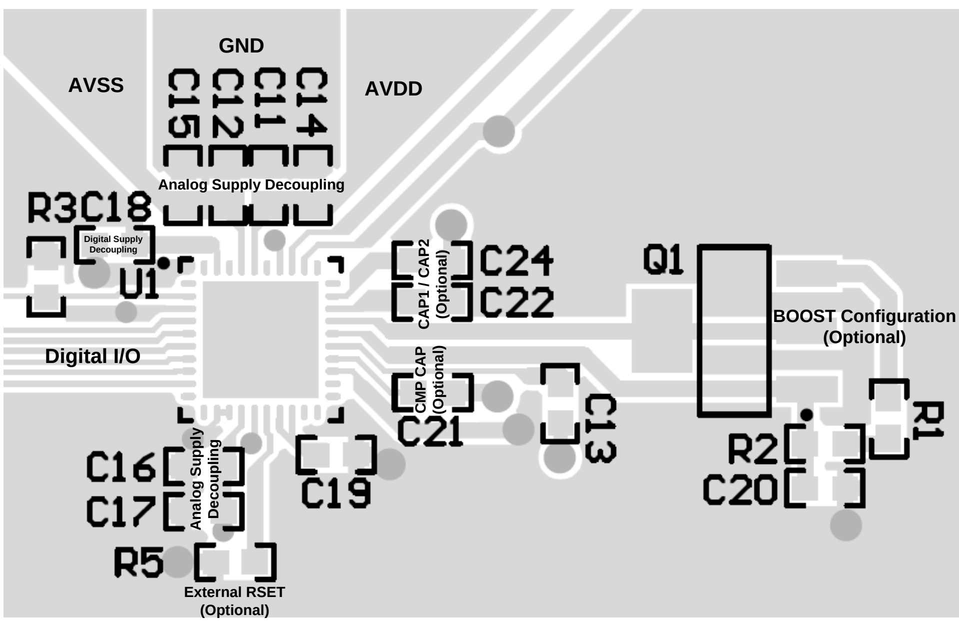


Figure 65. Example Layout

11.3 Thermal Considerations

The DACx750 is designed for a maximum junction temperature of 150°C. In cases where the maximum AVDD is driving maximum current into ground, this junction temperature can be exceeded. Use Equation 7 to determine the maximum junction temperature that can be reached.

$$\text{Power dissipation} = (T_J \max - T_A) / \theta_{JA} \quad (7)$$

where

- T_J max = 150°C
- T_A is the ambient temperature
- θ_{JA} is the package-dependent, junction-to-ambient thermal resistance, found in *Thermal Information*.

The power dissipation is calculated by multiplying all the supply voltages with the currents supplied, which are found in the *Power Requirements* subsection of *Electrical Characteristics*.

Consider an example: IOUT is enabled, supplying 24 mA into GND with a 25°C ambient temperature, AVDD of 24 V, and DVDD is generated internally. From the *Electrical Characteristics*, the max value of AIDD = 3 mA when IOUT is enabled and DAC code = 0x0000. Also, the max value of DIDD = 1 mA. Accordingly, the worst-case power dissipation is 24 V × (24 mA + 3 mA + 1 mA) = 672 mW. Using the θ_{JA} value for the TSSOP package, we get T_J max = 25°C + (32.3 × 0.672)°C = 46.7°C. At 85°C ambient temperature, the corresponding value of T_J max is 106.7°C. Using this type of analysis, the system designer can both specify and design for the equipment operating conditions. Note that for enhanced thermal performance, connect the thermal pad in both packages to a copper plane.

12 器件和文档支持

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *经 EMC/EMI 测试的隔离式单通道工业电压和电流输出驱动器参考设计*
- *《采用 DAC8760 系列实现 HART™ 通信》*

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 **21.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
DAC7750	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DAC8750	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.
HART is a registered trademark of HART Communication Foundation.
SPI, QSPI are trademarks of Motorola, Inc.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7750IPWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC7750IPWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC7750IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC7750IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750	Samples
DAC8750IPWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples
DAC8750IPWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples
DAC8750IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples
DAC8750IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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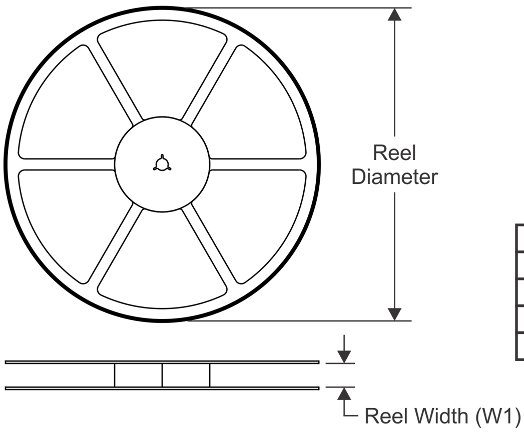
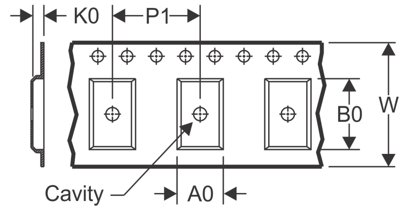
TAPE AND REEL INFORMATION

REEL DIMENSIONS

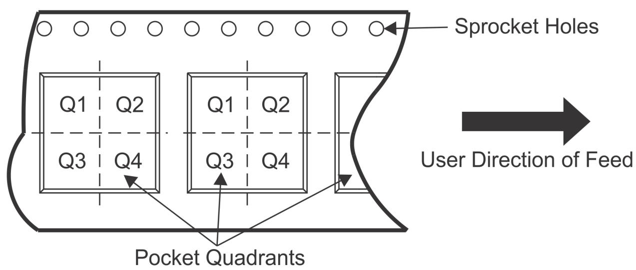


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

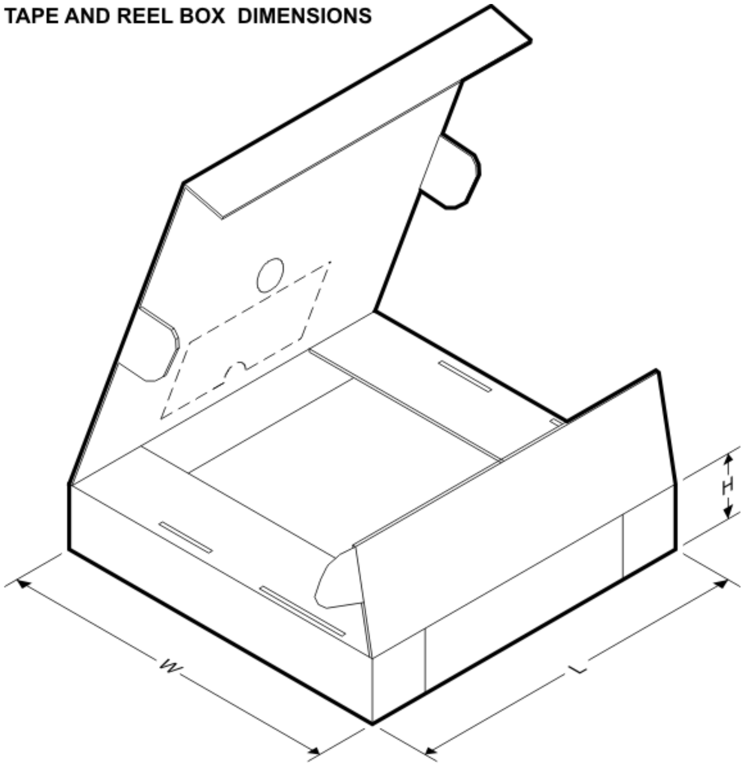
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7750IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC7750IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC7750IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8750IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC8750IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8750IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7750IPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC7750IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC7750IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
DAC8750IPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC8750IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC8750IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

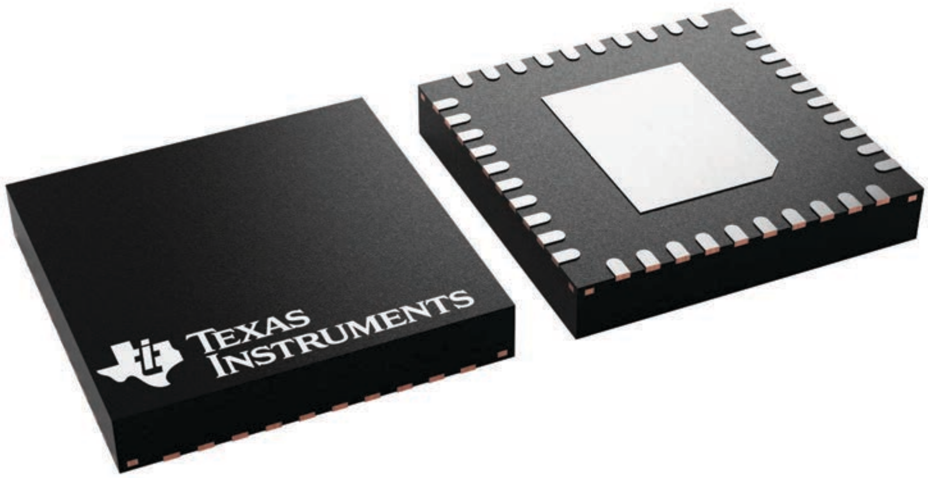
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

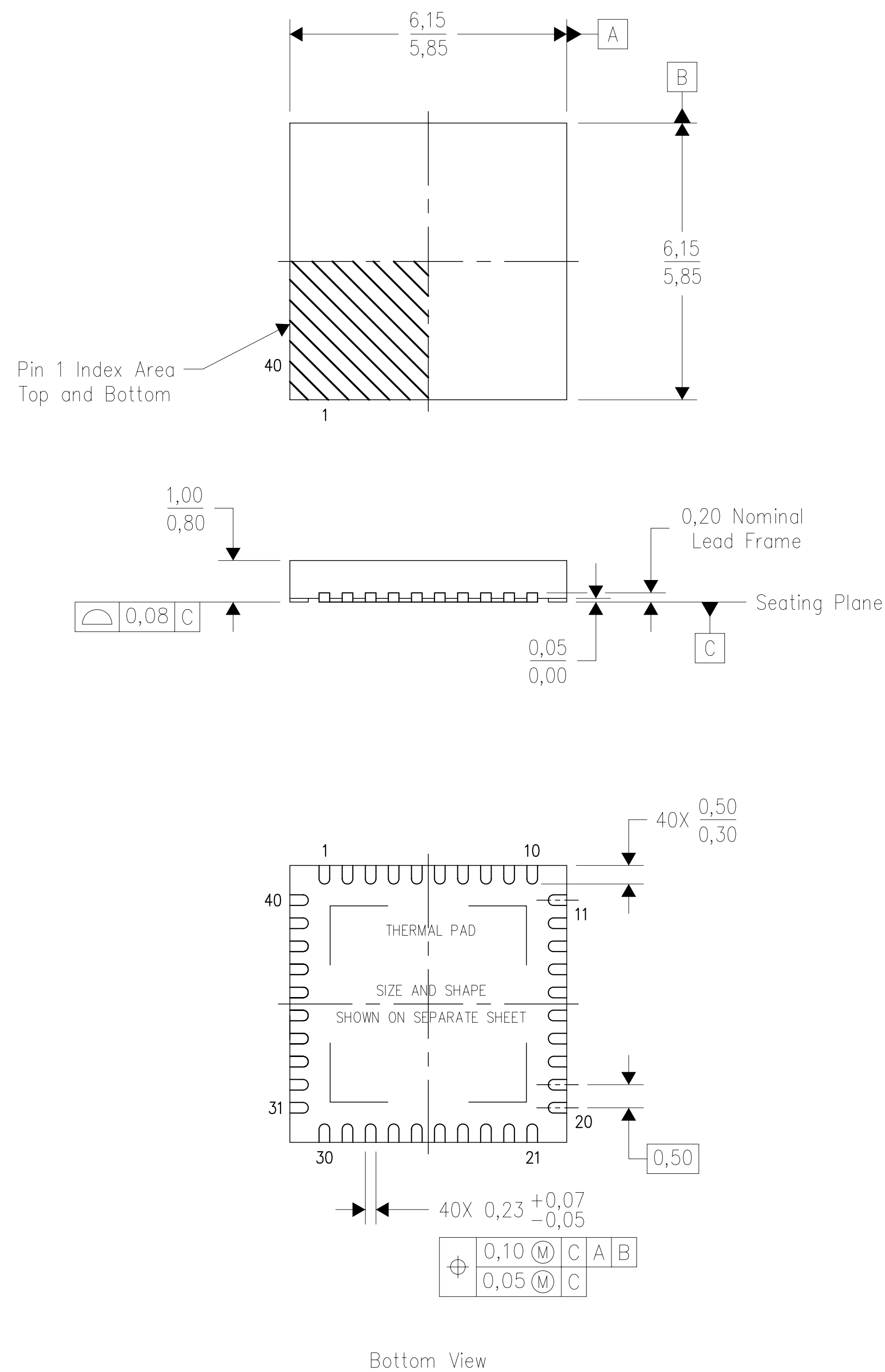
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Package complies to JEDEC MO–220 variation VJJD–2.

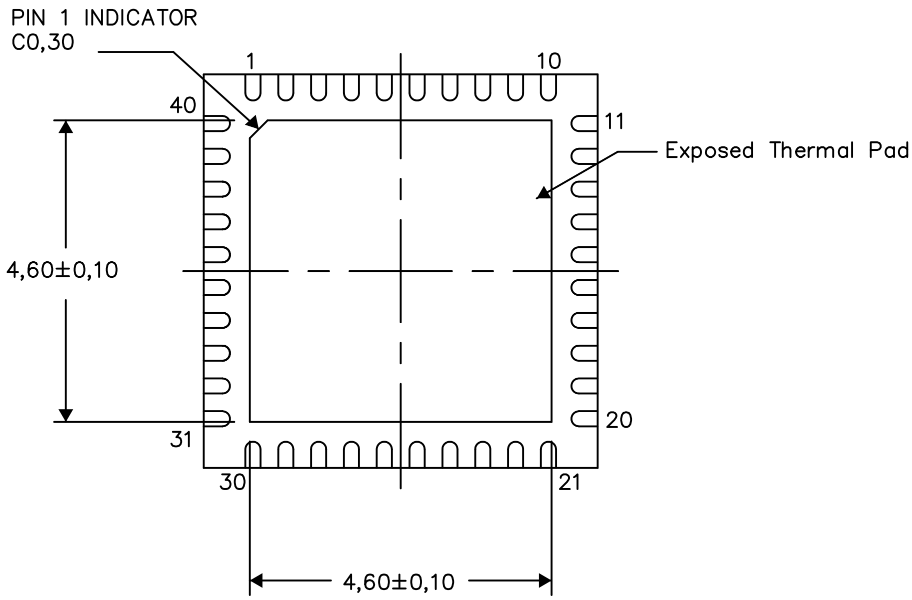
RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



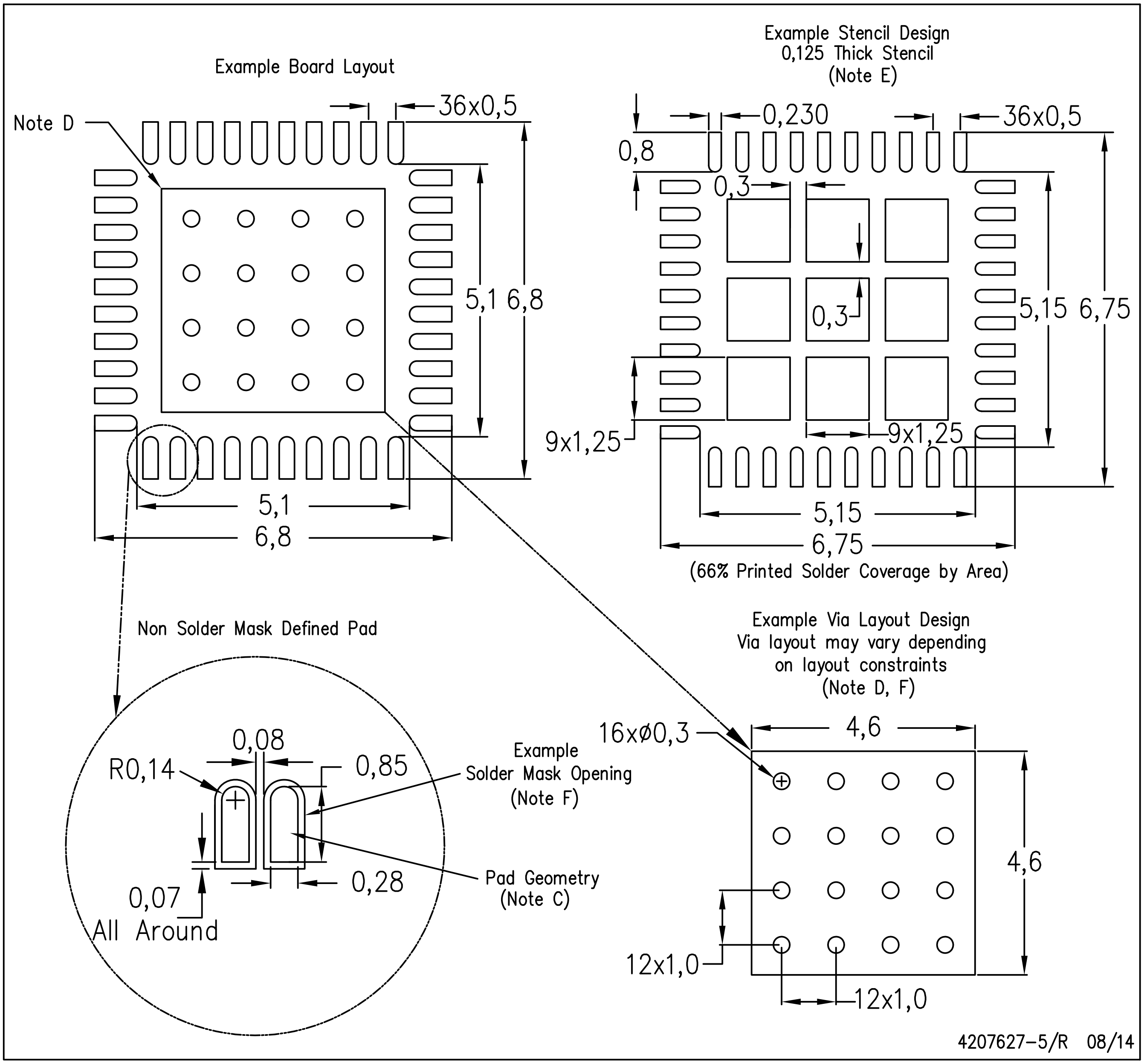
Bottom View

Exposed Thermal Pad Dimensions

4206355-5/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

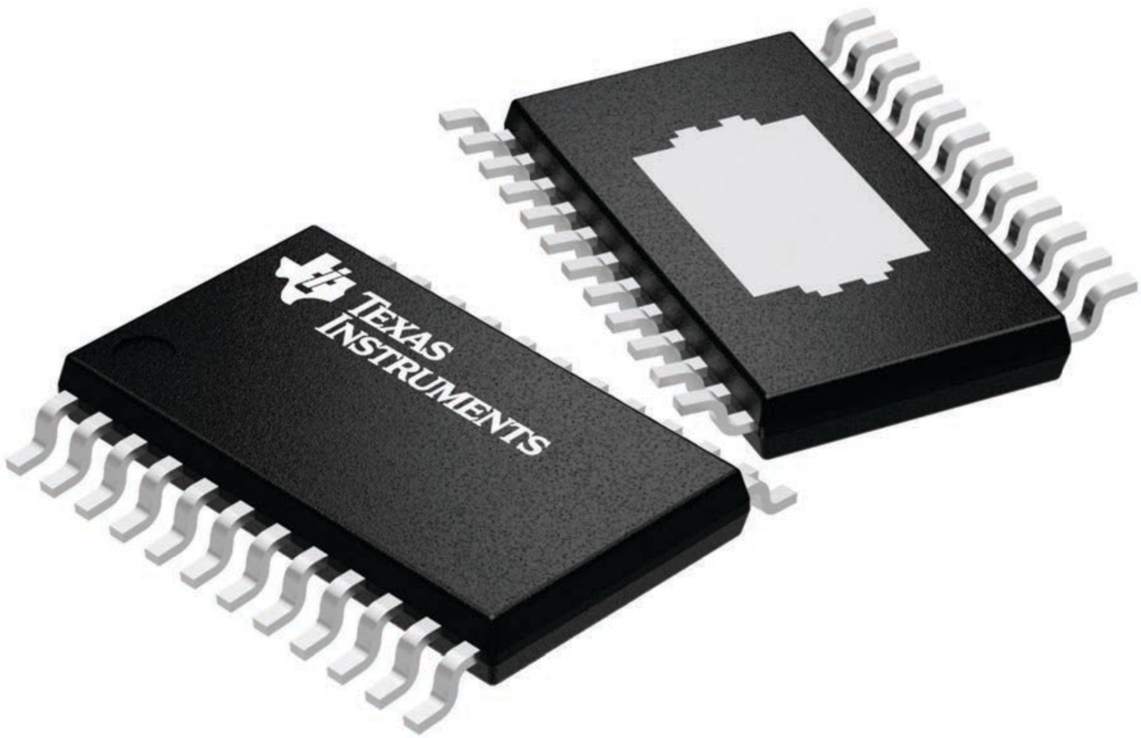
PWP 24

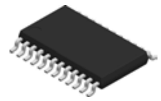
PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

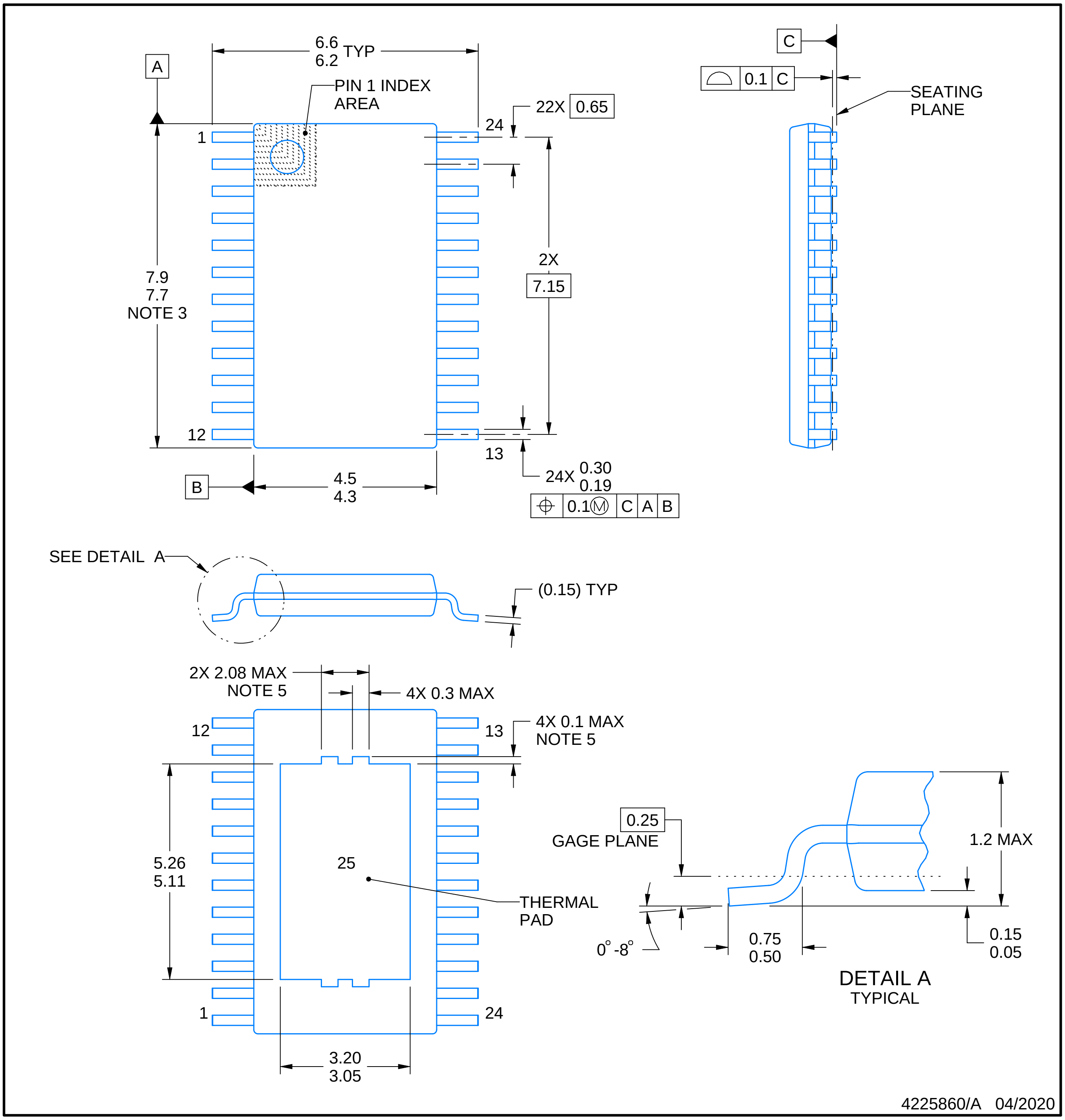
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





PACKAGE OUTLINE

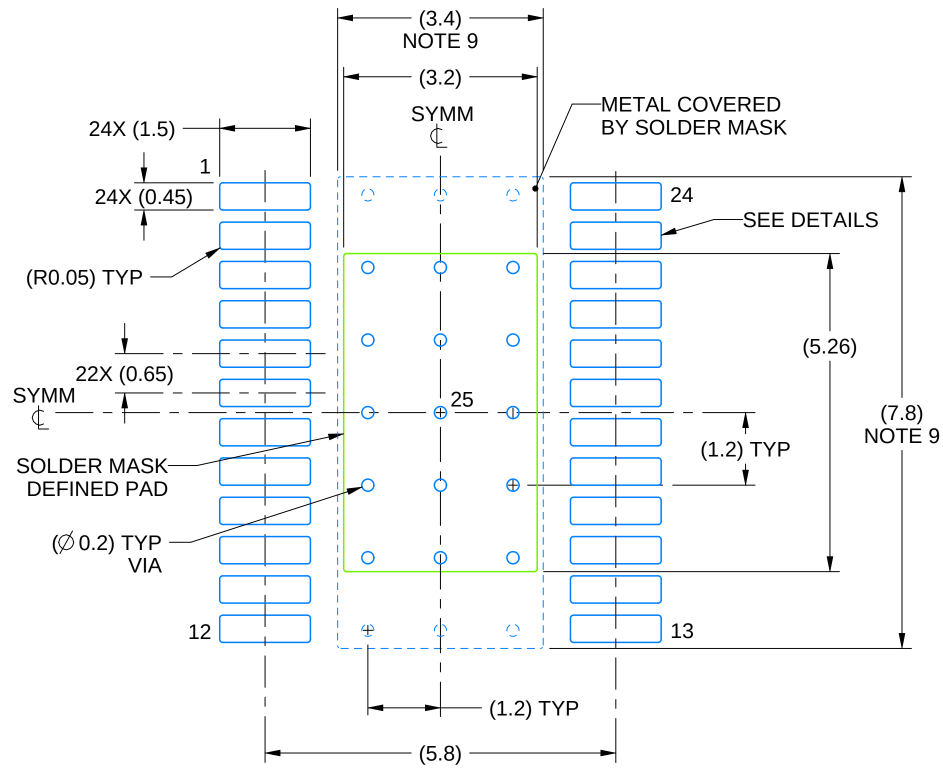
SMALL OUTLINE PACKAGE



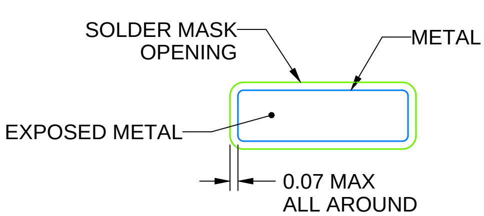
PowerPAD is a trademark of Texas Instruments.

NOTES:

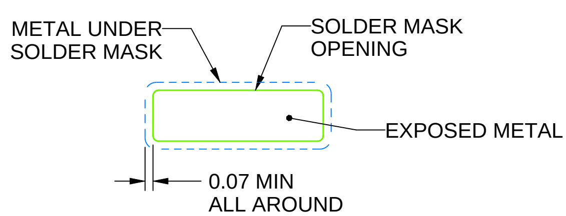
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



NON-SOLDER MASK
DEFINED



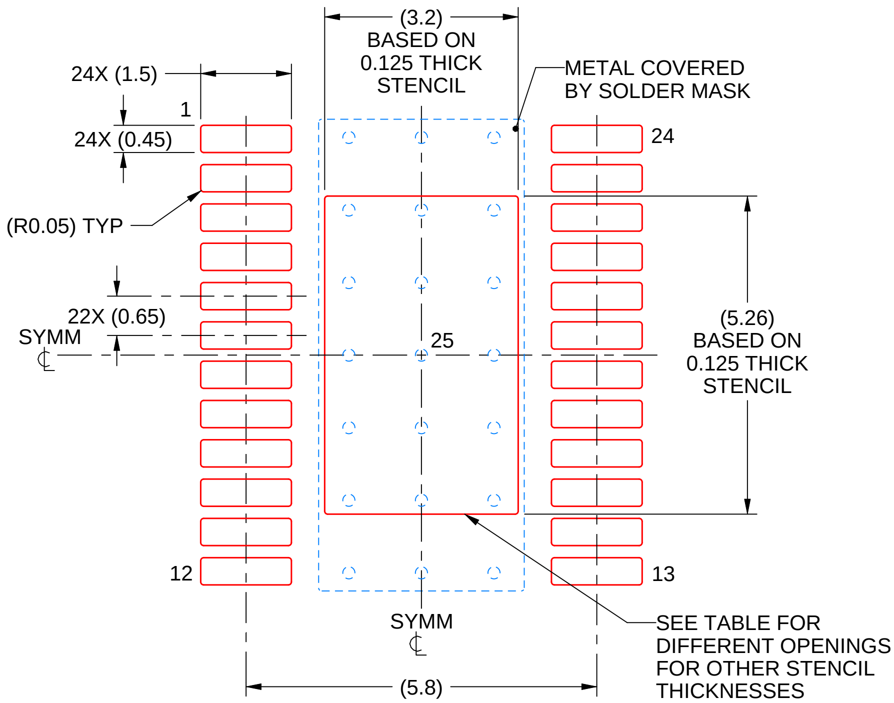
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225860/A 04/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

4225860/A 04/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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