

Gate Driver Providing Galvanic Isolation Series Isolation Voltage 2500 Vrms 1ch Gate Driver Providing Galvanic Isolation

BM60059FV-C

General Description

The BM60059FV-C is a gate driver with an isolation voltage of 2500 Vrms. It has an I/O delay time of 450 ns, minimum input pulse width of 400 ns, and incorporates the fault signal output function, under voltage lockout (UVLO) function, short circuit protection (SCP) function, active miller clamping function, temperature monitoring, switching controller function, gate constant current driving function and output state feedback function.

Features

- AEC-Q100 Qualified^(Note 1)
- Fault Signal Output Function
- Under Voltage Lockout Function
- Short Circuit Protection Function
- Fast Turn Off Function for Short Circuit Protection Soft Turn Off Function for Short Circuit Protection (Adjustable turn off time)
- Active Miller Clamping
- **Temperature Monitor**
- Switching Controller
- Gate Constant Current Driving Function
- Output State Feedback Function

(Note 1) Grade1

Applications

- Automotive Inverter System
- Automotive DCDC Converter
- Industrial Inverter System
- **UPS System**

Typical Application Circuit

Key Specifications

- **Isolation Voltage:**
- Maximum Gate Drive Voltage:
- I/O Delay Time:
- Minimum Input Pulse Width:

2500 Vrms 24 V 450 ns (Max) 400 ns

Package

SSOP-B28W

W (Typ) x D (Typ) x H (Max) 9.2 mm x 10.4 mm x 2.4 mm





OProduct structure : Silicon integrated circuit OThis product has no designed protection against radioactive rays.

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Recommended Range of External Constants

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Pin Name	Symbol	Min	Тур	Max	Unit
TC (As Temperature monitor)	R _{TC}	1.25	-	50	kΩ
TC (No Temperature monitor)	R _{TC}	0.1	1	10	MΩ
V_BATT	C_{VBATT}	3	-	-	μF
VCC2	C _{VCC2}	0.4	-	-	μF
VREG	CVREG	0.3	1	10	μF

C_{VREG} : For supplying gate charge current of MOS for fly back converter and driving internal transformer.

 C_{VCC2} : For supplying gate charge current of MOS FET/IGBT.

Pin Configurations



Pin Descriptions

Pin No.	Pin Name	Function
1	GND2	Output-side ground pin
2	PROOUT2	Fast turn off pin for short circuit protection
3	PROOUT1	Soft turn off pin for short circuit protection / Gate voltage input pin
4	SCPIN1	Short circuit detection pin 1
5	SCPIN2	Short circuit detection pin 2
6	TO1	Constant current output pin / Sensor voltage input pin 1
7	TO2	Constant current output pin / Sensor voltage input pin 2
8	TC	Resistor connection pin for setting constant current source output
9	VCC2	Output-side power supply pin
10	OUTREF	Reference voltage pin for constant current driving
11	OUT1HG	Source side MOS buffer driving pin
12	OUT1L	Sink side output pin
13	OUT2	Output pin for Miller Clamp
14	GND2	Output-side ground pin
15	GND1	Input-side ground pin
16	FLT	Fault output pin
17	DIS	Input enabling signal input pin
18	INA	Control input pin
19	TO_SEL	Temperature information selecting pin
20	SENSOR	Temperature information output pin
21	OSFB	Output state feedback output pin
22	FB	Error amplifier inverting input pin for switching controller
23	COMP	Error amplifier output pin for switching controller
24	V_BATT	Main power supply pin
25	VREG	Input-side internal power supply pin
26	FET_G	MOS FET for transformer drive control pin for switching controller
27	SENSE	Current feedback resistor connection pin for switching controller
28	GND1	Input-side ground pin

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Main Power Supply Voltage	VBATTMAX	-0.3 to +40.0 ^(Note 2)	V
Input-side Control Block Supply Voltage	V _{REGMAX}	-0.3 to +7.0 ^(Note 2)	V
Output-side Supply Voltage	V _{CC2MAX}	-0.3 to +30.0 ^(Note 3)	V
INA, DIS, TOSEL Pin Input Voltage	VINMAX	-0.3 to +7.0 ^(Note 2)	V
FLT, OSFB Pin Input Voltage	V _{FLTMAX}	-0.3 to +7.0 ^(Note 2)	V
FLT, OSFB Pin Output Current	I _{FLT}	10	mA
SENSOR Pin Output Current	I _{SENSOR}	10	mA
FB Pin Input Voltage	V _{FBMAX}	-0.3 to V _{BATT} + 0.3 or + 4.3 ^(Note 2)	V
FET_G Pin Output Current (Peak 5 µs)	I _{FET_GPEAK}	1	А
SCPIN1, SCPIN2 pin Input Voltage	V _{SCPINMAX}	-0.3 to +6.0 ^(Note 3)	V
TO1, TO2 Pin Input Voltage	V _{TOMAX}	-0.3 to V _{CC2} + 0.3 ^(Note 3)	V
TO1, TO2 Pin Output Current	I _{TOMAX}	8	mA
OUT1L Pin Output Current (Peak 5 µs)	I _{OUT1LPEAK}	self limited ^(Note 4)	А
OUT2 Pin Output Current (Peak 5 µs)	I _{OUT2PEAK}	self limited ^(Note 4)	А
PROOUT1 Pin Output Current (Peak 10 µs)	I _{PROOUT1PEAK}	self limited ^(Note 4)	А
PROOUT2 Pin Output Current (Peak 5 µs)	I _{PROOUT2PEAK}	self limited ^(Note 4)	А
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 2) Relative to GND1 (Note 3) Relative to GND2

(*Note 4*) Should not exceed Tjmax = $150 \degree$ C

Thermal Resistance(Note 5)

	Currential	Thermal Resistance (Typ)		Linit		
Parameter			Symbol	1s ^(Note 7) 2s	s2p ^(Note 8)	Unit
SSOP-B28W			<u> </u>	<u> </u>		
Junction to Ambient			θ_{JA}	112.9	64.4	°C/W
Junction to Top Characterization Parameter ^(Note 6) Ψ_{JT}				34	23	°C/W
Iote 6) The thermal characterization surface of the component p Iote 7) Using a PCB board based of Iote 8) Using a PCB board based of	ackage. on JESD51-3.	report the difference between	junction tempera	ature and the temperature at	the top center	of the out
Layer Number of Measurement Board	Material	Board Size				
Single	FR-4	114.3 mm x 76.2 mm >	k 1.57 mmt			
Тор						
Copper Pattern	Thickness					
Footprints and Traces	70 µm					
Layer Number of Measurement Board	Material	Board Size				
4 Layers	FR-4	114.3 mm x 76.2 mm	x 1.6 mmt			
Тор		2 Internal Laye	ers	Bottom		7
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness	S
	1		+	74.2 mm x 74.2 mm		

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Main Power Supply Voltage	V _{BATT} ^(Note 9)	4.5	24.0	V
Output-side Supply Voltage	V _{CC2} ^(Note 10)	14	24	V
TO1, TO2 pin Input Voltage	V _{TO} ^(Note 10)	1.35	3.84	V
Operating Temperature	Topr	-40	+125	°C

(Note 9) Relative to GND1 (Note 10) Relative to GND2

(Note 10) Relative to GND2

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance ($V_{IO} = 500 \text{ V}$)	Rs	> 10 ⁹	Ω
Insulation Withstand Voltage (1 min)	V _{ISO}	2500	Vrms
Insulation Test Voltage (1 s)	V _{ISO}	3000	Vrms

Electrical Characteristics (Unless otherwise specified Ta = -40 °C to +125 °C, V_{BATT} = 5 V to 24 V, V_{CC2} = 14 V to 24 V)

nless otherwise specified Ta = -4 Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General			71			
Main Power Supply	I _{BATT1}	0.5	1.2	2.0	mA	FET_G switching operation
Circuit Current 1	·DATT	0.0				INA, DIS not switching
Main Power Supply	I _{BATT2}	0.4	1.1	1.9	mA	FET_G Not switching
Circuit Current 2	-DATI2					INA, DIS not switching
Main Power Supply	I _{BATT3}	0.6	1.3	2.1	mA	FET_G switching operation INA = 10 kHz,
Circuit Current 3			-			Duty = 50 % DIS = L
Main Power Supply Circuit Current 4	I _{BATT4}	0.6	1.4	2.3	mA	FET_G switching operation INA = 20 kHz, Duty = 50 % DIS = L
Output-side Circuit Current	I _{CC2}	2.8	5.0	7.6	mA	$R_{TC} = 10 \text{ k}\Omega$
VREG Output Voltage 1	V _{REG1}	4.5	5.0	5.5	V	$5 \text{ V} \le \text{V}_{BATT} \le 24 \text{ V}$
VREG Output Voltage 2	V _{REG2}	4.0	4.5	-	V	$V_{BATT} = 4.5 V$
Switching Controller	- REOZ					VBAIT - NO V
FET_G Output Voltage H1	V _{FETGH1}	4.5	5.0	5.5	V	$5 \text{ V} \le \text{V}_{BATT} \le 24 \text{ V}$ I _{FET_G} = 0 A (open)
FET_G Output Voltage H2	V _{FETGH2}	4.0	4.5	_	V	V _{BATT} = 4.5 V
FET_G Output Voltage L	V _{FETGL}	0	-	0.3	V	$I_{FET_G} = 0 A (open)$ $I_{FET_G} = 0 A (open)$
FET_G On Resistance (Source-side)	R _{ONGH}	3	6	12	Ω	$I_{\text{FET}_G} = -10 \text{ mA}$
FET_G On Resistance (Sink-side)	R _{ONGL}	0.3	0.6	1.3	Ω	$I_{FET_G} = +10 \text{ mA}$
Oscillation Frequency	f _{OSC_SW}	170	200	230	kHz	
Soft-start Time	t _{SS}	-	-	50	ms	
FB Threshold Voltage	V _{FB}	1.47	1.50	1.53	V	
FB Input Current	I _{FB}	-0.8	0	+0.8	μA	
COMP Output Sink Current	I _{COMPSINK}	-160	-80	-40	μA	
COMP Output Source Current	ICOMPSOURCE	40	80	160	μA	
V_BATT UVLO Off Voltage	VUVLOBATTH	4.05	4.25	4.45	V	
V BATT UVLO On Voltage	VUVLOBATTL	3.95	4.15	4.35	V	
Maximum On Duty	D _{ONMAX}	75	85	95	%	
Logic Block						
Logic High Level Input Voltage	V _{INH}	$0.7 \text{ x } V_{\text{REG}}$	-	5.5	V	INA, DIS, TO_SEL
Logic Low Level Input Voltage	V _{INL}	0	-	0.3 x V _{REG}	V	INA, DIS, TO_SEL
Logic Pull Down Resistance	R _{IND}	25	50	100	kΩ	INA, TO_SEL
Logic Pull Up Resistance	RINU	25	50	100	kΩ	DIS
Logic Input Filtering Time	t _{INFIL}	80	130	180	ns	INA, DIS

Electrical Characteristics - continued

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Output						
OUT1HG H Level Output Voltage	V _{OUT1HGH}	V _{CC2} - 0.8	-	-	V	I _{OUT1HG} = -40 mA
OUT1HG L Level Output Voltage	V _{OUT1HGL}	-	-	0.6	V	I _{OUT1HG} = +40 mA
OUTREF Reference Voltage	VOUTREF	1.96	2.00	2.04	V	Relative to VCC2 (Absolute Value)
OUT1L On Resistance	R OUT1L	-	0.15	0.30	Ω	$I_{OUT1L} = 40 \text{ mA}$
OUT1L Maximum Current	I _{OUTMAX1}	10	-	-	А	$V_{CC2} = 15 V$, Guaranteed by design
OUT1 Turn On Time	t _{PON}	210	330	450	ns	INA, DIS
OUT1 Turn Off Time	t _{POFF}	210	330	450	ns	INA, DIS
OUT1HG-OUT1L Dead Time	t _{DEAD}	100	160	220	ns	
OUT1HG L to H Transition Time	tout1hglh	-	25	50	ns	Between OUT1HG and VCC2 = 1000 pF Guaranteed by design
PROOUT1 On Resistance	R _{ONPRO1}	0.4	0.9	2.0	Ω	$I_{PROOUT1} = 40 \text{ mA}$
PROOUT2 On Resistance	R _{ONPRO2}	0.2	0.4	0.9	Ω	I _{PROOUT2} = 40 mA
OUT2 On Resistance	R _{ON2}	0.25	0.45	1.00	Ω	$I_{OUT2} = 40 \text{ mA}$
OUT2 On Threshold Voltage	V _{OUT2ON}	1.8	2.0	2.2	V	
OUT2 On Delay Time	t _{OUT2ON}	-	70	115	ns	
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Guaranteed by design





Electrical Characteristics - continued

ParameterSymbolMinTypMaxUnitCondTemperature MonitorTC Voltage V_{TC} 0.9801.0001.020VTO1, TO2 Output Current I_{TO} 0.9751.0001.025mA $R_{TC} = 10 \text{ k}\Omega$ TO1, TO2 Output Current Offset $I_{TOOFFSET}$ -220+22 μ A $R_{TC} = 10 \text{ k}\Omega$ SENSOR Output Frequencyfosc_To81014kHzSENSOR Output Duty1DSENSOR187.590.092.5% $V_{TO1} = V_{TO2} =$ SENSOR Output Duty2DSENSOR247.050.053.0% $V_{TO1} = V_{TO2} =$ SENSOR Output Duty3DSENSOR35.610.014.4% $V_{TO1} = V_{TO2} =$ TO1,TO2 Input Voltage Offset $V_{TOOFFSET}$ -130+13mVGuaranteed HTO_SEL Switching TimetroseL1.0 μ sSENSOR On Resistance(Source-side)RSENSORH-60160ΩI_SENSOR = -5 mSENSOR On ResistanceR_SENSORL-60160ΩI_SENSOR = +5 mSENSOR On ResistanceRSENSORL-60160ΩI_SENSOR = +5 mSENSOR On ResistanceNESENSORL-60160ΩI_SENSOR = +5 mSENSOR On ResistanceNESENSOR-60160ΩI_SENSOR = +5 mSENSOR On ResistanceNESENSOR-60160ΩI_SENSOR = +5 mSENSOR ON Resi	1.35 V 2.59 V 3.84 V by design
TC Voltage V_{TC} 0.9801.0001.020VTO1, TO2 Output Current I_{TO} 0.9751.0001.025mA $R_{TC} = 10 \text{ k}\Omega$ TO1, TO2 Output Current Offset $I_{TOOFFSET}$ -220+22 μ A $R_{TC} = 10 \text{ k}\Omega$ SENSOR Output Frequencyfosc_TO81014kHzSENSOR Output Duty1D_{SENSOR1}87.590.092.5% $V_{TO1} = V_{TO2} =$ SENSOR Output Duty2D_{SENSOR2}47.050.053.0% $V_{TO1} = V_{TO2} =$ SENSOR Output Duty3D_{SENSOR3}5.610.014.4% $V_{TO1} = V_{TO2} =$ TO1, TO2 Input Voltage Offset $V_{TOOFFSET}$ -130+13mVGuaranteed HTO_SEL Switching TimetroseL1.0 μ sSENSOR On Resistance $R_{SENSORH}$ -60160 Ω $I_{SENSOR} = -5 \text{ m}$ SENSOR On Resistance $R_{SENSORL}$ -60160 Ω $I_{SENSOR} = +5 \text{ m}$ Protection Functions60160 Ω $I_{SENSOR} = +5 \text{ m}$	2.59 V 3.84 V by design
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TO1, TO2 Output Current OffsetITOOFFSET-220+22μA $R_{TC} = 10 \text{ k}\Omega$ SENSOR Output Frequencyfosc_To81014kHzSENSOR Output Duty1DSENSOR187.590.092.5% $V_{TO1} = V_{TO2} =$ SENSOR Output Duty2DSENSOR247.050.053.0% $V_{TO1} = V_{TO2} =$ SENSOR Output Duty3DSENSOR35.610.014.4% $V_{TO1} = V_{TO2} =$ TO1, TO2 Input Voltage Offset $V_{TOOFFSET}$ -130+13mVGuaranteed toTO_SEL Switching TimetroseL1.0 μ ssensor = -5 mSENSOR On Resistance (Source-side) $R_{SENSORL}$ -60160 Ω $I_{SENSOR} = +5 m$ Protection Functions60160 Ω $I_{SENSOR} = +5 m$	2.59 V 3.84 V by design
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TO1,TO2 Input Voltage Offset $V_{TOOFFSET}$ -130+13mVGuaranteed toTO_SEL Switching Time t_{TOSEL} 1.0 μ sSENSOR On Resistance (Source-side) $R_{SENSORH}$ -60160 Ω Isensor = -5 mSENSOR On Resistance (Sink-side) $R_{SENSORL}$ -60160 Ω Isensor = -5 mProtection Functions $R_{SENSORL}$ -60160 Ω Isensor = +5 m	by design
TO_SEL Switching Time t_{TOSEL} 1.0 μ sSENSOR On Resistance (Source-side) $R_{SENSORH}$ -60160 Ω $I_{SENSOR} = -5 \text{ m}$ SENSOR On Resistance (Sink-side) $R_{SENSORL}$ -60160 Ω $I_{SENSOR} = +5 \text{ m}$ Protection Functions V V V V V V	
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(Source-side) Resistance SENSOR On Resistance Rsensort (Sink-side) - Protection Functions	IIA
(Sink-side) R _{SENSORL} - 60 160 Ω I _{SENSOR} = +5 r Protection Functions	
Protection Functions	م ۸
VREG UVLO Off Voltage V _{UVL01H} 4.05 4.25 4.45 V	
VREG UVLO On Voltage V _{UVLO1L} 3.95 4.15 4.35 V	
VREG UVLO Filtering Time t _{UVLO1FIL} 2 10 30 µs	
VREG UVLO Delay Time	
(OUT1HG) t _{DUVL010UT1HG} 2 10 30 µs	
(FLT) t _{DUVL01FLT} 2 10 30 μs	
Output side over oneVuvlo2H10.711.712.7VThreshold VoltageVuvlo2H10.711.712.7V	
Output side over oneVuvelock9.710.711.7VThreshold VoltageVuvelock9.710.711.7V	
Filtering Time t _{UVL02FIL} 2 10 30 µs	
Output-side LIVLO Delay Time	
(OUT1HG) t _{DUVL020UT1HG} 2 10 30 µs	
(FLT) t _{DUVLO2FLT} 3 - 65 µs	
Short Current Detection	
Voltage V _{SCDET} 0.67 0.70 0.73 V	
Short Current Detection	
Delay Time (OUT1HG) $t_{DSCPOUT1HG}$ 0.02 0.07 0.11 μ s OUT1HG = 1	kΩ Pull up
Short Current Detection PROOLIT1 -	30 k0
Delay Time (PROOUT1) t _{DSCPPRO1} 0.02 0.05 0.08 µs Pull up	00 1132
Short Current Detection PROOLIT2 -	30 kO
Delay Time (PROOUT2) $t_{DSCPPRO2}$ 0.02 0.05 0.08 µs Pull up	50 K22
Short Current Detection	
Delay Time (FLT) t _{DSCPFLT} 1 - 35 µs	
	K12 Pull up
FLT Output On Resistance R_{FLTL} -3080 Ω $I_{FLT} = 5 \text{ mA}$	
Fault Output Holding Time t _{FLTRLS} 30 40 50 ms	
Gate State H DetectionVOSFBH4.55.05.5V	
Threshold Voltage	
Gate State L DetectionVOSFBL4.04.55.0V	
Threshold Voltage	
OSFB Output Filtering Time t _{OSFBFIL} 5.0 7.4 9.8 µs	
$OSFB \ Output \ On \ Resistance \qquad R_{OSFBL} \qquad - \qquad 30 \qquad 80 \qquad \Omega \qquad I_{OSFB} = 5 \ mA$	
OSFB Output Holding Time t _{OSFBRLS} 30 40 50 ms	











(Reference data)





vs Main Power Supply Voltage







Figure 24. Maximum On Duty vs Main Power Supply Voltage



Figure 27. Logic Pull Up Resistance vs VREG Output Voltage

Figure 28. Logic Input Filtering Time vs VREG Output Voltage

(Reference data)



 $(I_{OUT1L} = 40 \text{ mA})$

(Relative to VCC2)

(Reference data)



vs Output-side Supply Voltage (Between OUT1HG and VCC2 = 1000 pF)





(Reference data)





Output-side Supply Voltage $(R_{TC} = 10 \text{ k}\Omega)$

(Reference data)



 $(V_{TO1} = V_{TO2} = 1.35 \text{ V})$

Supply Voltage $(V_{TO1} = V_{TO2} = 2.59 \text{ V})$







(OUT1HG) vs Temperature

















Description of Pins and Cautions on Layout of Board

- 1. V_BATT (Main power supply pin) This is the main power supply pin. Connect a bypass capacitor between the V_BATT pin and the GND1 pin in order to suppress voltage variations.
- 2. GND1 (Input-side ground pin) This is the ground pin on the input-side.
- VCC2 (Output-side power supply pin) The VCC2 pin is a power supply pin on the output-side. To reduce voltage fluctuations due to the driving current of the internal transformer and output current, connect a bypass capacitor between the VCC2 pin and the GND2 pin.
- 4. GND2 (Output-side ground pin) This is the ground pin on the output-side. Connect the GND2 pin to the emitter/source of output device.
- 5. INA (Control input pin), DIS (Input enabling signal input pin) These are the pins for determining the output logic

These are the phils for determining the output logic.						
DIS	INA	OUT1HG	OUT1L			
Н	Х	Н	L			
L	L	Н	L			
L	Н	L	Hi-Z			
			X: Don't care			

6. FLT (Fault output pin)

The FLT pin is an open drain pin that sends a fault signal when a fault occurs (i.e., when the V_BATT UVLO / VREG UVLO / VCC2 UVLO or short circuit protection function (SCP) is activated).

Status	FLT
Normal operation	Hi-Z
Fault	L

7. OSFB (Output state feedback output pin)

This is an open drain pin which compares gate logic of the output device monitored with the PROOUT1 pin and the DIS or INA pin input logic, and outputs Low when they disaccord.

Status	DIS	INA	PROOUT1 (input)	OSFB		
	Н	Х	Н	L		
	Н	Х	L	Hi-Z		
Normal operation	L	L	Н	L		
	L	L	L	Hi-Z		
	L	Н	Н	Hi-Z		
	L	Н	L	L		
Fault X		Х	Х	Hi-Z		
L	-	•	•	X: Don't care		

 SENSOR (Temperature information output pin), TO_SEL (Temperature information selecting pin) This is a pin which outputs the voltage of either the TO1 pin or TO2 pin converted to Duty cycle. The TO_SEL pin determines which information to output, either the TO1 pin or TO2 pin.

TO_SEL	SENSOR Output
L	Output information of the TO1 pin
Н	Output information of the TO2 pin

- FB (Error amplifier inverting input pin for switching controller)
 This is a voltage feedback pin of the switching controller. Connect it to the VREG pin when the switching controller is not used.
- COMP (Error amplifier output pin for switching controller) This is the gain control pin of the switching controller. Connect a phase compensation capacitor and resistor. When the switching controller is not used, connect it to the GND1 pin.

Description of Pins and Cautions on Layout of Board - continued

11. VREG (Input-side internal power supply pin)

This is the internal power supply pin on the input side. Be sure to connect a capacitor between the VREG pin and the GND1 pin in order to prevent from oscillation and suppress voltage variation due to FET_G output current and internal transformer driving current.

It is also possible to supply voltage (4.5 V to 5.5 V) externally to the VREG pin. In this case, please short the VREG pin and the V_BATT pin.

- FET_G (MOS FET for transformer drive control pin for switching controller) This is the MOS FET control pin for the switching controller transformer drive. Leave it open when the switching controller is not used.
- SENSE (Current feedback resistor connection pin for switching controller) This is a pin connected to the resistor of the switching controller current feedback. Connect it to VREG when switching controller is not used.
- 14. OUT1HG (Source side MOS buffer driving pin) This is the buffer driving pin for gate on side. Connect it to the gate pin of the buffer (Pch MOS FET). Also, connect a resistor R_{OUT1HG} between the OUT1HG pin and the VCC2 pin to control the gate voltage of the buffer.
- 15. OUTREF (Reference voltage pin for constant current drive) This is the reference pin for gate constant current drive. Connect a resistor R_{OUTREF} between the VCC2 pin and the source pin of the buffer (Pch MOS FET). Also, connect the source pin of the buffer to the OUTREF pin.
- 16. OUT1L (Sink side output pin) This is the driving pin for gate off side.
- 17. OUT2 (Output pin for Miller Clamp) This is the miller clamp pin for preventing a rise of gate voltage. The OUT2 pin should be open when miller clamp function is not used.
- 18. PROOUT1 (Soft turn off pin for short circuit protection / Gate voltage input pin), PROOUT2 (Fast turn off pin for short circuit protection) This is a pin for soft turn off of output device when short-circuit protection is activated. Both the PROOUT1 pin and the PROOUT2 pin are turned on for t_{PRO2ON} from short circuit detection. After t_{PRO2ON}, only the PROOUT1 pin is turned on. It also functions as monitoring gate voltage pin for miller clamp function and output state feedback function.
- 19. SCPIN1, SCPIN2 (Short circuit detection pin) These are pins used to detect current for short circuit protection. When the SCPIN1 pin or the SCPIN2 pin voltage is more than V_{SCDET}, the SCP function is activated. There is a possibility of the IC malfunction in an open state. To avoid such trouble, short the SCPIN1 or SCPIN2 pin to the GND2 when the SCP function is not used.
- 20. TC (Resistor connection pin for setting constant current source output) The TC pin is a resistor connection pin for setting the constant current output for temperature monitor. If an arbitrary resistance value is connected between the TC pin and the GND2 pin, it is possible to set the constant current value output from the TO1 pin and the TO2 pin.
- 21. TO1, TO2 (Constant current output / Sensor voltage input pin) The TO1 pin and the TO2 pin are constant current output / sensor voltage input pins for temperature monitor. It can be used as a sensor input by connecting a device with arbitrary impedance between the TOx pin and the GND2. Furthermore, the TOx (x = 1 or 2) pin disconnect detection function is built-in.

1. Fault Status Output

This function is used to output a fault signal from the FLT pin when a fault occurs (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) is activated), after fault state cancellation, the FLT pin holds a fault signal until fault output holding time (t_{FLTRLS}).

Status	FLT pin
Normal	Hi-Z
Fault occurs	L



Figure 74. Fault Status Output Timing Chart

2. Under Voltage Lockout (UVLO) Function

The BM60059FV-C incorporates the under voltage lockout (UVLO) function on V_BATT, VREG and VCC2. When the power supply voltage drops to the UVLO ON voltage, the OUT1HG pin outputs "H" signal and the OUT1L pin and the FLT pin both output the "L" signal. When the power supply voltage rises to the UVLO OFF voltage, these pins are reset. However, during the fault output holding time set in "Fault Status Output" section, the OUT1HG pin holds the "H" signal and the OUT1L pin and the FLT pin hold the "L" signal. In addition, to prevent miss-triggering due to noise, filtering time t_{UVLO1FIL} and t_{UVLO2FIL} are set on V_BATT, VREG and VCC2.



3. Short Circuit Protection (SCP) Function

When the SCPIN1 pin or the SCPIN2 pin voltage exceeds the V_{SCDET} , the SCP function is activated. When the SCP function is activated, the OUT1HG pin voltage is set to the "H" level, the OUT1L pin voltage is set to the "Hi-Z" level and the PROOUT1 pin, the PROOUT2 pin and the FLT pin voltage go to the "L" level first (Fast Turn Off). Next, after t_{PRO2ON} has passed from the Short Current Detection, the PROOUT2 pin is set to the "Hi-Z" level (Soft Turn Off). And then, when short-circuit current, the OUT1L pin becomes the "L" level. Finally, when the fault output holding time has elapsed, the SCP function is released and the FLT pin becomes the "Hi-Z" level. The PROOUT1 pin holds the "L" state until the OUT1HG pin becomes the "L" level.

Please take note that when the OUT1L pin is "L", the short-circuit is not detected.









4. Miller Clamp Function

When the OUT1HG pin = H, the OUT1 pin = L and the PROOUT1 pin voltage < V_{OUT2ON} , the internal MOS of the OUT2 pin is turned ON and the miller clamp function operates. This state is kept until the OUT1HG pin becomes L and the OUT1L pin becomes Hi-Z. While the short circuit protection function is activated, miller clamp function operates after the lapse of soft turn off release time t_{SCPOFF}.

Short current protection	SCPINx (x = 1 or 2)	INA	PROOUT1 Input	OUT2
Operated $\geq V_{\text{SCDET}}$		Х	Х	Hi-Z
Not operated	Х	L	≥ V _{OUT2ON}	Hi-Z
	Х	L	< V _{OUT2ON}	L
	Х	Н	Х	Hi-Z





Figure 80. Block Diagram of Miller Clamp Function



Figure 81. Timing Chart of Miller Clamp Function

SCPINx: SCPIN1 or SCPIN2

5. Gate Constant Current Driving Function

This IC has a gate constant current driving function. Charge the gate of the output element with a constant current by connecting buffer (Pch MOS FET M_{OUT1H}) and resistors (R_{OUTREF}, R_{OUT1HG}) as shown in Figure 82. I_{GATE} can be set using the following formula:

$$I_{GATE}[A] = V_{OUTREF}[V] / R_{OUTREF}[\Omega]$$

The table below shows the recommended components for the external parts (M_{OUT1H} , R_{OUTREF} , and R_{OUT1HG}). If using other component for M_{OUT1H} or using resistors outside the recommended range, please make sure that there is no overshoot or oscillation of the current in the operating temperature condition and current setting.

Symbol	Manufacturer	Recommended	Recomme	Unit	
Symbol	Manufacturer	Components	Min	Max	Unit
M _{OUT1H}	ROHM	RSR015P06HZGTL	-	-	-
ROUTREF	ROHM	MCR Series	0.34	-	Ω
R _{OUT1HG}	ROHM	LTR Series	0.5	2.5	kΩ



Figure 82. Block Diagram of Gate Constant Current Driving Function

6. Output State Feedback Function

When the gate logic of output device monitored with the PROOUT1 pin and input logic are compared, and they are different, the OSFB pin outputs L. In order to prevent the detection error due to delay of input and output, OSFB filter time t_{OSFBON} is provided. After resolving the mismatch state, hold the OSFB to Low until OSFB output holding time $(t_{OSFBRLS})$ is completed.

- 7. Switching Regulator
 - (1) Basic action

This IC has a switching controller which turns ON/OFF in synchronous with internal clock. When V_{BATT} voltage is supplied ($V_{BATT} > V_{UVLOBATTH}$), the FET_G pin starts switching by soft-start. Output voltage is determined by the following equation through the external resistance and winding ratio "n" of the flyback transformer (n = Secondary side winding number / FB side winding number).

$$V_{OUT} = V_{FB} \times \{(R1 + R2) / R2\} \times n[V]$$

(2) Max Duty

When, for example, the output load is large and the voltage level of the SENSE pin does not reach current detection level, the output is forcibly turned off by Maximum On Duty (D_{ONMAX}).

(3) Pin conditions when switching controller is not used

Implement pin setting as shown below when switching controller is not used.

Pin Number	Pin Name	Treatment Method
22	FB	Connect to VREG
23	COMP	Connect to GND1
24	V_BATT	Connect to power supply
25	VREG	Connect a capacitor
26	FET_G	No connection
27	SENSE	Connect to VREG



Figure 83. Block Diagram of Switching Controller

8. Temperature Monitor Function

This IC has a built-in constant current output circuit that supplies a constant current output from the TO1 and TO2 pins. The current value I_{TO} can be adjusted depending on the resistance value connected between the TC pin and the GND2 pin. Furthermore, the TO1 pin and the TO2 pin have voltage input function. The SENSOR pin outputs the signal of the TO1 pin or the TO2 pin voltage converted to Duty. The TO_SEL pin determines which output is selected whether the TO1 pin or the TO2 pin. When TO_SEL = Low, the TO1 pin is selected. When TO_SEL = High, the TO2 pin is selected. When only one of the TO1 or the TO2 pin is used, connect the other TOx pin to GND2. (x = 1 or 2)

$$I_{TO}[\text{mA}] = 10 \times V_{TC}[\text{V}] / R_{TC}[\text{k}\Omega]$$



Figure 84. Block Diagram of Temperature Monitor Function



Figure 85. Timing Chart of Temperature Monitor Function

Description of Functions and Examples of Constant Setting - continued 9. I/O Condition Table

9.	I/O Condition Table														
		Input				Output									
No	Status	VREG	ΝΛΓΟΙΝ	V_BATT	SCPINx	DIS	INA	PROOUT1 Input	OUT1HG	OUT1L	OUT2	PROOUT1	PROOUT2	FLT	OSFB
1	SCP	0	0	0	Н	L	Н	Х	Н	Ζ	Ζ	L	L→Z	L	Ζ
2	VREG UVLO	UVLO	Х	Х	L	Х	Х	Н	Н	L	Ζ	Ζ	Z	L	Ζ
3		UVLO	Х	Х	L	Х	Х	L	Н	L	L	Ζ	Z	L	Ζ
4	VCC2 UVLO	Х	UVLO	Х	L	Х	Х	Н	Н	L	Ζ	Ζ	Z	L	Ζ
5	VCC2 UVLO	Х	UVLO	Х	L	Х	Х	L	Н	L	L	Ζ	Z	L	Ζ
6	V_BATT UVLO	Х	Х	UVLO	L	Х	Х	Н	Н	L	Ζ	Ζ	Z	L	Ζ
7	V_BATTOVEO	Х	Х	UVLO	L	Х	Х	L	Н	L	L	Ζ	Z	L	Ζ
8	Disable	0	0	0	L	Н	Х	Н	Н	L	Ζ	Ζ	Z	Ζ	L
9	Disable	0	0	0	L	Н	Х	L	Н	L	L	Ζ	Z	Ζ	Ζ
10	Normal Operation	0	0	0	L	L	L	Н	Н	L	Ζ	Ζ	Z	Ζ	L
11	11 L Input	0	0	0	L	L	L	L	Н	L	L	Ζ	Z	Ζ	Ζ
12	Normal Operation	0	0	0	L	L	Н	Η	L	Ζ	Ζ	Ζ	Z	Ζ	Ζ
13	3 H Input	0	0	0	L	L	Н	L	L	Ζ	Ζ	Ζ	Z	Ζ	L
L	SCPINX: SCPIN1 or SCPIN2 of Power supply voltage > LIVLO_X: Don't care_7. Hi-7														

SCPINx: SCPIN1 or SCPIN2, o: Power supply voltage > UVLO, X: Don't care, Z: Hi-Z
Selection of Components Externally Connected

The following are the recommended external components.



I/O Equivalence Circuits

., o _quira	ience Circuits	[]	
Pin No.	Pin Name Pin Function	Input Output Equivalent Circuit Diagram	
	SCPIN1	VCC2 Internal Power Supply	
4	Short circuit detection pin 1		
5	SCPIN2		
	Short circuit detection pin 2	GND2	
6	TO1		
		VCC2	
	Constant current output pin / Sensor voltage input pin 1		
7	TO2		
	Constant current output pin / Sensor voltage input pin 2		
8	тс		
	Resistor connection pin for setting constant current source output		
	OUTREF		
10			
	Reference voltage pin for constant current drive		

I/O Equivalence Circuits - continued

Pin No.	Pin Name	Input Output Equivalent Circuit Diagram		
FILLINO.	Pin Function			
11	OUT1HG			
	Source side MOS buffer driving pin	OUT1HG		
	OUT1L			
12	Sink side output pin			
40	OUT2			
13	Output pin for Miller Clamp	OUT1L		
2	PROOUT2			
2	Fast turn off pin for short circuit protection	GND2		
3	PROOUT1	Internal Power Supply		
	Soft turn off pin for short circuit protection / Gate voltage input pin			
10	FLT			
16	Fault output pin			
	OSFB			
21	Output state feedback output pin	GND1		
20	SENSOR			
	Temperature information output pin			

I/O Equivalence Circuits - continued

Pin No.	Pin Name	Input Output Equivalent Circuit Diagram	
Pin No.	Pin Function		
17	DIS		
	Input enabling signal input pin		
18	INA		
10	Control input pin		
19	TO_SEL		
19	Temperature information selecting pin		
22	FB		
	Error amplifier inverting input pin for switching controller		
23	СОМР		
	Error amplifier output pin for switching controller		

I/O Equivalence Circuits - continued

Pin No.	Pin Name	Input Output Equivalent Circuit Diagram	
PIN NO.	Pin Function	Input Output Equivalent Circuit Diagram	
25	VREG	Internal Power Supply	
	Input-side internal power supply pin		
26	FET_G		
	MOS FET for transformer drive control pin for switching controller		
27	SENSE	VREG O	
	Current feedback resistor connection pin for switching controller	SENSE O M SENSE	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Figure 86. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
29.Nov.2019	001	New Release

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