

# LP87322B/D/E/F-Q1 双路高电流降压转换器和双路线性稳压器

## 1 特性

- 符合 AEC-Q100 标准，其中包括以下内容：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
- 输入电压：2.8V 至 5.5V
- 两个高效降压直流/直流转换器：
  - 输出电压：0.7V 至 3.36V
  - 最大输出电流 2A
  - 可编程输出电压转换率范围：0.5mV/μs 至 10mV/μs
  - 2MHz 开关频率
  - 用于降低 EMI 的扩频模式和相位交错
- 两个线性稳压器：
  - 输入电压：2.5V 至 5.5V
  - 输出电压：0.8V 至 3.3V
  - 最大输出电流 300mA
- 可配置通用输出信号 (GPO、GPO2)
- 具有可编程屏蔽的中断功能
- 可编程电源正常信号 (PGOOD)
- 输出短路和过载保护
- 过热警告和保护
- 过压保护 (OVP) 和欠压锁定 (UVLO)
- 具有可湿性侧面的 28 引脚 5mm × 5mm VQFN 封装

## 2 应用

- 汽车音响主机和组合仪表
- 汽车摄像头模块
- 环视系统 ECU
- 雷达系统 ECU
- 汽车显示屏

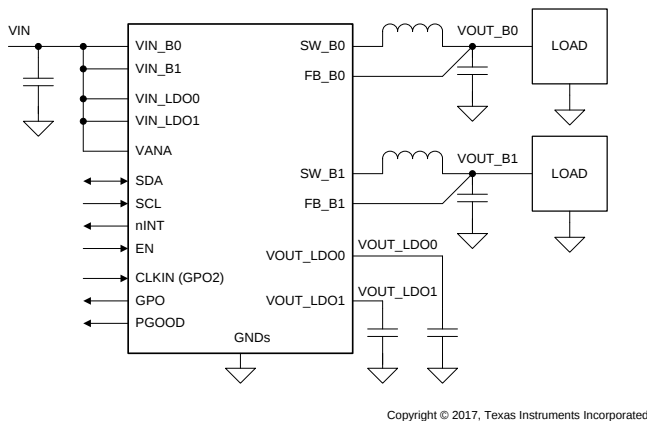
## 3 说明

LP87322B/D/E/F-Q1 专为满足最新处理器和平台的电源管理要求而设计，这些处理器和平台用于汽车摄像头和雷达应用。该器件包含两个降压直流/直流转换器和两个线性稳压器以及通用数字输出信号。该器件由 I<sup>2</sup>C 兼容串行接口和使能信号进行控制。

自动 PWM/PFM (AUTO 模式) 操作可在较宽输出电流范围内最大限度地提高效率。LP87322B/D/E/F-Q1 支持远程电压感应，可补偿稳压器输出与负载点 (POL) 之间的 IR 压降，从而提高输出电压的精度。此外，可以强制开关时钟进入 PWM 模式以及将其与外部时钟同步，从而最大限度地降低干扰。

LP87322B/D/E/F-Q1 器件还支持可编程启动和关断延迟与排序 (包括与使能信号同步的 GPO 信号)。在启动和电压变化期间，器件会对输出转换率进行控制，从而最大限度地减小输出电压过冲和浪涌电流。

简化原理图



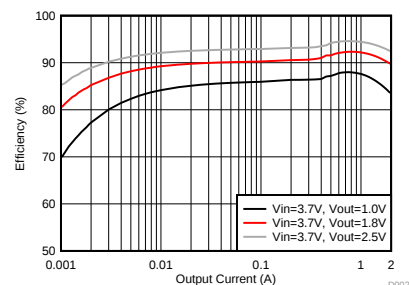
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器件信息

| 器件型号            | 封装        | 封装尺寸 (标称值)      |
|-----------------|-----------|-----------------|
| LP87322E/F      | VQFN (28) | 5.00mm × 5.00mm |
| LP87322B/D (预览) |           |                 |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

直流/直流效率与输出电流



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## 4 修订历史记录

| 日期         | 修订版本 | 说明    |
|------------|------|-------|
| 2017 年 9 月 | *    | 初始发行版 |

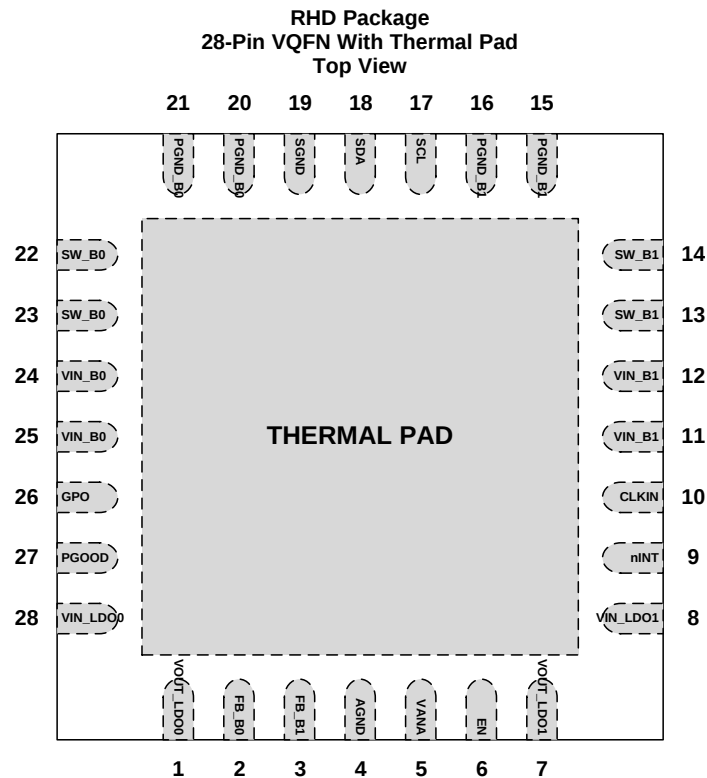
## 5 器件比较表

| 可订购器件 <sup>(1)</sup>            | 降压 1 电压 |
|---------------------------------|---------|
| (L)P87322BRHDRQ1 <sup>(2)</sup> | 1200mV  |
| (L)P87322DRHDRQ1 <sup>(2)</sup> | 1800mV  |
| LP87322ERHDRQ1                  | 1350mV  |
| LP87322FRHDRQ1                  | 1500mV  |

(1) 以“P8732...”开头的订购编号用于原型器件。当器件上市之后，订购编号将更改为以“LP8732...”开头。

(2) 预览：器件已宣布，但未进行生产。现已推出样片。

## 6 Pin Configuration and Functions



**Pin Functions**

| PIN    |           | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                 |
|--------|-----------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NUMBER | NAME      |                     |                                                                                                                                                                             |
| 1      | VOUT_LDO0 | P/O                 | LDO0 output. If LDO0 is not used, leave the pin floating.                                                                                                                   |
| 2      | FB_B0     | A                   | Output voltage feedback (positive) for Buck 0                                                                                                                               |
| 3      | FB_B1     | A                   | Output voltage feedback (positive) for Buck 1                                                                                                                               |
| 4      | AGND      | G                   | Ground                                                                                                                                                                      |
| 5      | VANA      | P/I                 | Supply voltage for analog and digital blocks. Must be connected to same node with VIN_Bx.                                                                                   |
| 6      | EN        | D/I                 | Programmable enable signal for regulators and GPOs. If the pin is not used, leave the pin floating.                                                                         |
| 7      | VOUT_LDO1 | P/O                 | LDO1 output. If LDO1 is not used, leave the pin floating.                                                                                                                   |
| 8      | VIN_LDO1  | P/I                 | Power input for LDO1. If LDO1 is not used, connect the pin to VANA.                                                                                                         |
| 9      | nINT      | D/O                 | Open-drain interrupt output. Active LOW. If the pin is not used, connect the pin to ground.                                                                                 |
| 10     | CLKIN     | D/I/O               | External clock input. Alternative function is general-purpose digital output (GPO2). If the pin is not used, leave the pin floating.                                        |
| 11, 12 | VIN_B1    | P/I                 | Input for Buck 1. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed. |
| 13, 14 | SW_B1     | P/O                 | Buck 1 switch node. If the Buck 1 is not used, leave the pin floating.                                                                                                      |
| 15, 16 | PGND_B1   | P/G                 | Power ground for Buck 1                                                                                                                                                     |
| 17     | SCL       | D/I                 | Serial interface clock input for I <sup>2</sup> C access. Connect a pullup resistor. If the I <sup>2</sup> C interface is not used, connect the pin to Ground.              |
| 18     | SDA       | D/I/O               | Serial interface data input and output for I <sup>2</sup> C access. Connect a pullup resistor. If the I <sup>2</sup> C interface is not used, connect the pin to Ground.    |
| 19     | SGND      | G                   | Ground                                                                                                                                                                      |
| 20, 21 | PGND_B0   | P/G                 | Power ground for Buck 0                                                                                                                                                     |

(1) A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

**Pin Functions (continued)**

| PIN         |          | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                 |
|-------------|----------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NUMBER      | NAME     |                     |                                                                                                                                                                             |
| 22, 23      | SW_B0    | P/O                 | Buck 0 switch node. If the Buck 0 is not used, leave the pin floating.                                                                                                      |
| 24, 25      | VIN_B0   | P/I                 | Input for Buck 0. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed. |
| 26          | GPO      | D/O                 | General-purpose digital output. If the pin is not used, leave the pin floating.                                                                                             |
| 27          | PGOOD    | D/O                 | Power-good indication signal. If the pin is not used, leave the pin floating.                                                                                               |
| 28          | VIN_LDO0 | P/I                 | Power input for LDO0. If LDO0 is not used, connect the pin to VANA.                                                                                                         |
| Thermal Pad | —        | —                   | Connect to PCB ground plane using multiple vias for good thermal performance.                                                                                               |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                                                  |                                                               | MIN  | MAX                                 | UNIT |
|--------------------------------------------------|---------------------------------------------------------------|------|-------------------------------------|------|
| VIN_Bx, VANA                                     | Voltage on power connections (must use the same input supply) | −0.3 | 6                                   | V    |
| VIN_LDOx                                         | Voltage on power connections                                  | −0.3 | 6                                   | V    |
| SW_Bx                                            | Voltage on buck switch nodes                                  | −0.3 | (VIN_Bx + 0.3 V) with 6-V maximum   | V    |
| FB_Bx                                            | Voltage on buck voltage sense nodes                           | −0.3 | (VANA + 0.3 V) with 6-V maximum     | V    |
| VOUT_LDOx                                        | Voltage on LDO output                                         | −0.3 | (VIN_LDOx + 0.3 V) with 6-V maximum | V    |
| SDA, SCL, nINT, EN                               | Voltage on logic pins (input or output pins)                  | −0.3 | 6                                   | V    |
| PGOOD, GPO, CLKIN (GPO2)                         | Voltage on logic pins (input or output pins)                  | −0.3 | (VANA + 0.3 V) with 6-V maximum     | V    |
| T <sub>J-MAX</sub>                               | Junction temperature                                          | −40  | 150                                 | °C   |
| T <sub>stg</sub>                                 | Storage temperature                                           | −65  | 150                                 |      |
| Maximum lead temperature (soldering, 10 seconds) |                                                               |      | 260                                 |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground.

### 7.2 ESD Ratings

|                                            |                                                         | VALUE                                     | UNIT  |
|--------------------------------------------|---------------------------------------------------------|-------------------------------------------|-------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> |                                           | ±2000 |
|                                            | Charged-device model (CDM), per AEC Q100-011            | All pins                                  | ±500  |
|                                            |                                                         | Corner pins (1, 7, 8, 14, 15, 21, 22, 28) | ±750  |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                      |                                                                                                             | MIN | MAX                     | UNIT |
|----------------------|-------------------------------------------------------------------------------------------------------------|-----|-------------------------|------|
| <b>INPUT VOLTAGE</b> |                                                                                                             |     |                         |      |
| VIN_Bx, VANA         | Voltage on power connections (must use the same input supply)                                               | 2.8 | 5.5                     | V    |
| VIN_LDOx             | Voltage on LDO inputs                                                                                       | 2.5 | 5.5                     | V    |
| EN, nINT             | Voltage on logic pins (input or output pins)                                                                | 0   | 5.5                     | V    |
| CLKIN                | Voltage on logic pins (input pin)                                                                           | 0   | VANA with 5.5-V maximum | V    |
| PGOOD, GPO, GPO2     | Voltage on logic pins (output pins)                                                                         | 0   | VANA                    | V    |
| SCL, SDA             | Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes | 0   | 1.95                    | V    |
|                      | Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), and Fast+ (1 MHz) Modes                       | 0   | VANA with 3.6-V maximum | V    |
| <b>TEMPERATURE</b>   |                                                                                                             |     |                         |      |
| T <sub>J</sub>       | Junction temperature                                                                                        | −40 | 140                     | °C   |
| T <sub>A</sub>       | Ambient temperature                                                                                         | −40 | 125                     | °C   |

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | LP87322B/D/E/F-Q1 | UNIT |
|-------------------------------|----------------------------------------------|-------------------|------|
|                               |                                              | RHD (VQFN)        |      |
|                               |                                              | 28 PINS           |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 36.7              | °C/W |
| R <sub>θJCTop</sub>           | Junction-to-case (top) thermal resistance    | 26.6              | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 8.9               | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.4               | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 8.8               | °C/W |
| R <sub>θJCbott</sub>          | Junction-to-case (bottom) thermal resistance | 2.2               | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 7.5 Electrical Characteristics

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

| PARAMETER                                   |                                                     | TEST CONDITIONS                                                                                                                         | MIN     | TYP | MAX  | UNIT |
|---------------------------------------------|-----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|---------|-----|------|------|
| EXTERNAL COMPONENTS                         |                                                     |                                                                                                                                         |         |     |      |      |
| C <sub>IN_BUCK</sub>                        | Input filtering capacitance for buck regulators     | Effective capacitance, connected from VIN_Bx to PGND_Bx                                                                                 | 1.9     | 10  |      | μF   |
| C <sub>OUT_BUCK</sub>                       | Output filtering capacitance for buck regulators    | Effective capacitance                                                                                                                   | 10      | 22  | 500  | μF   |
| C <sub>POL_BUCK</sub>                       | Point-of-load (POL) capacitance for buck regulators | Optional POL capacitance                                                                                                                |         | 22  |      | μF   |
| C <sub>OUT-TOTAL_BUCK</sub>                 | Buck output capacitance, total (local and POL)      | Total output capacitance                                                                                                                |         |     | 500  | μF   |
| C <sub>IN_LDO</sub>                         | Input filtering capacitance for LDO regulators      | Effective capacitance, connected from VIN_LDOx to AGND. C <sub>IN_LDO</sub> must be at least two times larger than C <sub>OUT_LDO</sub> | 0.6     | 2.2 |      | μF   |
| C <sub>OUT_LDO</sub>                        | Output filtering capacitance for LDO regulators     | Effective capacitance                                                                                                                   | 0.4     | 1   | 2.7  | μF   |
| ESR <sub>C</sub>                            | Input and output capacitor ESR                      | [1-10] MHz                                                                                                                              |         | 2   | 10   | mΩ   |
| L                                           | Inductor                                            | Inductance of the inductor                                                                                                              | 0.47    |     |      | μH   |
|                                             |                                                     |                                                                                                                                         | -30%30% |     |      |      |
| DCR <sub>L</sub>                            | Inductor DCR                                        |                                                                                                                                         |         | 25  |      | mΩ   |
| BUCK REGULATORS                             |                                                     |                                                                                                                                         |         |     |      |      |
| V <sub>(VIN_Bx)</sub> , V <sub>(VANA)</sub> | Input voltage range                                 | VIN_Bx and VANA pins must be connected to the same supply line                                                                          | 2.8     | 3.7 | 5.5  | V    |
| V <sub>OUT_Bx</sub>                         | Output voltage                                      | Programmable voltage range                                                                                                              | 0.7     | 1   | 3.36 | V    |
|                                             |                                                     | Step size, 0.7 V ≤ V <sub>OUT</sub> < 0.73 V                                                                                            | 10      |     |      | mV   |
|                                             |                                                     | Step size, 0.73 V ≤ V <sub>OUT</sub> < 1.4 V                                                                                            | 5       |     |      |      |
|                                             |                                                     | Step size, 1.4 V ≤ V <sub>OUT</sub> ≤ 3.36 V                                                                                            | 20      |     |      |      |

(1) All voltage values are with respect to network ground.

(2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the most likely norm.

## Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

| PARAMETER                               |                                                                                                               | TEST CONDITIONS                                                                                                               | MIN              | TYP  | MAX               | UNIT       |    |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|------------------|------|-------------------|------------|----|
| I <sub>OUT_Bx</sub>                     | Output current                                                                                                | Output current                                                                                                                | 2 <sup>(3)</sup> |      |                   | A          |    |
|                                         | Input and Output voltage difference                                                                           | Minimum voltage between V <sub>(VIN_Bx)</sub> and V <sub>OUT</sub> to fulfill the electrical characteristics                  | 0.8              |      |                   | V          |    |
| V <sub>OUT_Bx_DC</sub>                  | DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature | Force PWM mode, V <sub>OUT</sub> < 1 V                                                                                        | -20              |      |                   | 20         | mV |
|                                         |                                                                                                               | Force PWM mode, V <sub>OUT</sub> ≥ 1 V                                                                                        | -2%              |      |                   | 2%         |    |
|                                         |                                                                                                               | PFM mode, V <sub>OUT</sub> < 1 V, the average output voltage level is increased by max. 20 mV                                 | -20mV            |      |                   | 40mV       | mV |
|                                         |                                                                                                               | PFM mode, V <sub>OUT</sub> ≥ 1 V, the average output voltage level is increased by max. 20 mV                                 | -2%              |      |                   | 2% + 20 mV |    |
| Ripple voltage                          | PWM mode, L = 0.47 μH                                                                                         | 10                                                                                                                            |                  |      | mV <sub>p-p</sub> |            |    |
|                                         | PFM mode, L = 0.47 μH                                                                                         | 25                                                                                                                            |                  |      |                   |            |    |
| DC <sub>LNR</sub>                       | DC line regulation                                                                                            | I <sub>OUT</sub> = 1 A                                                                                                        | ±0.05            |      |                   | %/V        |    |
| DC <sub>LDR</sub>                       | DC load regulation in PWM mode                                                                                | V <sub>OUT_Bx</sub> = 1 V, I <sub>OUT</sub> from 0 to I <sub>OUT(max)</sub>                                                   | 0.3%             |      |                   |            |    |
| T <sub>LDSR</sub>                       | Transient load step response                                                                                  | I <sub>OUT</sub> = 0.1 A to 2 A, T <sub>R</sub> = T <sub>F</sub> = 400 ns, PWM mode                                           | ±55              |      |                   | mV         |    |
| T <sub>LNSR</sub>                       | Transient line response                                                                                       | V <sub>(VIN_Bx)</sub> stepping 3 V ↔ 3.5 V, T <sub>R</sub> = T <sub>F</sub> = 10 μs, I <sub>OUT</sub> = I <sub>OUT(max)</sub> | ±10              |      |                   | mV         |    |
| I <sub>LIM_FWD</sub>                    | Forward current limit for both bucks (peak for every switching cycle)                                         | Programmable range                                                                                                            | 1.5              |      |                   | 3          | A  |
|                                         |                                                                                                               | Step size                                                                                                                     | 0.5              |      |                   |            |    |
|                                         |                                                                                                               | Accuracy, V <sub>(VIN_Bx)</sub> ≥ 3 V, I <sub>LIM</sub> = 3 A                                                                 | -5%              | 7.5% | 20%               |            |    |
|                                         |                                                                                                               | Accuracy, 2.8 V ≤ V <sub>(VIN_Bx)</sub> < 3 V, I <sub>LIM</sub> = 3 A                                                         | -20%             | 7.5% | 20%               |            |    |
| I <sub>LIM_NEG</sub>                    | Negative current limit                                                                                        |                                                                                                                               | 1.6              | 2.0  | 3.0               | A          |    |
| R <sub>DS(ON)</sub> <sub>HS FET</sub>   | On-resistance, high-side FET                                                                                  | Each phase, between VIN_Bx and SW_Bx pins (I = 1 A)                                                                           | 50               |      |                   | 110        | mΩ |
| R <sub>DS(ON)</sub> <sub>LS FET</sub>   | On-resistance, low-side FET                                                                                   | Each phase, between SW_Bx and PGND_Bx pins (I = 1 A)                                                                          | 45               |      |                   | 90         | mΩ |
| f <sub>SW</sub>                         | Switching frequency                                                                                           | PWM mode                                                                                                                      | 1.8              | 2    | 2.2               | MHz        |    |
|                                         | Start-up time (soft start)                                                                                    | From ENx to V <sub>OUT_Bx</sub> = 0.35 V (slew-rate control begins)                                                           | 120              |      |                   | μs         |    |
| Output voltage slew-rate <sup>(4)</sup> | SLEW_RATEx[2:0] = 010, C <sub>OUT-TOTAL_BUCK</sub> < 80 μF                                                    | -15%                                                                                                                          | 10               | 15%  | mV/μs             |            |    |
|                                         | SLEW_RATEx[2:0] = 011, C <sub>OUT-TOTAL_BUCK</sub> < 130 μF                                                   |                                                                                                                               |                  |      |                   |            |    |
|                                         | SLEW_RATEx[2:0] = 100, C <sub>OUT-TOTAL_BUCK</sub> < 250 μF                                                   |                                                                                                                               |                  |      |                   |            |    |
|                                         | SLEW_RATEx[2:0] = 101, C <sub>OUT-TOTAL_BUCK</sub> < 500 μF                                                   |                                                                                                                               |                  |      |                   |            |    |
|                                         | SLEW_RATEx[2:0] = 110, C <sub>OUT-TOTAL_BUCK</sub> < 500 μF                                                   |                                                                                                                               |                  |      |                   |            |    |
|                                         | SLEW_RATEx[2:0] = 111, C <sub>OUT-TOTAL_BUCK</sub> < 500 μF                                                   |                                                                                                                               |                  |      |                   |            |    |
| I <sub>PFM-PWM</sub>                    | PFM-to-PWM - current threshold <sup>(5)</sup>                                                                 | 550                                                                                                                           |                  |      | mA                |            |    |

(3) The maximum output current can be limited by the forward current limit  $I_{LIM\_FWD}$ . The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature.

(4) The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current.

(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependent on the output voltage, input voltage and the inductor current level.

## Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

| PARAMETER                                                           |                                                                                                            | TEST CONDITIONS                                                                                                                                                  | MIN | TYP     | MAX | UNIT              |
|---------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|-----|-------------------|
| I <sub>PWM-PFM</sub>                                                | PWM-to-PFM - current threshold <sup>(5)</sup>                                                              |                                                                                                                                                                  |     | 290     |     | mA                |
| R <sub>DIS_Bx</sub>                                                 | Output pull-down resistance                                                                                | Regulator disabled                                                                                                                                               | 150 | 250     | 350 | Ω                 |
| Output voltage monitoring for PGOOD pin and for Powergood Interrupt |                                                                                                            | V <sub>(VIN_Bx)</sub> and V <sub>(VANA)</sub> fixed 3.7 V                                                                                                        |     |         |     |                   |
|                                                                     |                                                                                                            | Overvoltage threshold (compared to DC output voltage level, V <sub>VOUT_Bx_DC</sub> )                                                                            | 39  | 50      | 64  | mV                |
|                                                                     |                                                                                                            | Undervoltage threshold (compared to DC output voltage level, V <sub>VOUT_Bx_DC</sub> )                                                                           | −53 | −40     | −29 |                   |
|                                                                     |                                                                                                            | Deglitch time during operation and after voltage change                                                                                                          | 4   |         | 15  | μs                |
|                                                                     | Gating time for PGOOD signal after regulator enable or voltage change                                      | PGOOD_MODE = 0                                                                                                                                                   |     | 800     |     | μs                |
| LDO REGULATORS                                                      |                                                                                                            |                                                                                                                                                                  |     |         |     |                   |
| V <sub>IN_LDOx</sub>                                                | Input voltage range for LDO power inputs                                                                   | V <sub>IN_LDOx</sub> can be higher or lower than V <sub>(VANA)</sub>                                                                                             | 2.5 | 3.7     | 5.5 | V                 |
| V <sub>OUT_LDOx</sub>                                               | Output voltage                                                                                             | Programmable voltage range                                                                                                                                       | 0.8 |         | 3.3 | V                 |
|                                                                     |                                                                                                            | Step size                                                                                                                                                        |     | 0.1     |     |                   |
| I <sub>OUT_LDOx</sub>                                               | Output current                                                                                             |                                                                                                                                                                  |     |         | 300 | mA                |
|                                                                     | Dropout voltage                                                                                            | V <sub>(VIN_LDOx)</sub> − V <sub>(VOUT_LDOx)</sub> , I <sub>OUT</sub> = I <sub>OUT(max)</sub> , Programmed output voltage is higher than V <sub>(VIN_LDOx)</sub> |     |         | 200 | mV                |
| V <sub>OUT_LDO_DC</sub>                                             | DC output voltage accuracy, includes voltage reference, DC load and line regulations, process, temperature | V <sub>OUT</sub> < 1 V                                                                                                                                           | −20 |         | 20  | mV                |
|                                                                     |                                                                                                            | V <sub>OUT</sub> ≥ 1 V                                                                                                                                           | −2% |         | 2%  |                   |
| DC <sub>LNR</sub>                                                   | DC line regulation                                                                                         | I <sub>OUT</sub> = 1 mA                                                                                                                                          |     | 0.1     |     | %/V               |
| DC <sub>LDR</sub>                                                   | DC load regulation                                                                                         | I <sub>OUT</sub> = 1 mA to I <sub>OUT(max)</sub>                                                                                                                 |     | 0.8%    |     |                   |
| T <sub>LDSR</sub>                                                   | Transient load step response                                                                               | I <sub>OUT</sub> = 1 mA to 300 mA, T <sub>R</sub> = T <sub>F</sub> = 1 μs                                                                                        |     | −50/+40 |     | mV                |
| T <sub>LNSR</sub>                                                   | Transient line response                                                                                    | V <sub>(VIN_LDOx)</sub> stepping 3 V ↔ 3.5 V, T <sub>R</sub> = T <sub>F</sub> = 10 μs, I <sub>OUT</sub> = I <sub>OUT(max)</sub>                                  |     | ±7      |     | mV                |
| PSRR                                                                | Power supply ripple rejection                                                                              | f = 10 kHz, I <sub>OUT</sub> = I <sub>OUT(max)</sub>                                                                                                             |     | 53      |     | dB                |
|                                                                     | Noise                                                                                                      | 10 Hz < F < 100 kHz, I <sub>OUT</sub> = I <sub>OUT(max)</sub>                                                                                                    |     | 82      |     | μV <sub>rms</sub> |
| I <sub>SHORT(LDOx)</sub>                                            | LDO current limit                                                                                          | V <sub>OUT</sub> = 0 V                                                                                                                                           | 400 | 500     | 600 | mA                |
|                                                                     | Start-up time                                                                                              | From enable to valid output voltage                                                                                                                              |     | 300     |     | μs                |
|                                                                     | Slew rate during start-up                                                                                  |                                                                                                                                                                  |     | 15      |     | mV/μs             |
| R <sub>DIS_LDOx</sub>                                               | Output pulldown resistance                                                                                 | Regulator disabled                                                                                                                                               | 150 | 250     | 350 | Ω                 |

## Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{\text{VANA}}$ ,  $V_{\text{VIN\_BX}}$ ,  $V_{\text{VIN\_LDOX}}$ ,  $V_{\text{VOUT\_BX}}$ ,  $V_{\text{VOUT\_LDOX}}$  and  $I_{\text{OUT}}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{\text{VANA}} = V_{\text{VIN\_BX}} = V_{\text{VIN\_LDOX}} = 3.7\text{ V}$ , and  $V_{\text{OUT}} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

| PARAMETER                                                             | TEST CONDITIONS                                                                                          | MIN  | TYP  | MAX   | UNIT    |
|-----------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|------|------|-------|---------|
| Output voltage monitoring for PGOOD pin and for power-good interrupt  | Overvoltage monitoring, voltage rising (compared to DC output voltage level, V <sub>OUT_LDO_DC</sub> )   | 106% | 108% | 110%  |         |
|                                                                       | Overvoltage monitoring, hysteresis                                                                       | 3%   | 3.5% | 4%    |         |
|                                                                       | Undervoltage monitoring, voltage falling (compared to DC output voltage level, V <sub>OUT_LDO_DC</sub> ) | 90%  | 92%  | 94%   |         |
|                                                                       | Undervoltage monitoring, hysteresis                                                                      | 3%   | 3.5% | 4%    |         |
|                                                                       | Deglintch time during operation and after voltage change                                                 | 4    |      | 15    | μs      |
| Gating time for PGOOD signal after regulator enable or voltage change | PGOOD_MODE = 0                                                                                           |      | 800  |       | μs      |
| EXTERNAL CLOCK AND PLL                                                |                                                                                                          |      |      |       |         |
| f <sub>EXT_CLK</sub> External input clock <sup>(6)</sup>              | Nominal frequency                                                                                        | 1    |      | 24    | MHz     |
|                                                                       | Nominal frequency step size                                                                              |      | 1    |       |         |
|                                                                       | Required accuracy from nominal frequency                                                                 | –30% |      | 10%   |         |
| External clock detection                                              | Delay for missing clock detection                                                                        |      |      | 1.8   | μs      |
|                                                                       | Delay and debounce for clock detection                                                                   |      |      | 20    |         |
| Clock change delay (internal to external)                             | Delay from valid clock detection to use of external clock                                                |      | 600  |       | μs      |
| PLL output clock jitter                                               | Cycle to cycle                                                                                           |      | 300  |       | ps, p-p |
| PROTECTION FUNCTIONS                                                  |                                                                                                          |      |      |       |         |
| Thermal warning                                                       | Temperature rising, TDIE_WARN_LEVEL = 0                                                                  | 115  | 125  | 135   | °C      |
|                                                                       | Temperature rising, TDIE_WARN_LEVEL = 1                                                                  | 127  | 137  | 147   |         |
|                                                                       | Hysteresis                                                                                               |      | 20   |       |         |
| Thermal shutdown                                                      | Temperature rising                                                                                       | 140  | 150  | 160   | °C      |
|                                                                       | Hysteresis                                                                                               |      | 20   |       |         |
| VANA <sub>OVP</sub> VANA overvoltage                                  | Voltage rising                                                                                           | 5.6  | 5.8  | 6.1   | V       |
|                                                                       | Voltage falling                                                                                          | 5.45 | 5.73 | 5.96  |         |
|                                                                       | Hysteresis                                                                                               | 40   |      |       |         |
| VANA <sub>UVL</sub> VANA undervoltage lockout                         | Voltage rising                                                                                           | 2.51 | 2.63 | 2.75  | V       |
|                                                                       | Voltage falling                                                                                          | 2.5  | 2.6  | 2.7   |         |
| Buck short-circuit detection                                          | Threshold                                                                                                | 280  | 360  | 440   | mV      |
| LDO short-circuit detection                                           | Threshold                                                                                                | 190  | 300  | 450   | mV      |
| LOAD CURRENT MEASUREMENT FOR BUCK REGULATORS                          |                                                                                                          |      |      |       |         |
| Current measurement range                                             | Maximum code                                                                                             |      |      | 10.22 | A       |
| Resolution                                                            | LSB                                                                                                      |      | 20   |       | mA      |
| Measurement accuracy                                                  | I <sub>OUT</sub> > 1 A                                                                                   |      | <10% |       |         |
| Measurement time                                                      | PFM mode (automatically changing to PWM mode for the measurement)                                        |      | 45   |       | μs      |
|                                                                       | PWM mode                                                                                                 |      | 4    |       |         |
| CURRENT CONSUMPTION                                                   |                                                                                                          |      |      |       |         |

(6) The external clock frequency must be selected so that buck switching frequency is above 1.7 MHz.

## Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

| PARAMETER                                                                                                              | TEST CONDITIONS                                                             | MIN              | TYP | MAX        | UNIT             |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|------------------|-----|------------|------------------|
| Standby current consumption, regulators disabled                                                                       |                                                                             |                  | 9   |            | $\mu\text{A}$    |
| Active current consumption, one buck regulator enabled in Auto mode, internal RC oscillator, PGOOD monitoring enabled  | $I_{OUT\_Bx} = 0\text{ mA}$ , not switching                                 |                  | 58  |            | $\mu\text{A}$    |
| Active current consumption, two buck regulators enabled in Auto mode, internal RC oscillator, PGOOD monitoring enabled | $I_{OUT\_Bx} = 0\text{ mA}$ , not switching                                 |                  | 100 |            | $\mu\text{A}$    |
| Active current consumption during PWM operation, one buck regulator enabled                                            | $I_{OUT\_Bx} = 0\text{ mA}$                                                 |                  | 15  |            | $\text{mA}$      |
| Active current consumption during PWM operation, two buck regulators enabled                                           | $I_{OUT\_Bx} = 0\text{ mA}$                                                 |                  | 30  |            | $\text{mA}$      |
| LDO regulator enabled                                                                                                  | Additional current consumption per LDO, $I_{OUT\_LDOx} = 0\text{ mA}$       |                  | 86  |            | $\mu\text{A}$    |
| PLL and clock detector current consumption                                                                             | $f_{EXT\_CLK} = 1\text{ MHz}$ , Additional current consumption when enabled |                  | 2   |            | $\text{mA}$      |
| <b>DIGITAL INPUT SIGNALS EN, SCL, SDA, CLKIN</b>                                                                       |                                                                             |                  |     |            |                  |
| $V_{IL}$ Input low level                                                                                               |                                                                             |                  |     | 0.4        | $\text{V}$       |
| $V_{IH}$ Input high level                                                                                              |                                                                             | 1.2              |     |            |                  |
| $V_{HYS}$ Hysteresis of Schmitt Trigger inputs                                                                         |                                                                             | 10               | 80  | 200        | $\text{mV}$      |
| EN/CLKIN pulldown resistance                                                                                           | $EN\_PD/CLKIN\_PD = 1$                                                      |                  | 500 |            | $\text{k}\Omega$ |
| <b>DIGITAL OUTPUT SIGNALS nINT, SDA</b>                                                                                |                                                                             |                  |     |            |                  |
| $V_{OL}$ Output low level                                                                                              | nINT: $I_{SOURCE} = 2\text{ mA}$                                            |                  |     | 0.4        | $\text{V}$       |
|                                                                                                                        | SDA: $I_{SOURCE} = 20\text{ mA}$                                            |                  |     | 0.4        | $\text{V}$       |
| $R_P$ External pullup resistor for nINT                                                                                | To VIO Supply                                                               |                  | 10  |            | $\text{k}\Omega$ |
| <b>DIGITAL OUTPUT SIGNALS PGOOD, GPO, GPO2</b>                                                                         |                                                                             |                  |     |            |                  |
| $V_{OL}$ Output low level                                                                                              | $I_{SOURCE} = 2\text{ mA}$                                                  |                  |     | 0.4        | $\text{V}$       |
| $V_{OH}$ Output high level, configured to push-pull                                                                    | $I_{SINK} = 2\text{ mA}$                                                    | $V_{VANA} - 0.4$ |     | $V_{VANA}$ | $\text{V}$       |
| $V_{PU}$ Supply voltage for external pull-up resistor, configured to open-drain                                        |                                                                             |                  |     | $V_{VANA}$ | $\text{V}$       |
| $R_{PU}$ External pull-up resistor, configured to open-drain                                                           |                                                                             |                  | 10  |            | $\text{k}\Omega$ |
| <b>ALL DIGITAL INPUTS</b>                                                                                              |                                                                             |                  |     |            |                  |
| $I_{LEAK}$ Input current                                                                                               | All logic inputs over pin voltage range                                     | -1               |     | 1          | $\mu\text{A}$    |

## 7.6 I<sup>2</sup>C Serial Bus Timing Parameters

These specifications are ensured by design. Unless otherwise noted,  $V_{IN\_BX} = 3.7$  V. See <sup>(1)</sup> and 图 1.

|              |                                                      | MIN                             | MAX  | UNIT    |
|--------------|------------------------------------------------------|---------------------------------|------|---------|
| $f_{SCL}$    | Serial clock frequency                               | Standard mode                   | 100  | kHz     |
|              |                                                      | Fast mode                       | 400  |         |
|              |                                                      | Fast mode+                      | 1    | MHz     |
|              |                                                      | High-speed mode, $C_b = 100$ pF | 3.4  |         |
|              |                                                      | High-speed mode, $C_b = 400$ pF | 1.7  |         |
| $t_{LOW}$    | SCL low time                                         | Standard mode                   | 4.7  | $\mu$ s |
|              |                                                      | Fast mode                       | 1.3  |         |
|              |                                                      | Fast mode+                      | 0.5  |         |
|              |                                                      | High-speed mode, $C_b = 100$ pF | 0.16 |         |
|              |                                                      | High-speed mode, $C_b = 400$ pF | 0.32 |         |
| $t_{HIGH}$   | SCL high time                                        | Standard mode                   | 4    | $\mu$ s |
|              |                                                      | Fast mode                       | 0.6  |         |
|              |                                                      | Fast mode+                      | 0.26 |         |
|              |                                                      | High-speed mode, $C_b = 100$ pF | 0.06 |         |
|              |                                                      | High-speed mode, $C_b = 400$ pF | 0.12 |         |
| $t_{SU;DAT}$ | Data setup time                                      | Standard mode                   | 250  | ns      |
|              |                                                      | Fast mode                       | 100  |         |
|              |                                                      | Fast mode+                      | 50   |         |
|              |                                                      | High-speed mode                 | 10   |         |
| $t_{HD;DAT}$ | Data hold time                                       | Standard mode                   | 10   | ns      |
|              |                                                      | Fast mode                       | 10   |         |
|              |                                                      | Fast mode+                      | 10   |         |
|              |                                                      | High-speed mode, $C_b = 100$ pF | 10   |         |
|              |                                                      | High-speed mode, $C_b = 400$ pF | 10   |         |
| $t_{SU;STA}$ | Setup time for a start or a repeated start condition | Standard mode                   | 4.7  | $\mu$ s |
|              |                                                      | Fast mode                       | 0.6  |         |
|              |                                                      | Fast mode+                      | 0.26 |         |
|              |                                                      | High-speed mode                 | 0.16 |         |
| $t_{HD;STA}$ | Hold time for a start or a repeated start condition  | Standard mode                   | 4    | $\mu$ s |
|              |                                                      | Fast mode                       | 0.6  |         |
|              |                                                      | Fast mode+                      | 0.26 |         |
|              |                                                      | High-speed mode                 | 0.16 |         |
| $t_{BUF}$    | Bus free time between a stop and start condition     | Standard mode                   | 4.7  | $\mu$ s |
|              |                                                      | Fast mode                       | 1.3  |         |
|              |                                                      | Fast mode +                     | 0.5  |         |
| $t_{SU;STO}$ | Setup time for a stop condition                      | Standard mode                   | 4    | $\mu$ s |
|              |                                                      | Fast mode                       | 0.6  |         |
|              |                                                      | Fast mode+                      | 0.26 |         |
|              |                                                      | High-speed mode                 | 0.16 |         |
| $t_{rDA}$    | Rise time of SDA signal                              | Standard mode                   | 1000 | ns      |
|              |                                                      | Fast mode                       | 20   |         |
|              |                                                      | Fast mode+                      | 120  |         |
|              |                                                      | High-speed mode, $C_b = 100$ pF | 10   |         |
|              |                                                      | High-speed mode, $C_b = 400$ pF | 20   |         |

(1)  $C_b$  refers to the capacitance of one bus line.

## I<sup>2</sup>C Serial Bus Timing Parameters (continued)

These specifications are ensured by design. Unless otherwise noted,  $V_{IN\_BX} = 3.7\text{ V}$ . See <sup>(1)</sup> and 图 1.

|            |                                                                                                            | MIN                                         | MAX                                 | UNIT |
|------------|------------------------------------------------------------------------------------------------------------|---------------------------------------------|-------------------------------------|------|
| $t_{fDA}$  | Fall time of SDA signal                                                                                    | Standard mode                               | 300                                 | ns   |
|            |                                                                                                            | Fast mode                                   | $20 \times (V_{DD} / 5.5\text{ V})$ |      |
|            |                                                                                                            | Fast mode+                                  | $20 \times (V_{DD} / 5.5\text{ V})$ |      |
|            |                                                                                                            | High-speed mode, $C_b = 100\text{ pF}$      | 10                                  |      |
|            |                                                                                                            | High-speed mode, $C_b = 400\text{ pF}$      | 30                                  |      |
| $t_{rCL}$  | Rise time of SCL signal                                                                                    | Standard mode                               | 1000                                | ns   |
|            |                                                                                                            | Fast mode                                   | 20                                  |      |
|            |                                                                                                            | Fast mode+                                  | 120                                 |      |
|            |                                                                                                            | High-speed mode, $C_b = 100\text{ pF}$      | 10                                  |      |
|            |                                                                                                            | High-speed mode, $C_b = 400\text{ pF}$      | 20                                  |      |
| $t_{rCL1}$ | Rise time of SCL signal after a repeated start condition and after an acknowledge bit                      | High-speed mode, $C_b = 100\text{ pF}$      | 10                                  | ns   |
|            |                                                                                                            | High-speed mode, $C_b = 400\text{ pF}$      | 20                                  |      |
| $t_{fCL}$  | Fall time of a SCL signal                                                                                  | Standard mode                               | 300                                 | ns   |
|            |                                                                                                            | Fast mode                                   | $20 \times (V_{DD} / 5.5\text{ V})$ |      |
|            |                                                                                                            | Fast mode +                                 | $20 \times (V_{DD} / 5.5\text{ V})$ |      |
|            |                                                                                                            | High-speed mode, $C_b = 10 - 100\text{ pF}$ | 10                                  |      |
|            |                                                                                                            | High-speed mode, $C_b = 400\text{ pF}$      | 20                                  |      |
| $C_b$      | Capacitive load for each bus line (SCL and SDA)                                                            |                                             | 400                                 | pF   |
| $t_{SP}$   | Pulse width of spike suppressed (SCL and SDA spikes that are less than the indicated width are suppressed) | Standard mode, fast mode, and fast mode+    | 50                                  | ns   |
|            |                                                                                                            | High-speed mode                             | 10                                  |      |

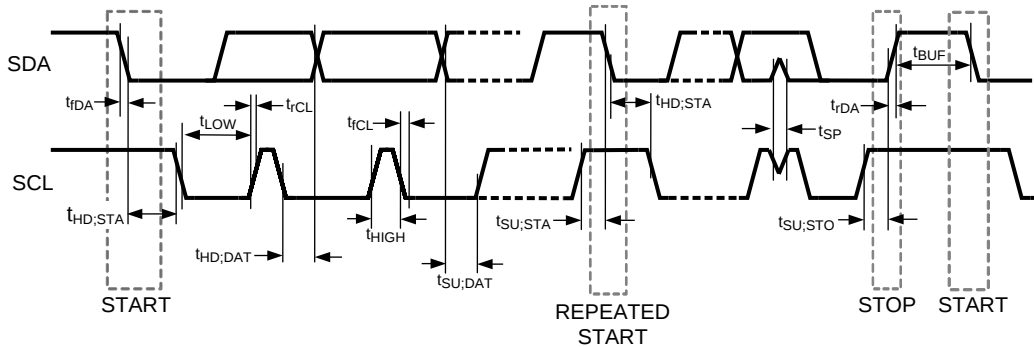


图 1. I<sup>2</sup>C Timing

## 7.7 Typical Characteristics

Unless otherwise specified:  $V_{(VIN\_Bx)} = V_{(VIN\_LDOx)} = V_{(VANA)} = 3.7\text{ V}$ ,  $V_{OUT\_Bx} = 1\text{ V}$ ,  $V_{OUT\_LDO} = 1\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $L = 0.47\text{ }\mu\text{H}$  (TOKO DFE252012PD-R47M),  $C_{OUT\_BUCK} = 22\text{ }\mu\text{F}$ ,  $C_{POL\_BUCK} = 22\text{ }\mu\text{F}$ , and  $C_{OUT\_LDO} = 1\text{ }\mu\text{F}$ .

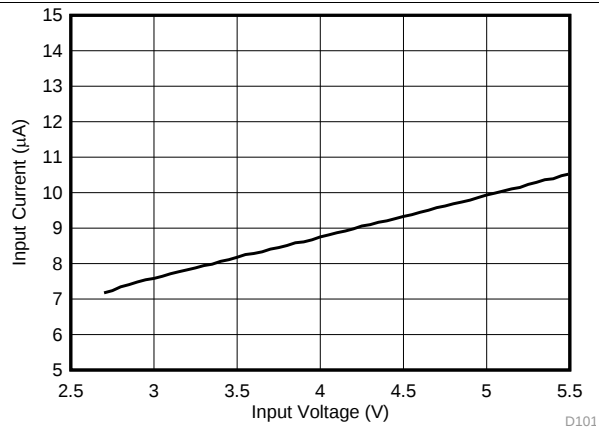


图 2. Standby Current Consumption vs Input Voltage

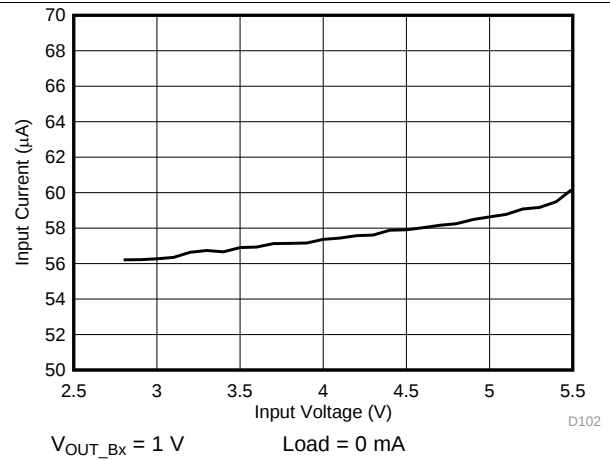


图 3. Active State Current Consumption vs Input Voltage, One Buck Regulator Enabled in PFM Mode

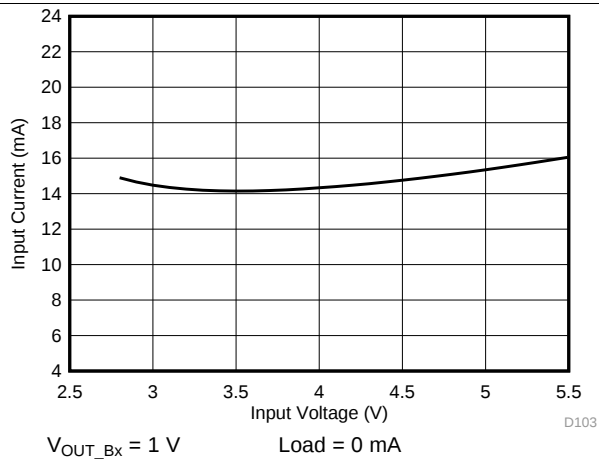


图 4. Active State Current Consumption vs Input Voltage, One Buck Regulator Enabled in Forced PWM Mode

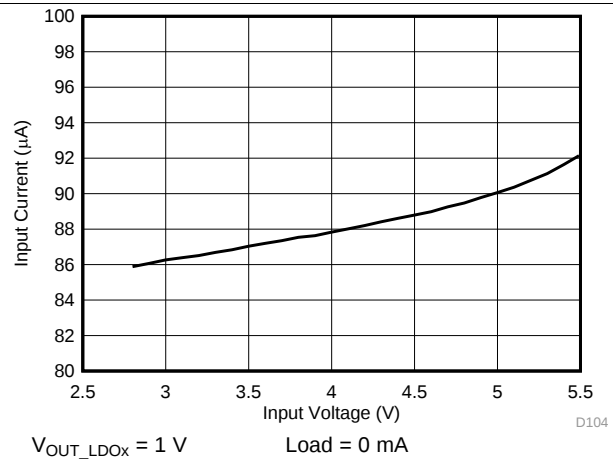


图 5. Active State Current Consumption vs Input Voltage, One LDO Regulator Enabled

## 8 Detailed Description

### 8.1 Overview

The LP87322B/D/E/F-Q1 is a high-efficiency, high-performance flexible power supply device with two step-down DC-DC converter cores (Buck0 and Buck1) and two low-dropout (LDO) linear regulators (LDO0 and LDO1) for automotive applications. 表 1 lists the output characteristics of the regulators.

**表 1. Supply Specification**

| SUPPLY | OUTPUT                     |                                                                     |                                              |
|--------|----------------------------|---------------------------------------------------------------------|----------------------------------------------|
|        | V <sub>OUT</sub> RANGE (V) | RESOLUTION (mV)                                                     | I <sub>MAX</sub> MAXIMUM OUTPUT CURRENT (mA) |
| Buck0  | 0.7 to 3.36                | 10 (0.7 V to 0.73 V)<br>5 (0.73 V to 1.4 V)<br>20 (1.4 V to 3.36 V) | 2000                                         |
| Buck1  | 0.7 to 3.36                | 10 (0.7 V to 0.73 V)<br>5 (0.73 V to 1.4 V)<br>20 (1.4 V to 3.36 V) | 2000                                         |
| LDO0   | 0.8 to 3.3                 | 100                                                                 | 300                                          |
| LDO1   | 0.8 to 3.3                 | 100                                                                 | 300                                          |

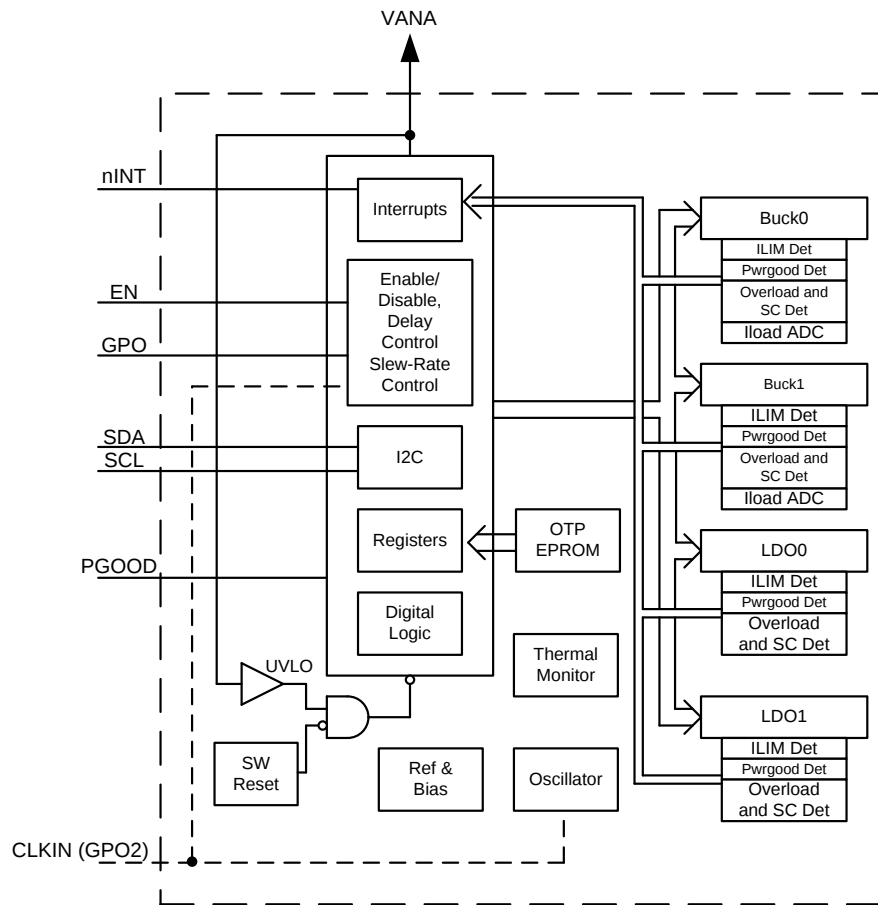
The LP87322B/D/E/F-Q1 also supports switching clock synchronization to an external clock (CLKIN pin). The nominal frequency of the external clock can be from 1 MHz to 24 MHz with 1-MHz steps.

Additional features include:

- Soft-start
- Input voltage protection:
  - Undervoltage lockout
  - Overvoltage protection
- Output voltage monitoring and protection:
  - Overvoltage monitoring
  - Undervoltage monitoring
  - Overload protection
- Thermal warning
- Thermal shutdown

The LP87322B/D/E/F-Q1 has one dedicated general purpose digital output (GPO) signal. CLKIN pin can be programmed as a second GPO signal (GPO2) if external clock is not needed. The output type (open-drain or push-pull) is programmable for the GPOs.

## 8.2 Functional Block Diagram



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## 8.3 Feature Description

### 8.3.1 DC-DC Converters

#### 8.3.1.1 Overview

The LP87322B/D/E/F-Q1 includes two step-down DC-DC converter cores. The cores are designed for flexibility; most of the functions are programmable, thus giving a possibility to optimize the regulator operation for each application. The buck regulators deliver 0.7-V to 3.36-V regulated voltage rails from a 2.8-V to 5.5-V supply voltage.

The LP87322B/D/E/F-Q1 has the following features:

- DVS support with programmable slew rate
- Automatic mode control based on the loading (PFM or PWM mode)
- Forced PWM mode option
- Optional external clock input to minimize crosstalk
- Optional spread-spectrum technique to reduce EMI
- Phase control for optimized EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Power Good flag with maskable interrupt

## Feature Description (接下页)

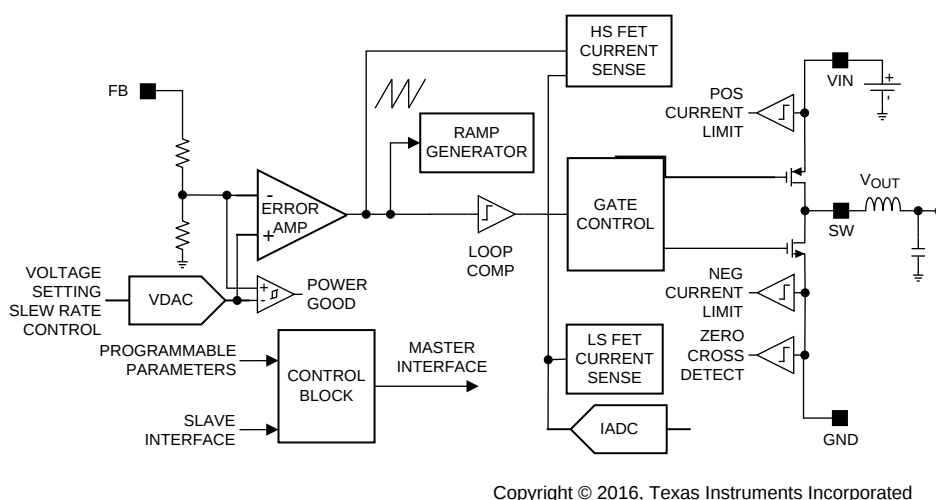
- Power Good signal (PGOOD) with selectable sources
- Average output current sensing (for PFM entry and load current measurement)

The following parameters can be programmed via registers, the default values are set by OTP bits:

- Output voltage
- Forced PWM operation
- Switch current limit
- Output voltage slew rate
- Enable and disable delays

There are two modes of operation for the buck converter, depending on the output current required: pulse-width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 600 mA or higher. Lighter output current loads cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. The forced PWM mode can be selected to maintain fixed switching frequency at all load current levels.

A block diagram of a single core is shown in 图 6.



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图 6. Detailed Block Diagram Showing One Core

### 8.3.1.2 Transition Between PWM and PFM Modes

PWM mode operation optimizes efficiency at mid to full load at the expense of light-load efficiency. The LP87322B/D/E/F-Q1 converter operates in PWM mode at load current of about 600 mA or higher. At lighter load current levels the device automatically switches into PFM mode for reduced current consumption when forced PWM mode is disabled (AUTO mode operation). By combining the PFM and the PWM modes a high efficiency is achieved over a wide output-load current range.

### 8.3.1.3 Buck Converter Load Current Measurement

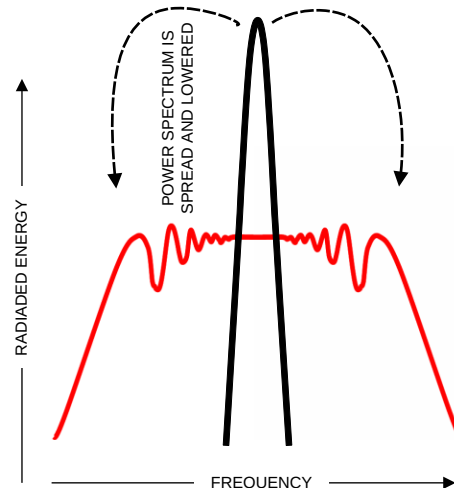
Buck load current can be monitored via I<sup>2</sup>C registers. The monitored buck converter is selected with the LOAD\_CURRENT\_BUCK\_SELECT bit in SEL\_I\_LOAD register. A write to this selection register starts a current measurement sequence. The regulator is automatically forced to PWM mode for the measurement period. The measurement sequence is 50  $\mu$ s long, maximum.

LP87322B/D/E/F-Q1 can be configured to give out an interrupt (I\_MEAS\_INT bit in INT\_TOP\_1 register) after the load current measurement sequence is finished. Load current measurement interrupt can be masked with I\_MEAS\_MASK bit (TOP\_MASK\_1 register). The measurement result can be read from registers I\_LOAD\_1 and I\_LOAD\_2. Register I\_LOAD\_1 bits BUCK\_LOAD\_CURRENT[7:0] give out the LSB bits and register I\_LOAD\_2 bit BUCK\_LOAD\_CURRENT[8] the MSB bit. The measurement result BUCK\_LOAD\_CURRENT[8:0] LSB is 20 mA, and maximum code value of the measurement corresponds to 10.22 A.

## Feature Description (接下页)

### 8.3.1.4 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP87322B/D/E/F-Q1 has register selectable spread-spectrum mode which minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies around the center frequency, reducing the EMI emissions radiated by the converter and associated passive components and PCB traces (see 图 7). This feature is available only when internal RC oscillator is used (EN\_PLL bit is 0 in PLL\_CTRL register), and it is enabled with the EN\_SPREAD\_SPEC bit in CONFIG register, and it affects both buck cores.



Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP87322B/D/E/F-Q1 spreads that energy over a large bandwidth.

**图 7. Spread-Spectrum Modulation**

### 8.3.2 Sync Clock Functionality

The LP87322B/D/E/F-Q1 device contains a CLKIN input to synchronize the switching clock of the buck regulators with the external clock. The block diagram of the clocking and PLL module is shown in 图 8. Depending on the EN\_PLL bit in PLL\_CTRL register and the external clock availability, the external clock is selected and interrupt is generated as shown in 表 2. The interrupt can be masked with SYNC\_CLK\_MASK bit in TOP\_MASK\_1 register. The nominal frequency of the external input clock is set by EXT\_CLK\_FREQ[4:0] bits in PLL\_CTRL register, and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/+10%) of the selected frequency for valid clock detection.

The SYNC\_CLK\_INT interrupt in INT\_TOP\_1 register is also generated in cases where the external clock is expected but it is not available. These cases are start-up (read OTP-to-standby transition) when EN\_PLL is 1 and Buck regulator enable (standby-to-active transition) when EN\_PLL is 1.

## Feature Description (接下页)

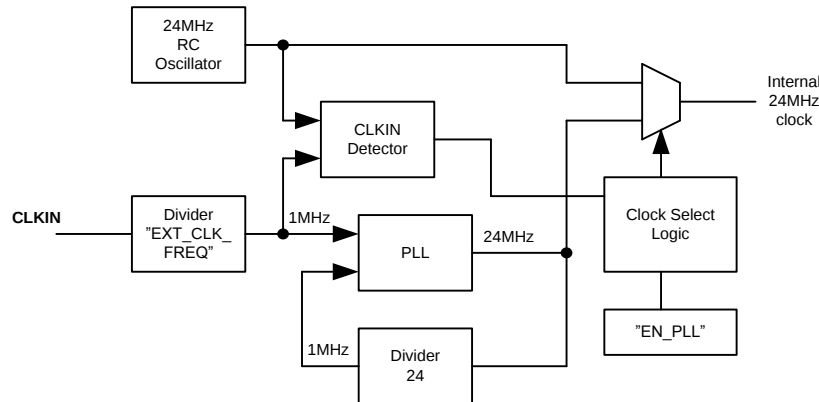


图 8. Clock and PLL Module

表 2. PLL Operation

| DEVICE OPERATION MODE | EN_PLL | PLL AND CLOCK DETECTOR STATE | INTERRUPT FOR EXTERNAL CLOCK              | CLOCK                                             |
|-----------------------|--------|------------------------------|-------------------------------------------|---------------------------------------------------|
| STANDBY               | 0      | Disabled                     | No                                        | Internal RC                                       |
| ACTIVE                | 0      | Disabled                     | No                                        | Internal RC                                       |
| STANDBY               | 1      | Enabled                      | When external clock appears or disappears | Automatic change to external clock when available |
| ACTIVE                | 1      | Enabled                      | When external clock appears or disappears | Automatic change to external clock when available |

### 8.3.3 Low-Dropout Linear Regulators (LDOs)

The LP87322B/D/E/F-Q1 device includes two identical linear regulators, LDO0 and LDO1, targeting analog loads with low noise requirements. The LDO regulators deliver 0.8-V to 3.3-V regulated voltage rails from a 2.5-V to 5.5-V input voltage. Both regulators have dedicated inputs which can be higher or lower than the device system voltage  $V_{(VANA)}$  to minimize the power dissipation.

### 8.3.4 Power-Up

The power-up sequence for the LP87322B/D/E/F-Q1 is as follows:

- VANA (and VIN\_Bx) reach minimum recommended levels ( $V_{VANA} > V_{ANA_{UVLO}}$ ). This initiates power-on-reset (POR), OTP reading, and enables the system I/O interface. The I<sup>2</sup>C host should allow at least 1.2 ms before writing or reading data to the LP87322B/D/E/F-Q1.
- Device enters standby mode.
- The host can change the default register setting by I<sup>2</sup>C if needed.
- The regulators can be enabled/disabled and the GPO signals can be controlled by EN pin and by I<sup>2</sup>C interface.

Transitions between the operating modes are shown in [Modes of Operation](#).

### 8.3.5 Regulator Control

#### 8.3.5.1 Enabling and Disabling Regulators

The regulators can be enabled when the device is in STANDBY or ACTIVE state. There are two ways for enable and disable the buck regulators:

- Using BUCKx\_EN bit in BUCKx\_CTRL\_1 register (BUCKx\_EN\_PIN\_CTRL bit is 0 in BUCKx\_CTRL\_1 register)
- Using EN control pin (BUCKx\_EN bit is 1 AND BUCKx\_EN\_PIN\_CTRL bit is 1)

Similarly there are two ways to enable and disable the LDO regulators:

- Using LDOx\_EN bit in LDOx\_CTRL register (LDOx\_EN\_PIN\_CTRL bit is 0 in LDOx\_CTRL register)
- Using EN control pin (LDOx\_EN bit is 1 **AND** LDOx\_EN\_PIN\_CTRL bit is 1)

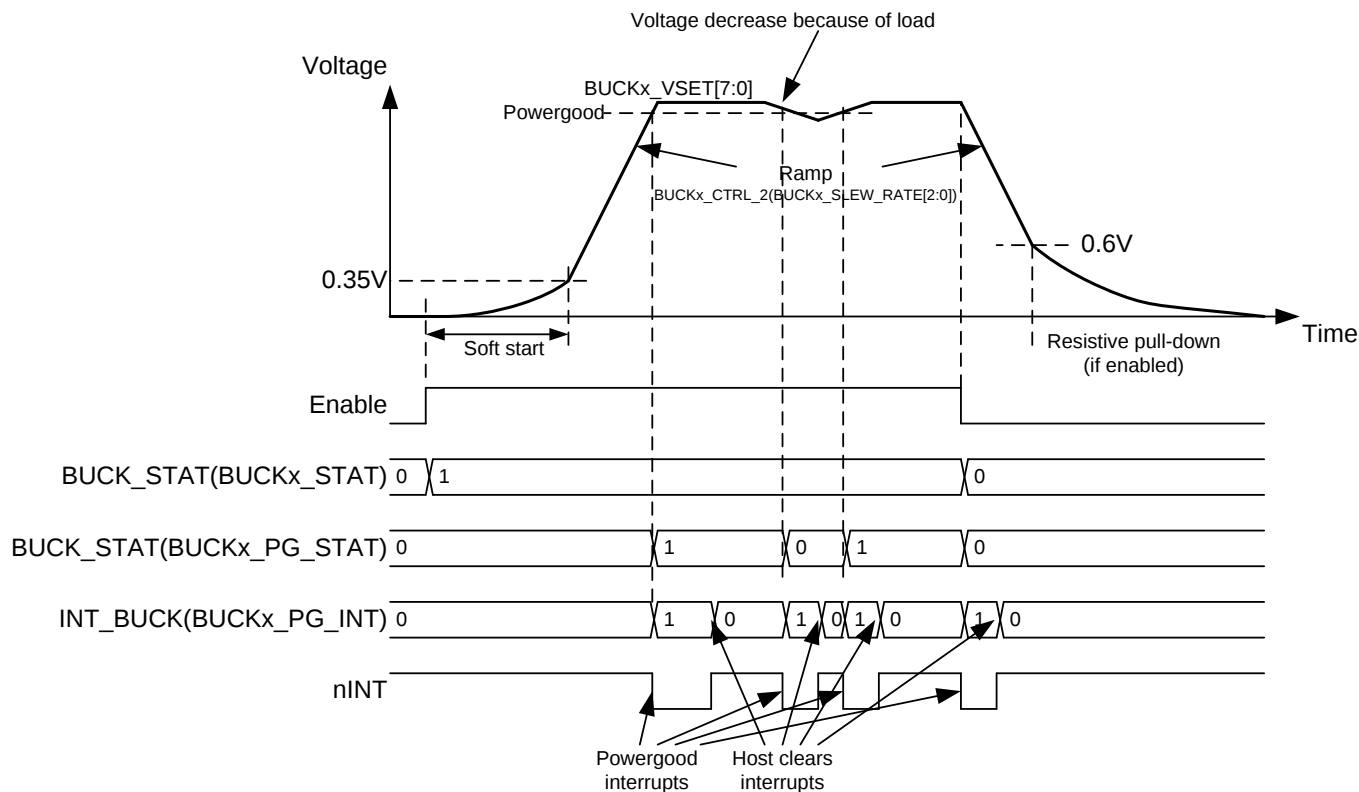
If the EN control pin is used for enable and disable then the delay from the control signal rising edge to start-up is set by BUCKx\_STARTUP\_DELAY[3:0] bits in BUCKx\_DELAY register and LDOx\_STARTUP\_DELAY[3:0] bits in LDOx\_DELAY register and the delay from control signal falling edge to shutdown is set by BUCKx\_SHUTDOWN\_DELAY[3:0] bits in BUCKx\_DELAY register and LDOx\_SHUTDOWN\_DELAY[3:0] bits in LDOx\_DELAY register. The delays are valid only for EN signal transitions and not for control with I<sup>2</sup>C writings to BUCKx\_EN and LDOx\_EN bits.

The control of the regulator (with 0-ms delays) is shown in 表 3.

**表 3. Regulator Control**

|                                                     | BUCKx_EN /<br>LDOx_EN | BUCKx_EN_PIN_CTRL /<br>LDOx_EN_PIN_CTRL | EN PIN     | BUCKx OUTPUT VOLTAGE /<br>LDOx OUTPUT VOLTAGE |
|-----------------------------------------------------|-----------------------|-----------------------------------------|------------|-----------------------------------------------|
| Enable/disable control with<br>BUCKx_EN/LDOx_EN bit | 0                     | Don't Care                              | Don't Care | Disabled                                      |
|                                                     | 1                     | 0                                       | Don't Care | BUCKx_VSET[7:0] / LDOx_VSET[4:0]              |
| Enable/disable control with<br>EN pin               | 1                     | 1                                       | Low        | Disabled                                      |
|                                                     | 1                     | 1                                       | High       | BUCKx_VSET[7:0] / LDOx_VSET[4:0]              |

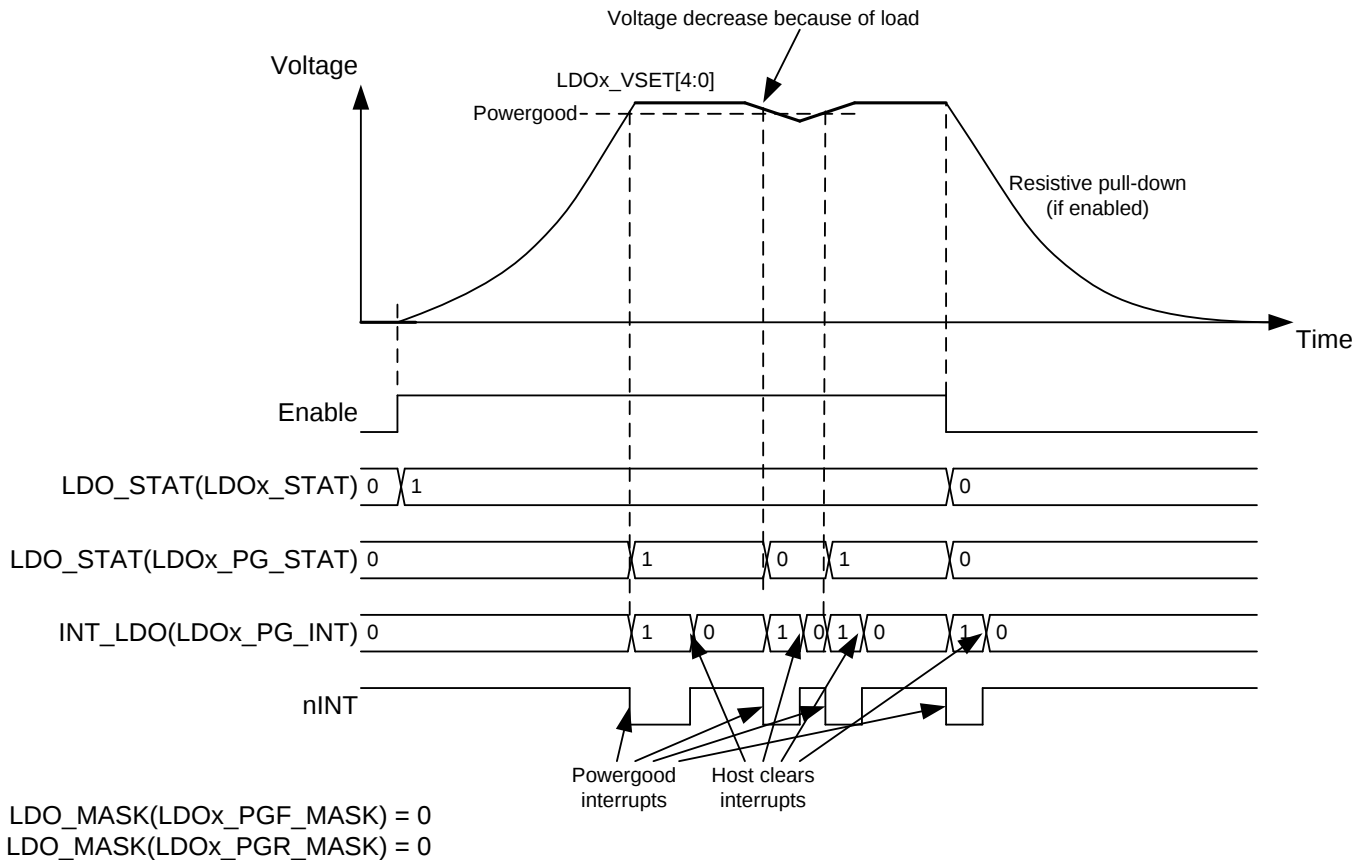
The buck regulator is enabled by the EN pin or by I<sup>2</sup>C writing as shown in 图 9. The soft-start circuit limits the in-rush current during start-up. When the output voltage rises to a 0.35-V level, the output voltage becomes slew-rate controlled. If there is a short circuit at the output, and the output voltage does not increase above the 0.35-V level in 1 ms or the output voltage drops below 0.35-V level during operation (for minimum of 1 ms), the regulator is disabled, and BUCKx\_SC\_INT interrupt in INT\_BUCK register is set. When the output voltage reaches the Power-Good threshold level the BUCKx\_PG\_INT interrupt flag in INT\_BUCK register is set. The Power-Good interrupt flag when reaching valid output voltage can be masked using BUCKx\_PGR\_MASK bit in BUCK\_MASK register. The Power-Good interrupt flag can be also generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BUCKx\_PGF\_MASK bit in BUCK\_MASK register. A BUCKx\_PG\_STAT bit in BUCK\_STAT register shows always the validity of the output voltage: 1 means valid and 0 means invalid output voltage. A PGOOD\_WINDOW\_BUCK bit in PGOOD\_CTRL\_1 register sets the detection method for the valid buck output voltage, either undervoltage detection or undervoltage and overvoltage detection.



BUCK\_MASK(BUCKx\_PGF\_MASK) = 0  
BUCK\_MASK(BUCKx\_PGR\_MASK) = 0

**图 9. Buck Regulator Enable and Disable**

The LDO regulator is enabled by the EN pin or by I<sup>2</sup>C writing as shown in 图 10. The soft-start circuit limits the in-rush current during start-up. Output voltage increase rate is less than 100 mV/μsec during soft-start. If there is a short circuit at the output, and the output voltage does not increase above the 0.3-V level in 1 ms or the output voltage drops below 0.3-V level during operation (for minimum of 1 ms), the regulator is disabled, and LDOx\_SC\_INT interrupt in INT\_LDO register is set. When the output voltage reaches the Power-Good threshold level the LDOx\_PG\_INT interrupt flag in INT\_LDO register is set. The Power-Good interrupt flag when reaching valid output voltage can be masked using LDOx\_PGR\_MASK bit in LDO\_MASK register. The Power-Good interrupt flag can be also generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by LDOx\_PGF\_MASK bit in LDO\_MASK register. A LDOx\_PG\_STAT bit in LDO\_STAT register shows always the validity of the output voltage; 1 means valid, and 0 means invalid output voltage. A PGOOD\_WINDOW\_LDO bit in PGOOD\_CTRL\_1 register sets the detection method for the valid LDO output voltage, either undervoltage detection or undervoltage and overvoltage detection.



**图 10. LDO Regulator Enable and Disable**

The EN input pin have an integrated pulldown resistor. The pulldown resistor is controlled with EN\_PD bit in CONFIG register.

### 8.3.5.2 Changing Output Voltage

The output voltage of the regulator can be changed by writing to the BUCKx\_VOUT / LDOx\_VOUT register. The voltage change for buck regulator is always slew-rate controlled, and the slew-rate is defined by the BUCKx\_SLEW\_RATE[2:0] bits in BUCKx\_CTRL\_2 register. During voltage change the forced PWM mode is used automatically. When the programmed output voltage is achieved, the mode becomes the one defined by load current, and the BUCKx\_FPWM bit in BUCKx\_CTRL\_1 register.

The voltage change and Power-Good interrupts are shown in 图 11.

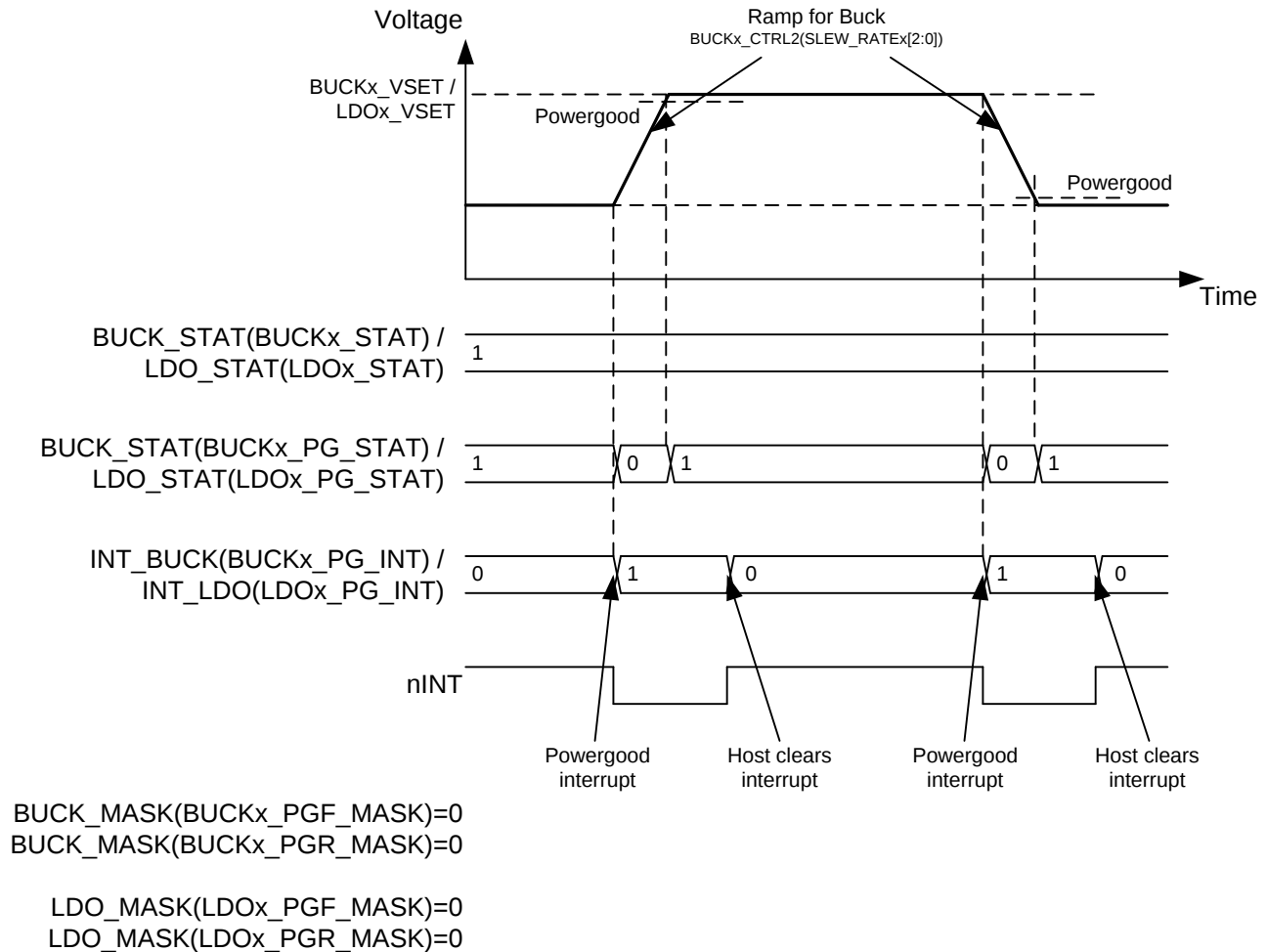


图 11. Regulator Output Voltage Change

During an LDO voltage change the internal reference for the Power-Good detection is also changed. For this reason the Power Good may toggle during the LDO voltage change can indicate valid output even when the output voltage is changing. This period takes less than 100  $\mu\text{s}$  and after that time the Power Good gives correct value.

### 8.3.6 Enable and Disable Sequences

The LP87322B/D/E/F-Q1 device supports start-up and shutdown sequencing with programmable delays for different regulator outputs using single EN control signal. The Buck regulator is selected for delayed control with:

- $\text{BUCKx\_EN} = 1$  in  $\text{BUCKx\_CTRL\_1}$  register
- $\text{BUCKx\_EN\_PIN\_CTRL} = 1$  in  $\text{BUCKx\_CTRL\_1}$  register
- $\text{BUCKx\_VSET}[7:0]$  bits in  $\text{BUCKx\_VOUT}$  register defines the voltage when EN pin is high
- The delay from rising edge of EN pin to the regulator enable is set by  $\text{BUCKx\_STARTUP\_DELAY}[3:0]$  bits in  $\text{BUCKx\_DELAY}$  register and
- The delay from falling edge of EN pin to the regulator disable is set by  $\text{BUCKx\_SHUTDOWN\_DELAY}[3:0]$  bits in  $\text{BUCKx\_DELAY}$  register.

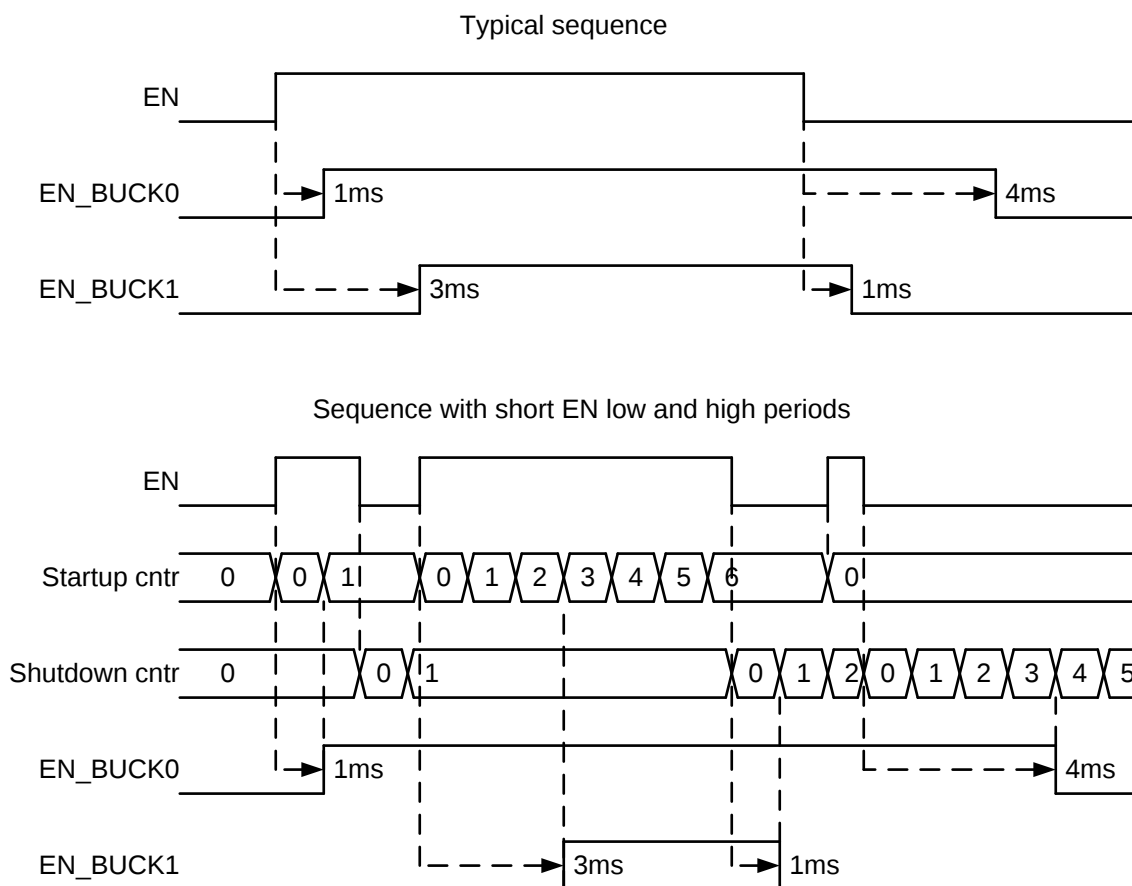
In the same way the LDO regulator is selected for delayed control with:

- LDOx\_EN = 1 in LDOx\_CTRL register
- LDOx\_EN\_PIN\_CTRL = 1 in LDOx\_CTRL register
- LDOx\_VSET[4:0] bits in LDOx\_VOUT register defines the voltage when EN pin is high
- The delay from rising edge of EN pin to the regulator enable is set by LDOx\_STARTUP\_DELAY[3:0] bits in LDOx\_DELAY register and
- The delay from falling edge of EN pin to the regulator disable is set by LDOx\_SHUTDOWN\_DELAY[3:0] bits in LDOx\_DELAY register.

The GPO (and GPO2) digital output signals can be also controlled as a part of start-up and shutdown sequencing with the following settings:

- GPOx\_EN = 1 in GPO\_CTRL register
- GPOx\_EN\_PIN\_CTRL = 1 in GPO\_CTRL register
- The delay from rising edge of EN pin to the rising edge of GPO/GPO2 signal is set by GPOx\_STARTUP\_DELAY[3:0] bits in GPOx\_DELAY register and
- The delay from falling edge of EN pin to the falling edge of GPO/GPO2 signal is set by GPOx\_SHUTDOWN\_DELAY[3:0] bits in GPOx\_DELAY register.

An example of the start-up and shutdown sequences for the buck regulators are shown in 图 12. The start-up and shutdown delays for the Buck0 regulator are 1 ms and 4 ms; for the Buck1 regulator start-up and shutdown delays are 3 ms and 1 ms. The delay settings are used only for enable/disable control with EN signal.



**图 12. Start-Up and Shutdown Sequencing**

### 8.3.7 Device Reset Scenarios

There are three reset methods implemented on the LP87322B/D/E/F-Q1:

- Software reset with SW\_RESET bit in RESET register

- Undervoltage lockout (UVLO) reset from VANA supply

An SW reset occurs when SW\_RESET bit is written 1. The bit is automatically cleared after writing. This event disables all the regulators immediately, drives GPO and GPO2 signals low, resets all the register bits to the default values and OTP bits are loaded (see 图 18). I<sup>2</sup>C interface is not reset during software reset.

If VANA supply voltage falls below the UVLO threshold level then all the regulators are disabled immediately, GPO and GPO2 signals are driven low, and all the register bits are reset to the default values. When the VANA supply voltage transition above UVLO threshold level an internal POR occurs. OTP bits are loaded to the registers and a startup is initiated according to the register settings.

### 8.3.8 Diagnosis and Protection Features

The LP87322B/D/E/F-Q1 is capable of providing four levels of protection features:

- Information of valid regulator output voltage which sets interrupt or PGOOD signal;
- Warnings for diagnosis which sets interrupt;
- Protection events which are disabling the regulators; and
- Faults which are causing the device to shutdown.

The LP87322B/D/E/F-Q1 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. nINT is released again after a clear of flags is complete. The nINT signal stays low until all the pending interrupts are cleared.

When a fault is detected or software requested reset, it is indicated by a RESET\_REG\_INT interrupt flag in INT\_TOP\_2 register after next start-up. If the RESET\_REG\_MASK is set to masked in the OTP, the interrupt is not generated. The mask bit change with I<sup>2</sup>C does not affect, because the RESET\_REG\_MASK bit is loaded from OTP during reset sequence.

**表 4. Summary of Interrupt Signals**

| EVENT                                                                                                                                                        | OUTCOME                                                             | INTERRUPT BIT              | INTERRUPT MASK BIT | STATUS BIT      | RECOVERY/INTERRUPT CLEAR                                                                               |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|----------------------------|--------------------|-----------------|--------------------------------------------------------------------------------------------------------|
| Buck current limit triggered                                                                                                                                 | No effect                                                           | BUCK_INT<br>BUCKx_ILIM_INT | BUCKx_ILIM_MASK    | BUCKx_ILIM_STAT | Write 1 to BUCKx_ILIM_INT bit<br>Interrupt is not cleared if current limit is active                   |
| LDO current limit triggered                                                                                                                                  | No effect                                                           | LDO_INT<br>LDOx_ILIM_INT   | LDOx_ILIM_MASK     | LDOx_ILIM_STAT  | Write 1 to LDOx_ILIM_INT bit<br>Interrupt is not cleared if current limit is active                    |
| Buck short circuit (V <sub>VOUT</sub> < 0.35 V at 1 ms after enable) or overload (V <sub>VOUT</sub> decreasing below 0.35 V during operation, 1-ms debounce) | Regulator disable                                                   | BUCK_INT<br>BUCKx_SC_INT   | N/A                | N/A             | Write 1 to BUCKx_SC_INT bit                                                                            |
| LDO short circuit (V <sub>VOUT</sub> < 0.3 V at 1 ms after enable) or overload (V <sub>VOUT</sub> decreasing below 0.3 V during operation, 1-ms debounce)    | Regulator disable                                                   | LDO_INT<br>LDOx_SC_INT     | N/A                | N/A             | Write 1 to LDOx_SC_INT bit                                                                             |
| Thermal warning                                                                                                                                              | No effect                                                           | TDIE_WARN_INT              | TDIE_WARN_MASK     | TDIE_WARN_STAT  | Write 1 to TDIE_WARN_INT bit<br>Interrupt is not cleared if temperature is above thermal warning level |
| Thermal shutdown                                                                                                                                             | All regulators disabled immediately and GPO and GPO2 are set to low | TDIE_SD_INT                | N/A                | TDIE_SD_STAT    | Write 1 to TDIE_SD_INT bit<br>Interrupt is not cleared if temperature is above thermal shutdown level  |
| VANA overvoltage (VANA <sub>OVP</sub> )                                                                                                                      | All regulators disabled immediately and GPO and GPO2 are set to low | OVP_INT                    | N/A                | OVP_STAT        | Write 1 to OVP_INT bit<br>Interrupt is not cleared if VANA voltage is above VANA <sub>OVP</sub> level  |
| Buck power good, output voltage becomes valid                                                                                                                | No effect                                                           | BUCK_INT<br>BUCKx_PG_INT   | BUCKx_PGR_MASK     | BUCKx_PG_STAT   | Write 1 to BUCKx_PG_INT bit                                                                            |
| Buck power good, output voltage becomes invalid                                                                                                              | No effect                                                           | BUCK_INT<br>BUCKx_PG_INT   | BUCKx_PGF_MASK     | BUCKx_PG_STAT   | Write 1 to BUCKx_PG_INT bit                                                                            |
| LDO Power Good, output voltage becomes valid                                                                                                                 | No effect                                                           | LDO_INT<br>LDOx_PG_INT     | LDOx_PGR_MASK      | LDOx_PG_STAT    | Write 1 to LDOx_PG_INT bit                                                                             |

**表 4. Summary of Interrupt Signals (接下页)**

| EVENT                                                           | OUTCOME                                                                    | INTERRUPT BIT               | INTERRUPT MASK BIT | STATUS BIT    | RECOVERY/INTERRUPT CLEAR     |
|-----------------------------------------------------------------|----------------------------------------------------------------------------|-----------------------------|--------------------|---------------|------------------------------|
| LDO power good, output voltage becomes invalid                  | No effect                                                                  | LDO_INT<br>LDOx_PG_INT      | LDOx_PGF_MASK      | LDOx_PG_STAT  | Write 1 to LDOx_PG_INT bit   |
| PGOOD pin changing from active to inactive state <sup>(1)</sup> | No effect                                                                  | PGOOD_INT                   | PGOOD_MASK         | PGOOD_STAT    | Write 1 to PGOOD_INT bit     |
| External clock appears or disappears                            | No effect to regulators                                                    | SYNC_CLK_INT <sup>(2)</sup> | SYNC_CLK_MASK      | SYNC_CLK_STAT | Write 1 to SYNC_CLK_INT bit  |
| Load current measurement ready                                  | No effect                                                                  | I_MEAS_INT                  | I_MEAS_MASK        | N/A           | Write 1 to I_MEAS_INT bit    |
| Supply voltage VANA <sub>UVLO</sub> triggered (VANA falling)    | Immediate shutdown, registers reset to default values                      | N/A                         | N/A                | N/A           | N/A                          |
| Supply voltage VANA <sub>UVLO</sub> triggered (VANA rising)     | Startup, registers reset to default values and OTP bits loaded             | RESET_REG_INT               | RESET_REG_MASK     | N/A           | Write 1 to RESET_REG_INT bit |
| Software requested reset                                        | Immediate shutdown followed by power up, registers reset to default values | RESET_REG_INT               | RESET_REG_MASK     | N/A           | Write 1 to RESET_REG_INT bit |

(1) PGOOD\_STAT bit is 1 when the PGOOD pin shows valid voltages. PGOOD\_POL bit in PGOOD\_CTRL\_1 register affects only PGOOD pin polarity, not Power Good and PGOOD\_INT interrupt polarity.

(2) Interrupt is generated during clock-detector operation and if clock is not available when clock detector is enabled.

### 8.3.8.1 Power-Good Information (PGOOD pin)

In addition to the interrupt-based indication of the current limit and the Power-Good level the LP87322B/D/E/F-Q1 device supports monitoring with PGOOD signal:

- Regulator output voltage,
- Input supply overvoltage,
- Thermal warning and
- Thermal shutdown.

Regulator output voltage monitoring (not current limit monitoring) can be selected for PGOOD indication. This selection is individual for both buck regulators and both LDO regulators and is set by EN\_PGOOD\_BUCKx bits in PGOOD\_CTRL\_1 register and EN\_PGOOD\_LDOx bits in PGOOD\_CTRL\_1 register. When a regulator is disabled, the monitoring is automatically masked to prevent it forcing PGOOD inactive. A thermal warning can be also selected for PGOOD indication with EN\_PGOOD\_TWARN bit in PGOOD\_CTRL\_2 register. The monitoring from all the output rails, thermal warning (TDIE\_WARN\_STAT), input overvoltage interrupt (OVP\_INT), and thermal shutdown interrupt (TDIE\_SD\_INT) are combined, and PGOOD pin is active only if all the selected sources shows a valid status.

The type of output voltage monitoring for PGOOD signal is selected by PGOOD\_WINDOW\_x bits in PGOOD\_CTRL\_1 register. If the bit is 0, only undervoltage is monitored; if the bit is 1, both undervoltage and overvoltage are monitored.

The polarity and the output type (push-pull or open-drain) are selected by the PGOOD\_POL and PGOOD\_OD bits in the PGOOD\_CTRL\_1 register.

PGOOD is only *active* or *asserted* when all enabled power resource output voltages are within specified tolerance for each requested/programmed output voltage.

PGOOD is *inactive* or *de-asserted* if any enabled power resource output voltages is outside specified tolerance for each requested/programmed output voltage.

The device OTP setting selects either gated (that is, *unusual*) or continuous (that is, *invalid*) mode of operation.

#### 8.3.8.1.1 PGOOD Pin Gated mode

The gated (or *unusual*) mode of operation is selected by setting PGOOD\_MODE bit to 0 in PGOOD\_CTRL\_2 register.

For the gated mode of operation, PGOOD behaves as follows:

- PGOOD is set to *active* or *asserted* state upon exiting OTP configuration as an initial default state.

- PGOOD status is suspended or unchanged during an 800-μs gated time period, thereby *gating-off* the status indication.
- During normal power-up sequencing and requested voltage changes, PGOOD state is not changed during an 800-μs gated time period. It typically remains *active* or *asserted* for normal conditions.
- During an *abnormal* power-up sequencing and requested voltage changes, PGOOD status could change to *inactive* or *de-asserted* after an 800-μs gated time period if any output voltage is outside of regulation range.
- Using the *gated mode of operation* could allow the PGOOD signal to initiate an immediate power shutdown sequence if the PGOOD signal is wired-OR with signal connected to EN input. This type of circuit configuration provides a smart PORz function for processor that eliminates the need for additional components to generate PORz upon start-up and to monitor voltage levels of key voltage domains.

The fault sets corresponding fault bit 1 in PG\_FAULT register. The detected fault must be cleared to continue the PGOOD monitoring. The overvoltage and thermal shutdown are cleared by writing 1 to the OVP\_INT and TDIE\_SD\_INT interrupt bits in INT\_TOP\_1 register. The regulator fault is cleared by writing 1 to the corresponding register bit in PG\_FAULT register. The interrupts can be also cleared with VANA UVLO by toggling the input supply. An example of PGOOD pin operation in gated mode is shown in [图 13](#).

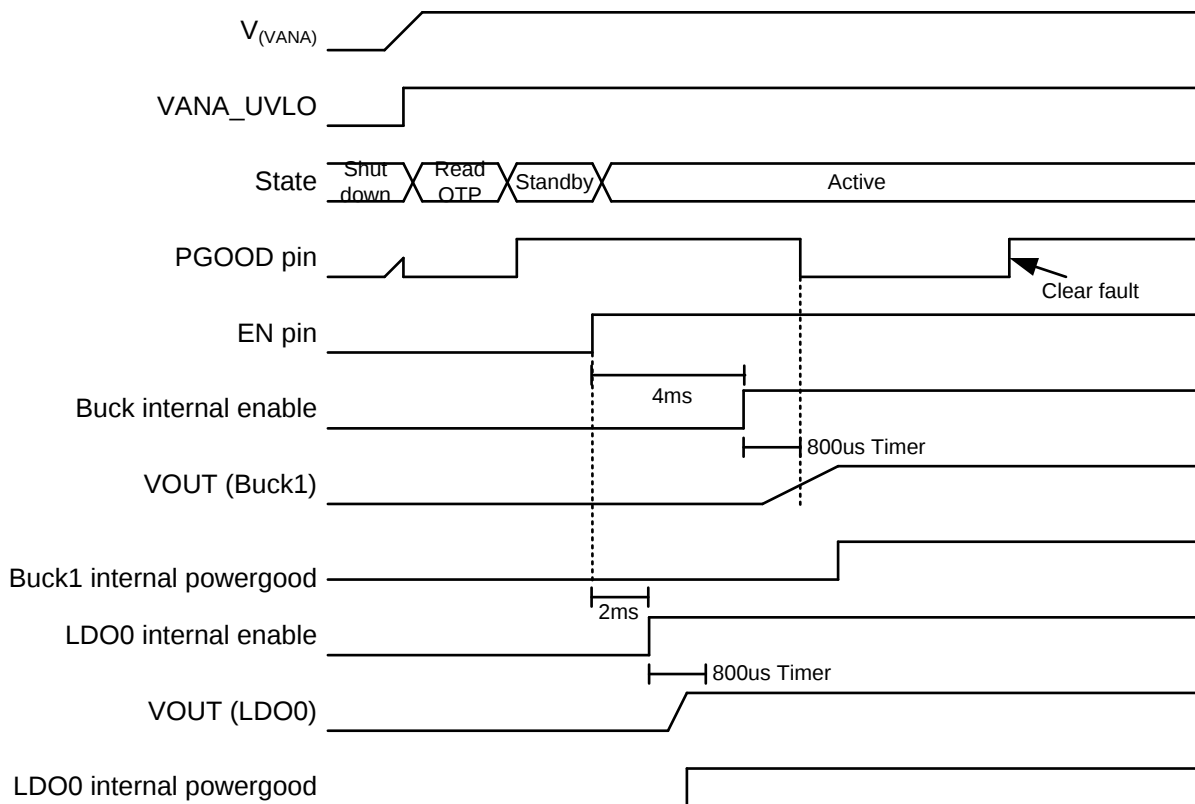


图 13. PGOOD Pin Operation in Gated Mode

#### 8.3.8.1.2 PGOOD Pin Continuous Mode

The continuous (or *invalid*) mode of operation is selected by setting PGOOD\_MODE bit to 1 in PGOOD\_CTRL\_2 register.

For the continuous mode of operation, PGOOD behaves as follows:

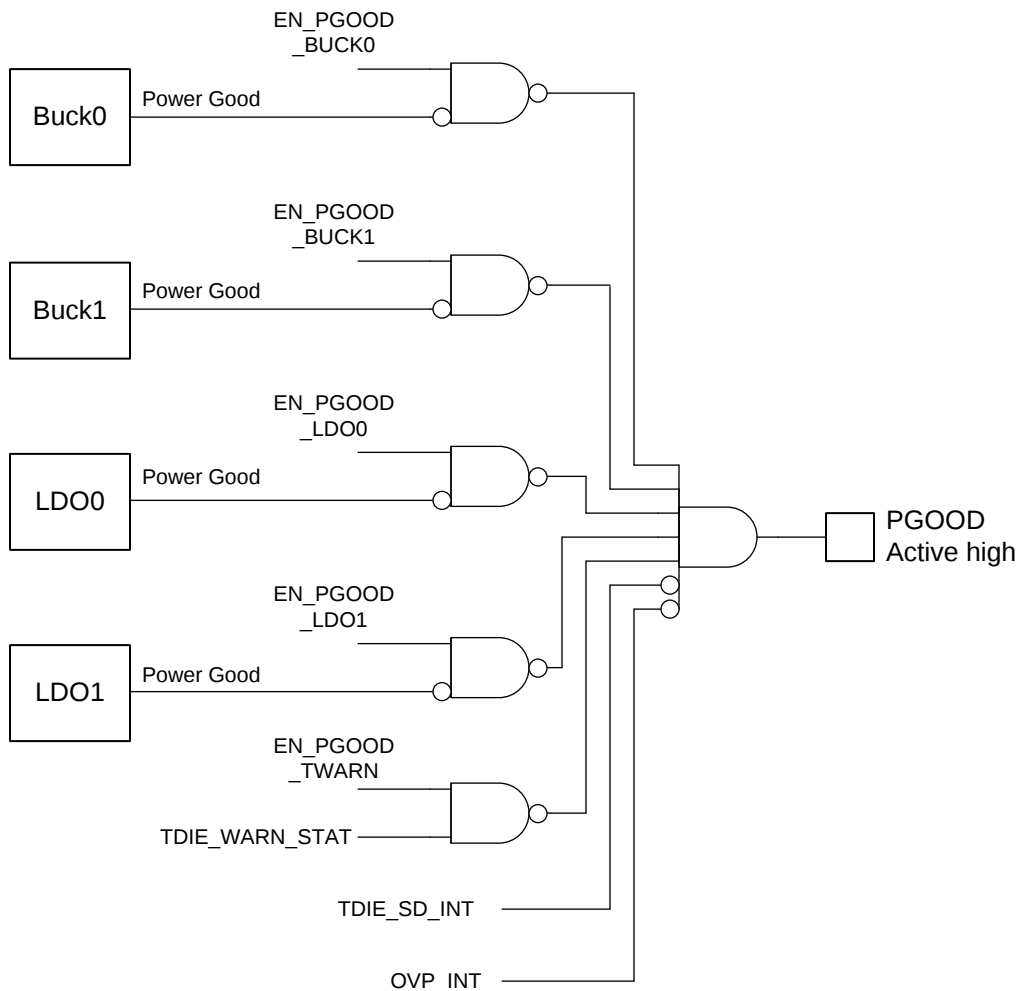
- PGOOD is set to *active* or *asserted* state upon exiting OTP configuration.
- PGOOD is set to *inactive* or *de-asserted* as soon as regulator is enabled.
- PGOOD status begins indicating output voltage regulation status immediately and continuously.
- During power-up sequencing and requested voltage changes, PGOOD will toggle between *inactive* or *de-asserted* while output voltages are outside of regulation ranges and *active* or *asserted* when inside of regulation ranges.

The PG\_FAULT register bits are latched and maintain the fault information until host clears the fault bit by writing 1 to the bit. The PGOOD signal indicates also a thermal shutdown and input overvoltage interrupts, which are cleared by clearing the interrupt bits.

When regulator voltage is transitioning from one target voltage to another, the PGOOD signal is set inactive.

When the PGOOD signal becomes inactive, the source for the fault can be read from PG\_FAULT register. If the invalid output voltage becomes valid again the PGOOD signal becomes active. Thus the PGOOD signal shows all the time if the monitored output voltages are valid. The block diagram for this operation is shown in 图 14 and an example of operation is shown in 图 15.

The PGOOD signal can be also configured so that it maintains inactive state even when the monitored outputs are valid but there are PG\_FAULT\_x bits in PG\_FAULT register pending clearance. This type of operation is selected by setting PGFAULT\_GATES\_PGOOD bit to 1 in PGOOD\_CTRL\_2 register.



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**图 14. PGOOD Block Diagram (Continuous Mode)**

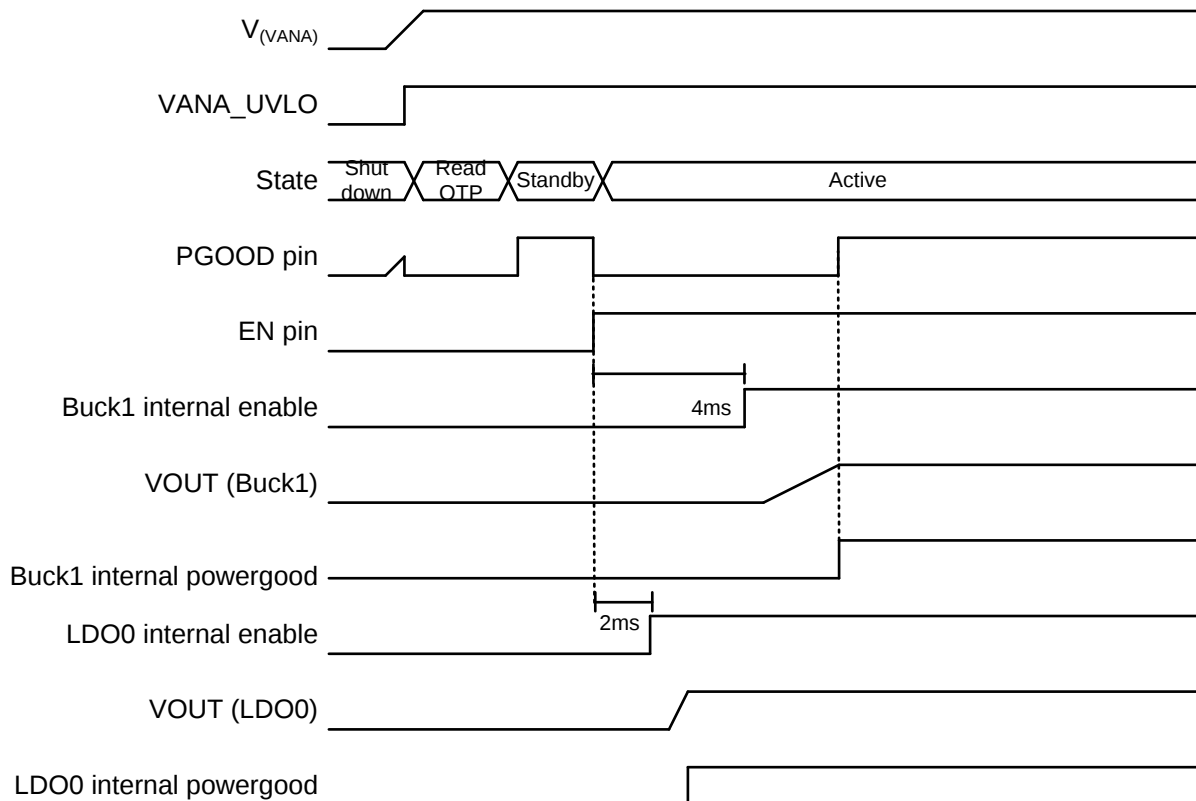
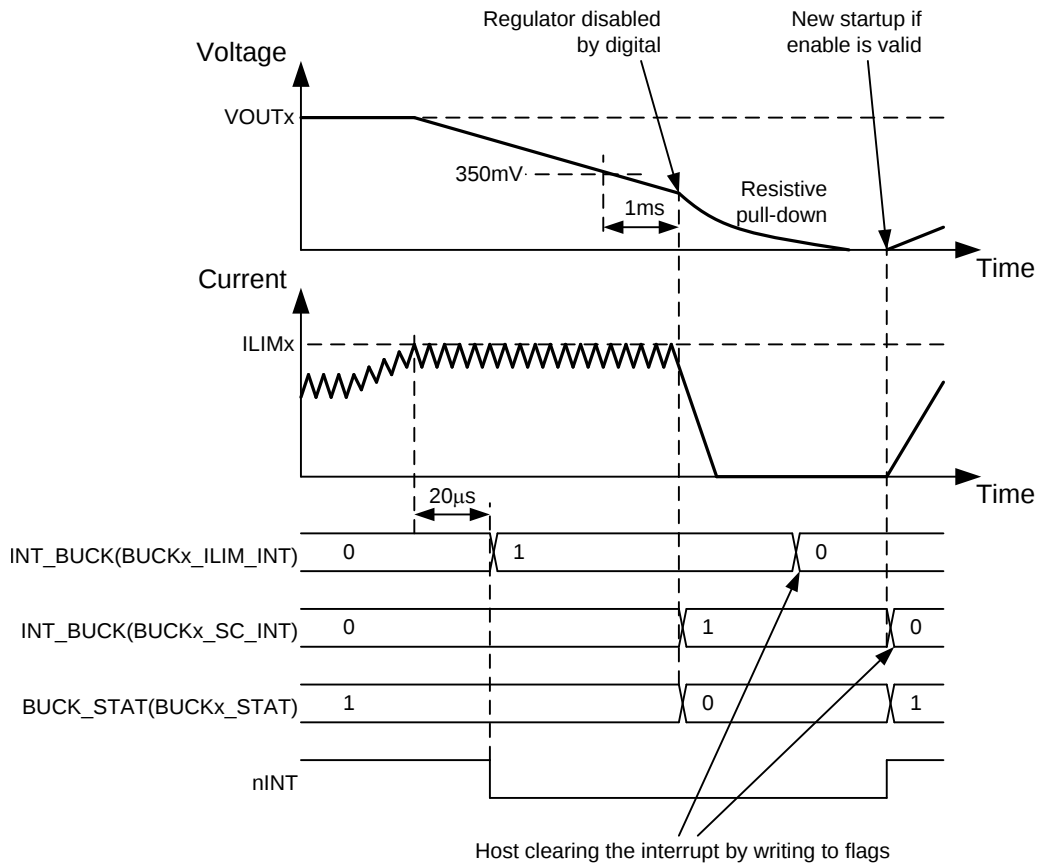


图 15. PGOOD Pin Operation in Continuous Mode

### 8.3.8.2 Warnings for Diagnosis (Interrupt)

#### 8.3.8.2.1 Output Power Limit

The Buck regulators have programmable output peak current limits. The limits are individually programmed for both regulators with BUCKx\_ILIM[2:0] bits in BUCKx\_CTRL\_2 register. If the load current is increased so that the current limit is triggered, the regulator continues to regulate to the limit current level (peak current regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 20  $\mu$ s, the LP87322B/D/E/F-Q1 device sets the BUCKx\_ILIM\_INT bit in INT\_BUCK register and pulls the nINT pin low. The host processor can read BUCKx\_ILIM\_STAT bits in BUCK\_STAT register to see if the regulator is still in peak current regulation mode and the interrupt is cleared by writing 1 to BUCKx\_ILIM\_INT bit. The current limit interrupt can be masked by setting BUCKx\_ILIM\_MASK bit in BUCK\_MASK register to 1. The Buck overload situation is shown in 图 16.



**图 16. Buck Regulator Overload Situation**

The LDO regulators include also current limit circuitry. If the load current is increased so that the current limit is triggered, the regulator limits the output current to the threshold level. The voltage may decrease if the load current is higher than the current limit. If the current regulation continues for 20 μs, the LP87322B/D/E/F-Q1 device sets the LDOx\_ILIM\_INT bit in INT\_LDO register and pulls the nINT pin low. The host processor can read LDOx\_ILIM\_STAT bits in LDO\_STAT register to see if the regulator is still in current regulation mode and the interrupt is cleared by writing 1 to LDOx\_ILIM\_INT bit. The current limit interrupt can be masked by setting LDOx\_ILIM\_MASK bit in LDO\_MASK register to 1. The LDO overload situation is shown in 图 17.

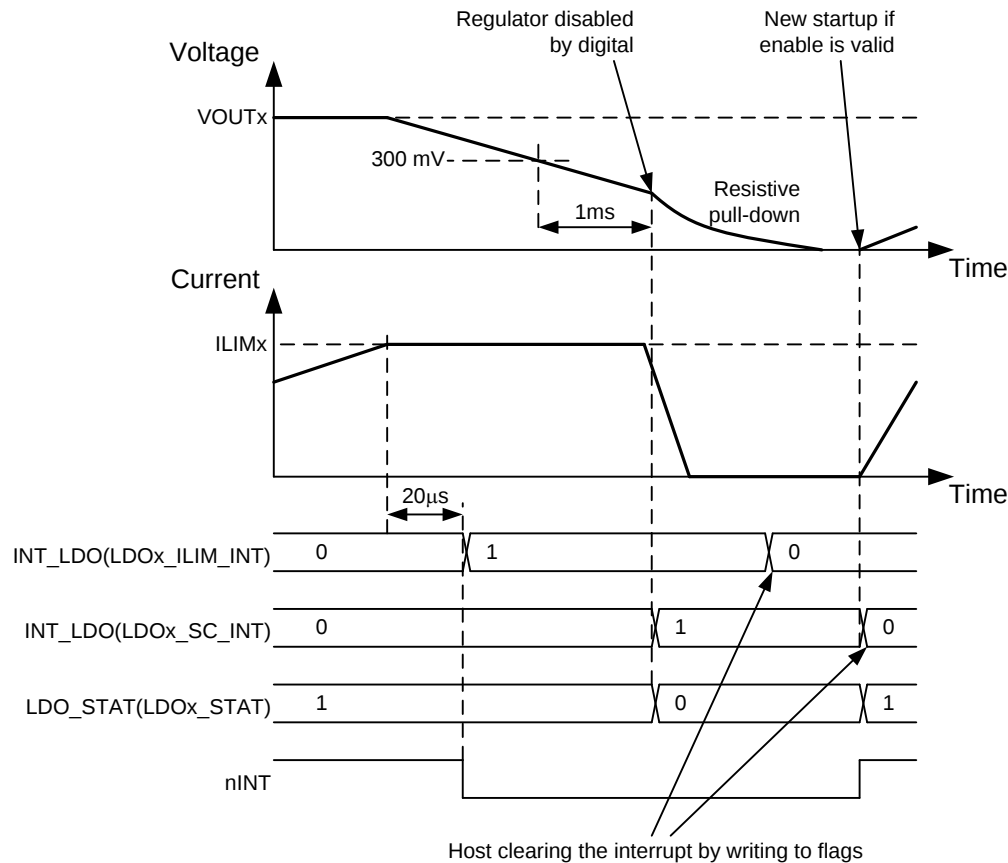


图 17. LDO Regulator Overload Situation

### 8.3.8.2.2 Thermal Warning

The LP87322B/D/E/F-Q1 device includes a protection feature against overtemperature by setting an interrupt for host processor. The threshold level of the thermal warning is selected with TDIE\_WARN\_LEVEL bit in CONFIG register.

If the LP87322B/D/E/F-Q1 device temperature increases above thermal warning level the device sets TDIE\_WARN\_INT bit in INT\_TOP\_1 register and pulls the nINT pin low. The status of the thermal warning can be read from TDIE\_WARN\_STAT bit in TOP\_STAT register, and the interrupt is cleared by writing 1 to TDIE\_WARN\_INT bit. The thermal warning interrupt can be masked by setting TDIE\_WARN\_MASK bit in TOP\_MASK\_1 register to 1.

### 8.3.8.3 Protection (Regulator Disable)

If the regulator is disabled because of protection or fault (short-circuit protection, overload protection, thermal shutdown, input overvoltage protection, or UVLO), the output power FETs are set to high-impedance mode, and the output pulldown resistor is enabled (if enabled with BUCKx\_RDIS\_EN bit in BUCKx\_CTRL\_1 register and LDOx\_RDIS\_EN bit in LDOx\_CTRL register). The turnoff time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pull-down resistor. The pulldown resistors are active as long as VANA voltage is above approximately a 1.2-V level.

#### 8.3.8.3.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP87322B/D/E/F-Q1 to protect itself and external components against short circuit at the output or against overload during start-up. For buck and LDO regulators the fault thresholds are about 350 mV (buck) and 300 mV (LDO), and the protection is triggered and the regulator is disabled if the output voltage is below the threshold level 1 ms after the regulator is enabled.

In a similar way the overload situation is protected during normal operation. If the output voltage falls below 0.35 V and 0.3 V and remains below the threshold level for 1 ms the regulator is disabled.

In buck regulator short-circuit and overload situations the BUCKx\_SC\_INT bit in INT\_BUCK register and the INT\_BUCKx bit in INT\_TOP\_1 register are set to 1, the BUCKx\_STAT bit in BUCK\_STAT register is set to 0, and the nINT signal is pulled low. In LDO regulator short-circuit and overload situations the LDOx\_SC\_INT bit in INT\_LDO register and the INT\_LDOx bit in INT\_TOP\_1 register are set to 1, the LDOx\_STAT bit in LDO\_STAT register is set to 0, and the nINT signal is pulled low. The host processor clears the interrupt by writing 1 to the BUCKx\_SC\_INT or to the LDOx\_SC\_INT bit. Upon clearing the interrupt the regulator makes a new start-up attempt if the regulator is in an enabled state.

### 8.3.8.3.2 Overvoltage Protection

The LP87322B/D/E/F-Q1 device monitors the input voltage from the VANA pin in standby and active operation modes. If the input voltage rises above  $V_{ANA_{OVP}}$  voltage level, all the regulators are disabled immediately (without switching ramp, no shutdown delays), pulldown resistors discharge the output voltages if they are enabled (BUCKx\_RDIS\_EN = 1 in BUCKx\_CTRL\_1 register and LDOx\_RDIS\_EN = 1 in LDOx\_CTRL register), GPOs are set to logic low level, nINT signal is pulled low, OVP\_INT bit in INT\_TOP\_1 register is set to 1, and BUCKx\_STAT bit in BUCK\_STAT register and LDOx\_STAT bit in LDO\_STAT register are set to 0. The host processor clears the interrupt by writing 1 to the OVP\_INT bit. If the input voltage is above overvoltage detection level the interrupt is not cleared. The host can read the status of the overvoltage from the OVP\_STAT bit in TOP\_STAT register. Regulators cannot be enabled as long as the input voltage is above overvoltage detection level or the overvoltage interrupt is pending.

### 8.3.8.3.3 Thermal Shutdown

The LP87322B/D/E/F-Q1 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the regulators are disabled immediately (without switching ramp, no shutdown delays), the TDIE\_SD\_INT bit in INT\_TOP\_1 register is set to 1, the nINT signal is pulled low, and the device enters STANDBY. nINT is cleared by writing 1 to the TDIE\_SD\_INT bit. If the temperature is above thermal shutdown level the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE\_SD\_STAT bit in TOP\_STAT register. Regulators cannot be enabled as long as the junction temperature is above thermal shutdown level or the thermal shutdown interrupt is pending.

### 8.3.8.4 Fault (Power Down)

#### 8.3.8.4.1 Undervoltage Lockout

When the input voltage falls below  $V_{ANA_{UVLO}}$  at the VANA pin, the buck and LDO regulators are disabled immediately (without switching ramp, no shutdown delays), and the output capacitor is discharged using the pulldown resistor, and the LP87322B/D/E/F-Q1 device enters SHUTDOWN. When  $V_{(VANA)}$  voltage is above  $V_{ANA_{UVLO}}$  threshold level, the device powers up to STANDBY state.

If the reset interrupt is unmasked by default (OTP bit for RESET\_REG\_MASK is 0 in TOP\_MASK\_2 register) the RESET\_REG\_INT interrupt bit in INT\_TOP\_2 register indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the RESET\_REG\_INT bit. If the host processor reads the RESET\_REG\_INT interrupt bit after detecting an nINT low signal, it knows that the input supply voltage has been below  $V_{ANA_{UVLO}}$  level (or the host has requested reset with SW\_RESET bit in RESET register), and the registers are reset to default values.

### 8.3.9 Operation of the GPO Signals

The LP87322B/D/E/F-Q1 device supports up to 2 general purpose output signals, GPO and GPO2. The GPO2 signal is multiplexed with CLKIN signal. The selection between CLKIN and GPO2 pin function is set with CLKIN\_PIN\_SEL bit in CONFIG register.

The GPO pins are configured with the following bits:

- GPOx\_OD bit in GPO\_CTRL register defines the type of the output, either push-pull with  $V_{(VANA)}$  level or open drain

The logic level of the GPOx pin is set by EN\_GPOx bit in GPO\_CTRL register.

The control of the GPOs can be included to start-up and shutdown sequences. The GPO control for a sequence with EN pin is selected by GPOx\_EN\_PIN\_CTRL bit in GPO\_CTRL register. For start-up and shutdown sequence control see [Enable and Disable Sequences](#).

### 8.3.10 Digital Signal Filtering

The digital signals have a debounce filtering. The signal or supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

**表 5. Digital Signal Filtering**

| EVENT                                  | SIGNAL/SUPPLY                                 | RISING EDGE LENGTH                             | FALLING EDGE LENGTH               |
|----------------------------------------|-----------------------------------------------|------------------------------------------------|-----------------------------------|
| Enable/disable for BUCKx, LDOx or GPOx | EN                                            | 3 $\mu$ s <sup>(1)</sup>                       | 3 $\mu$ s <sup>(1)</sup>          |
| VANA UVLO                              | VANA                                          | 3 $\mu$ s <sup>(1)</sup> (VANA voltage rising) | Immediate (VANA voltage falling)  |
| VANA overvoltage                       | VANA                                          | 1 $\mu$ s (VANA voltage rising)                | 20 $\mu$ s (VANA voltage falling) |
| Thermal warning                        | TDIE_WARN_INT                                 | 20 $\mu$ s                                     | 20 $\mu$ s                        |
| Thermal shutdown                       | TDIE_SD_INT                                   | 20 $\mu$ s                                     | 20 $\mu$ s                        |
| Current limit                          | VOUTx_ILIM                                    | 20 $\mu$ s                                     | 20 $\mu$ s                        |
| Overload                               | FB_B0, FB_B1,<br>VOUT_LDO0, VOUT_LDO1         | 1 ms                                           | N/A                               |
| PGOOD pin and power-good interrupt     | PGOOD / FB_B0, FB_B1,<br>VOUT_LDO0, VOUT_LDO1 | 6 $\mu$ s                                      | 6 $\mu$ s                         |

(1) No glitch filtering, only synchronization.

## 8.4 Device Functional Modes

### 8.4.1 Modes of Operation

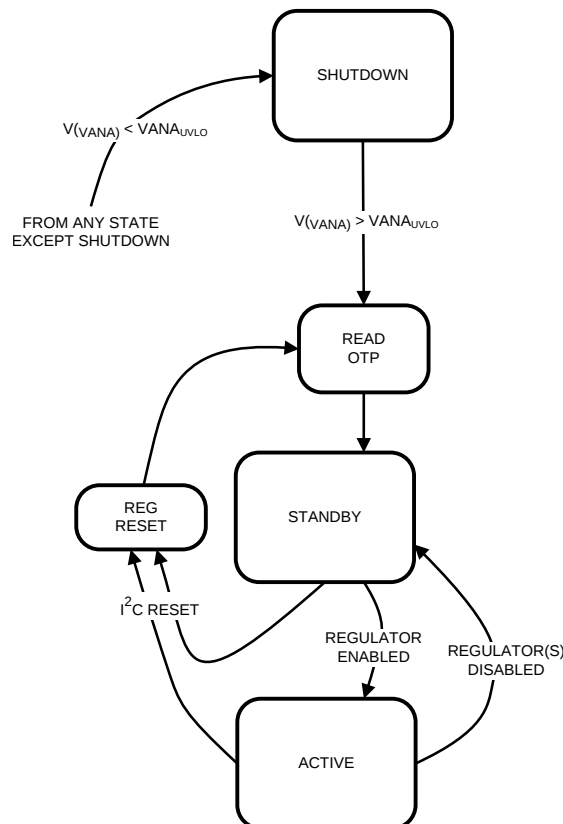
**SHUTDOWN:** The  $V_{(VANA)}$  voltage is below  $VANA_{UVLO}$  threshold level. All switch, reference, control, and bias circuitry of the LP87322B/D/E/F-Q1 device are turned off.

**READ OTP:** The main supply voltage  $V_{(VANA)}$  is above  $VANA_{UVLO}$  level. The regulators are disabled, and the reference and bias circuitry of the LP87322B/D/E/F-Q1 are enabled. The OTP bits are loaded to registers.

**STANDBY:** The main supply voltage  $V_{(VANA)}$  is above  $VANA_{UVLO}$  level. The regulators are disabled, and the reference, control and bias circuitry of the LP87322B/D/E/F-Q1 are enabled. All registers can be read or written by the host processor via the system serial interface. The regulators can be enabled if needed.

**ACTIVE:** The main supply voltage  $V_{(VANA)}$  is above  $VANA_{UVLO}$  level. At least one regulator is enabled. All registers can be read or written by the host processor via the system serial interface.

The operating modes and transitions between the modes are shown in 图 18.



**图 18. Device Operation Modes**

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C-Compatible Interface

The I<sup>2</sup>C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The LP87322B/D/E/F-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

#### 8.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

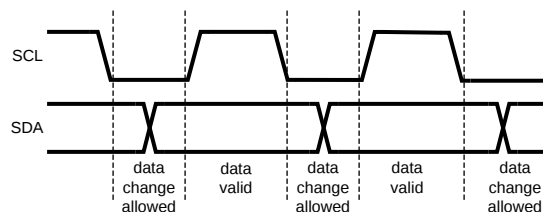


图 19. Data Validity Diagram

#### 8.5.1.2 Start and Stop Conditions

The LP87322B/D/E/F-Q1 is controlled via an I<sup>2</sup>C-compatible interface. START and STOP conditions classify the beginning and end of the I<sup>2</sup>C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates the START and STOP conditions.

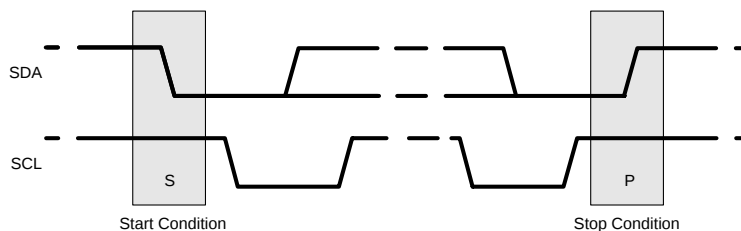


图 20. Start and Stop Sequences

The I<sup>2</sup>C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I<sup>2</sup>C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. 图 21 shows the SDA and SCL signal timing for the I<sup>2</sup>C-compatible bus. See the 图 1 for timing values.

## Programming (接下页)

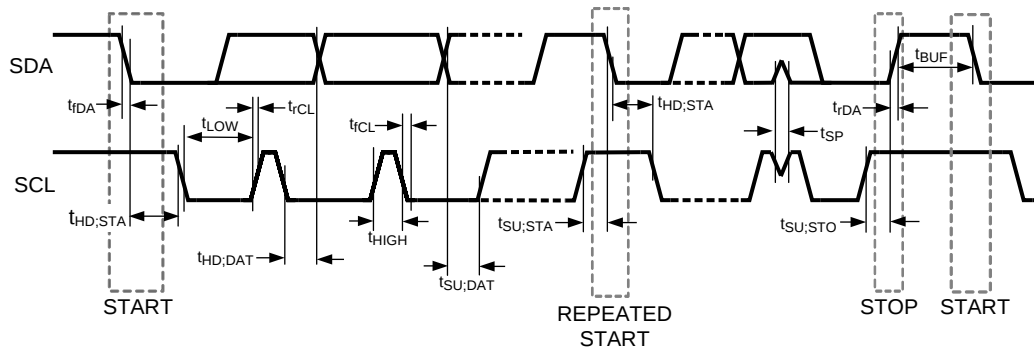


图 21. I²C-Compatible Timing

### 8.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP87322B/D/E/F-Q1 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP87322B/D/E/F-Q1 generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

#### 注

If the  $V_{(VANA)}$  voltage is below  $VANA_{UVLO}$  threshold level during I²C communication the LP87322B/D/E/F-Q1 device does not drive SDA line. The ACK signal and data transfer to the master is disabled at that time.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

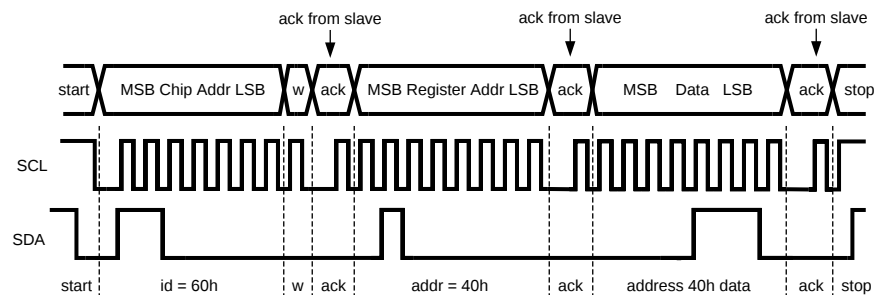
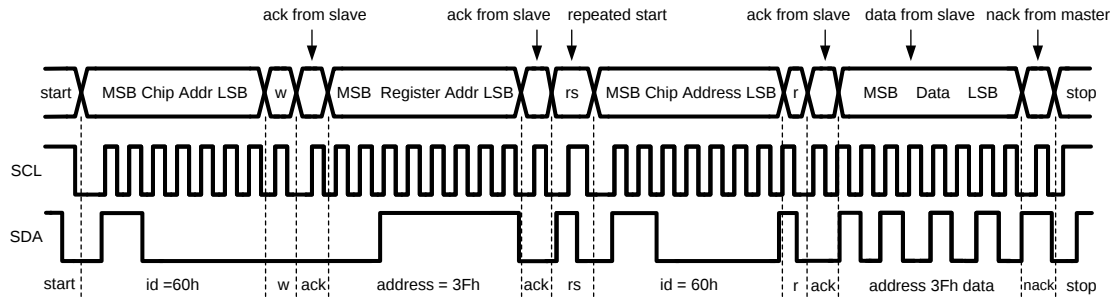


图 22. Write Cycle (w = write; SDA = 0). Example Device Address = 0x60

## Programming (接下页)



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

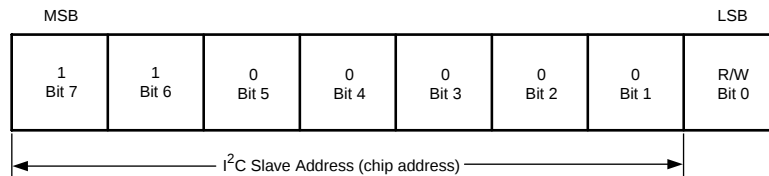
图 23. Read Cycle (r = read; SDA = 1). Example Device Address = 0x60

### 8.5.1.4 I<sup>2</sup>C-Compatible Chip Address

注

The device address for the LP87322B/D/E/F-Q1 is 0x61.

After the START condition, the I<sup>2</sup>C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data is written. The third byte contains the data for the selected register.



Here in an example with device address of 1100000Bin = 60Hex.

图 24. Device Address Example

### 8.5.1.5 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP87322B/D/E/F-Q1, the internal address index counter is incremented by one and the next register is written. 表 6 shows writing sequence to two consecutive registers. Note that auto increment feature does not work for read.

表 6. Auto-Increment Example

| MASTER ACTION      | START | DEVICE ADDRESS S = 0x61 | WRITE |     | REGISTER ADDRESS |     | DATA |     | DATA |     | STOP |
|--------------------|-------|-------------------------|-------|-----|------------------|-----|------|-----|------|-----|------|
| LP87322 B/D/E/F-Q1 |       |                         |       | ACK |                  | ACK |      | ACK |      | ACK |      |

## 8.6 Register Maps

### 8.6.1 Register Descriptions

The LP87322B/D/E/F-Q1 is controlled by a set of registers through the I<sup>2</sup>C-compatible interface. The device registers, their addresses and their abbreviations are listed in 表 7. A more detailed description is given in the [DEV\\_REV](#) to [I\\_LOAD\\_1](#) sections.

The asterisk (\*) marking indicates register bits which are updated from OTP memory during READ OTP state.

#### 注

This register map describes the default values for a device with orderable code of LP87322B/D/E/FRHQR1. For other device versions the default values read from OTP memory can be different.

**表 7. Summary of LP87322B/D/E/F-Q1 Control Registers**

| Addr | Register     | Read / Write | D7                        | D6                | D5                 | D4                | D3                       | D2                   | D1               | D0             |
|------|--------------|--------------|---------------------------|-------------------|--------------------|-------------------|--------------------------|----------------------|------------------|----------------|
| 0x00 | DEV_REV      | R            | DEVICE_ID[1:0]            |                   | Reserved           |                   |                          |                      |                  |                |
| 0x01 | OTP_REV      | R            | OTP_ID[7:0]               |                   |                    |                   |                          |                      |                  |                |
| 0x02 | BUCK0_CTRL_1 | R/W          | Reserved                  |                   |                    |                   | BUCK0_FP_WM              | BUCK0_RDIS_EN        | BUCK0_EN_PIN_CTL | BUCK0_EN       |
| 0x03 | BUCK0_CTRL_2 | R/W          | Reserved                  |                   | BUCK0_ILIM[2:0]    |                   |                          | BUCK0_SLEW_RATE[2:0] |                  |                |
| 0x04 | BUCK1_CTRL_1 | R/W          | Reserved                  |                   |                    |                   | BUCK1_FP_WM              | BUCK1_RDIS_EN        | BUCK1_EN_PIN_CTL | BUCK1_EN       |
| 0x05 | BUCK1_CTRL_2 | R/W          | Reserved                  |                   | BUCK1_ILIM[2:0]    |                   |                          | BUCK1_SLEW_RATE[2:0] |                  |                |
| 0x06 | BUCK0_VOUT   | R/W          | BUCK0_VSET[7:0]           |                   |                    |                   |                          |                      |                  |                |
| 0x07 | BUCK1_VOUT   | R/W          | BUCK1_VSET[7:0]           |                   |                    |                   |                          |                      |                  |                |
| 0x08 | LDO0_CTRL    | R/W          | Reserved                  |                   |                    |                   |                          | LDO0_RDIS_EN         | LDO0_EN_PIN_CTL  | LDO0_EN        |
| 0x09 | LDO1_CTRL    | R/W          | Reserved                  |                   |                    |                   |                          | LDO1_RDIS_EN         | LDO1_EN_PIN_CTL  | LDO1_EN        |
| 0x0A | LDO0_VOUT    | R/W          | Reserved                  |                   |                    | LDO0_VSET[4:0]    |                          |                      |                  |                |
| 0x0B | LDO1_VOUT    | R/W          | Reserved                  |                   |                    | LDO1_VSET[4:0]    |                          |                      |                  |                |
| 0x0C | BUCK0_DELAY  | R/W          | BUCK0_SHUTDOWN_DELAY[3:0] |                   |                    |                   | BUCK0_STARTUP_DELAY[3:0] |                      |                  |                |
| 0x0D | BUCK1_DELAY  | R/W          | BUCK1_SHUTDOWN_DELAY[3:0] |                   |                    |                   | BUCK1_STARTUP_DELAY[3:0] |                      |                  |                |
| 0x0E | LDO0_DELAY   | R/W          | LDO0_SHUTDOWN_DELAY[3:0]  |                   |                    |                   | LDO0_STARTUP_DELAY[3:0]  |                      |                  |                |
| 0x0F | LDO1_DELAY   | R/W          | LDO1_SHUTDOWN_DELAY[3:0]  |                   |                    |                   | LDO1_STARTUP_DELAY[3:0]  |                      |                  |                |
| 0x10 | GPO_DELAY    | R/W          | GPO_SHUTDOWN_DELAY[3:0]   |                   |                    |                   | GPO_STARTUP_DELAY[3:0]   |                      |                  |                |
| 0x11 | GPO2_DELAY   | R/W          | GPO2_SHUTDOWN_DELAY[3:0]  |                   |                    |                   | GPO2_STARTUP_DELAY[3:0]  |                      |                  |                |
| 0x12 | GPO_CTRL     | R/W          | Reserved                  | GPO2_OD           | GPO2_EN_PIN_CTL    | GPO2_EN           | Reserved                 | GPO_OD               | GPO_EN_PIN_CTL   | GPO_EN         |
| 0x13 | CONFIG       | R/W          | Reserved                  | STARTUP_DELAY_SEL | SHUTDOWN_DELAY_SEL | CLKIN_PIN_SEL     | CLKIN_PD                 | EN_PD                | TDIE_WARN_LEVEL  | EN_SPREAD_SPEC |
| 0x14 | PLL_CTRL     | R/W          | Reserved                  | EN_PLL            | Reserved           | EXT_CLK_FREQ[4:0] |                          |                      |                  |                |

## Register Maps (接下页)

**表 7. Summary of LP87322B/D/E/F-Q1 Control Registers (接下页)**

| Addr | Register    | Read / Write | D7                     | D6              | D5               | D4                | D3              | D2              | D1                   | D0              |                          |
|------|-------------|--------------|------------------------|-----------------|------------------|-------------------|-----------------|-----------------|----------------------|-----------------|--------------------------|
| 0x15 | PGOOD_CTL_1 | R/W          | PGOOD_POL              | PGOOD_OD        | PGOOD_WINDOW_LDO | PGOOD_WINDOW_BUCK | EN_PGOOD_LDO1   | EN_PGOOD_LDO0   | EN_PGOOD_BUCK1       | EN_PGOOD_BUCK0  |                          |
| 0x16 | PGOOD_CTL_2 | R/W          | Reserved               |                 |                  |                   |                 | EN_PGOOD_TWARN  | PG_FAULT_GATES_PGOOD | PGOOD_MODE      |                          |
| 0x17 | PG_FAULT    | R            | Reserved               |                 |                  |                   | PG_FAULT_LDO1   | PG_FAULT_LDO0   | PG_FAULT_BUCK1       | PG_FAULT_BUCK0  |                          |
| 0x18 | RESET       | R/W          | Reserved               |                 |                  |                   |                 |                 |                      |                 | SW_RESET                 |
| 0x19 | INT_TOP_1   | R/W          | PGOOD_INT              | INT_LDO         | INT_BUCK         | SYNC_CLK_INT      | TDIE_SD_INT     | TDIE_WARN_INT   | OVP_INT              | I_MEAS_INT      |                          |
| 0x1A | INT_TOP_2   | R/W          | Reserved               |                 |                  |                   |                 |                 |                      |                 | RESET_REG_INT            |
| 0x1B | INT_BUCK    | R/W          | Reserved               | BUCK1_PG_INT    | BUCK1_SC_INT     | BUCK1_ILIM_INT    | Reserved        | BUCK0_PG_INT    | BUCK0_SC_INT         | BUCK0_ILIM_INT  |                          |
| 0x1C | INT_LDO     | R/W          | Reserved               | LDO1_PG_INT     | LDO1_SC_INT      | LDO1_ILIM_INT     | Reserved        | LDO0_PG_INT     | LDO0_SC_INT          | LDO0_ILIM_INT   |                          |
| 0x1D | TOP_STAT    | R            | PGOOD_STAT             | Reserved        |                  | SYNC_CLK_STAT     | TDIE_SD_STAT    | TDIE_WARN_STAT  | OVP_STAT             | Reserved        |                          |
| 0x1E | BUCK_STAT   | R            | BUCK1_STAT             | BUCK1_PG_STAT   | Reserved         | BUCK1_ILIM_STAT   | BUCK0_STAT      | BUCK0_PG_STAT   | Reserved             | BUCK0_ILIM_STAT |                          |
| 0x1F | LDO_STAT    | R            | LDO1_STAT              | LDO1_PG_STAT    | Reserved         | LDO1_ILIM_STAT    | LDO0_STAT       | LDO0_PG_STAT    | Reserved             | LDO0_ILIM_STAT  |                          |
| 0x20 | TOP_MASK_1  | R/W          | PGOOD_INT_MASK         | Reserved        |                  | SYNC_CLK_MASK     | Reserved        | TDIE_WARN_MASK  | Reserved             | I_MEAS_MASK     |                          |
| 0x21 | TOP_MASK_2  | R/W          | Reserved               |                 |                  |                   |                 |                 |                      |                 | RESET_REG_MASK           |
| 0x22 | BUCK_MASK   | R/W          | BUCK1_PG_F_MASK        | BUCK1_PG_R_MASK | Reserved         | BUCK1_ILIM_MASK   | BUCK0_PG_F_MASK | BUCK0_PG_R_MASK | Reserved             | BUCK0_ILIM_MASK |                          |
| 0x23 | LDO_MASK    | R/W          | LDO1_PGF_MASK          | LDO1_PGR_MASK   | Reserved         | LDO1_ILIM_MASK    | LDO0_PGF_MASK   | LDO0_PGR_MASK   | Reserved             | LDO0_ILIM_MASK  |                          |
| 0x24 | SEL_I_LOAD  | R/W          | Reserved               |                 |                  |                   |                 |                 |                      |                 | LOAD_CURRENT_BUCK_SELECT |
| 0x25 | I_LOAD_2    | R            | Reserved               |                 |                  |                   |                 |                 |                      |                 | BUCK_LOAD_CURRENT[8]     |
| 0x26 | I_LOAD_1    | R            | BUCK_LOAD_CURRENT[7:0] |                 |                  |                   |                 |                 |                      |                 |                          |

### 8.6.1.1 DEV\_REV

Address: 0x00

| D7             | D6             | D5       | D4      | D3                       | D2 | D1 | D0 |
|----------------|----------------|----------|---------|--------------------------|----|----|----|
| DEVICE_ID[1:0] |                | Reserved |         |                          |    |    |    |
| Bits           | Field          | Type     | Default | Description              |    |    |    |
| 7:6            | DEVICE_ID[1:0] | R        | 0x1*    | Device specific ID code. |    |    |    |
| 5:0            | Reserved       | R        | 00 0010 |                          |    |    |    |

### 8.6.1.2 OTP\_REV

Address: 0x01

| D7          | D6          | D5   | D4                               | D3                                            | D2 | D1 | D0 |
|-------------|-------------|------|----------------------------------|-----------------------------------------------|----|----|----|
| OTP_ID[7:0] |             |      |                                  |                                               |    |    |    |
| Bits        | Field       | Type | Default                          | Description                                   |    |    |    |
| 7:0         | OTP_ID[7:0] | R    | 0x2B,<br>0x2D,<br>0x2E,<br>0x2F* | Identification Code of the OTP EPROM Version. |    |    |    |

### 8.6.1.3 BUCK0\_CTRL\_1

Address: 0x02

| D7       | D6                | D5   | D4      | D3                                                                                                                                               | D2            | D1                | D0       |
|----------|-------------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------------|----------|
| Reserved |                   |      |         | BUCK0_FPWM                                                                                                                                       | BUCK0_RDIS_EN | BUCK0_EN_PIN_CTRL | BUCK0_EN |
| Bits     | Field             | Type | Default | Description                                                                                                                                      |               |                   |          |
| 7:4      | Reserved          | R/W  | 0000    |                                                                                                                                                  |               |                   |          |
| 3        | BUCK0_FPWM        | R/W  | 0 *     | Buck0 mode selection:<br>0 - Automatic transitions between PFM and PWM modes (AUTO mode)<br>1 - Forced to PWM operation.                         |               |                   |          |
| 2        | BUCK0_RDIS_EN     | R/W  | 1       | Enable output discharge resistor ( $R_{DIS\_BX}$ ) when Buck0 is disabled:<br>0 - Discharge resistor disabled<br>1 - Discharge resistor enabled. |               |                   |          |
| 1        | BUCK0_EN_PIN_CTRL | R/W  | 1 *     | Enable control for Buck0:<br>0 - only BUCK0_EN bit controls Buck0<br>1 - BUCK0_EN bit AND EN pin control Buck0.                                  |               |                   |          |
| 0        | BUCK0_EN          | R/W  | 1 *     | Enable Buck0 regulator:<br>0 - Buck0 regulator is disabled<br>1 - Buck0 regulator is enabled.                                                    |               |                   |          |

### 8.6.1.4 BUCK0\_CTRL\_2

Address: 0x03

| D7       | D6 | D5              | D4 | D3 | D2                   | D1 | D0 |
|----------|----|-----------------|----|----|----------------------|----|----|
| Reserved |    | BUCK0_ILIM[2:0] |    |    | BUCK0_SLEW_RATE[2:0] |    |    |

| Bits | Field                | Type | Default | Description                                                                                                                                                                                                                              |
|------|----------------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | Reserved             | R/W  | 00      |                                                                                                                                                                                                                                          |
| 5:3  | BUCK0_ILIM[2:0]      | R/W  | 0x3*    | Sets the switch current limit of Buck0. Can be programmed at any time during operation:<br>0x0 - 1.5 A<br>0x1 - 2.0 A<br>0x2 - 2.5 A<br>0x3 - 3.0 A<br>0x4 - Reserved<br>0x5 - Reserved<br>0x6 - Reserved<br>0x7 - Reserved              |
| 2:0  | BUCK0_SLEW_RATE[2:0] | R/W  | 0x2*    | Sets the output voltage slew rate for Buck0 regulator (rising and falling edges):<br>0x0 - Reserved<br>0x1 - Reserved<br>0x2 - 10 mV/μs<br>0x3 - 7.5 mV/μs<br>0x4 - 3.8 mV/μs<br>0x5 - 1.9 mV/μs<br>0x6 - 0.94 mV/μs<br>0x7 - 0.47 mV/μs |

### 8.6.1.5 BUCK1\_CTRL\_1

Address: 0x04

| D7       | D6 | D5 | D4 | D3         | D2            | D1                | D0       |
|----------|----|----|----|------------|---------------|-------------------|----------|
| Reserved |    |    |    | BUCK1_FPWM | BUCK1_RDIS_EN | BUCK1_EN_PIN_CTRL | BUCK1_EN |

| Bits | Field             | Type | Default | Description                                                                                                                                           |
|------|-------------------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | Reserved          | R/W  | 0000    |                                                                                                                                                       |
| 3    | BUCK1_FPWM        | R/W  | 0 *     | Buck1 mode selection:<br>0 - Automatic transitions between PFM and PWM modes (AUTO mode)<br>1 - Forced to PWM operation.                              |
| 2    | BUCK1_RDIS_EN     | R/W  | 1       | Enable output discharge resistor (R <sub>DIS_Bx</sub> ) when Buck1 is disabled:<br>0 - Discharge resistor disabled<br>1 - Discharge resistor enabled. |
| 1    | BUCK1_EN_PIN_CTRL | R/W  | 1 *     | Enable control for Buck1:<br>0 - only BUCK1_EN bit controls Buck1<br>1 - BUCK1_EN bit AND EN pin control Buck1.                                       |
| 0    | BUCK1_EN          | R/W  | 1 *     | Enable Buck1 regulator:<br>0 - Buck1 regulator is disabled<br>1 - Buck1 regulator is enabled.                                                         |

### 8.6.1.6 BUCK1\_CTRL\_2

Address: 0x05

| D7       | D6 | D5              | D4 | D3 | D2                   | D1 | D0 |
|----------|----|-----------------|----|----|----------------------|----|----|
| Reserved |    | BUCK1_ILIM[2:0] |    |    | BUCK1_SLEW_RATE[2:0] |    |    |

| Bits | Field                | Type | Default | Description                                                                                                                                                                                                                              |
|------|----------------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | Reserved             | R/W  | 00      |                                                                                                                                                                                                                                          |
| 5:3  | BUCK1_ILIM[2:0]      | R/W  | 0x3*    | Sets the switch current limit of Buck1. Can be programmed at any time during operation:<br>0x0 - 1.5 A<br>0x1 - 2.0 A<br>0x2 - 2.5 A<br>0x3 - 3.0 A<br>0x4 - Reserved<br>0x5 - Reserved<br>0x6 - Reserved<br>0x7 - Reserved              |
| 2:0  | BUCK1_SLEW_RATE[2:0] | R/W  | 0x3*    | Sets the output voltage slew rate for Buck1 regulator (rising and falling edges):<br>0x0 - Reserved<br>0x1 - Reserved<br>0x2 - 10 mV/μs<br>0x3 - 7.5 mV/μs<br>0x4 - 3.8 mV/μs<br>0x5 - 1.9 mV/μs<br>0x6 - 0.94 mV/μs<br>0x7 - 0.47 mV/μs |

### 8.6.1.7 BUCK0\_VOUT

Address: 0x06

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| D7              | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| BUCK0_VSET[7:0] |    |    |    |    |    |    |    |

| Bits | Field           | Type | Default | Description                                                                                                                                                                                                                                                                                                                          |
|------|-----------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | BUCK0_VSET[7:0] | R/W  | 0xB1*   | Sets the output voltage of Buck0 regulator<br><b>Reserved, DO NOT USE</b><br>0x00 ... 0x13<br><b>0.7 V - 0.73 V, 10 mV steps</b><br>0x14 - 0.7V<br>...<br>0x17 - 0.73 V<br><b>0.73 V - 1.4 V, 5 mV steps</b><br>0x18 - 0.735 V<br>...<br>0x9D - 1.4 V<br><b>1.4 V - 3.36 V, 20 mV steps</b><br>0x9E - 1.42 V<br>...<br>0xFF - 3.36 V |

### 8.6.1.8 BUCK1\_VOUT

Address: 0x07

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| D7              | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| BUCK1_VSET[7:0] |    |    |    |    |    |    |    |

| Bits | Field           | Type | Default                                                                   | Description                                                                                                                                                                                                                                                                                                                          |
|------|-----------------|------|---------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | BUCK1_VSET[7:0] | R/W  | LP87322B: 0x75,<br>LP87322D : 0xB1,<br>LP87322E: 0x93,<br>LP87322F: 0xA2* | Sets the output voltage of Buck0 regulator<br><b>Reserved, DO NOT USE</b><br>0x00 ... 0x13<br><b>0.7 V - 0.73 V, 10 mV steps</b><br>0x14 - 0.7V<br>...<br>0x17 - 0.73 V<br><b>0.73 V - 1.4 V, 5 mV steps</b><br>0x18 - 0.735 V<br>...<br>0x9D - 1.4 V<br><b>1.4 V - 3.36 V, 20 mV steps</b><br>0x9E - 1.42 V<br>...<br>0xFF - 3.36 V |

### 8.6.1.9 LDO0\_CTRL

Address: 0x08

| D7       | D6 | D5 | D4 | D3 | D2           | D1               | D0      |
|----------|----|----|----|----|--------------|------------------|---------|
| Reserved |    |    |    |    | LDO0_RDIS_EN | LDO0_EN_PIN_CTRL | LDO0_EN |

| Bits | Field            | Type | Default | Description                                                                                                                                            |
|------|------------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3  | Reserved         | R/W  | 0 0000  |                                                                                                                                                        |
| 2    | LDO0_RDIS_EN     | R/W  | 1       | Enable output discharge resistor (R <sub>DIS_LDOx</sub> ) when LDO0 is disabled:<br>0 - Discharge resistor disabled<br>1 - Discharge resistor enabled. |
| 1    | LDO0_EN_PIN_CTRL | R/W  | 0 *     | Enable control for LDO0:<br>0 - only LDO0_EN bit controls LDO0<br>1 - LDO0_EN bit AND EN pin control LDO0.                                             |
| 0    | LDO0_EN          | R/W  | 0 *     | Enable LDO0 regulator:<br>0 - LDO0 regulator is disabled<br>1 - LDO0 regulator is enabled.                                                             |

### 8.6.1.10 LDO1\_CTRL

Address: 0x09

| D7       | D6 | D5 | D4 | D3 | D2           | D1               | D0      |
|----------|----|----|----|----|--------------|------------------|---------|
| Reserved |    |    |    |    | LDO1_RDIS_EN | LDO1_EN_PIN_CTRL | LDO1_EN |

| Bits | Field            | Type | Default | Description                                                                                                                                            |
|------|------------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3  | Reserved         | R/W  | 0 0000  |                                                                                                                                                        |
| 2    | LDO1_RDIS_EN     | R/W  | 1       | Enable output discharge resistor (R <sub>DIS_LDOx</sub> ) when LDO1 is disabled:<br>0 - Discharge resistor disabled<br>1 - Discharge resistor enabled. |
| 1    | LDO1_EN_PIN_CTRL | R/W  | 0 *     | Enable control for LDO1:<br>0 - only LDO1_EN bit controls LDO1<br>1 - LDO1_EN bit AND EN pin control LDO1.                                             |
| 0    | LDO1_EN          | R/W  | 0 *     | Enable LDO1 regulator:<br>0 - LDO1 regulator is disabled<br>1 - LDO1 regulator is enabled.                                                             |

### 8.6.1.11 LDO0\_VOUT

Address: 0x0A

| D7       | D6 | D5 | D4             | D3 | D2 | D1 | D0 |
|----------|----|----|----------------|----|----|----|----|
| Reserved |    |    | LDO0_VSET[4:0] |    |    |    |    |

| Bits | Field          | Type | Default | Description                                                                                                                                                           |
|------|----------------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5  | Reserved       | R/W  | 000     |                                                                                                                                                                       |
| 4:0  | LDO0_VSET[4:0] | R/W  | 0x02*   | Sets the output voltage of LDO0 regulator<br><b>0.8 V - 3.3 V, 100 mV steps</b><br>0x00 - 0.8V<br>...<br>0x19 - 3.3 V<br><b>Reserved, DO NOT USE</b><br>0x1A ... 0x1F |

### 8.6.1.12 LDO1\_VOUT

Address: 0x0B

| D7       | D6 | D5 | D4             | D3 | D2 | D1 | D0 |
|----------|----|----|----------------|----|----|----|----|
| Reserved |    |    | LDO1_VSET[4:0] |    |    |    |    |

| Bits | Field          | Type | Default | Description                                                                                                                                                           |
|------|----------------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5  | Reserved       | R/W  | 000     |                                                                                                                                                                       |
| 4:0  | LDO1_VSET[4:0] | R/W  | 0x0A*   | Sets the output voltage of LDO1 regulator<br><b>0.8 V - 3.3 V, 100 mV steps</b><br>0x00 - 0.8V<br>...<br>0x19 - 3.3 V<br><b>Reserved, DO NOT USE</b><br>0x1A ... 0x1F |

### 8.6.1.13 BUCK0\_DELAY

Address: 0x0C

| D7                        | D6 | D5 | D4 | D3                       | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| BUCK0_SHUTDOWN_DELAY[3:0] |    |    |    | BUCK0_STARTUP_DELAY[3:0] |    |    |    |

| Bits | Field                     | Type | Default | Description                                                                                                                                                                                                       |
|------|---------------------------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | BUCK0_SHUTDOWN_DELAY[3:0] | R/W  | 0x3*    | Shutdown delay of Buck0 from falling edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) |
| 3:0  | BUCK0_STARTUP_DELAY[3:0]  | R/W  | 0x0*    | Startup delay of Buck0 from rising edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)     |

### 8.6.1.14 BUCK1\_DELAY

Address: 0x0D

| D7                        | D6 | D5 | D4 | D3                       | D2 | D1 | D0 |
|---------------------------|----|----|----|--------------------------|----|----|----|
| BUCK1_SHUTDOWN_DELAY[3:0] |    |    |    | BUCK1_STARTUP_DELAY[3:0] |    |    |    |

| Bits | Field                     | Type | Default | Description                                                                                                                                                                                                       |
|------|---------------------------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | BUCK1_SHUTDOWN_DELAY[3:0] | R/W  | 0x2*    | Shutdown delay of Buck1 from falling edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) |
| 3:0  | BUCK1_STARTUP_DELAY[3:0]  | R/W  | 0x2*    | Startup delay of Buck1 from rising edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)     |

#### 8.6.1.15 LDO0\_DELAY

Address: 0x0E

| D7                       | D6 | D5 | D4 | D3                      | D2 | D1 | D0 |
|--------------------------|----|----|----|-------------------------|----|----|----|
| LDO0_SHUTDOWN_DELAY[3:0] |    |    |    | LDO0_STARTUP_DELAY[3:0] |    |    |    |

| Bits | Field                    | Type | Default | Description                                                                                                                                                                                                      |
|------|--------------------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | LDO0_SHUTDOWN_DELAY[3:0] | R/W  | 0x0*    | Shutdown delay of LDO0 from falling edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) |
| 3:0  | LDO0_STARTUP_DELAY[3:0]  | R/W  | 0x0*    | Startup delay of LDO0 from rising edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)     |

#### 8.6.1.16 LDO1\_DELAY

Address: 0x0F

| D7                       | D6 | D5 | D4 | D3                      | D2 | D1 | D0 |
|--------------------------|----|----|----|-------------------------|----|----|----|
| LDO1_SHUTDOWN_DELAY[3:0] |    |    |    | LDO1_STARTUP_DELAY[3:0] |    |    |    |

| Bits | Field                    | Type | Default | Description                                                                                                                                                                                                      |
|------|--------------------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | LDO1_SHUTDOWN_DELAY[3:0] | R/W  | 0x0*    | Shutdown delay of LDO1 from falling edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) |
| 3:0  | LDO1_STARTUP_DELAY[3:0]  | R/W  | 0x0*    | Startup delay of LDO1 from rising edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)     |

#### 8.6.1.17 GPO\_DELAY

Address: 0x10

| D7                      | D6 | D5 | D4 | D3                     | D2 | D1 | D0 |
|-------------------------|----|----|----|------------------------|----|----|----|
| GPO_SHUTDOWN_DELAY[3:0] |    |    |    | GPO_STARTUP_DELAY[3:0] |    |    |    |

| Bits | Field                   | Type | Default | Description                                                                                                                                                                                                          |
|------|-------------------------|------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | GPO_SHUTDOWN_DELAY[3:0] | R/W  | 0x0*    | Delay for GPO falling edge from falling edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) |

| Bits | Field                  | Type | Default | Description                                                                                                                                                                                                      |
|------|------------------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0  | GPO_STARTUP_DELAY[3:0] | R/W  | 0x7*    | Delay for GPO rising edge from rising edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register) |

### 8.6.1.18 GPO2\_DELAY

Address: 0x11

| D7                       | D6 | D5 | D4 | D3                      | D2 | D1 | D0 |
|--------------------------|----|----|----|-------------------------|----|----|----|
| GPO2_SHUTDOWN_DELAY[3:0] |    |    |    | GPO2_STARTUP_DELAY[3:0] |    |    |    |

| Bits | Field                    | Type | Default | Description                                                                                                                                                                                                           |
|------|--------------------------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | GPO2_SHUTDOWN_DELAY[3:0] | R/W  | 0x2*    | Delay for GPO2 falling edge from falling edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) |
| 3:0  | GPO2_STARTUP_DELAY[3:0]  | R/W  | 0x2*    | Delay for GPO2 rising edge from rising edge of EN signal:<br>0x0 - 0 ms<br>0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register)<br>...<br>0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)     |

### 8.6.1.19 GPO\_CTRL

Address: 0x12

| D7       | D6      | D5               | D4      | D3       | D2     | D1              | D0     |
|----------|---------|------------------|---------|----------|--------|-----------------|--------|
| Reserved | GPO2_OD | GPO2_EN_PIN_CTRL | GPO2_EN | Reserved | GPO_OD | GPO_EN_PIN_CTRL | GPO_EN |

| Bits | Field            | Type | Default | Description                                                                                                                           |
|------|------------------|------|---------|---------------------------------------------------------------------------------------------------------------------------------------|
| 7    | Reserved         | R    | 0       |                                                                                                                                       |
| 6    | GP02_OD          | R/W  | 1 *     | GPO2 signal type when configured as General Purpose Output (CLKIN pin):<br>0 - Push-pull output (VANA level)<br>1 - Open-drain output |
| 5    | GPO2_EN_PIN_CTRL | R/W  | 1 *     | Control for GPO2:<br>0 - Only GPO2_EN bit controls GPO2<br>1 - GPO2_EN bit AND EN pin control GPO2.                                   |
| 4    | GPO2_EN          | R/W  | 1 *     | Output level of GPO2 signal (when configured as General Purpose Output):<br>0 - Logic low level<br>1 - Logic high level               |
| 3    | Reserved         | R    | 0       |                                                                                                                                       |
| 2    | GPO_OD           | R/W  | 1 *     | GPO signal type:<br>0 - Push-pull output (VANA level)<br>1 - Open-drain output                                                        |
| 1    | GPO_EN_PIN_CTRL  | R/W  | 1 *     | Control for GPO:<br>0 - Only GPO_EN bit controls GPO<br>1 - GPO_EN bit AND EN pin control GPO.                                        |
| 0    | GPO_EN           | R/W  | 1 *     | Output level of GPO signal:<br>0 - Logic low level<br>1 - Logic high level                                                            |

### 8.6.1.20 CONFIG

Address: 0x13

| D7       | D6                | D5                 | D4            | D3       | D2     | D1              | D0             |
|----------|-------------------|--------------------|---------------|----------|--------|-----------------|----------------|
| Reserved | STARTUP_DELAY_SEL | SHUTDOWN_DELAY_SEL | CLKIN_PIN_SEL | CLKIN_PD | EN2_PD | TDIE_WARN_LEVEL | EN_SPREAD_SPEC |

| Bits | Field              | Type | Default | Description                                                                                                                                                            |
|------|--------------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | Reserved           | R/W  | 0       |                                                                                                                                                                        |
| 6    | STARTUP_DELAY_SEL  | R/W  | 0 *     | Startup delay range from EN signals.<br>0 - 0 ms - 7.5 ms with 0.5 ms steps<br>1 - 0 ms - 15 ms with 1 ms steps                                                        |
| 5    | SHUTDOWN_DELAY_SEL | R/W  | 0 *     | Shutdown delay range from EN signals.<br>0 - 0 ms - 7.5 ms with 0.5 ms steps<br>1 - 0 ms - 15 ms with 1 ms steps                                                       |
| 4    | CLKIN_PIN_SEL      | R/W  | 0 *     | CLKIN pin function:<br>0 - GPO2<br>1 - CLKIN                                                                                                                           |
| 3    | CLKIN_PD           | R/W  | 0 *     | Selects the pull down resistor on the CLKIN input pin. (valid also when selected as GPO2)<br>0 - Pull-down resistor is disabled.<br>1 - Pull-down resistor is enabled. |
| 2    | EN_PD              | R/W  | 1 *     | Selects the pull down resistor on the EN input pin.<br>0 - Pull-down resistor is disabled.<br>1 - Pull-down resistor is enabled.                                       |
| 1    | TDIE_WARN_LEVEL    | R/W  | 1 *     | Thermal warning threshold level.<br>0 - 125°C<br>1 - 137°C.                                                                                                            |
| 0    | EN_SPREAD_SPEC     | R/W  | 0 *     | Enable spread spectrum feature:<br>0 - Disabled<br>1 - Enabled                                                                                                         |

### 8.6.1.21 PLL\_CTRL

Address: 0x14

| D7       | D6     | D5       | D4                | D3 | D2 | D1 | D0 |
|----------|--------|----------|-------------------|----|----|----|----|
| Reserved | EN_PLL | Reserved | EXT_CLK_FREQ[4:0] |    |    |    |    |

| Bits | Field             | Type | Default | Description                                                                                                                                                                                                                                                        |
|------|-------------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | Reserved          | R/W  | 0       |                                                                                                                                                                                                                                                                    |
| 6    | EN_PLL            | R/W  | 0 *     | Selection of external clock and PLL operation:<br>0 - Forced to internal RC oscillator. PLL disabled.<br>1 - PLL is enabled in STANDBY and ACTIVE modes. Automatic external clock use when available, interrupt generated if external clock appears or disappears. |
| 5    | Reserved          | R/W  | 0       | <b>This bit must be set to '0'.</b>                                                                                                                                                                                                                                |
| 4:0  | EXT_CLK_FREQ[4:0] | R/W  | 0x01*   | Frequency of the external clock (CLKIN):<br>0x00 - 1 MHz<br>0x01 - 2 MHz<br>0x02 - 3 MHz<br>...<br>0x16 - 23 MHz<br>0x17 - 24 MHz<br>0x18...0x1F - Reserved<br>See electrical specification for input clock frequency tolerance.                                   |

### 8.6.1.22 PGOOD\_CTRL\_1

Address: 0x15

| D7        | D6       | D5               | D4                | D3            | D2            | D1             | D0             |
|-----------|----------|------------------|-------------------|---------------|---------------|----------------|----------------|
| PGOOD_POL | PGOOD_OD | PGOOD_WINDOW_LDO | PGOOD_WINDOW_BUCK | EN_PGOOD_LDO1 | EN_PGOOD_LDO0 | EN_PGOOD_BUCK1 | EN_PGOOD_BUCK0 |

| Bits | Field             | Type | Default | Description                                                                                                                                 |
|------|-------------------|------|---------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | PGOOD_POL         | R/W  | 0 *     | PGOOD signal polarity.<br>0 - PGOOD signal high when monitored outputs are valid<br>1 - PGOOD signal low when monitored outputs are valid   |
| 6    | PGOOD_OD          | R/W  | 1 *     | PGOOD signal type:<br>0 - Push-pull output (VANA level)<br>1 - Open-drain output                                                            |
| 5    | PGOOD_WINDOW_LDO  | R/W  | 1 *     | LDO Output voltage monitoring method for PGOOD signal:<br>0 - Only undervoltage monitoring<br>1 - Overvoltage and undervoltage monitoring.  |
| 4    | PGOOD_WINDOW_BUCK | R/W  | 1 *     | Buck Output voltage monitoring method for PGOOD signal:<br>0 - Only undervoltage monitoring<br>1 - Overvoltage and undervoltage monitoring. |
| 3    | EN_PGOOD_LDO1     | R/W  | 0 *     | PGOOD signal source control from LDO1<br>0 - LDO1 is not monitored<br>1 - LDO1 Power-Good threshold voltage monitored                       |
| 2    | EN_PGOOD_LDO0     | R/W  | 0 *     | PGOOD signal source control from LDO0<br>0 - LDO0 is not monitored<br>1 - LDO0 Power-Good threshold voltage monitored                       |
| 1    | EN_PGOOD_BUCK1    | R/W  | 1 *     | PGOOD signal source control from Buck1<br>0 - Buck1 is not monitored<br>1 - Buck1 Power-Good threshold voltage monitored                    |
| 0    | EN_PGOOD_BUCK0    | R/W  | 1 *     | PGOOD signal source control from Buck0<br>0 - Buck0 is not monitored<br>1 - Buck0 Power-Good threshold voltage monitored                    |

### 8.6.1.23 PGOOD\_CTRL\_2

Address: 0x16

| D7       | D6 | D5 | D4 | D3 | D2             | D1                   | D0         |
|----------|----|----|----|----|----------------|----------------------|------------|
| Reserved |    |    |    |    | EN_PGOOD_TWARN | PG_FAULT_GATES_PGOOD | PGOOD_MODE |

| Bits | Field                 | Type | Default | Description                                                                                                                                                                                         |
|------|-----------------------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3  | Reserved              | R/W  | 0 0000  |                                                                                                                                                                                                     |
| 2    | EN_PGOOD_TWARN        | R/W  | 1 *     | Thermal warning control for PGOOD signal:<br>0 - Thermal warning not monitored<br>1 - PGOOD inactive if thermal warning flag is active.                                                             |
| 1    | PG_FAULT_GATE_S_PGOOD | R/W  | 0 *     | Type of operation for PGOOD signal:<br>0 - Indicates live status of monitored voltage outputs.<br>1 - Indicates status of PG_FAULT register, inactive when at least one PG_FAULT_x bit is inactive. |
| 0    | PGOOD_MODE            | R/W  | 0 *     | Operating mode for PGOOD signal:<br>0 - Gated mode<br>1 - Continuous mode                                                                                                                           |

### 8.6.1.24 PG\_FAULT

Address: 0x17

| D7       | D6 | D5 | D4 | D3            | D2            | D1             | D0             |
|----------|----|----|----|---------------|---------------|----------------|----------------|
| Reserved |    |    |    | PG_FAULT_LD01 | PG_FAULT_LD00 | PG_FAULT_BUCK1 | PG_FAULT_BUCK0 |

| Bits | Field              | Type | Default | Description                                                                                                                                                                                                                                      |
|------|--------------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | Reserved           | R/W  | 0000    |                                                                                                                                                                                                                                                  |
| 3    | PG_FAULT_LDO1      | R/W  | 0       | Source for PGOOD inactive signal:<br>0 - LDO1 has not set PGOOD signal inactive.<br>1 - LDO1 is selected for PGOOD signal and it has set PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when LDO1 output is valid.    |
| 2    | PG_FAULT_LDO0      | R/W  | 0       | Source for PGOOD inactive signal:<br>0 - LDO0 has not set PGOOD signal inactive.<br>1 - LDO0 is selected for PGOOD signal and it has set PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when LDO0 output is valid.    |
| 1    | PG_FAULT_BUCK<br>1 | R/W  | 0       | Source for PGOOD inactive signal:<br>0 - Buck1 has not set PGOOD signal inactive.<br>1 - Buck1 is selected for PGOOD signal and it has set PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid. |
| 0    | PG_FAULT_BUCK<br>0 | R/W  | 0       | Source for PGOOD inactive signal:<br>0 - Buck0 has not set PGOOD signal inactive.<br>1 - Buck0 is selected for PGOOD signal and it has set PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid. |

### 8.6.1.25 RESET

Address: 0x18

|          |    |    |    |    |    |    |          |
|----------|----|----|----|----|----|----|----------|
| D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0       |
| Reserved |    |    |    |    |    |    | SW_RESET |

| Bits | Field    | Type | Default  | Description                                                                                                                                                                                    |
|------|----------|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1  | Reserved | R/W  | 000 0000 |                                                                                                                                                                                                |
| 0    | SW_RESET | R/W  | 0        | Software commanded reset. When written to 1, the registers will be reset to default values, OTP memory is read, and the I <sup>2</sup> C interface is reset. The bit is automatically cleared. |

### 8.6.1.26 INT\_TOP\_1

Address: 0x19

|           |         |          |                  |             |                   |         |            |
|-----------|---------|----------|------------------|-------------|-------------------|---------|------------|
| D7        | D6      | D5       | D4               | D3          | D2                | D1      | D0         |
| PGOOD_INT | LDO_INT | BUCK_INT | SYNC_CLK_IN<br>T | TDIE_SD_INT | TDIE_WARN_I<br>NT | OVP_INT | I_MEAS_INT |

| Bits | Field         | Type | Default | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|------|---------------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | PGOOD_INT     | R/W  | 0       | Latched status bit indicating that the PGOOD pin has changed from active to inactive. Write 1 to clear interrupt.                                                                                                                                                                                                                                                                             |
| 6    | LDO_INT       | R    | 0       | Interrupt indicating that LDO1 and/or LDO0 have a pending interrupt. The reason for the interrupt is indicated in INT_LDO register. This bit is cleared automatically when INT_LDO register is cleared to 0x00.                                                                                                                                                                               |
| 5    | BUCK_INT      | R    | 0       | Interrupt indicating that Buck1 and/or Buck0 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.                                                                                                                                                                           |
| 4    | SYNC_CLK_INT  | R/W  | 0       | Latched status bit indicating that the external clock has appeared or disappeared. Write 1 to clear interrupt.                                                                                                                                                                                                                                                                                |
| 3    | TDIE_SD_INT   | R/W  | 0       | Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The regulators have been disabled if they were enabled and GPO and GPO2 signals are driven low. The regulators cannot be enabled if this bit is active. The actual status of the thermal shutdown is indicated by TDIE_SD_STAT bit in TOP_STAT register. Write 1 to clear interrupt. |
| 2    | TDIE_WARN_INT | R/W  | 0       | Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TDIE_WARN_STAT bit in TOP_STAT register. Write 1 to clear interrupt.                                                                                                                                                         |

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| Bits | Field      | Type | Default | Description                                                                                                                                                                                                                                                                                                                 |
|------|------------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | OVP_INT    | R/W  | 0       | Latched status bit indicating that the input voltage has exceeded the over-voltage detection level. The regulators have been disabled if they were enabled and GPO and GPO2 signals are driven low. The actual status of the over-voltage is indicated by OVP_STAT bit in TOP_STAT register.<br>Write 1 to clear interrupt. |
| 0    | I_MEAS_INT | R/W  | 0       | Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers.<br>Write 1 to clear interrupt.                                                                                                                                                                      |

**8.6.1.27 INT\_TOP\_2**

Address: 0x1A

| D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0            |
|----------|----|----|----|----|----|----|---------------|
| Reserved |    |    |    |    |    |    | RESET_REG_INT |

| Bits | Field         | Type | Default  | Description                                                                                                                                                                                                                                                                                                                             |
|------|---------------|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1  | Reserved      | R/W  | 000 0000 |                                                                                                                                                                                                                                                                                                                                         |
| 0    | RESET_REG_INT | R/W  | 0        | Latched status bit indicating that either VANA supply voltage has been below undervoltage threshold level or the host has requested a reset using SW_RESET bit in RESET register. The regulators have been disabled, and registers are reset to default values and the normal startup procedure is done.<br>Write 1 to clear interrupt. |

**8.6.1.28 INT\_BUCK**

Address: 0x1B

| D7       | D6           | D5           | D4             | D3       | D2           | D1           | D0             |
|----------|--------------|--------------|----------------|----------|--------------|--------------|----------------|
| Reserved | BUCK1_PG_INT | BUCK1_SC_INT | BUCK1_ILIM_INT | Reserved | BUCK0_PG_INT | BUCK0_SC_INT | BUCK0_ILIM_INT |

| Bits | Field          | Type | Default | Description                                                                                                                              |
|------|----------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | Reserved       | R/W  | 0       |                                                                                                                                          |
| 6    | BUCK1_PG_INT   | R/W  | 0       | Latched status bit indicating that Buck1 Power-Good event has been detected.<br>Write 1 to clear.                                        |
| 5    | BUCK1_SC_INT   | R/W  | 0       | Latched status bit indicating that the Buck1 output voltage has been over 1 ms below short-circuit threshold level.<br>Write 1 to clear. |
| 4    | BUCK1_ILIM_INT | R/W  | 0       | Latched status bit indicating that the Buck1 output current limit has been active.<br>Write 1 to clear.                                  |
| 3    | Reserved       | R/W  | 0       |                                                                                                                                          |
| 2    | BUCK0_PG_INT   | R/W  | 0       | Latched status bit indicating that Buck0 Power-Good event has been detected.<br>Write 1 to clear.                                        |
| 1    | BUCK0_SC_INT   | R/W  | 0       | Latched status bit indicating that the Buck0 output voltage has been over 1 ms below short-circuit threshold level.<br>Write 1 to clear. |
| 0    | BUCK0_ILIM_INT | R/W  | 0       | Latched status bit indicating that the Buck0 output current limit has been active.<br>Write 1 to clear.                                  |

**8.6.1.29 INT\_LDO**

Address: 0x1C

| D7       | D6          | D5          | D4            | D3       | D2          | D1          | D0            |
|----------|-------------|-------------|---------------|----------|-------------|-------------|---------------|
| Reserved | LDO1_PG_INT | LDO1_SC_INT | LDO1_ILIM_INT | Reserved | LDO0_PG_INT | LDO0_SC_INT | LDO0_ILIM_INT |

| Bits | Field         | Type | Default | Description                                                                                                                          |
|------|---------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7    | Reserved      | R/W  | 0       |                                                                                                                                      |
| 6    | LDO1_PG_INT   | R/W  | 0       | Latched status bit indicating that LDO1 Power-Good event has been detected. Write 1 to clear.                                        |
| 5    | LDO1_SC_INT   | R/W  | 0       | Latched status bit indicating that the LDO1 output voltage has been over 1 ms below short-circuit threshold level. Write 1 to clear. |
| 4    | LDO1_ILIM_INT | R/W  | 0       | Latched status bit indicating that the LDO1 output current limit has been active. Write 1 to clear.                                  |
| 3    | Reserved      | R/W  | 0       |                                                                                                                                      |
| 2    | LDO0_PG_INT   | R/W  | 0       | Latched status bit indicating that LDO0 Power-Good event has been detected. Write 1 to clear.                                        |
| 1    | LDO0_SC_INT   | R/W  | 0       | Latched status bit indicating that the LDO0 output voltage has been over 1 ms below short-circuit threshold level. Write 1 to clear. |
| 0    | LDO0_ILIM_INT | R/W  | 0       | Latched status bit indicating that the LDO0 output current limit has been active. Write 1 to clear.                                  |

### 8.6.1.30 TOP\_STAT

Address: 0x1D

| D7         | D6       | D5 | D4            | D3           | D2             | D1       | D0       |
|------------|----------|----|---------------|--------------|----------------|----------|----------|
| PGOOD_STAT | Reserved |    | SYNC_CLK_STAT | TDIE_SD_STAT | TDIE_WARN_STAT | OVP_STAT | Reserved |

| Bits | Field          | Type | Default | Description                                                                                                                                                                      |
|------|----------------|------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | PGOOD_STAT     | R    | 0       | Status bit indicating the status of PGOOD pin:<br>0 - PGOOD pin is inactive<br>1 - PGOOD pin is active                                                                           |
| 6:5  | Reserved       | R    | 00      |                                                                                                                                                                                  |
| 4    | SYNC_CLK_STAT  | R    | 0       | Status bit indicating the status of external clock (CLKIN):<br>0 - External clock frequency is valid<br>1 - External clock frequency is not valid.                               |
| 3    | TDIE_SD_STAT   | R    | 0       | Status bit indicating the status of thermal shutdown:<br>0 - Die temperature below thermal shutdown level<br>1 - Die temperature above thermal shutdown level.                   |
| 2    | TDIE_WARN_STAT | R    | 0       | Status bit indicating the status of thermal warning:<br>0 - Die temperature below thermal warning level<br>1 - Die temperature above thermal warning level.                      |
| 1    | OVP_STAT       | R    | 0       | Status bit indicating the status of input overvoltage monitoring:<br>0 - Input voltage below overvoltage threshold level<br>1 - Input voltage above overvoltage threshold level. |
| 0    | Reserved       | R    | 0       |                                                                                                                                                                                  |

### 8.6.1.31 BUCK\_STAT

Address: 0x1E

| D7         | D6            | D5       | D4              | D3         | D2            | D1       | D0              |
|------------|---------------|----------|-----------------|------------|---------------|----------|-----------------|
| BUCK1_STAT | BUCK1_PG_STAT | Reserved | BUCK1_ILIM_STAT | BUCK0_STAT | BUCK0_PG_STAT | Reserved | BUCK0_ILIM_STAT |

| Bits | Field         | Type | Default | Description                                                                                                                                    |
|------|---------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | BUCK1_STAT    | R    | 0       | Status bit indicating the enable/disable status of Buck1:<br>0 - Buck1 regulator is disabled<br>1 - Buck1 regulator is enabled.                |
| 6    | BUCK1_PG_STAT | R    | 0       | Status bit indicating Buck1 output voltage validity (raw status)<br>0 - Buck1 output voltage is valid.<br>1 - Buck1 output voltage is invalid. |

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| Bits | Field           | Type | Default | Description                                                                                                                                                         |
|------|-----------------|------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5    | Reserved        | R    | 0       |                                                                                                                                                                     |
| 4    | BUCK1_ILIM_STAT | R    | 0       | Status bit indicating Buck1 current limit status (raw status)<br>0 - Buck1 output current is below current limit level<br>1 - Buck1 output current limit is active. |
| 3    | BUCK0_STAT      | R    | 0       | Status bit indicating the enable/disable status of Buck0:<br>0 - Buck0 regulator is disabled<br>1 - Buck0 regulator is enabled.                                     |
| 2    | BUCK0_PG_STAT   | R    | 0       | Status bit indicating Buck0 output voltage validity (raw status)<br>0 - Buck0 output voltage is valid.<br>1 - Buck0 output voltage is invalid.                      |
| 1    | Reserved        | R    | 0       |                                                                                                                                                                     |
| 0    | BUCK0_ILIM_STAT | R    | 0       | Status bit indicating Buck0 current limit status (raw status)<br>0 - Buck0 output current is below current limit level<br>1 - Buck0 output current limit is active. |

**8.6.1.32 LDO\_STAT**

Address: 0x1F

| D7        | D6           | D5       | D4             | D3        | D2           | D1       | D0             |
|-----------|--------------|----------|----------------|-----------|--------------|----------|----------------|
| LDO1_STAT | LDO1_PG_STAT | Reserved | LDO1_ILIM_STAT | LDO0_STAT | LDO0_PG_STAT | Reserved | LDO0_ILIM_STAT |

| Bits | Field          | Type | Default | Description                                                                                                                                                      |
|------|----------------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | LDO1_STAT      | R    | 0       | Status bit indicating the enable/disable status of LDO1:<br>0 - LDO1 regulator is disabled<br>1 - LDO1 regulator is enabled.                                     |
| 6    | LDO1_PG_STAT   | R    | 0       | Status bit indicating LDO1 output voltage validity (raw status)<br>0 - LDO1 output voltage is valid.<br>1 - LDO1 output voltage is invalid.                      |
| 5    | Reserved       | R    | 0       |                                                                                                                                                                  |
| 4    | LDO1_ILIM_STAT | R    | 0       | Status bit indicating LDO1 current limit status (raw status)<br>0 - LDO1 output current is below current limit level<br>1 - LDO1 output current limit is active. |
| 3    | LDO0_STAT      | R    | 0       | Status bit indicating the enable/disable status of LDO0:<br>0 - LDO0 regulator is disabled<br>1 - LDO0 regulator is enabled.                                     |
| 2    | LDO0_PG_STAT   | R    | 0       | Status bit indicating LDO0 output voltage validity (raw status)<br>0 - LDO0 output voltage is valid.<br>1 - LDO0 output voltage is invalid.                      |
| 1    | Reserved       | R    | 0       |                                                                                                                                                                  |
| 0    | LDO0_ILIM_STAT | R    | 0       | Status bit indicating LDO0 current limit status (raw status)<br>0 - LDO0 output current is below current limit level<br>1 - LDO0 output current limit is active. |

**8.6.1.33 TOP\_MASK\_1**

Address: 0x20

| D7             | D6       | D5 | D4            | D3       | D2             | D1       | D0                |
|----------------|----------|----|---------------|----------|----------------|----------|-------------------|
| PGOOD_INT_MASK | Reserved |    | SYNC_CLK_MASK | Reserved | TDIE_WARN_MASK | Reserved | I_LOAD_READY_MASK |

| Bits | Field          | Type | Default | Description                                                                                                                                                                                            |
|------|----------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | PGOOD_INT_MASK | R/W  | 1 *     | Masking for Power-Good interrupt (PGOOD_INT in INT_TOP_1 register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect PGOOD_STAT status bit in TOP_STAT register. |
| 6:5  | Reserved       | R/W  | 00      |                                                                                                                                                                                                        |

| Bits | Field          | Type | Default | Description                                                                                                                                                                                                                |
|------|----------------|------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4    | SYNC_CLK_MASK  | R/W  | 1 *     | Masking for external clock detection interrupt (SYNC_CLK_INT in INT_TOP_1 register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect SYNC_CLK_STAT status bit in TOP_STAT register. |
| 3    | Reserved       | R/W  | 0       |                                                                                                                                                                                                                            |
| 2    | TDIE_WARN_MASK | R/W  | 0 *     | Masking for thermal warning interrupt (TDIE_WARN_INT in INT_TOP_1 register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect TDIE_WARN_STAT status bit in TOP_STAT register.        |
| 1    | Reserved       | R/W  | 0       |                                                                                                                                                                                                                            |
| 0    | I_MEAS_MASK    | R/W  | 0 *     | Masking for load current measurement ready interrupt (MEAS_INT in INT_TOP_1 register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.                                                                          |

#### 8.6.1.34 TOP\_MASK\_2

Address: 0x21

| D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0             |
|----------|----|----|----|----|----|----|----------------|
| Reserved |    |    |    |    |    |    | RESET_REG_MASK |

| Bits | Field          | Type | Default  | Description                                                                                                                                                                                                                                                       |
|------|----------------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1  | Reserved       | R/W  | 000 0000 |                                                                                                                                                                                                                                                                   |
| 0    | RESET_REG_MASK | R/W  | 1 *      | Masking for register reset interrupt (RESET_REG_INT in INT_TOP_2 register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This change of this bit by I <sup>2</sup> C writing has no effect because it will be read from OTP memory during reset. |

#### 8.6.1.35 BUCK\_MASK

Address: 0x22

| D7             | D6             | D5       | D4              | D3             | D2             | D1       | D0              |
|----------------|----------------|----------|-----------------|----------------|----------------|----------|-----------------|
| BUCK1_PGF_MASK | BUCK1_PGR_MASK | Reserved | BUCK1_ILIM_MASK | BUCK0_PGF_MASK | BUCK0_PGR_MASK | Reserved | BUCK0_ILIM_MASK |

| Bits | Field           | Type | Default | Description                                                                                                                                                                                                                                        |
|------|-----------------|------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | BUCK1_PGF_MASK  | R/W  | 1 *     | Masking of Power Good invalid detection for Buck1 power good interrupt (BUCK1_PG_INT in INT_BUCK register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register. |
| 6    | BUCK1_PGR_MASK  | R/W  | 1 *     | Masking of Power Good valid detection for Buck1 Power Good interrupt (BUCK1_PG_INT in INT_BUCK register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register.   |
| 5    | Reserved        | R    | 0       |                                                                                                                                                                                                                                                    |
| 4    | BUCK1_ILIM_MASK | R/W  | 0 *     | Masking for Buck1 current limit detection interrupt (BUCK1_ILIM_INT in INT_BUCK register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect BUCK1_ILIM_STAT status bit in BUCK_STAT register.                |
| 3    | BUCK0_PGF_MASK  | R/W  | 1 *     | Masking of Power Good invalid detection for Buck0 power good interrupt (BUCK0_PG_INT in INT_BUCK register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register. |

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| Bits | Field           | Type | Default | Description                                                                                                                                                                                                                                      |
|------|-----------------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2    | BUCK0_PGR_MASK  | R/W  | 1 *     | Masking of Power Good valid detection for Buck0 power good interrupt (BUCK0_PG_INT in INT_BUCK register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register. |
| 1    | Reserved        | R    | 0       |                                                                                                                                                                                                                                                  |
| 0    | BUCK0_ILIM_MASK | R/W  | 0 *     | Masking for Buck0 current limit detection interrupt (BUCK0_ILIM_INT in INT_BUCK register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect BUCK0_ILIM_STAT status bit in BUCK_STAT register.              |

**8.6.1.36 LDO\_MASK**

Address: 0x23

| D7            | D6            | D5       | D4             | D3            | D2            | D1       | D0             |
|---------------|---------------|----------|----------------|---------------|---------------|----------|----------------|
| LDO1_PGF_MASK | LDO1_PGR_MASK | Reserved | LDO1_ILIM_MASK | LDO0_PGF_MASK | LDO0_PGR_MASK | Reserved | LDO0_ILIM_MASK |

| Bits | Field          | Type | Default | Description                                                                                                                                                                                                                                   |
|------|----------------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | LDO1_PGF_MASK  | R/W  | 0 *     | Masking of Power Good invalid detection for LDO1 power good interrupt (LDO1_PG_INT in INT_LDO register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect LDO1_PG_STAT status bit in LDO_STAT register. |
| 6    | LDO1_PGR_MASK  | R/W  | 0 *     | Masking of Power Good valid detection for LDO1 power good interrupt (LDO1_PG_INT in INT_LDO register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect LDO1_PG_STAT status bit in LDO_STAT register.   |
| 5    | Reserved       | R    | 0       |                                                                                                                                                                                                                                               |
| 4    | LDO1_ILIM_MASK | R/W  | 0 *     | Masking for LDO1 current limit detection interrupt (LDO1_ILIM_INT in INT_LDO register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect LDO1_ILIM_STAT status bit in LDO_STAT register.                |
| 3    | LDO0_PGF_MASK  | R/W  | 0 *     | Masking of Power Good invalid detection for LDO0 power good interrupt (LDO0_PG_INT in INT_LDO register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect LDO0_PG_STAT status bit in LDO_STAT register. |
| 2    | LDO0_PGR_MASK  | R/W  | 0 *     | Masking of Power Good valid detection for LDO0 power good interrupt (LDO0_PG_INT in INT_LDO register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect LDO0_PG_STAT status bit in LDO_STAT register.   |
| 1    | Reserved       | R    | 0       |                                                                                                                                                                                                                                               |
| 0    | LDO0_ILIM_MASK | R/W  | 0 *     | Masking for LDO0 current limit detection interrupt (LDO0_ILIM_INT in INT_LDO register):<br>0 - Interrupt generated<br>1 - Interrupt not generated.<br>This bit does not affect LDO0_ILIM_STAT status bit in LDO_STAT register.                |

**8.6.1.37 SEL\_I\_LOAD**

Address: 0x24

| D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0                       |
|----------|----|----|----|----|----|----|--------------------------|
| Reserved |    |    |    |    |    |    | LOAD_CURRENT_BUCK_SELECT |

| Bits | Field                    | Type | Default  | Description                                                                                                                                |
|------|--------------------------|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1  | Reserved                 | R/W  | 000 0000 |                                                                                                                                            |
| 0    | LOAD_CURRENT_BUCK_SELECT | R/W  | 0        | Start the current measurement on the selected regulator:<br>0 - Buck0<br>1 - Buck1<br>The measurement is started when register is written. |

### 8.6.1.38 I\_LOAD\_2

Address: 0x25

| D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0                   |
|----------|----|----|----|----|----|----|----------------------|
| Reserved |    |    |    |    |    |    | BUCK_LOAD_CURRENT[8] |

| Bits | Field                | Type | Default  | Description                                                                                                                                           |
|------|----------------------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1  | Reserved             | R    | 000 0000 |                                                                                                                                                       |
| 0    | BUCK_LOAD_CURRENT[8] | R    | 0        | This register describes the MSB bit of the average load current on selected regulator with a resolution of 20 mA per LSB and maximum 10.22-A current. |

### 8.6.1.39 I\_LOAD\_1

Address: 0x26

| D7                     | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|----|----|----|----|----|----|----|
| BUCK_LOAD_CURRENT[7:0] |    |    |    |    |    |    |    |

| Bits | Field                  | Type | Default   | Description                                                                                                                                          |
|------|------------------------|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | BUCK_LOAD_CURRENT[7:0] | R    | 0000 0000 | This register describes 8 LSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and maximum 10.22-A current. |

## 9 Application and Implementation

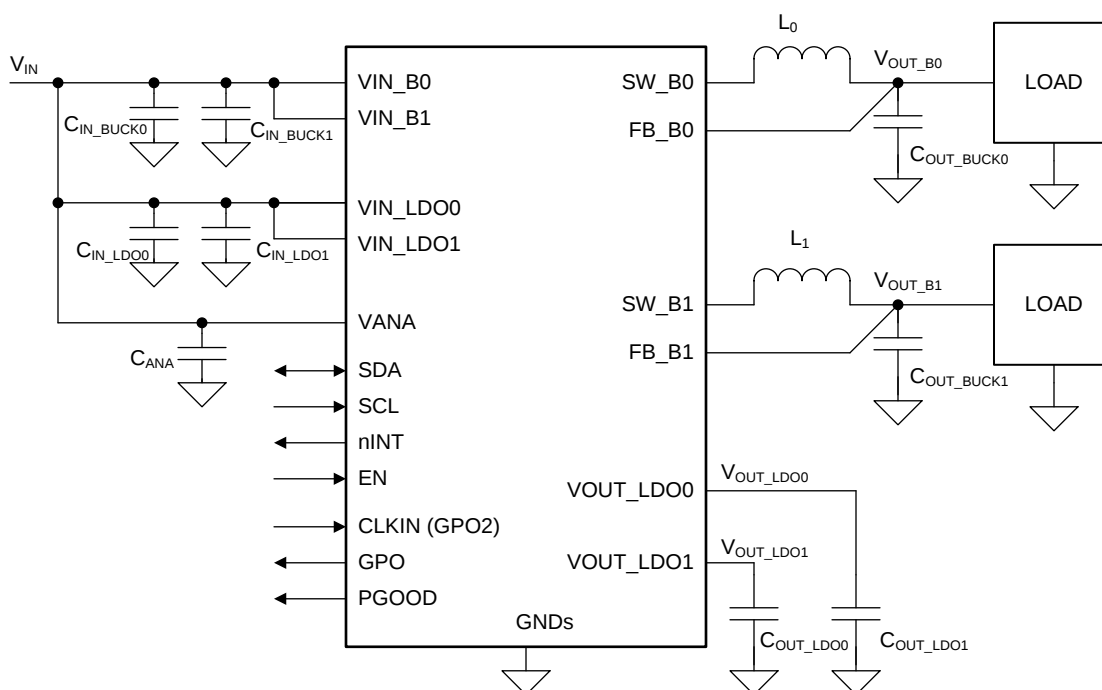
### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LP87322B/D/E/F-Q1 is a power management unit including two step-down regulators, two linear regulators, and two general-purpose digital output signals.

### 9.2 Typical Application



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图 25. LP87322B/D/E/F-Q1 Typical Application

#### 9.2.1 Design Requirements

##### 9.2.1.1 Inductor Selection

The inductors  $L_0$  and  $L_1$  are shown in the [Typical Application](#). The inductance and DCR of the inductor affects the control loop of the buck regulator. TI recommends using inductors similar to those listed in [表 8](#). Pay attention to the saturation current and temperature rise current of the inductor. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. Minimum effective inductance to ensure good performance is 0.22  $\mu\text{H}$  at maximum peak output current over the operating temperature range. DC resistance of the inductor must be less than 0.05  $\Omega$  for good efficiency at high-current condition. The inductor AC loss also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred as they radiate less noise.

## Typical Application (接下页)

**表 8. Recommended Inductors**

| MANUFACTURE<br>R | PART NUMBER      | VALUE              | DIMENSIONS L × W × H (mm) | RATED DC CURRENT<br>$I_{SAT}$ maximum (typical) /<br>$I_{TEMP}$ maximum (typical) (A) | DCR<br>typical / maximum<br>(mΩ) |
|------------------|------------------|--------------------|---------------------------|---------------------------------------------------------------------------------------|----------------------------------|
| TOKO             | DFE252012PD-R47M | 0.47 $\mu$ H (20%) | 2.5 × 2 × 1.2             | 5.2 (–) / 4 (–) <sup>(1)</sup>                                                        | — / 27                           |
| Tayo Yuden       | MDMK2020TR47MMV  | 0.47 $\mu$ H (20%) | 2 × 2 × 1.2               | 4.2 (4.8) / 2.3 (2.45)                                                                | 40 / 46                          |

(1) Operating temperature range is up to 125°C including self temperature rise.

### 9.2.1.2 Buck Input Capacitor Selection

The input capacitors  $C_{IN\_BUCK0}$  and  $C_{IN\_BUCK1}$  are shown in the [Typical Application](#). A ceramic input bypass capacitor of 10  $\mu$ F is required for each phase of the regulator. Place the input capacitor as close as possible to the VIN\_Bx pin and PGND\_Bx pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. Also the DC bias characteristics capacitors must be considered. Minimum effective input capacitance to ensure good performance is 1.9  $\mu$ F per buck input at maximum input voltage including tolerances, ambient temperature range and aging. This is assuming that there are at least 22  $\mu$ F of additional capacitance common for all the power input pins on the system power rail. See [表 9](#).

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition ferrite can be used in front of the input capacitor to reduce the EMI.

**表 9. Recommended Buck Input Capacitor (X7R Dielectric)**

| MANUFACTURER | PART NUMBER       | VALUE            | CASE SIZE | DIMENSIONS L × W × H<br>(mm) | VOLTAGE<br>RATING |
|--------------|-------------------|------------------|-----------|------------------------------|-------------------|
| Murata       | GCM21BR71A106KE22 | 10 $\mu$ F (10%) | 0805      | 2 × 1.25 × 1.25              | 10 V              |

### 9.2.1.3 Buck Output Capacitor Selection

The output capacitor  $C_{OUT\_BUCK0}$  and  $C_{OUT\_BUCK1}$  are shown in [Typical Application](#). A ceramic local output capacitor of 22  $\mu$ F is required per phase. Use ceramic capacitors, X7R type; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance to ensure good performance is 10  $\mu$ F per phase including the DC voltage roll-off, tolerances, aging, and temperature effects.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its  $R_{ESR}$ . The  $R_{ESR}$  is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part. See [表 10](#).

POL capacitors can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreases the PFM switching frequency. However, output capacitance higher than 150  $\mu$ F per phase is not necessarily of any benefit. Note that the output capacitor may be the limiting factor in the output voltage ramp, see [Specifications](#) for maximum output capacitance for different slew-rate settings. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown the output voltage is discharged to 0.6 V level using forced-PWM operation. This can increase the input voltage if the load current is small and the output capacitor is large compared to input capacitor. Below 0.6 V level the output capacitor is discharged by the internal discharge resistor and with large capacitor more time is required to settle  $V_{OUT}$  down as a consequence of the increased time constant.

**表 10. Recommended Buck Output Capacitors (X7R Dielectric)**

| MANUFACTURER | PART NUMBER       | VALUE            | CASE SIZE | DIMENSIONS L × W × H (mm) | VOLTAGE RATING |
|--------------|-------------------|------------------|-----------|---------------------------|----------------|
| Murata       | GCM31CR71A226KE02 | 22 $\mu$ F (10%) | 1206      | 3.2 × 1.6 × 1.6           | 10 V           |

#### 9.2.1.4 LDO Input Capacitor Selection

The input capacitors  $C_{IN\_LDO0}$  and  $C_{IN\_LDO1}$  are shown in the [图 25](#). A ceramic input capacitor of 2.2  $\mu$ F, 6.3 V is sufficient for most applications. Place the input capacitor as close as possible to the VIN\_LDOx pin and AGND pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. DC bias characteristics of capacitors must be considered, minimum effective input capacitance to ensure good performance is 0.6  $\mu$ F per LDO input at maximum input voltage including tolerances, ambient temperature range and aging. See [表 11](#).

**表 11. Recommended LDO Input Capacitors (X7R Dielectric)**

| MANUFACTURER | PART NUMBER       | VALUE             | CASE SIZE | DIMENSIONS L × W × H (mm) | VOLTAGE RATING |
|--------------|-------------------|-------------------|-----------|---------------------------|----------------|
| Murata       | GCM188R70J225KE22 | 2.2 $\mu$ F (10%) | 0603      | 1.6 × 0.8 × 0.8           | 6.3 V          |
| Murata       | GCM21BR71C475KA73 | 4.7 $\mu$ F (10%) | 0805      | 2 × 1.25 × 1.25           | 16 V           |

#### 9.2.1.5 LDO Output Capacitor Selection

The output capacitors  $C_{OUT\_LDO0}$  and  $C_{OUT\_LDO1}$  are shown in the [Typical Application](#). A ceramic output capacitor of minimum 1.0  $\mu$ F is required. Place the output capacitor as close to the VOUT\_LDOx pin and AGND pin of the device as possible. Use X7R type of capacitors, not Y5V or F. DC bias characteristics of capacitors must be considered, minimum effective output capacitance to ensure good performance is 0.4  $\mu$ F per LDO input at maximum input voltage including tolerances, ambient temperature range and aging. See [表 12](#).

The output capacitance must be smaller than the input capacitance in order to ensure the stability of the LDO. With a 1- $\mu$ F output capacitor it is recommended to use at least 2.2- $\mu$ F input capacitor; with a 2.2- $\mu$ F output capacitor at least 4.7- $\mu$ F input capacitance.

The VANA input is used to supply analog and digital circuits in the device. See [表 13](#) for recommended components from for VANA input supply filtering.

**表 12. Recommended LDO Output Capacitors (X7R Dielectric)**

| MANUFACTURER | PART NUMBER       | VALUE             | CASE SIZE | DIMENSIONS L × W × H (mm) | VOLTAGE RATING |
|--------------|-------------------|-------------------|-----------|---------------------------|----------------|
| Murata       | GCM188R71C105KA64 | 1 $\mu$ F (10%)   | 0603      | 1.6 × 0.8 × 0.8           | 16 V           |
| Murata       | GCM188R70J225KE22 | 2.2 $\mu$ F (10%) | 0603      | 1.6 × 0.8 × 0.8           | 6.3 V          |

**表 13. Recommended Supply Filtering Components**

| MANUFACTURER | PART NUMBER       | VALUE        | CASE SIZE | DIMENSIONS L × W × H (mm) | VOLTAGE RATING |
|--------------|-------------------|--------------|-----------|---------------------------|----------------|
| Murata       | GCM155R71C104KA55 | 100 nF (10%) | 0402      | 1 × 0.5 × 0.5             | 16 V           |
| Murata       | GCM188R71C104KA37 | 100 nF (10%) | 0603      | 1.6 × 0.8 × 0.8           | 16 V           |

### 9.2.2 Detailed Design Procedure

The performance of the LP87322B/D/E/F-Q1 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention must be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from system power rail during turnon of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate buck regulator power pins VIN\_Bx are not connected together internally. Connect the VIN\_Bx power connections together outside the package using power plane construction.

### 9.2.3 Application Curves

Unless otherwise specified:  $V_{(VIN\_Bx)} = V_{(VIN\_LDOx)} = V_{(VANA)} = 3.7\text{ V}$ ,  $V_{OUT\_Bx} = 1\text{ V}$ ,  $V_{OUT\_LDOx} = 1\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $L = 0.47\text{ }\mu\text{H}$  (TOKO DFE252012PD-R47M),  $C_{OUT\_BUCK} = 22\text{ }\mu\text{F}$ , and  $C_{POL\_BUCK} = 22\text{ }\mu\text{F}$ ,  $C_{OUT\_LDO} = 1\text{ }\mu\text{F}$ . Measurements are done using connections in the 图 25.

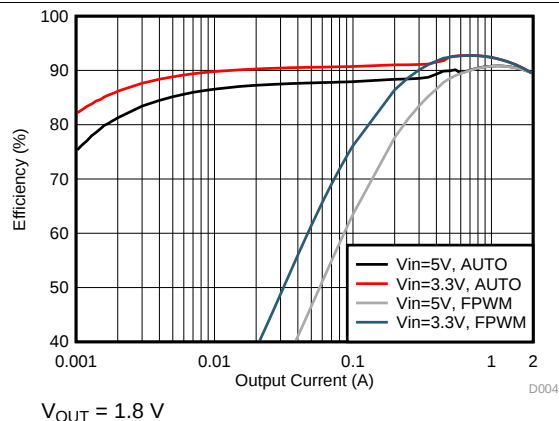


图 26. Buck Efficiency in PFM/PWM and Forced PWM Mode

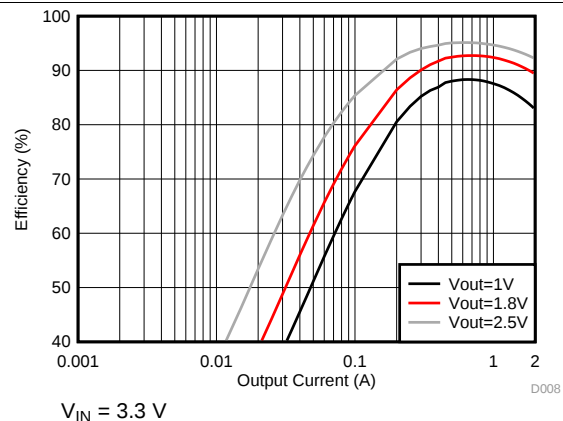


图 27. Buck Efficiency in Forced PWM Mode

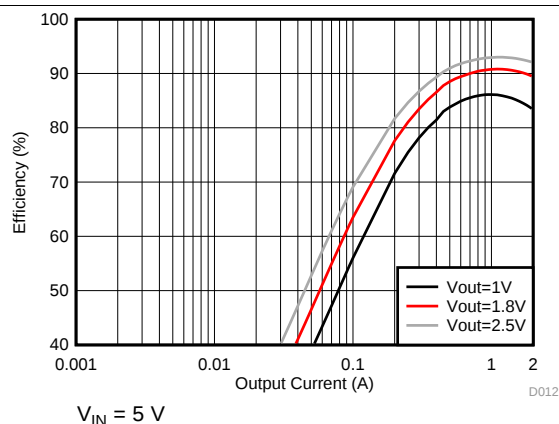


图 28. Buck Efficiency in Forced PWM Mode

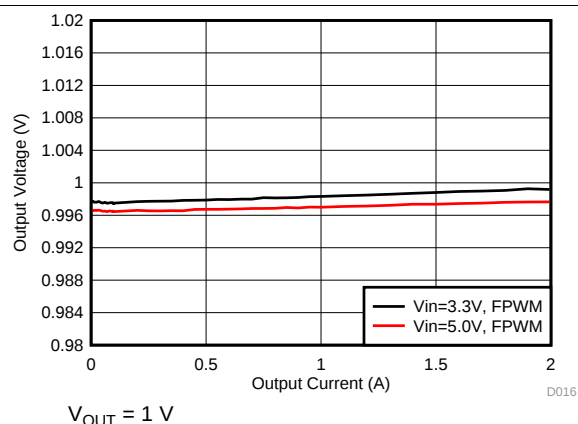


图 29. Buck Output Voltage vs Load Current in Forced PWM Mode

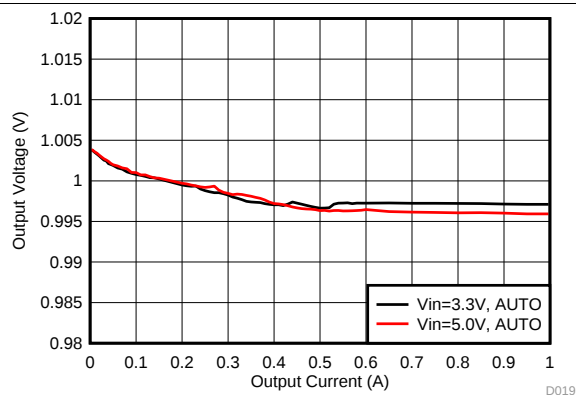


图 30. Buck Output Voltage vs Load Current in PFM/PWM Mode

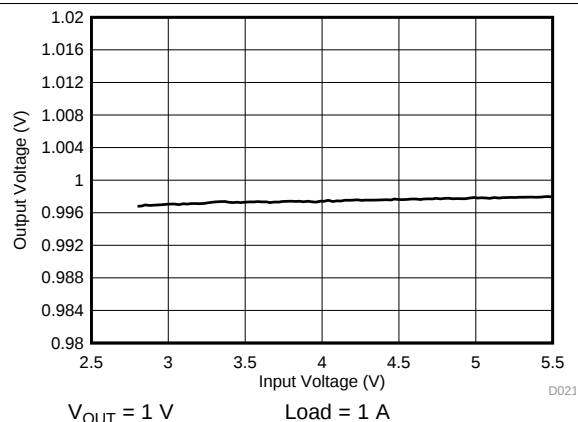


图 31. Buck Output Voltage vs Input Voltage in PWM Mode

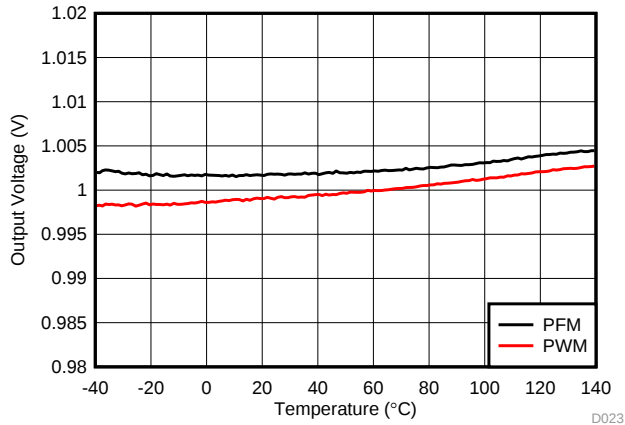


图 32. Buck Output Voltage vs Temperature

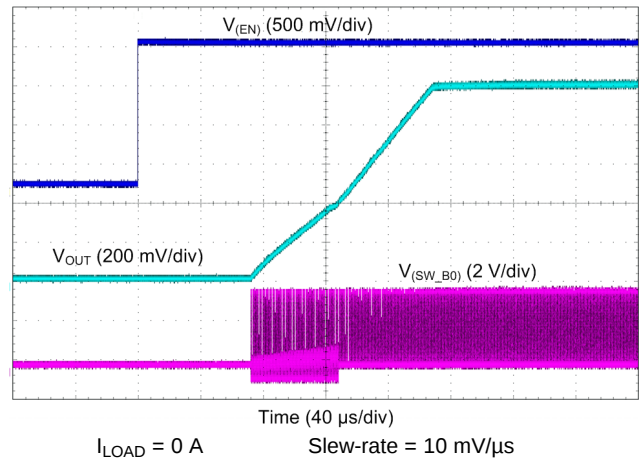


图 33. Buck Start-Up With EN1, Forced PWM Mode

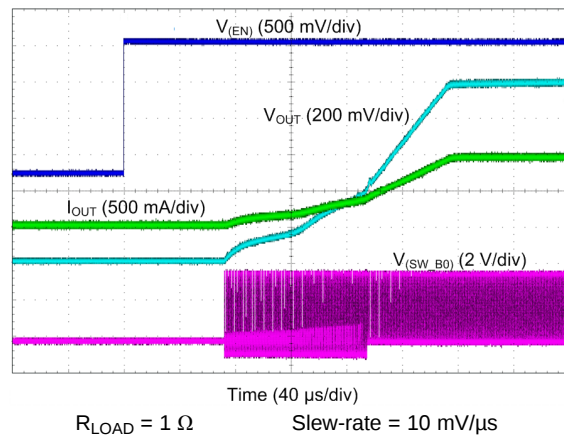


图 34. Buck Start-up with EN1, Forced PWM Mode

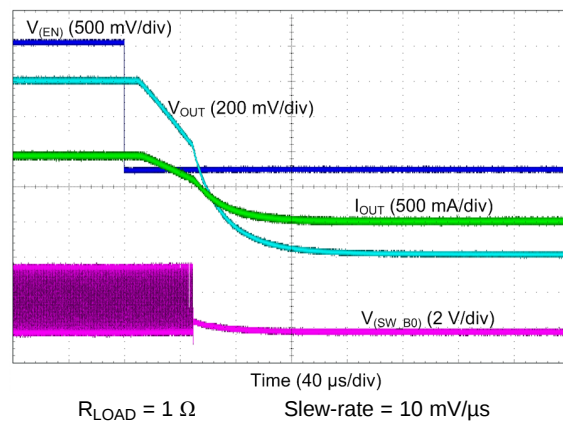


图 35. Buck Shutdown With EN1, Forced PWM Mode

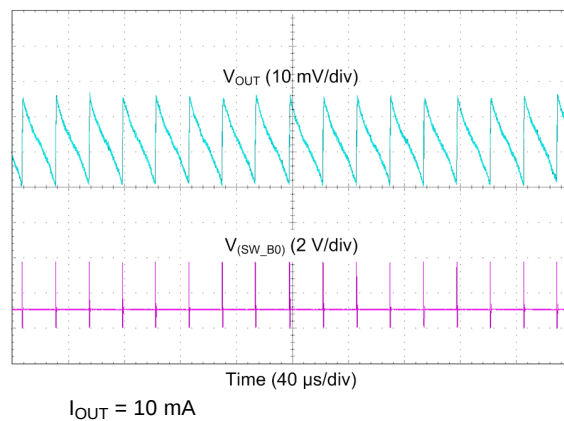


图 36. Buck Output Voltage Ripple, PFM Mode

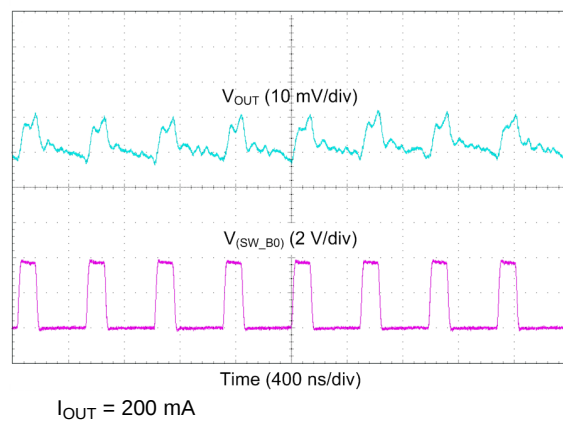


图 37. Buck Output Voltage Ripple, Forced PWM Mode

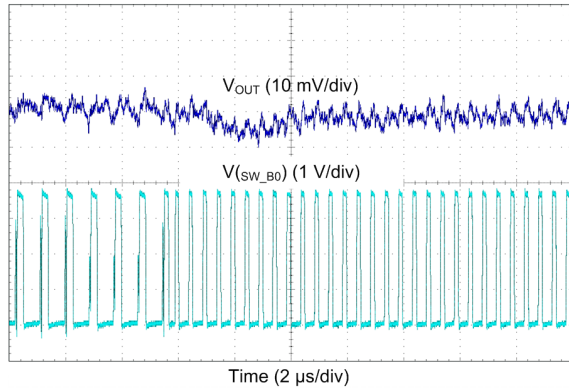


图 38. Buck Transient from PFM-to-PWM Mode

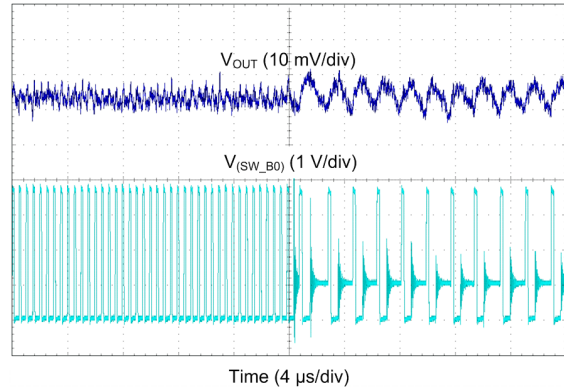
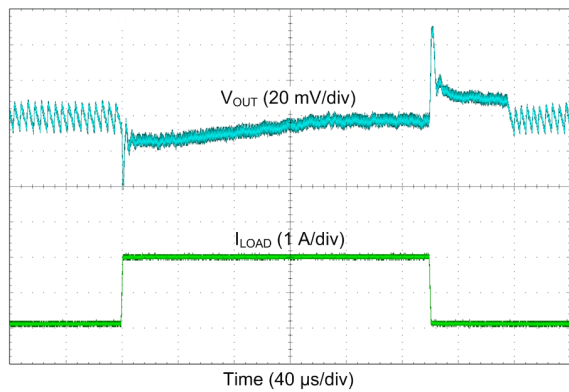
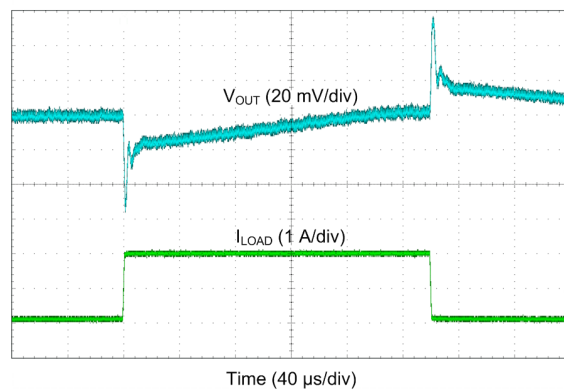


图 39. Buck Transient from PWM-to-PFM Mode



$I_{OUT} = 0.1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 0.1 \text{ A}$   $T_R = T_F = 400 \text{ ns}$

图 40. Buck Transient Load Step Response, AUTO Mode



$I_{OUT} = 0.1 \text{ A} \rightarrow 2 \text{ A} \rightarrow 0.1 \text{ A}$   $T_R = T_F = 400 \text{ ns}$

图 41. Buck Transient Load Step Response, Forced PWM Mode

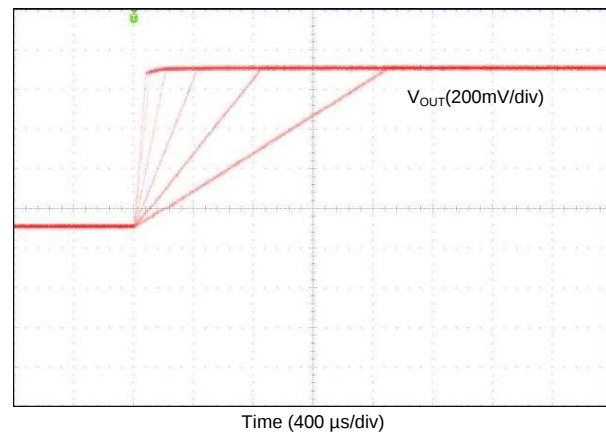


图 42. Buck  $V_{OUT}$  Transition from 0.6 V to 1.4 V With Different Slew Rate Settings

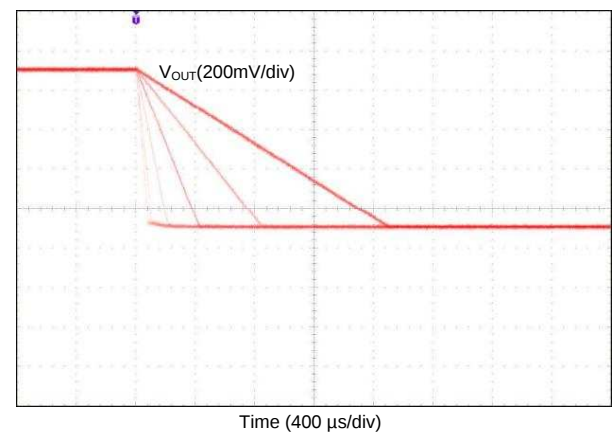


图 43. Buck  $V_{OUT}$  Transition from 1.4 V to 0.6 V With Different Slew Rate Settings

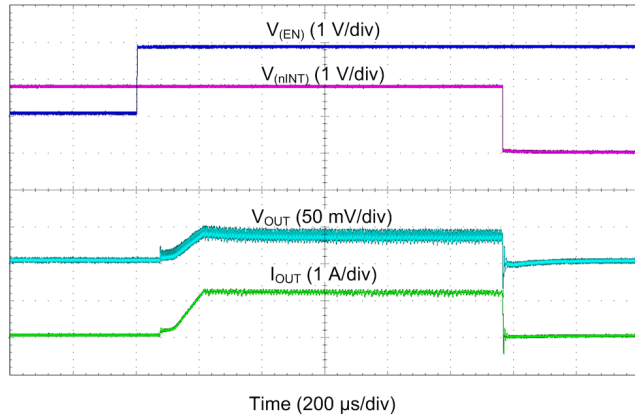


图 44. Buck Start-up With Short on Output

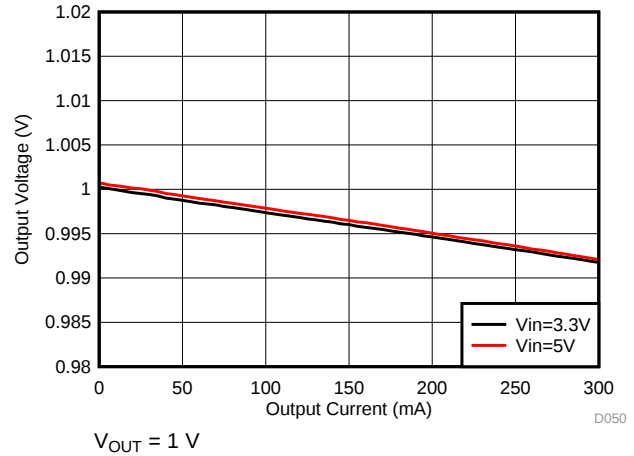


图 45. LDO Output Voltage vs Load Current

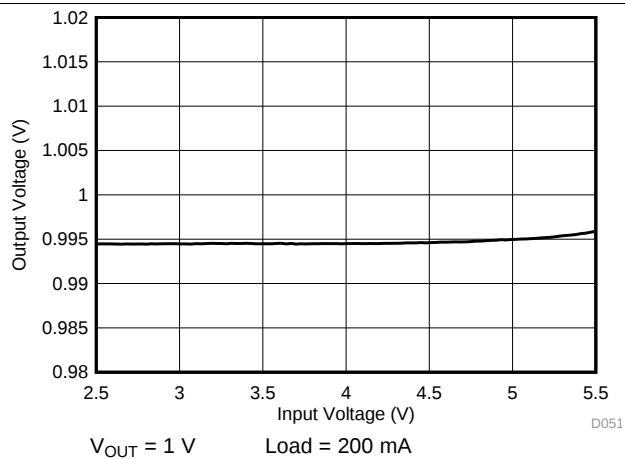


图 46. LDO Output Voltage vs Input Voltage

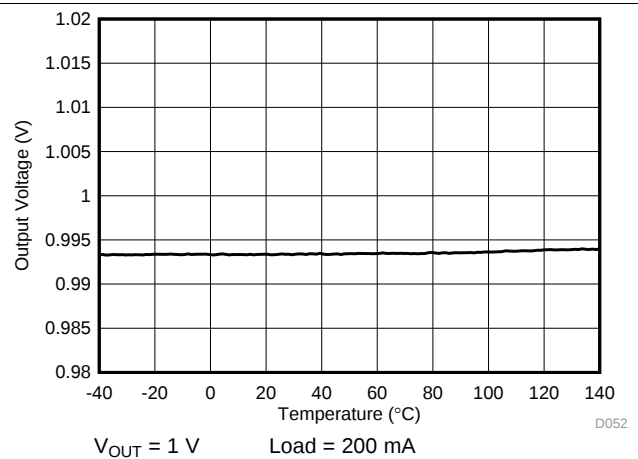


图 47. LDO Output Voltage vs Temperature

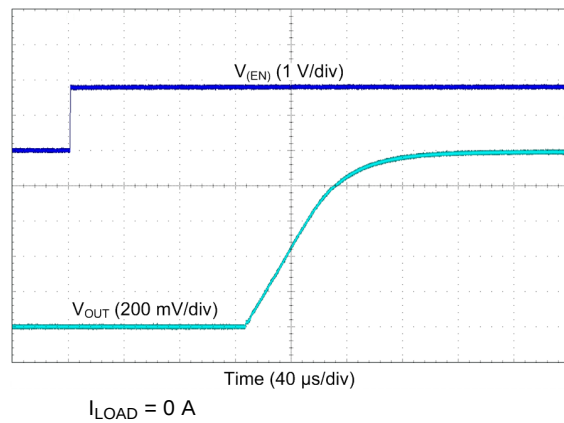


图 48. LDO Start-Up

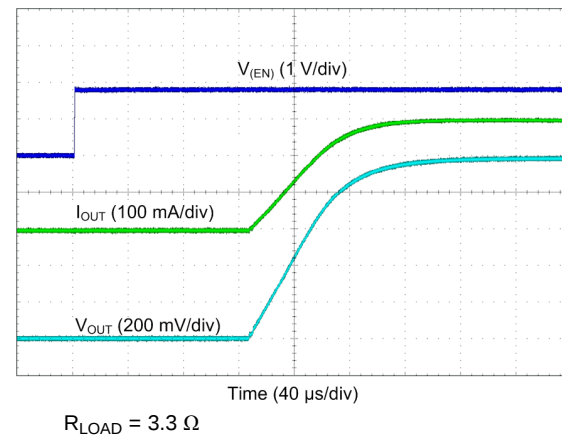


图 49. LDO Start-Up

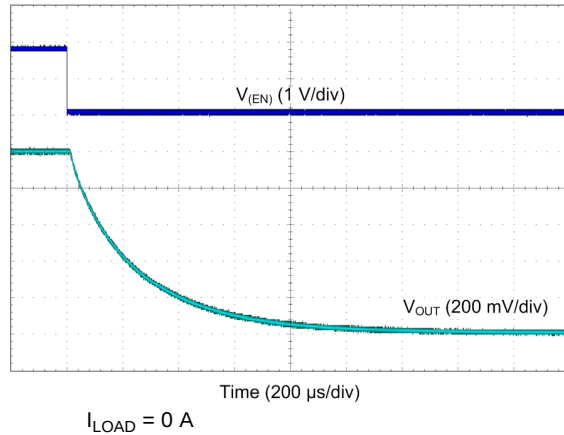


图 50. LDO Shutdown

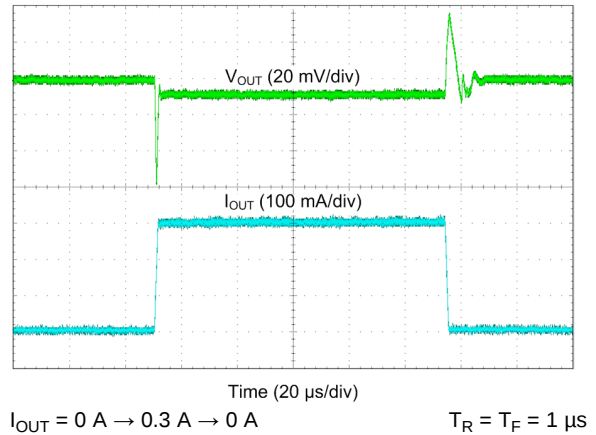


图 51. LDO Transient Load Step Response

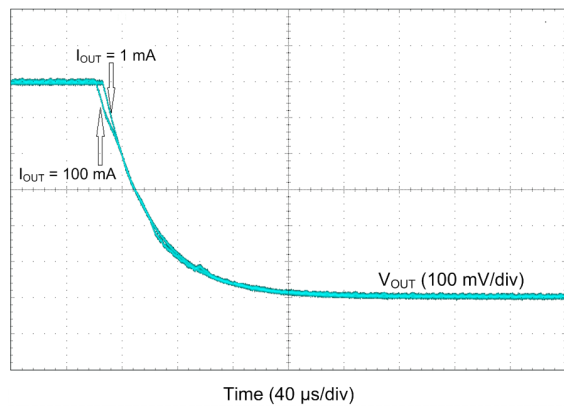


图 52. LDO  $V_{OUT}$  Transition from 1.8 V to 1.2 V

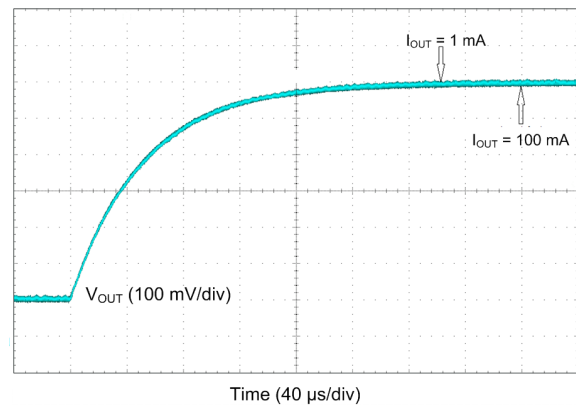


图 53. LDO  $V_{OUT}$  Transition from 1.2 V to 1.8 V

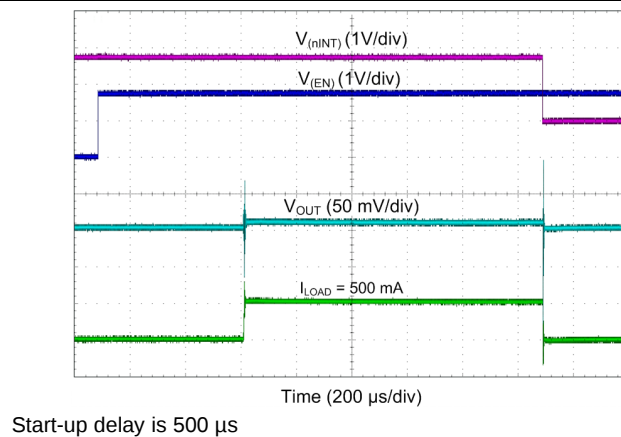


图 54. LDO Start-Up With Short on Output

## 10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. The VANA input and VIN\_Bx buck inputs must be connected together and they must use the same input supply. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high a drop in the LP87322B/D/E/F-Q1 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP87322B/D/E/F-Q1 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The VIN\_LDOx LDO input supply voltage range is 2.5 V to 5.5 V and can be higher or lower than VANA supply voltage.

## 11 Layout

### 11.1 Layout Guidelines

The high frequency and large switching currents of the LP87322B/D/E/F-Q1 make the choice of layout important. Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamperes to several amps, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place  $C_{IN}$  as close as possible to the VIN\_Bx pin and the PGND\_Bx pin. Route the  $V_{IN}$  trace wide and thick to avoid IR drops. The trace between the positive node of the input capacitor and the VIN\_Bx pin(s) of LP87322B/D/E/F-Q1, as well as the trace between the negative node of the input capacitor and power PGND\_Bx pin(s), must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor — parasitic inductance on these traces must be kept as small as possible for proper device operation. The parasitic inductance can be reduced by using a ground plane as close as possible to top layer by using thin dielectric layer between top layer and ground plane.
2. The output filter, consisting of L and COUT, converts the switching signal at SW\_Bx to the noiseless output voltage. It must be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the output capacitors of the LP87322B/D/E/F-Q1 and the input capacitors of the load direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) must be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.

**Layout Guidelines (接下页)**

4. If remote voltage sensing can be used for the load, connect the LP87322B/D/E/F-Q1 feedback pins FB\_Bx to the respective sense pins on the load capacitor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND\_Bx, VIN\_Bx, and SW\_Bx, as well as high bandwidth signals such as the I<sup>2</sup>C. Avoid both capacitive and inductive coupling by keeping the sense lines short and direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. If series resistors are used for load current measurement, place them after connection of the voltage feedback.
5. PGND\_Bx, VIN\_Bx and SW\_Bx must be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND\_Bx, VIN\_Bx and SW\_Bx.
6. LDO performance (PSRR, noise and transient response) depend on the layout of the PCB. Best performance is achieved by placing CIN and COUT as close to the LP87322B/D/E/F-Q1 device as practical. The ground connections for CIN and COUT must be back to the LP87322B/D/E/F-Q1 AGND with as wide and as short of a copper trace as is practical and with multiple vias if routing is done on other layer. Avoid connections using long trace lengths, narrow trace widths, or connection through small via. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ( $R_{\theta JA}$ ) and junction-to-board ( $R_{\theta JB}$ ) thermal resistances, thereby reducing the device junction temperature,  $T_J$ . TI strongly recommends performance of a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process by using a thermal modeling analysis software.

## 11.2 Layout Example

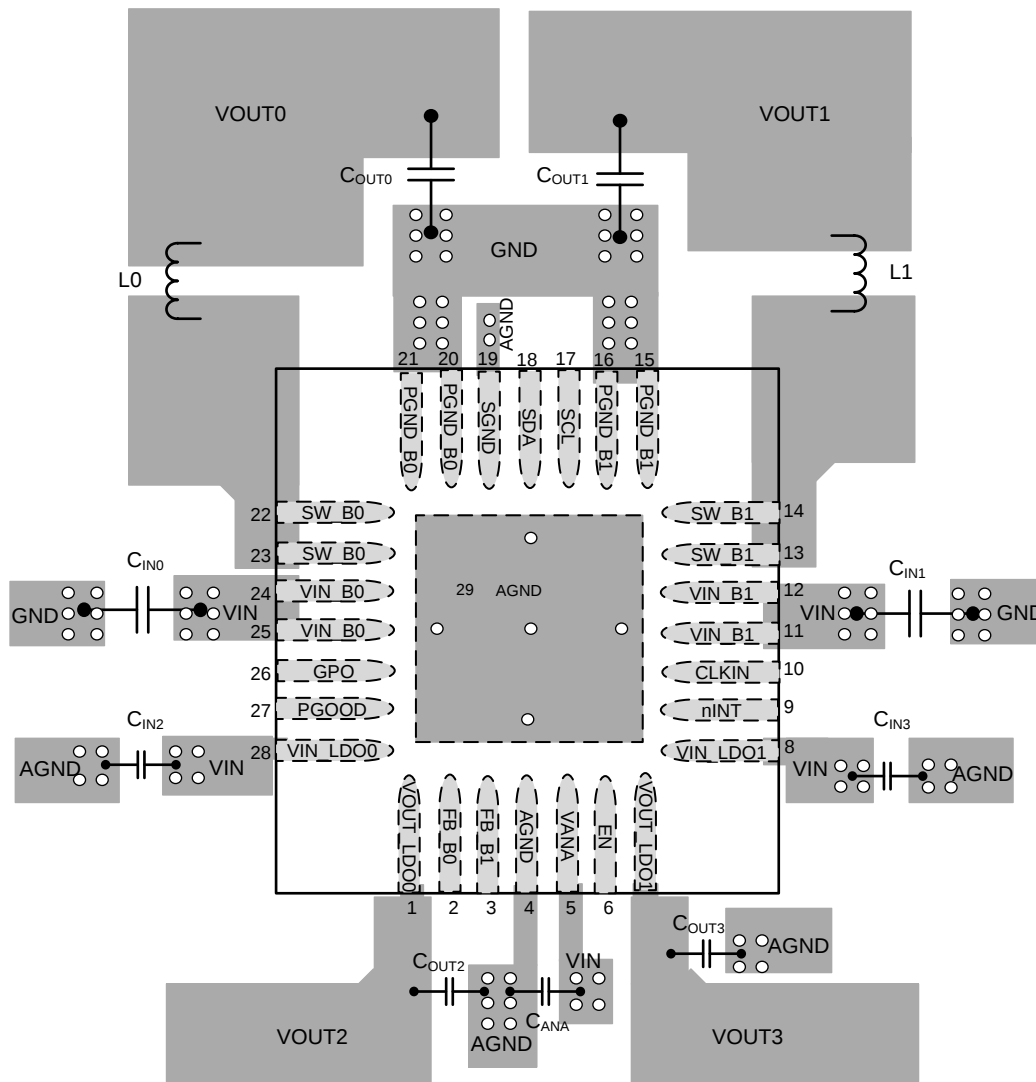


图 55. LP87322B/D/E/F-Q1 Board Layout

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 文档支持

#### 12.2.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及立即订购快速访问。

表 14. 相关链接

| 器件          | 产品文件夹                 | 立即订购                  | 技术文档                  | 工具和软件                 | 支持和社区                 |
|-------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| LP87322B-Q1 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| LP87322D-Q1 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| LP87322E-Q1 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| LP87322F-Q1 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |

### 12.3 接收文档更新通知

要接收文档更新通知，请导航至 **TI.com** 上的器件产品文件夹。单击右上角的 **通知我** 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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**设计支持** **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 12.5 商标

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### 12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)    | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|----------------------------|-------------------------|
| LP87322ERHDRQ1   | ACTIVE        | VQFN         | RHD                | 28   | 3000           | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 125   | LP8732<br>(2E-Q1, 2ERHDQ1) | <a href="#">Samples</a> |
| LP87322ERHDTQ1   | ACTIVE        | VQFN         | RHD                | 28   | 250            | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 125   | LP8732<br>2E-Q1            | <a href="#">Samples</a> |
| LP87322FRHDRQ1   | ACTIVE        | VQFN         | RHD                | 28   | 3000           | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 125   | LP8732<br>(2F-Q1, 2FRHDQ1) | <a href="#">Samples</a> |
| LP87322FRHDTQ1   | ACTIVE        | VQFN         | RHD                | 28   | 250            | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 125   | LP8732<br>2F-Q1            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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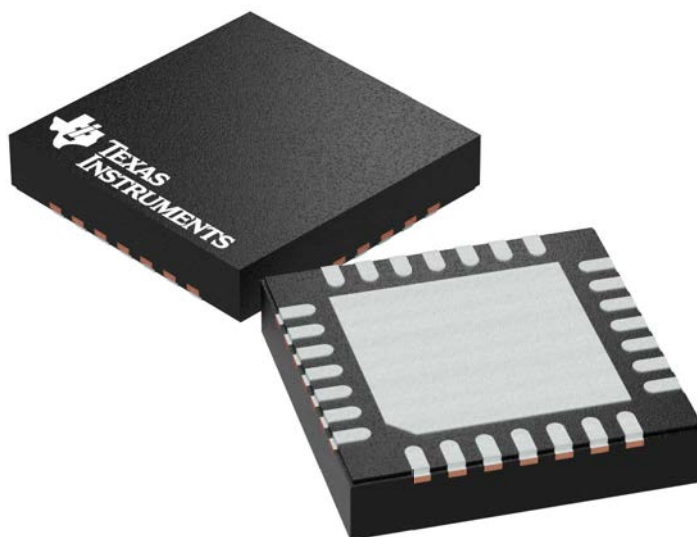
## GENERIC PACKAGE VIEW

**RHD 28**

**VQFN - 1 mm max height**

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



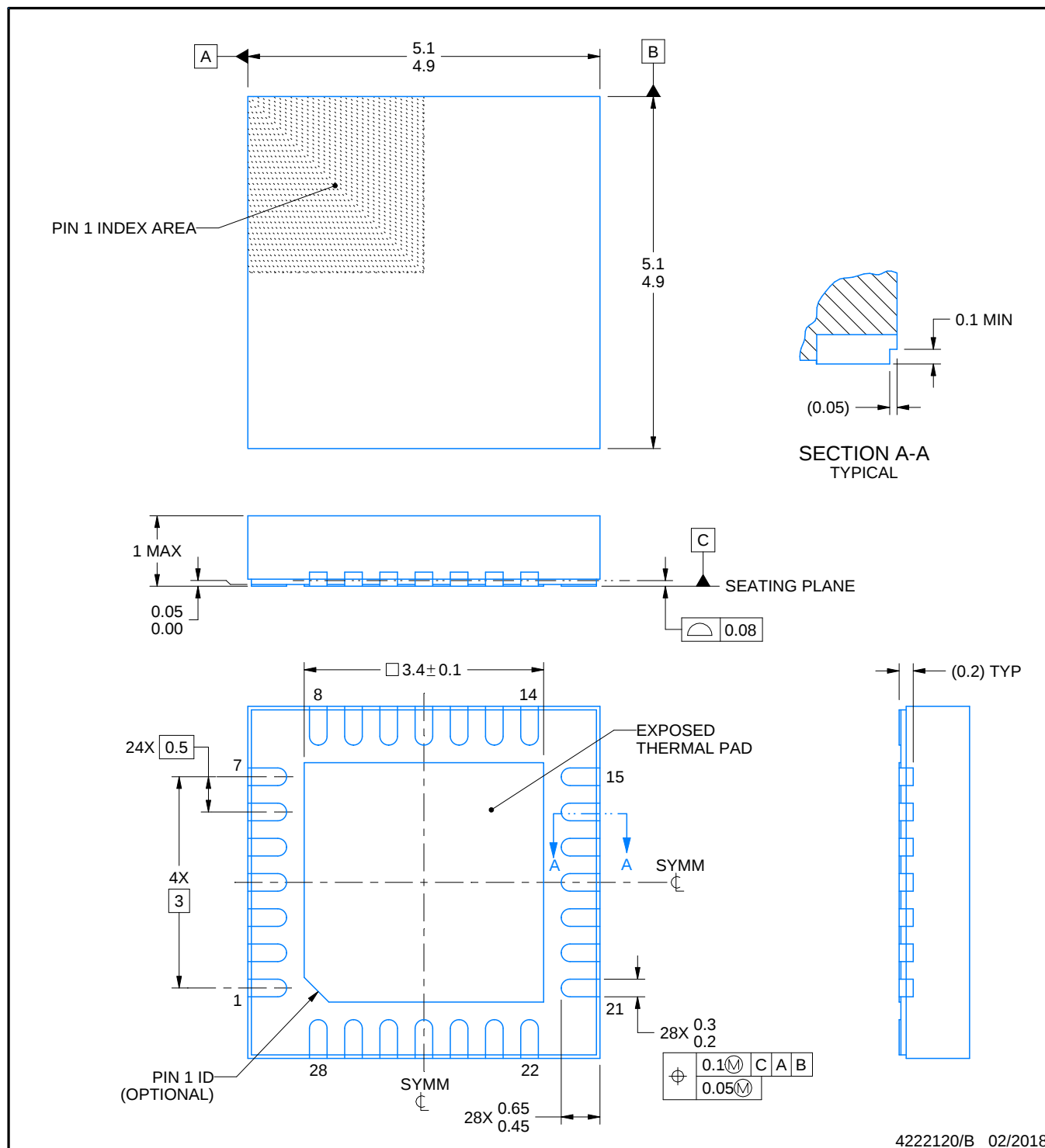
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204400/G



## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

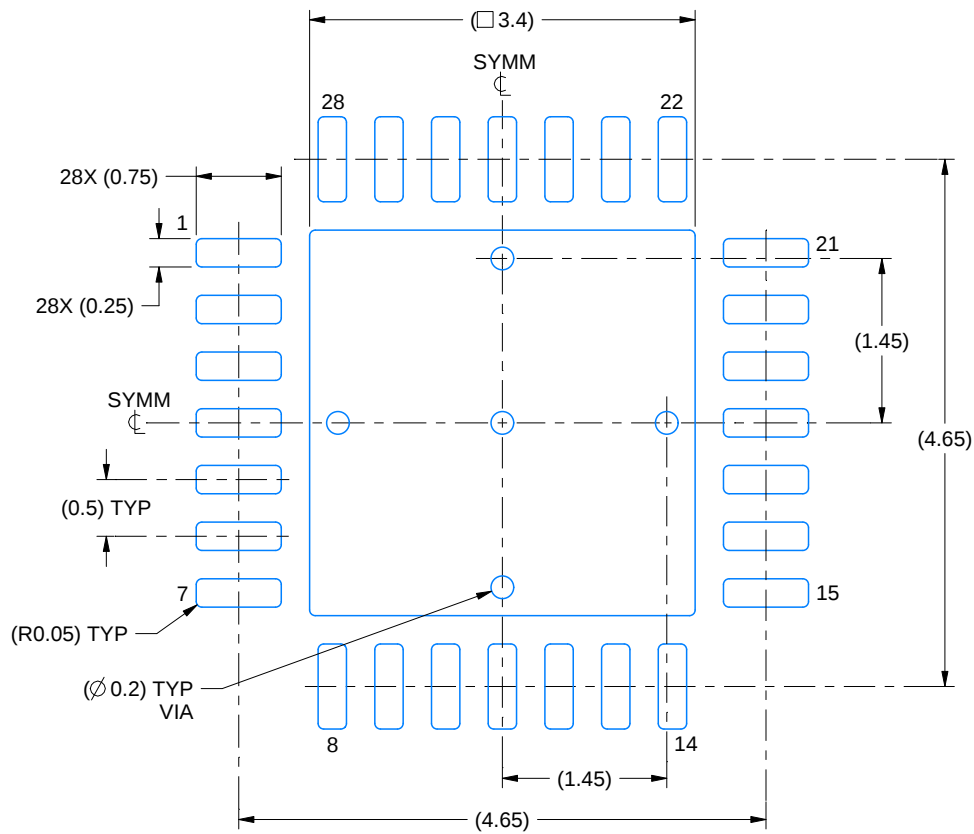
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

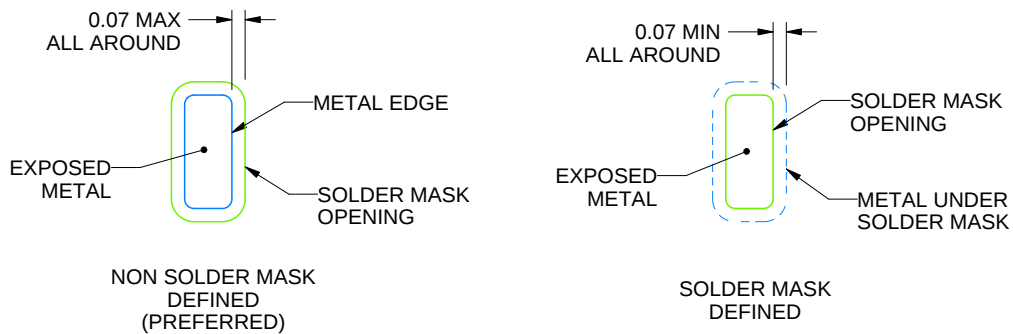
RHD0028W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222120/B 02/2018

NOTES: (continued)

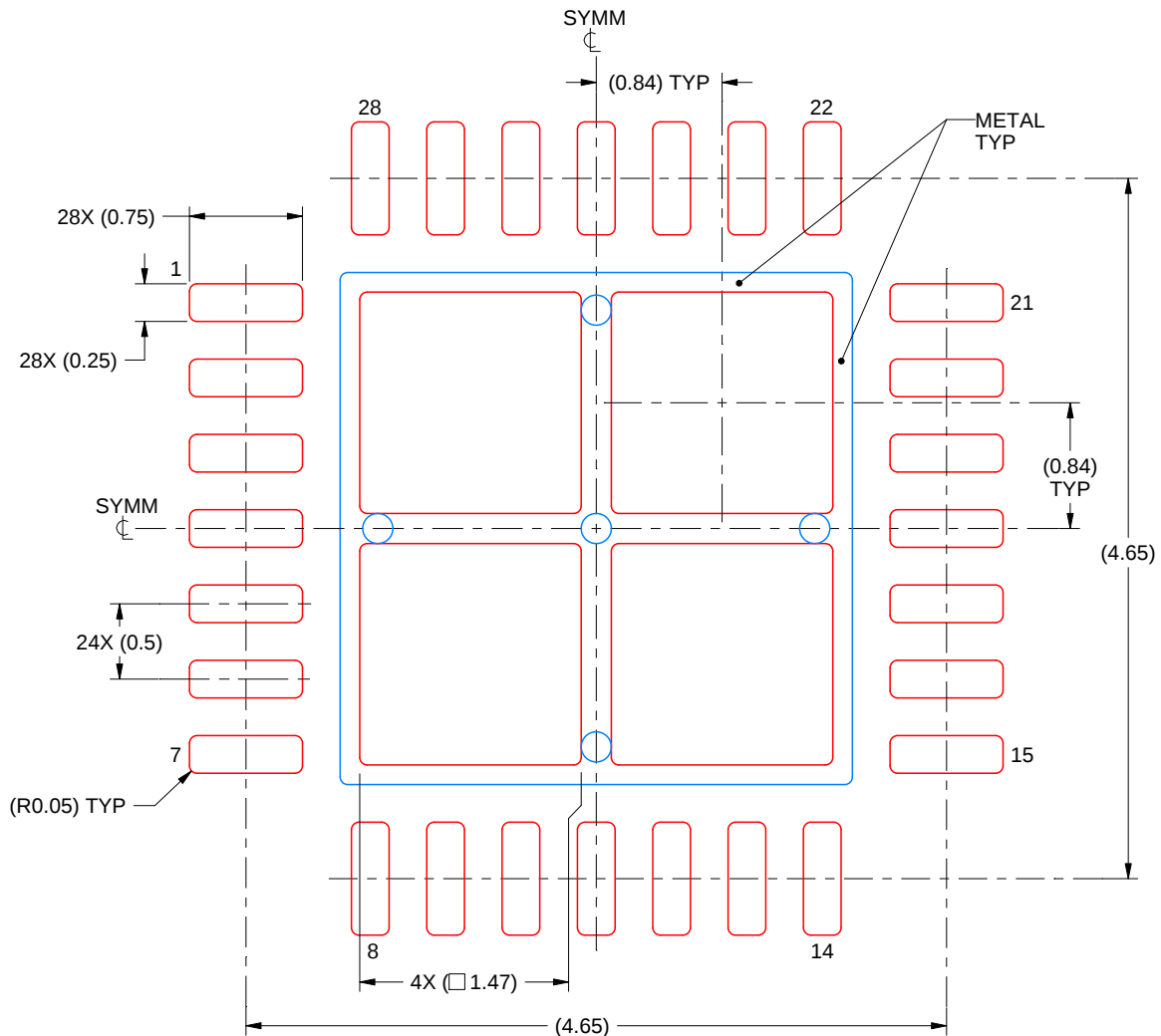
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

RHD0028W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
75% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4222120/B 02/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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