SN74LVC1G14-Q1 单路施密特触发逆变器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体放电模型 (HBM) ESD 分类等级 2
  - 器件带电器件模型 (CDM) ESD 分类等级 C5
- 支持 5V V_{CC} 运行
- 输入电压高达 5.5V
- 电压为 3.3V 时，t_{pd} 最大值为 4.6ns
- 低功耗，10μA 最大 I_{CC}
- 电压为 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持局部关断模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

2 应用

- 车身控制模块
- 引擎控制模块
- 信息娱乐系统
- 远程信息处理

3 说明

这款单路施密特触发逆变器支持 1.65V 至 5.5V V_{CC} 工作。

SN74LVC1G14-Q1 器件包含一个逆变器，并执行布尔函数 $Y = \overline{A}$。该器件以独立逆变器的形式工作，但出于施密特操作方面的原因，正向 (V_{T+}) 和负向 (V_{T-}) 信号的输入阈值可能有所不同。
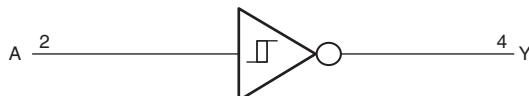
该器件完全 适用于 I_{off} 为了部分断电的应用。I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

器件信息[1]

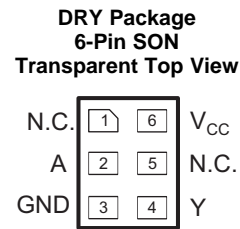| 器件型号	封装	封装尺寸（标称值）
SN74LVC1G14-Q1	SC70 (5)	2.10mm × 2.00mm
	SON (6)	1.45mm x 1.00mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (March 2017) to Revision B   **Page**

• 已添加 向器件信息 表添加了 SON (6) DRY 封装 1
• Added DRY package pinout to *Pin Configurations and Functions* section 3

Changes from Original (February 2015) to Revision A   **Page**

• 已更改 在器件信息 表中将封装类型更改为了 DCK (SC70) 并更正了封装尺寸 1
• Deleted θ_{JA} from *Absolute Maximum Ratings* table 3
• 已添加 接收文档更新通知 部分和社区资源 部分 12

5 Pin Configuration and Functions

DCK Package
5-Pin SC70
(Top View)

N.C. — 1 5 — V_{CC}
A — 2
GND — 3 4 — Y

DRY Package
6-Pin SON
Transparent Top View

N.C. — 1 6 — V_{CC}
A — 2 5 — N.C.
GND — 3 4 — Y
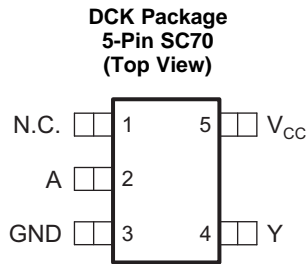
N.C. – No internal connection

See mechanical drawings for dimensions.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DCK (SC70)	DRY (SON)		
	NO.	NO.		
A	2	2	I	Input
GND	3	3	—	Ground
N.C.	1	1, 6	—	No Connect
V_{CC}	5	5	—	Supply / Power Pin
Y	4	4	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

				MIN	MAX	UNIT
V_{CC}	Supply voltage			−0.5	6.5	V
V_I	Input voltage[2]			−0.53	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]			−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2] [3]			−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$			−50	mA
I_{OK}	Output clamp current	$V_O < 0$			−50	mA
I_O	Continuous output current				±50	mA
	Continuous current through V_{CC} or GND				±100	mA
T_{stg}	Storage temperature			−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

See[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
T_A	Operating free-air temperature		−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1G14-Q1		UNIT
		DCK (SC70)	DRY (SON)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	280	264	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66	167	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67	142	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	26	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66	142	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{T+} Positive-going input threshold voltage			1.65 V	0.79		1.16	V
			2.3 V	1.11		1.56	
			3 V	1.5		1.87	
			4.5 V	2.16		2.74	
			5.5 V	2.61		3.33	
V_{T-} Negative-going input threshold voltage			1.65 V	0.39		0.64	V
			2.3 V	0.58		0.89	
			3 V	0.84		1.16	
			4.5 V	1.41		1.79	
			5.5 V	1.87		2.29	
ΔV_T Hysteresis $(V_{T+} - V_{T-})$			1.65 V	0.37		0.62	V
			2.3 V	0.48		0.77	
			3 V	0.56		0.87	
			4.5 V	0.71		1.04	
			5.5 V	0.71		1.11	
V_{OH}	$I_{OL} = -100$ µA		1.65 V to 4.5 V	$V_{CC} - 0.1$			V
	$I_{OL} = -4$ mA		1.65 V	1.2			
	$I_{OL} = -8$ mA		2.3 V	1.9			
	$I_{OL} = -16$ mA		3 V	2.4			
	$I_{OL} = -24$ mA			2.3			
	$I_{OL} = -32$ mA		4.5 V	3.8			
V_{OL}	$I_{OL} = 100$ µA		1.65 V to 4.5 V			0.1	V
	$I_{OL} = 4$ mA		1.65 V			0.45	
	$I_{OL} = 8$ mA		2.3 V			0.3	
	$I_{OL} = 16$ mA		3 V			0.4	
	$I_{OL} = 24$ mA					0.55	
	$I_{OL} = 32$ mA		4.5 V			0.70	
I_I	A input	$V_I = 5.5$ V or GND	0 to 5.5 V			±5	µA
I_{off}		V_I or $V_O = 5.5$ V	0			±10	µA
I_{CC}		$V_I = 5.5$ V or GND, $I_O = 0$	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_i		$V_I = V_{CC}$ or GND	3.3 V		4.5		pF

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25$°C.

6.6 Switching Characteristics, C$_L$ = 15 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$ = 1.8 V ± 0.15 V		V$_{CC}$ = 2.5 V ± 0.2 V		V$_{CC}$ = 3.3 V ± 0.3 V		V$_{CC}$ = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns

6.7 Switching Characteristics, C$_L$ = 30 pF or 50 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$ = 1.8 V ± 0.15 V		V$_{CC}$ = 2.5 V ± 0.2 V		V$_{CC}$ = 3.3 V ± 0.3 V		V$_{CC}$ = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t$_{pd}$	A	Y	3.8	13	2	8	1.8	6.5	1.2	6	ns

6.8 Operating Characteristics

T$_A$ = 25°C

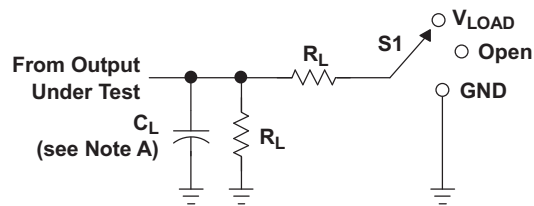| PARAMETER	TEST CONDITIONS	V$_{CC}$ = 1.8 V	V$_{CC}$ = 2.5 V	V$_{CC}$ = 3.3 V	V$_{CC}$ = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C$_{pd}$ Power dissipation capacitance	f = 10 MHz	20	21	22	25	pF

6.9 Typical Characteristics
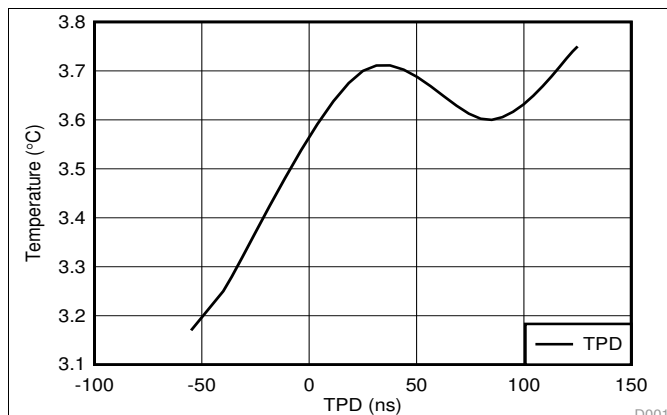
Figure 1. TPD Across Temperature at 3.3 V V$_{CC}$
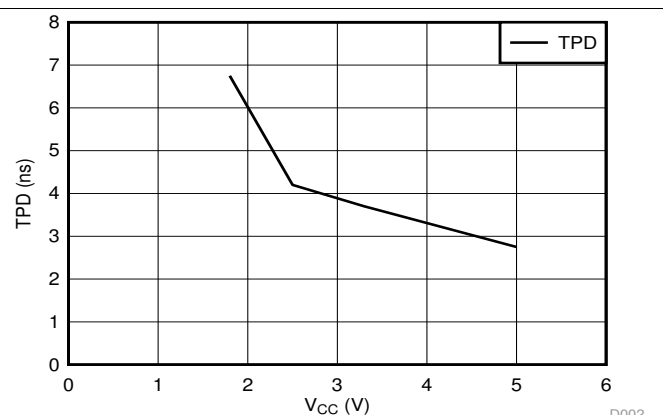
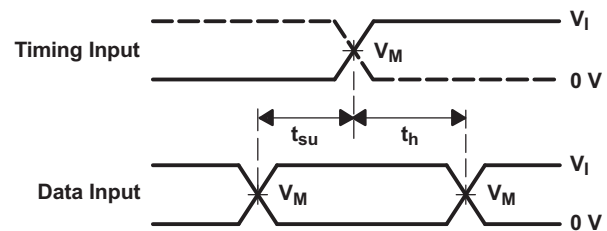**Figure 2. TPD Across V$_{CC}$ at 25°C**

7 Parameter Measurement Information

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

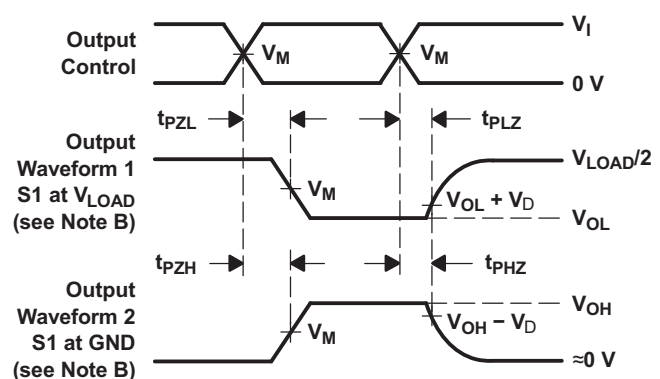| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V

VOLTAGE WAVEFORMS PULSE DURATION
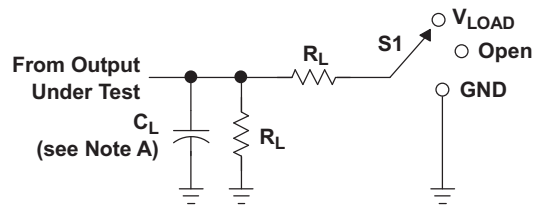
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

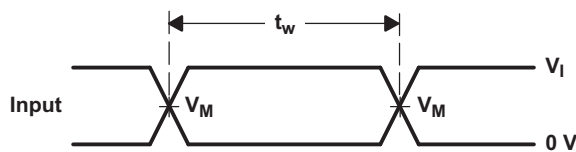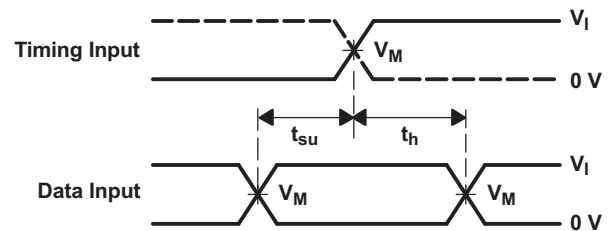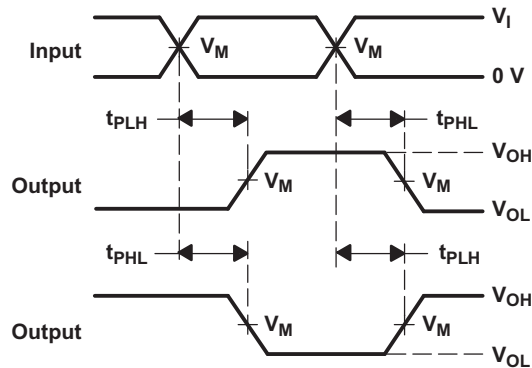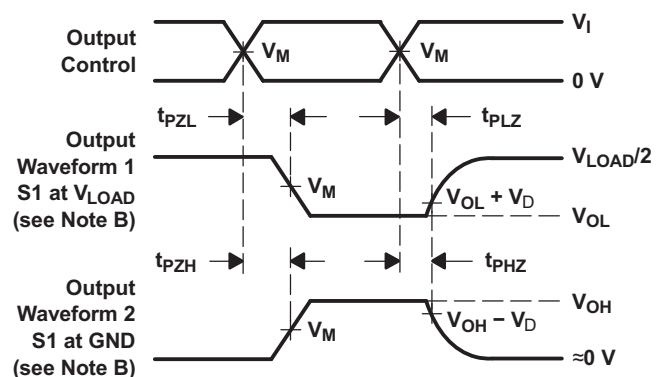**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G14-Q1 device contains one Schmitt Trigger Inverter and performs the Boolean function $Y = \overline{A}$. The device functions as an independent inverter, but because of Schmitt Trigger action, it will have different input threshold levels for a positive-going (V_{t+}) and negative-going (V_{t-}) signals.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuit disables the output, preventing damaging current back-flow through the device when it is powered down.

8.2 Functional Block Diagram
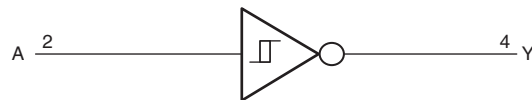
8.3 Feature Description

- Wide operating voltage range
- Operates from 1.65 V to 5 V V_{CC} and Input Operation
- Inputs Accept Voltages to 5.5 V
- Allows down voltage translation
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation which allows voltages on the inputs and outputs, when V_{CC} is 0 V

8.4 Device Functional Modes

Table 1 shows the functional modes of the SN74LVC1G14-Q1 device.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G14-Q1 is a high drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC}.

9.2 Typical Application
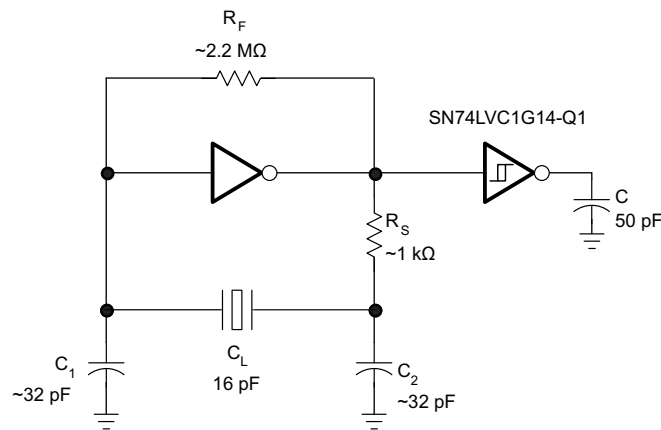
Copyright © 2017, Texas Instruments Incorporated

Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   – Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC} .
2. Recommended Output Conditions
   – Load currents should not exceed (I_O max) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   – Outputs should not be pulled above V_{CC}.

Typical Application (continued)
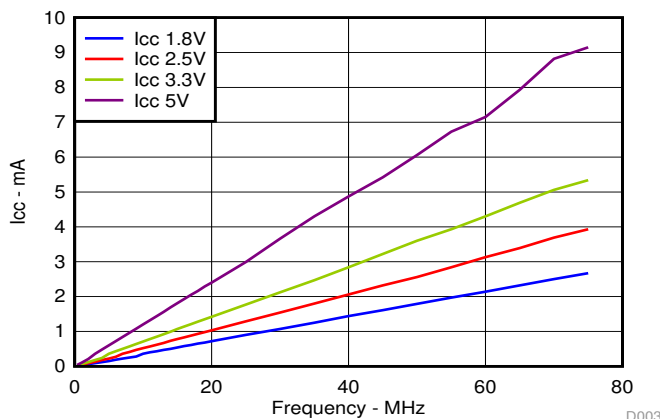
9.2.3 Application Curve

Figure 6. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input terminals should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.
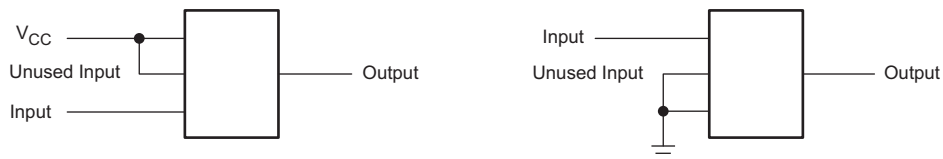
11.2 Layout Example

Figure 7. Layout Schematic

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G14QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJM	Samples
SN74LVC1G14QDRYRQ1	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

10-Dec-2020

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G14QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G14QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G14QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G14QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

2,15
1,85

5   4

1,40
1,10

2,40
1,80

Pin 1
Index Area

1   2   3

0,65

5X 0,30
0,15

1,30

⊕ | 0,10 Ⓜ

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
0,80

⌒ | 0,10

Seating Plane

0,10
0,00

4093553−3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AA.

DCK (R−PDSO−G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

2,2

6x0,35

0,85

2,2

2x0,65

2x1,30

2x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−2/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS
INSTRUMENTS

B | 1.05 / 0.95 | A

PIN 1 INDEX AREA

1.5 / 1.4

0.55 MAX

C

SEATING PLANE

0.05 / 0.00

0.08 C

3X 0.6

SYMM

(0.05) TYP

(0.127) TYP

3

4

4X 0.5

SYMM

2X 1

1

6

6X 0.25 / 0.15

PIN 1 ID (OPTIONAL)

0.1 (M) C A(S) B(S)
0.05 (M) C

6X 0.35 / 0.25

4222207/B   02/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM
℄

6X (0.3)

1

6X (0.2)

6

SYMM
℄

4X (0.5)

3

4

(R0.05) TYP

(0.6)
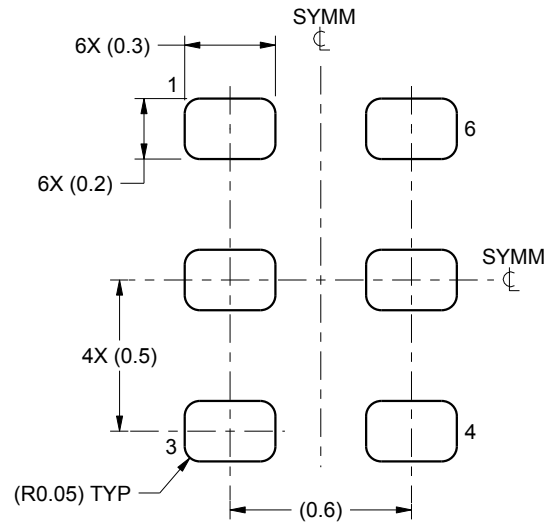
LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X

0.05 MAX
ALL AROUND

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED
(PREFERRED)**
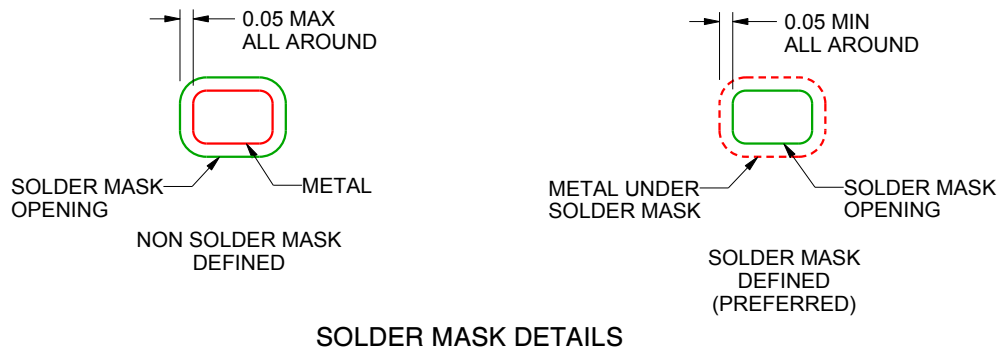
SOLDER MASK DETAILS

4222207/B   02/2016

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

SYMM

6X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)
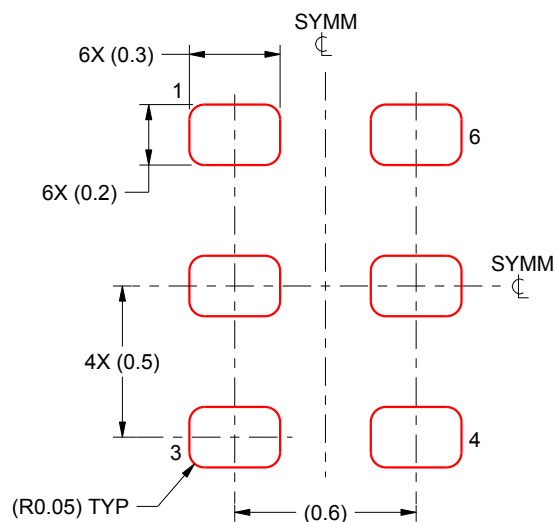
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B   02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.