RAD-TOLERANT CLASS V, HEX SCHMITT-TRIGGER INVERTER

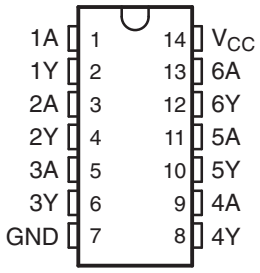
Check for Samples: SN54AC14-SP

FEATURES

- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max tpd of 9.5 ns at 5 V**
- **Rad-Tolerant: 50 kRad(Si) TID** (1)
  - **TID Dose Rate < 2mRad/sec**
- **QML-V Qualified, SMD 5962-87624**

(1) Radiation tolerance is a typical value based upon initial device qualification. Radiation Lot Acceptance Testing is available - contact factory for details.

J OR W PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. Because of the Schmitt action, they have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

ORDERING INFORMATION(1)

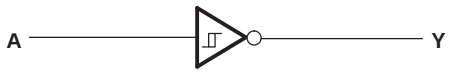
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – J	Tube	5962-8762402VCA	5962-8762402VCA
	CFP – W	Tube	5962-8762402VDA	5962-8762402VDA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE
(EACH INVERTER)

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 or V_I > V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O < 0		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		–12	mA
		V_{CC} = 4.5 V		–24	
		V_{CC} = 5.5 V		–24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
T_A	Operating free-air temperature		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C		T_A = –55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
V_{T+} Positive-going threshold		3 V		2.3		2.3	V
		4.5 V		3.2		3.2	
		5.5 V		3.9		3.9	
$V_{T–}$ Negative-going threshold		3 V	0.5		0.5		V
		4.5 V	0.9		0.9		
		5.5 V	1.1		1.1		
ΔV_T Hysteresis ($V_{T+} – V_{T-}$)		3 V	0.3	1.3	0.3	1.3	V
		4.5 V	0.4	1.4	0.4	1.4	
		5.5 V	0.5	1.6	0.5	1.6	
V_{OH}	I_{OH} = –50 µA	3 V	2.9		2.9		V
		4.5 V	4.4		4.4		
		5.5 V	5.4		5.4		
	I_{OH} = –12 mA	3 V	2.56		2.4		
	I_{OH} = –24 mA	4.5 V	3.86		3.7		
		5.5 V	4.86		4.7		
	I_{OH} = –50 mA[1]	5.5 V			3.85		
V_{OL}	I_{OL} = 50 µA	3 V		0.1		0.1	V
		4.5 V		0.1		0.1	
		5.5 V		0.1		0.1	
	I_{OL} = 12 mA	3 V		0.5		0.5	
	I_{OL} = 24 mA	4.5 V		0.5		0.5	
		5.5 V		0.5		0.5	
	I_{OL} = 50 mA[1]	5.5 V				1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V		±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V		4		80	µA
I_{CCt}	$V_I = V_{CC}/2$ V One input at V_I, other input at V_{CC} or GND[2]	5.5 V		7.5		7.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		8		8	pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
(2) V_I is incremented in 0.1-V steps to 3.7 V.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = –55°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6	13.5	1	16	ns
t_{PHL}			1.5	6	11.5	1	14	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = –55°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5	10	1.5	12	ns
t_{PHL}			1.5	5	8.5	1.5	10	

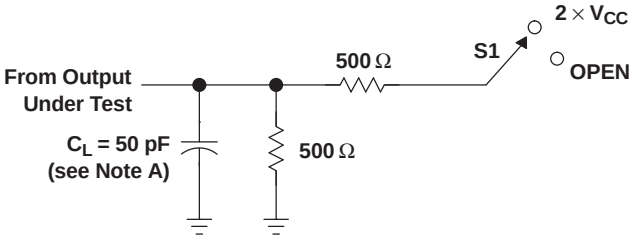
OPERATING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

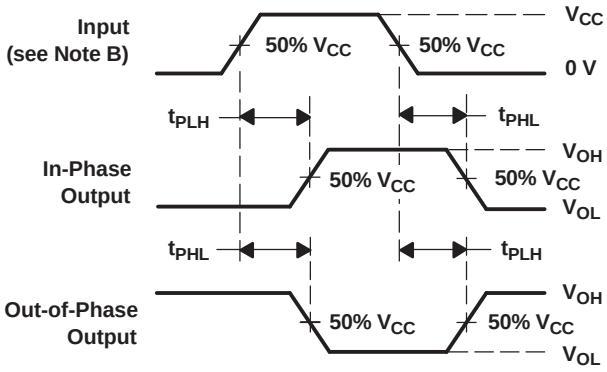
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	25	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open



LOAD CIRCUIT



VOLTAGE WAVEFORMS

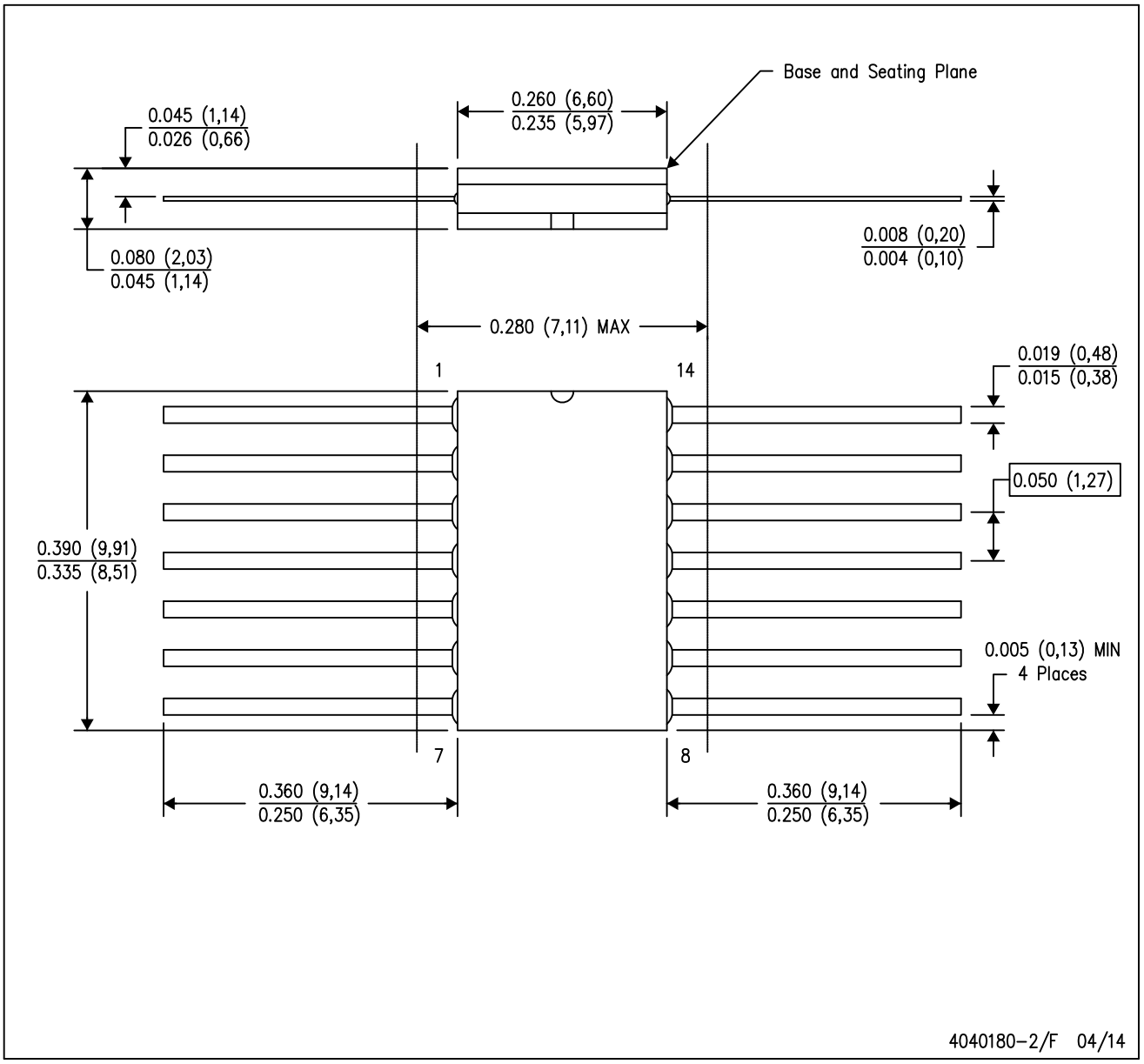
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision A (March, 2010) to Revision B	Page
• Added I_{CCt} parameter to Electrical Characteristics	3

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

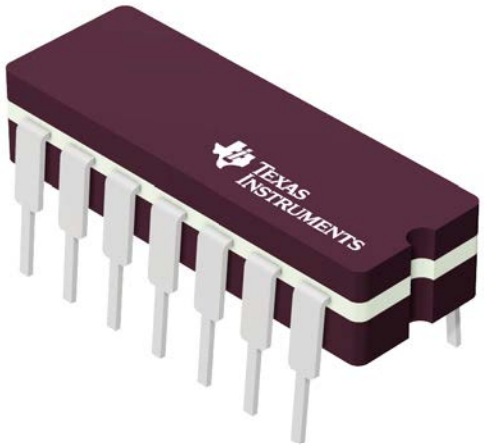


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

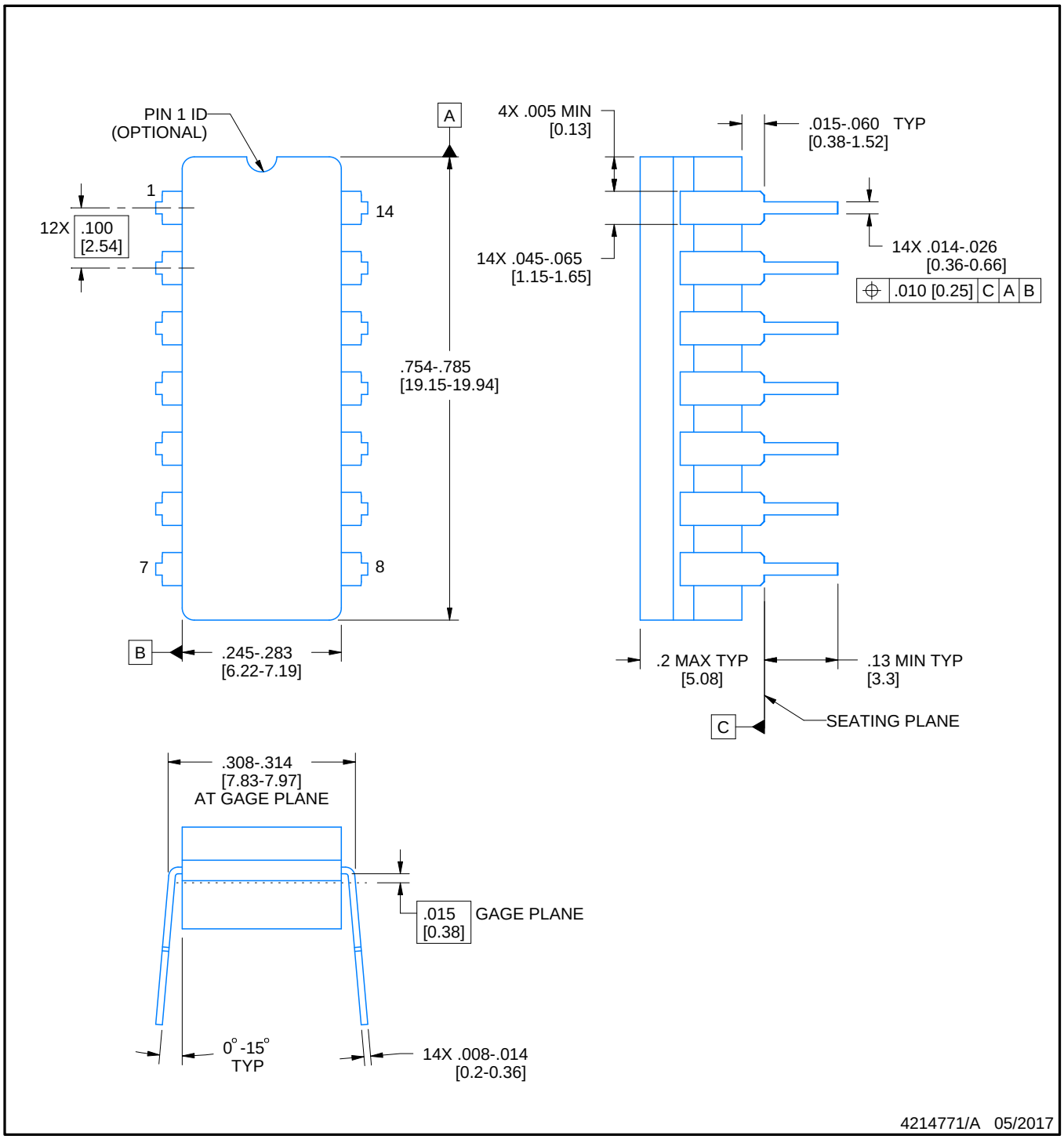
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

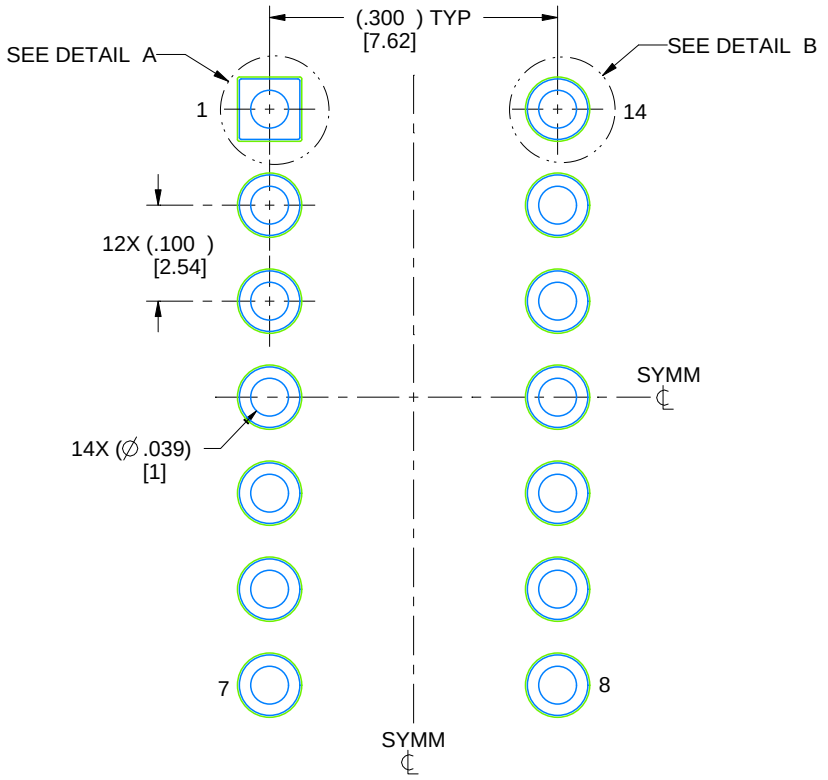
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

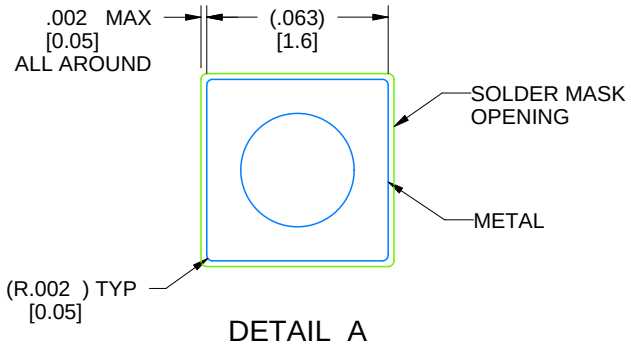
J0014A

CDIP - 5.08 mm max height

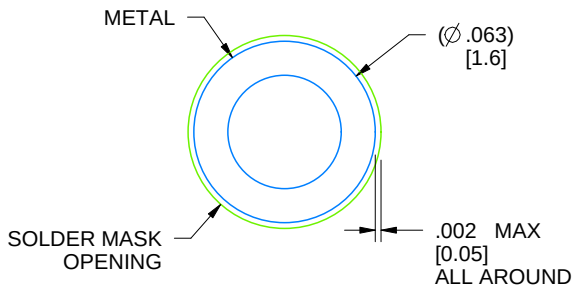
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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