

具有可配置电压转换、三态输出和总线保持输入的 SN74AXCH1T45 1 位双电源总线收发器

1 特性

- 完全可配置的双电源轨设计可允许各个端口在 0.65V 至 3.6V 的电源电压范围内运行
- 工作温度: -40°C 至 $+125^{\circ}\text{C}$
- 无干扰电源定序
- 总线保持数据输入消除了对外部上拉或下拉电阻的需求
- 最大静态电流 ($I_{\text{CCA}} + I_{\text{CCB}}$) 为 $8\mu\text{A}$ (最高 85°C) 和 $14\mu\text{A}$ (最高 125°C)
- 从 1.8V 转换到 3.3V 时, 支持高达 500Mbps 的转换速率
- V_{CC} 隔离特性
 - 如果任何一个 V_{CC} 输入低于 100mV, 则所有 I/O 输出均禁用且处于高阻抗状态
- I_{off} 支持局部关断模式运行
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
 - 8000V 人体放电模型
 - 1000V 充电器件模型

2 应用

- 个人电子产品
- 企业与通信
- 无线基础设施
- 楼宇自动化
- 电子销售终端
- 企业级固态硬盘

3 说明

SN74AXCH1T45 是一款采用两个独立可配置电源轨的单比特位同相总线收发器。 V_{CCA} 和 V_{CCB} 电源电压低至 0.65V 时, 该器件可正常工作。A 端口用于跟踪 V_{CCA} , 该端口可支持 0.65V 至 3.6V 范围内的任何电源电压。B 端口用于跟踪 V_{CCB} , 该端口也可支持 0.65V 至 3.6V 范围内的任何电源电压。此外, SN74AXCH1T45 还与单电源系统兼容。

DIR 引脚决定信号传播的方向。DIR 引脚配置为高电平时, 信号转换由端口 A 流向端口 B。DIR 配置为低电平时, 则由端口 B 流向端口 A。DIR 引脚以 V_{CCA} 为基准, 这意味着它的逻辑高电平和逻辑低电平阈值跟踪 V_{CCA} 电压。

有源总线保持电路会将未使用或未驱动的输入保持在有效逻辑状态。不建议在总线保持电路上使用上拉或下拉电阻器。如果 V_{CCA} 或 V_{CCB} 连上电源, 则总线保持电路分别在 A 端口或 B 端口上始终保持工作状态, 与方向控制引脚的状态无关。

该器件完全适用于使用 I_{off} 电流的局部掉电应用。当器件掉电时, I_{off} 保护电路可确保不从输入/输出或偏置到特定电压的快速 I/O 获取或向其提供多余电流。

V_{CC} 隔离特性可确保当 V_{CCA} 或 V_{CCB} 低于 100mV 时, I/O 端口均禁用其输出并进入高阻抗状态。

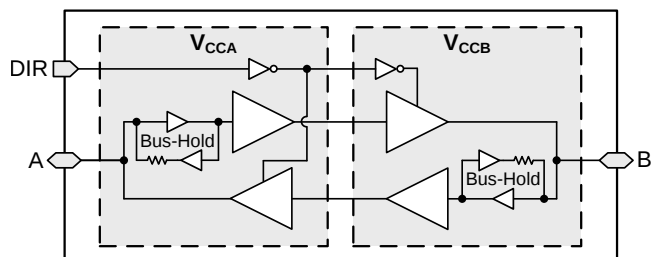
无干扰电源定序使电源轨能以任何顺序打开或关断, 从而提供强大的电源定序性能。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN74AXCH1T45DBV	SOT-23 (6)	2.90mm × 1.60mm
SN74AXCH1T45DCK	SC70 (6)	2.00mm × 1.25mm
SN74AXCH1T45DTQ	X2SON (6)	1.00mm × 0.80mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

功能方框图



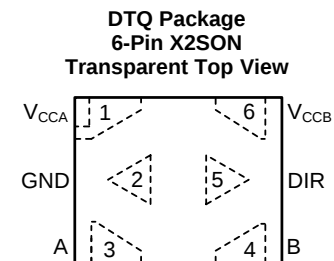
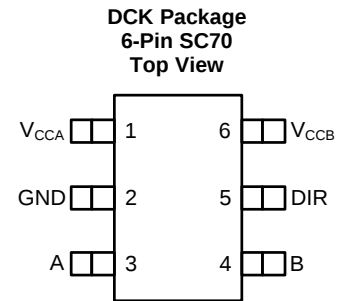
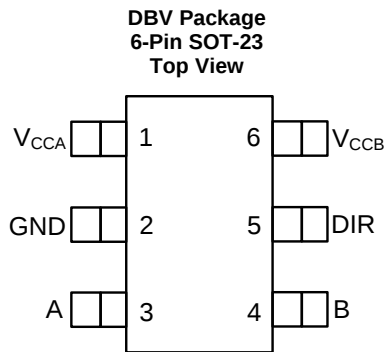
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4 修订历史记录

Changes from Original (December 2018) to Revision A	Page
• 已添加 将 DBV 和 DTQ 封装选项添加到器件信息表	1
• 更新了 修订历史记录部分	1
• Added pinout drawings for DBV and DTQ packages	3

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V _{CCA}	—	A-port supply voltage. 0.65V ≤ V _{CCA} ≤ 3.6 V
2	GND	—	Ground
3	A	I/O	Input/output A. This pin is referenced to V _{CCA} .
4	B	I/O	Input/output B. This pin is referenced to V _{CCB} .
5	DIR	I	Direction control signal. See for functionality
6	V _{CCB}	—	B-port supply voltage. 0.65V ≤ V _{CCB} ≤ 3.6 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CCA}	Supply voltage A		–0.5	4.2	V
V _{CCB}	Supply voltage B		–0.5	4.2	V
V _I	Input Voltage ⁽²⁾	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V _O	Voltage applied to any output in the high or low state ^{(2) (3)}	A Port	–0.5	V _{CCA} + 0.2	V
		B Port	–0.5	V _{CCB} + 0.2	
I _{IK}	Input clamp current	V _I < 0	–50		mA
I _{OK}	Output clamp current	V _O < 0	–50		mA
I _O	Continuous output current		–50	50	mA
	Continuous current through V _{CC} or GND		–100	100	mA
T _j	Junction Temperature			150	°C
T _{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

				MIN	MAX	UNIT
V _{CCA}	Supply voltage A			0.65	3.6	V
V _{CCB}	Supply voltage B			0.65	3.6	V
V _{IH}	High-level input voltage	Data Inputs	V _{CCI} = 0.65 V - 0.75 V	V _{CCI} × 0.70	V	
			V _{CCI} = 0.76 V - 1 V	V _{CCI} × 0.70		
			V _{CCI} = 1.1 V - 1.95 V	V _{CCI} × 0.65		
			V _{CCI} = 2.3 V - 2.7 V	1.6		
			V _{CCI} = 3 V - 3.6 V	2		
		Control Input (DIR) Referenced to V _{CCA}	V _{CCA} = 0.65 V - 0.75 V	V _{CCA} × 0.70		
			V _{CCA} = 0.76 V - 1 V	V _{CCA} × 0.70		
			V _{CCA} = 1.1 V - 1.95 V	V _{CCA} × 0.65		
			V _{CCA} = 2.3 V - 2.7 V	1.6		
			V _{CCA} = 3 V - 3.6 V	2		
V _{IL}	Low-level input voltage	Data Inputs	V _{CCI} = 0.65 V - 0.75 V	V _{CCI} × 0.30	V	
			V _{CCI} = 0.76 V - 1 V	V _{CCI} × 0.30		
			V _{CCI} = 1.1 V - 1.95 V	V _{CCI} × 0.35		
			V _{CCI} = 2.3 V - 2.7 V	0.7		
			V _{CCI} = 3 V - 3.6 V	0.8		
		Control Input (DIR) Referenced to V _{CCA}	V _{CCA} = 0.65 V - 0.75 V	V _{CCA} × 0.30		
			V _{CCA} = 0.76 V - 1 V	V _{CCA} × 0.30		
			V _{CCA} = 1.1 V - 1.95 V	V _{CCA} × 0.35		
			V _{CCA} = 2.3 V - 2.7 V	0.7		
			V _{CCA} = 3 V - 3.6 V	0.8		
V _I	Input voltage ⁽³⁾			0	3.6	V
V _O	Output voltage	Active State	0	V _{CCO}	V	
		Tri-State	0	3.6		
Δt/Δv	Input transition rate				100	ns/V
T _A	Operating free-air temperature			−40	125	°C

(1) V_{CCI} is the VCC associated with the input port.

(2) V_{CCO} is the VCC associated with the output port.

(3) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AXCH1T45			UNIT
		DBV (SOT-23)	DCK (SC70)	DTQ (X2SON)	
		6 PINS	6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	214.0	223.9	327.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	151.8	150.9	194.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	93.6	75.3	248.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	78.1	58.2	24.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	93.4	75.0	247.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)						UNIT
						-40°C to 85°C			-40°C to 125°C			
						MIN	TYP ⁽³⁾	MAX	MIN	TYP	MAX	
V _{OH}	High-level output voltage	V _I = V _{IH}	I _{OH} = -100 μA	0.7 V - 3.6 V	0.7 V - 3.6 V	V _{CCO} − 0.1			V _{CCO} − 0.1			V
			I _{OH} = -50 μA	0.65 V	0.65 V	0.55			0.55			
			I _{OH} = -200 μA	0.76 V	0.76 V	0.58			0.58			
			I _{OH} = -500 μA	0.85 V	0.85 V	0.65			0.65			
			I _{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I _{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I _{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I _{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I _{OH} = -12 mA	3 V	3 V	2.3			2.3			
V _{OL}	Low-level output voltage	V _I = V _{IL}	I _{OL} = 100 μA	0.7 V - 3.6 V	0.7 V - 3.6 V	0.1			0.1			V
			I _{OL} = 50 μA	0.65 V	0.65 V	0.1			0.1			
			I _{OL} = 200 μA	0.76 V	0.76 V	0.18			0.18			
			I _{OL} = 500 μA	0.85 V	0.85 V	0.2			0.2			
			I _{OL} = 3 mA	1.1 V	1.1 V	0.25			0.25			
			I _{OL} = 6 mA	1.4 V	1.4 V	0.35			0.35			
			I _{OL} = 8 mA	1.65 V	1.65 V	0.45			0.45			
			I _{OL} = 9 mA	2.3 V	2.3 V	0.55			0.55			
			I _{OL} = 12 mA	3 V	3 V	0.7			0.7			
I _{BHL}	Bus-hold low sustaining current ⁽⁴⁾	V _I = 0.20 V	0.65 V	0.65 V	4			4			μA	
		V _I = 0.23 V	0.76 V	0.76 V	8			7				
		V _I = 0.26 V	0.85 V	0.85 V	10			10				
		V _I = 0.39 V	1.1 V	1.1 V	20			20				
		V _I = 0.49 V	1.4 V	1.4 V	40			30				
		V _I = 0.58 V	1.65 V	1.65 V	55			45				
		V _I = 0.7 V	2.3 V	2.3 V	90			80				
		V _I = 0.8 V	3 V	3 V	145			135				
I _{BHH}	Bus-hold high sustaining current ⁽⁵⁾	V _I = 0.45 V	0.65 V	0.65 V	−4			−4			μA	
		V _I = 0.53 V	0.76 V	0.76 V	−8			−7				
		V _I = 0.59 V	0.85 V	0.85 V	−10			−10				
		V _I = 0.71 V	1.1 V	1.1 V	−20			−20				
		V _I = 0.91 V	1.4 V	1.4 V	−40			−30				
		V _I = 1.07 V	1.65 V	1.65 V	−55			−45				
		V _I = 1.6 V	2.3 V	2.3 V	−90			−80				
		V _I = 2.0 V	3 V	3 V	−145			−135				

 (1) V_{CCI} is the VCC associated with the input port.

 (2) V_{CCO} is the VCC associated with the output port.

(3) All typical data is taken at 25°C.

 (4) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}(MAX). I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL}(MAX).

 (5) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}(MIN). I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH}(MIN).

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)						UNIT
						-40°C to 85°C			-40°C to 125°C			
						MIN	TYP ⁽³⁾	MAX	MIN	TYP	MAX	
I _{BHLO}	Bus-hold low overdrive current ⁽⁶⁾	V _I = 0 to V _{CC}		0.75 V	0.75 V	40		40		μA		
				0.84 V	0.84 V	50		50				
				0.95 V	0.95 V	65		65				
				1.3 V	1.3 V	105		105				
				1.6 V	1.6 V	150		150				
				1.95 V	1.95 V	205		205				
				2.7 V	2.7 V	335		335				
				3.6V	3.6V	480		480				
I _{BHHO}	Bus-hold high overdrive current ⁽⁷⁾	V _I = 0 to V _{CC}		0.75 V	0.75 V	−40		−40		μA		
				0.84 V	0.84 V	−50		−50				
				0.95 V	0.95 V	−65		−65				
				1.3 V	1.3 V	−105		−105				
				1.6 V	1.6 V	−150		−150				
				1.95 V	1.95 V	−205		−205				
				2.7 V	2.7 V	−335		−335				
				3.6V	3.6V	−480		−480				
I _I	Input leakage current	Control input (DIR): V _I = V _{CCA} or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	−0.5	0.5	−1	1	μA		
		A or B Port: V _i = V _{CC1} or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	−4	4	−8	8			
I _{off}	Partial power down current	A or B Port: V _i or V _o = 0 V - 3.6 V		0 V	0 V - 3.6 V	−8	8	−12	12	μA		
				0 V - 3.6 V	0 V	−8	8	−12	12			
I _{CCA}	V _{CCA} supply current	V _I = V _{CC1} or GND	I _O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V	6		9		μA		
				0 V	3.6 V	−2		−8				
				3.6 V	0 V	2		8				
I _{CCB}	V _{CCB} supply current	V _I = V _{CC1} or GND	I _O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V	6		9		μA		
				0 V	3.6 V	2		8				
				3.6 V	0 V	−2		−8				
I _{CCA} + I _{CCB}	Combined supply current	V _I = V _{CC1} or GND	I _O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V	8		14		μA		
C _i	Control input capacitance	V _I = 3.3 V or GND		3.3 V	3.3 V	4.3		4.3		pF		
C _{iO}	Data I/O capacitance, A Port	V _O = 1.65V DC +1 MHz -16 dBm sine wave		3.3 V	0 V	7.4		7.4		pF		
C _{iO}	Data I/O capacitance, B Port	V _O = 1.65V DC +1 MHz -16 dBm sine wave		0 V	3.3 V	7.4		7.4		pF		

(6) An external driver must source at least I_{BHLO} to switch this node from low to high.

(7) An external driver must sink at least I_{BHHO} to switch this node from high to low.

Table 1. Switching Characteristics, $V_{CCA} = 0.7\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} Propagation delay	A	B	-40°C to 85°C	0.5	181	0.5	119	0.5	85	0.5	51	0.5	49	0.5	52	0.5	65	0.5	152	ns
			-40°C to 125°C	0.5	181	0.5	119	0.5	85	0.5	51	0.5	49	0.5	52	0.5	65	0.5	152	
	B	A	-40°C to 85°C	0.5	181	0.5	162	0.5	136	0.5	96	0.5	91	0.5	89	0.5	88	0.5	88	
			-40°C to 125°C	0.5	181	0.5	162	0.5	136	0.5	96	0.5	91	0.5	89	0.5	88	0.5	88	
t _{dis} Disable time	DIR	A	-40°C to 85°C	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	ns
			-40°C to 125°C	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	
	DIR	B	-40°C to 85°C	0.5	170	0.5	127	0.5	102	0.5	48	0.5	42	0.5	46	0.5	58	0.5	108	
			-40°C to 125°C	0.5	170	0.5	127	0.5	102	0.5	48	0.5	42	0.5	46	0.5	58	0.5	108	
t _{en} Enable time	DIR	A	-40°C to 85°C	0.5	343	0.5	278	0.5	231	0.5	141	0.5	132	0.5	134	0.5	144	0.5	193	ns
			-40°C to 125°C	0.5	343	0.5	278	0.5	231	0.5	141	0.5	132	0.5	134	0.5	144	0.5	193	
	DIR	B	-40°C to 85°C	0.5	326	0.5	257	0.5	222	0.5	194	0.5	191	0.5	191	0.5	197	0.5	277	
			-40°C to 125°C	0.5	326	0.5	257	0.5	222	0.5	194	0.5	191	0.5	191	0.5	197	0.5	277	

Table 2. Switching Characteristics, $V_{CCA} = 0.8\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} Propagation delay	A	B	-40°C to 85°C	0.5	162	0.5	98	0.5	65	0.5	33	0.5	28	0.5	26	0.5	27	0.5	37	ns
			-40°C to 125°C	0.5	162	0.5	98	0.5	65	0.5	33	0.5	28	0.5	26	0.5	27	0.5	37	
	B	A	-40°C to 85°C	0.5	119	0.5	98	0.5	81	0.5	54	0.5	45	0.5	44	0.5	43	0.5	42	
			-40°C to 125°C	0.5	119	0.5	98	0.5	81	0.5	54	0.5	45	0.5	44	0.5	43	0.5	42	
t _{dis} Disable time	DIR	A	-40°C to 85°C	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	ns
			-40°C to 125°C	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	
	DIR	B	-40°C to 85°C	0.5	160	0.5	117	0.5	90	0.5	39	0.5	31	0.5	29	0.5	29	0.5	37	
			-40°C to 125°C	0.5	160	0.5	117	0.5	90	0.5	39	0.5	31	0.5	29	0.5	29	0.5	37	
t _{en} Enable time	DIR	A	-40°C to 85°C	0.5	268	0.5	205	0.5	165	0.5	90	0.5	74	0.5	71	0.5	70	0.5	77	ns
			-40°C to 125°C	0.5	268	0.5	205	0.5	165	0.5	90	0.5	74	0.5	71	0.5	70	0.5	77	
	DIR	B	-40°C to 85°C	0.5	257	0.5	194	0.5	161	0.5	130	0.5	125	0.5	126	0.5	125	0.5	132	
			-40°C to 125°C	0.5	257	0.5	194	0.5	161	0.5	130	0.5	125	0.5	126	0.5	125	0.5	132	

Table 3. Switching Characteristics, $V_{CCA} = 0.9\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} Propagation delay	A	B	-40°C to 85°C	0.5	135	0.5	81	0.5	54	0.5	24	0.5	18	0.5	17	0.5	15	0.5	18	ns
			-40°C to 125°C	0.5	135	0.5	81	0.5	54	0.5	24	0.5	18	0.5	17	0.5	15	0.5	18	
	B	A	-40°C to 85°C	0.5	86	0.5	65	0.5	54	0.5	41	0.5	30	0.5	26	0.5	23	0.5	23	
			-40°C to 125°C	0.5	86	0.5	65	0.5	54	0.5	41	0.5	30	0.5	26	0.5	23	0.5	23	
t _{dis} Disable time	DIR	A	-40°C to 85°C	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	ns
			-40°C to 125°C	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	
	DIR	B	-40°C to 85°C	0.5	154	0.5	111	0.5	85	0.5	34	0.5	27	0.5	25	0.5	21	0.5	23	
			-40°C to 125°C	0.5	154	0.5	111	0.5	85	0.5	34	0.5	27	0.5	25	0.5	21	0.5	23	
t _{en} Enable time	DIR	A	-40°C to 85°C	0.5	227	0.5	166	0.5	131	0.5	71	0.5	53	0.5	48	0.5	42	0.5	44	ns
			-40°C to 125°C	0.5	227	0.5	166	0.5	131	0.5	71	0.5	53	0.5	48	0.5	42	0.5	44	
	DIR	B	-40°C to 85°C	0.5	206	0.5	152	0.5	125	0.5	96	0.5	91	0.5	89	0.5	89	0.5	92	
			-40°C to 125°C	0.5	206	0.5	152	0.5	125	0.5	96	0.5	91	0.5	89	0.5	89	0.5	92	

Table 4. Switching Characteristics, $V_{CCA} = 1.2\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} Propagation delay	A	B	-40°C to 85°C	0.5	95	0.5	54	0.5	41	0.5	16	0.5	11	0.5	9	0.5	8	0.5	8	ns
			-40°C to 125°C	0.5	95	0.5	54	0.5	41	0.5	16	0.5	11	0.5	9	0.5	8	0.5	8	
	B	A	-40°C to 85°C	0.5	51	0.5	33	0.5	24	0.5	16	0.5	13	0.5	11	0.5	8	0.5	8	
			-40°C to 125°C	0.5	51	0.5	33	0.5	24	0.5	16	0.5	13	0.5	11	0.5	8	0.5	8	
t _{dis} Disable time	DIR	A	-40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	ns
			-40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	
	DIR	B	-40°C to 85°C	0.5	148	0.5	105	0.5	78	0.5	30	0.5	23	0.5	20	0.5	16	0.5	16	
			-40°C to 125°C	0.5	148	0.5	105	0.5	78	0.5	30	0.5	23	0.5	20	0.5	16	0.5	16	
t _{en} Enable time	DIR	A	-40°C to 85°C	0.5	191	0.5	129	0.5	96	0.5	43	0.5	34	0.5	30	0.5	23	0.5	22	ns
			-40°C to 125°C	0.5	191	0.5	129	0.5	96	0.5	43	0.5	34	0.5	30	0.5	23	0.5	22	
	DIR	B	-40°C to 85°C	0.5	116	0.5	75	0.5	61	0.5	41	0.5	37	0.5	36	0.5	35	0.5	35	
			-40°C to 125°C	0.5	116	0.5	75	0.5	61	0.5	41	0.5	37	0.5	36	0.5	35	0.5	35	

Table 5. Switching Characteristics, $V_{CCA} = 1.5\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} Propagation delay	A	B	-40°C to 85°C	0.5	91	0.5	45	0.5	30	0.5	13	0.5	9	0.5	8	0.5	6	0.5	6	ns
			-40°C to 125°C	0.5	91	0.5	45	0.5	30	0.5	13	0.5	9	0.5	8	0.5	6	0.5	6	
	B	A	-40°C to 85°C	0.5	49	0.5	28	0.5	18	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5	
			-40°C to 125°C	0.5	49	0.5	28	0.5	18	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis} Disable time	DIR	A	-40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	ns
			-40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	
	DIR	B	-40°C to 85°C	0.5	146	0.5	103	0.5	76	0.5	28	0.5	21	0.5	19	0.5	15	0.5	14	
			-40°C to 125°C	0.5	146	0.5	103	0.5	76	0.5	28	0.5	21	0.5	19	0.5	15	0.5	14	
t_{en} Enable time	DIR	A	-40°C to 85°C	0.5	186	0.5	124	0.5	89	0.5	38	0.5	29	0.5	26	0.5	20	0.5	18	ns
			-40°C to 125°C	0.5	186	0.5	124	0.5	89	0.5	38	0.5	29	0.5	26	0.5	20	0.5	18	
	DIR	B	-40°C to 85°C	0.5	104	0.5	58	0.5	43	0.5	31	0.5	28	0.5	27	0.5	25	0.5	25	
			-40°C to 125°C	0.5	104	0.5	58	0.5	43	0.5	31	0.5	28	0.5	27	0.5	25	0.5	25	

Table 6. Switching Characteristics, $V_{CCA} = 1.8\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} Propagation delay	A	B	-40°C to 85°C	0.5	89	0.5	44	0.5	26	0.5	11	0.5	8	0.5	7	0.5	6	0.5	5	ns
			-40°C to 125°C	0.5	89	0.5	44	0.5	26	0.5	11	0.5	8	0.5	7	0.5	6	0.5	5	
	B	A	-40°C to 85°C	0.5	52	0.5	26	0.5	17	0.5	9	0.5	8	0.5	7	0.5	6	0.5	5	
			-40°C to 125°C	0.5	52	0.5	26	0.5	17	0.5	9	0.5	8	0.5	7	0.5	6	0.5	5	
t_{dis} Disable time	DIR	A	-40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	ns
			-40°C to 125°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	
	DIR	B	-40°C to 85°C	0.5	147	0.5	103	0.5	76	0.5	27	0.5	20	0.5	18	0.5	14	0.5	13	
			-40°C to 125°C	0.5	147	0.5	103	0.5	76	0.5	27	0.5	20	0.5	18	0.5	14	0.5	13	
t_{en} Enable time	DIR	A	-40°C to 85°C	0.5	185	0.5	122	0.5	86	0.5	35	0.5	27	0.5	24	0.5	19	0.5	17	ns
			-40°C to 125°C	0.5	185	0.5	122	0.5	86	0.5	35	0.5	27	0.5	24	0.5	19	0.5	17	
	DIR	B	-40°C to 85°C	0.5	100	0.5	54	0.5	37	0.5	27	0.5	25	0.5	24	0.5	22	0.5	22	
			-40°C to 125°C	0.5	100	0.5	54	0.5	37	0.5	27	0.5	25	0.5	24	0.5	22	0.5	22	

Table 7. Switching Characteristics, $V_{CCA} = 2.5\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} Propagation delay	A	B	-40°C to 85°C	0.5	88	0.5	42	0.5	23	0.5	8	0.5	6	0.5	6	0.5	5	0.5	5	ns
			-40°C to 125°C	0.5	88	0.5	42	0.5	23	0.5	8	0.5	6	0.5	6	0.5	5	0.5	5	
	B	A	-40°C to 85°C	0.5	65	0.5	27	0.5	15	0.5	8	0.5	6	0.5	6	0.5	5	0.5	4	
			-40°C to 125°C	0.5	65	0.5	27	0.5	15	0.5	8	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis} Disable time	DIR	A	-40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns
			-40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
	DIR	B	-40°C to 85°C	0.5	146	0.5	102	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
			-40°C to 125°C	0.5	146	0.5	102	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
t_{en} Enable time	DIR	A	-40°C to 85°C	0.5	191	0.5	122	0.5	85	0.5	33	0.5	25	0.5	22	0.5	17	0.5	16	ns
			-40°C to 125°C	0.5	191	0.5	122	0.5	85	0.5	33	0.5	25	0.5	22	0.5	17	0.5	16	
	DIR	B	-40°C to 85°C	0.5	95	0.5	50	0.5	31	0.5	20	0.5	18	0.5	17	0.5	17	0.5	17	
			-40°C to 125°C	0.5	95	0.5	50	0.5	31	0.5	20	0.5	18	0.5	17	0.5	17	0.5	17	

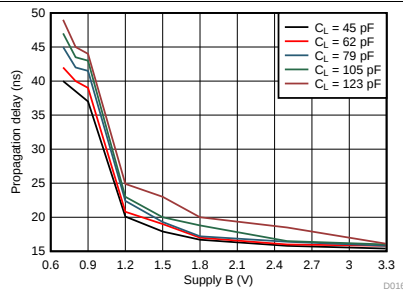
Table 8. Switching Characteristics, $V_{CCA} = 3.3\text{ V}$

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V _{CCB})																UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} Propagation delay	A	B	-40°C to 85°C	0.5	87	0.5	42	0.5	23	0.5	8	0.5	5	0.5	5	0.5	4	0.5	4	ns
			-40°C to 125°C	0.5	87	0.5	42	0.5	23	0.5	8	0.5	5	0.5	5	0.5	4	0.5	4	
	B	A	-40°C to 85°C	0.5	154	0.5	37	0.5	18	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	
			-40°C to 125°C	0.5	154	0.5	37	0.5	18	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis} Disable time	DIR	A	-40°C to 85°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	ns
			-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
	DIR	B	-40°C to 85°C	0.5	147	0.5	102	0.5	75	0.5	26	0.5	19	0.5	17	0.5	13	0.5	12	
			-40°C to 125°C	0.5	147	0.5	102	0.5	75	0.5	26	0.5	19	0.5	17	0.5	13	0.5	12	
t_{en} Enable time	DIR	A	-40°C to 85°C	0.5	275	0.5	129	0.5	88	0.5	34	0.5	24	0.5	21	0.5	17	0.5	16	ns
			-40°C to 125°C	0.5	275	0.5	129	0.5	88	0.5	34	0.5	24	0.5	21	0.5	17	0.5	16	
	DIR	B	-40°C to 85°C	0.5	94	0.5	49	0.5	30	0.5	18	0.5	16	0.5	16	0.5	15	0.5	15	
			-40°C to 125°C	0.5	94	0.5	49	0.5	30	0.5	18	0.5	16	0.5	16	0.5	15	0.5	15	

6.6 Operating Characteristics: $T_A = 25^\circ\text{C}$

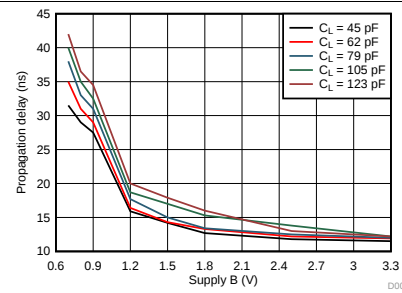
PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.0		pF
			0.8 V	0.8 V		2.0		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		1.9		
			1.8 V	1.8 V		2.0		
			2.5 V	2.5 V		2.4		
			3.3 V	3.3 V		3.0		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12		pF
			0.8 V	0.8 V		12		
			0.9 V	0.9 V		12		
			1.2 V	1.2 V		12		
			1.5 V	1.5 V		13		
			1.8 V	1.8 V		13		
			2.5 V	2.5 V		17		
			3.3 V	3.3 V		21		
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12		pF
			0.8 V	0.8 V		12		
			0.9 V	0.9 V		12		
			1.2 V	1.2 V		12		
			1.5 V	1.5 V		13		
			1.8 V	1.8 V		13		
			2.5 V	2.5 V		17		
			3.3 V	3.3 V		21		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.1		pF
			0.8 V	0.8 V		2.2		
			0.9 V	0.9 V		2.2		
			1.2 V	1.2 V		2.2		
			1.5 V	1.5 V		2.3		
			1.8 V	1.8 V		2.3		
			2.5 V	2.5 V		2.6		
			3.3 V	3.3 V		3.3		

6.7 Typical Characteristics



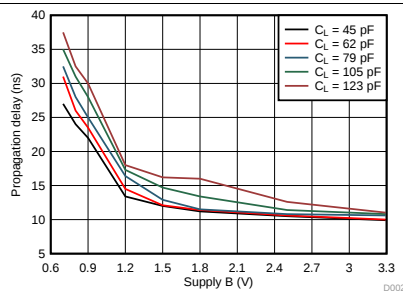
$T_A = 25^\circ\text{C}$ $V_{CCA} = 0.7\text{ V}$

图 1. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



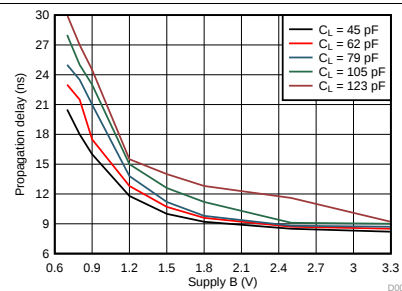
$T_A = 25^\circ\text{C}$ $V_{CCA} = 0.8\text{ V}$

图 2. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



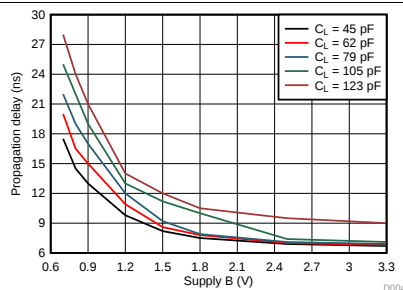
$T_A = 25^\circ\text{C}$ $V_{CCA} = 0.9\text{ V}$

图 3. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



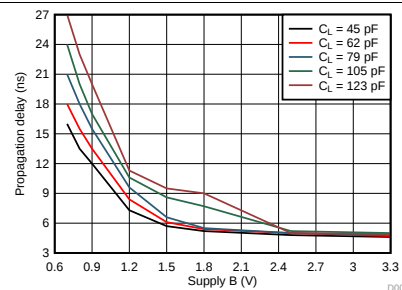
$T_A = 25^\circ\text{C}$ $V_{CCA} = 1.2\text{ V}$

图 4. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



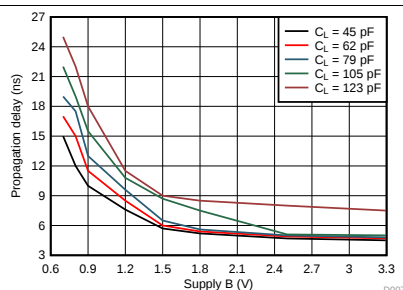
$T_A = 25^\circ\text{C}$ $V_{CCA} = 1.5\text{ V}$

图 5. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



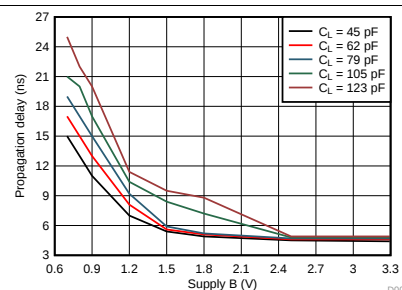
$T_A = 25^\circ\text{C}$ $V_{CCA} = 1.8\text{ V}$

图 6. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



$T_A = 25^\circ\text{C}$ $V_{CCA} = 3.3\text{ V}$

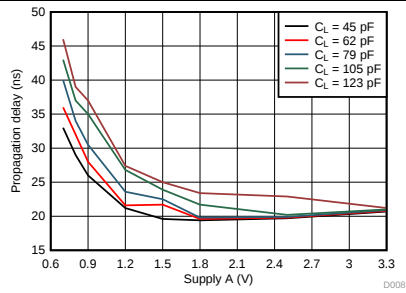
图 7. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



$T_A = 25^\circ\text{C}$ $V_{CCA} = 2.5\text{ V}$

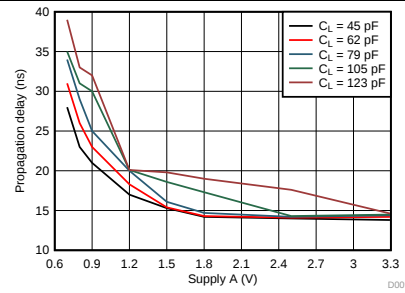
图 8. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance

Typical Characteristics (接下页)



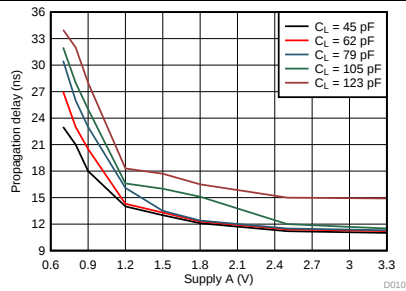
$T_A = 25^\circ\text{C}$ $V_{CCA} = 0.7\text{ V}$

图 9. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



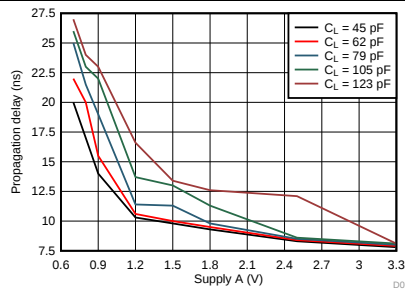
$T_A = 25^\circ\text{C}$ $V_{CCA} = 0.8\text{ V}$

图 10. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



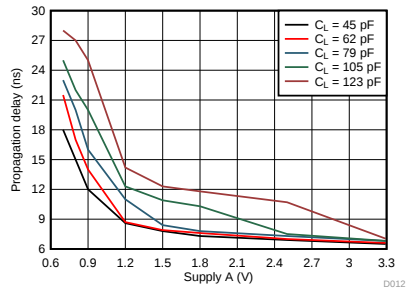
$T_A = 25^\circ\text{C}$ $V_{CCA} = 0.9\text{ V}$

图 11. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



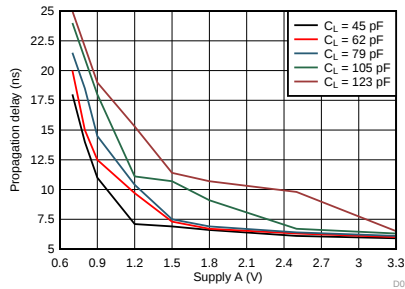
$T_A = 25^\circ\text{C}$ $V_{CCA} = 1.2\text{ V}$

图 12. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



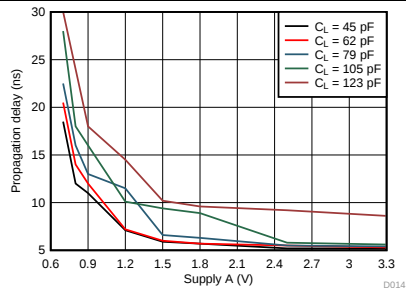
$T_A = 25^\circ\text{C}$ $V_{CCA} = 1.5\text{ V}$

图 13. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



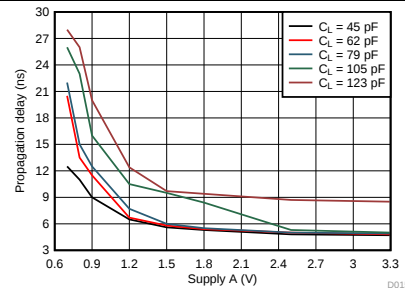
$T_A = 25^\circ\text{C}$ $V_{CCA} = 1.8\text{ V}$

图 14. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



$T_A = 25^\circ\text{C}$ $V_{CCA} = 2.5\text{ V}$

图 15. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



$T_A = 25^\circ\text{C}$ $V_{CCA} = 3.3\text{ V}$

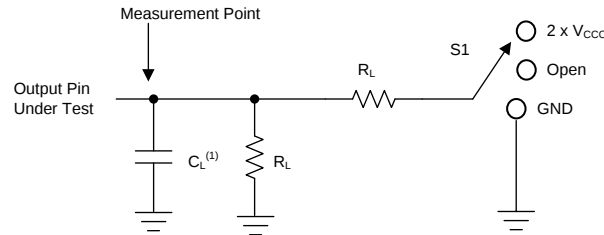
图 16. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 1 \text{ MHz}$
- $Z_O = 50 \Omega$
- $dv/dt \leq 1 \text{ ns/V}$

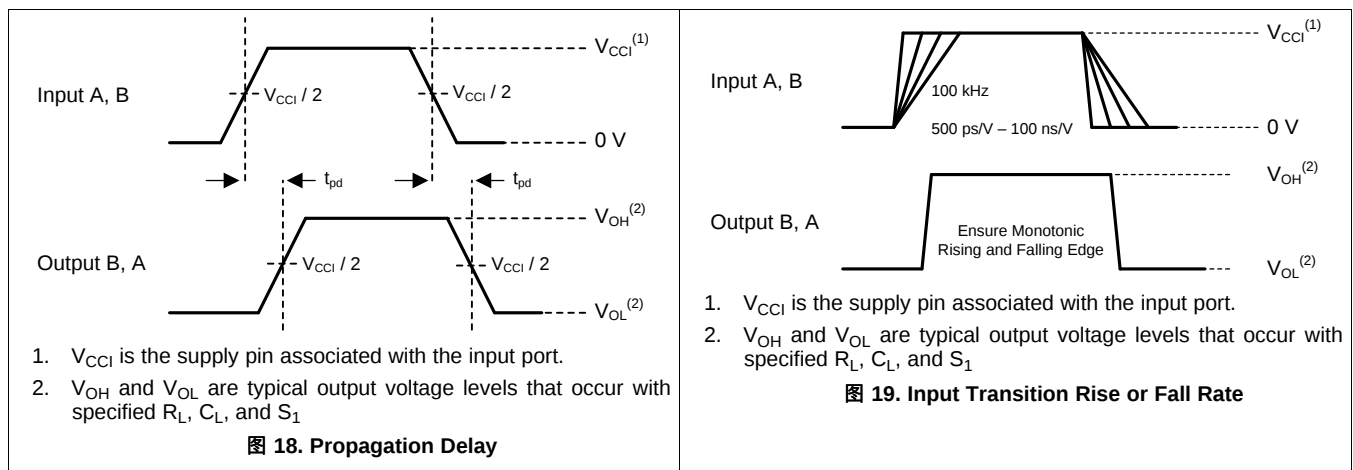


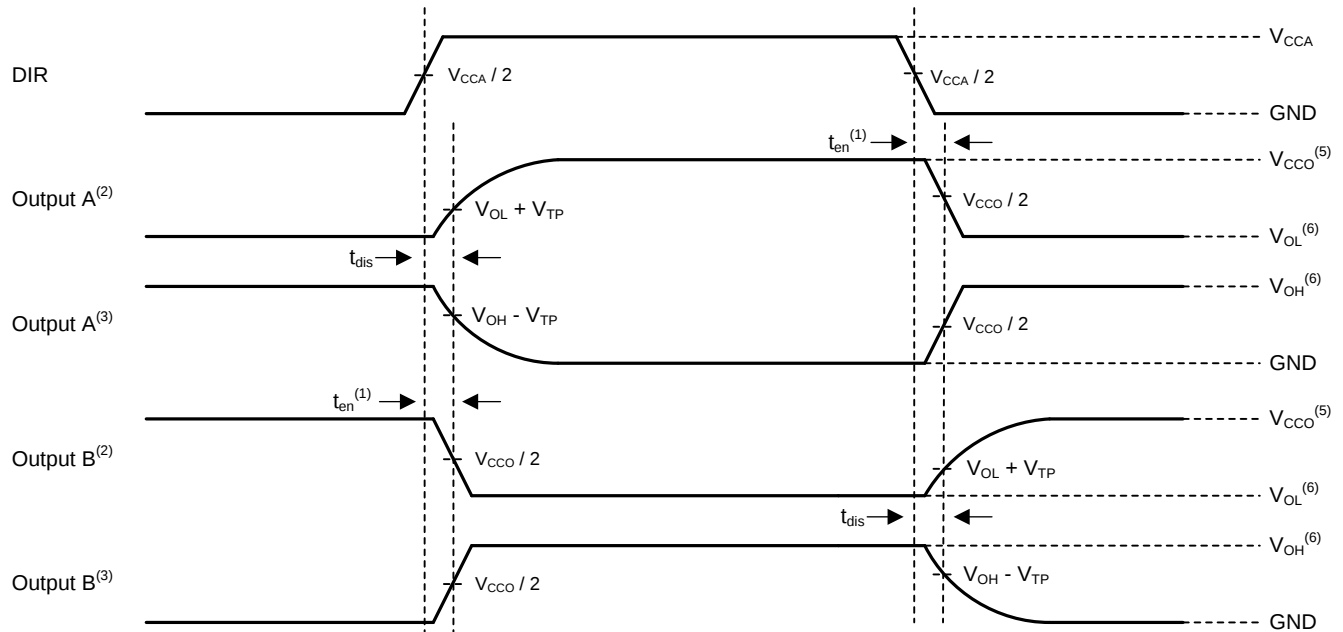
(1) C_L includes probe and jig capacitance.

图 17. Load Circuit

表 9. Load Circuit Conditions

Parameter	V_{CCO}	R_L	C_L	S_1	V_{TP}
$\Delta t/\Delta v$ Input transition rise or fall rate	0.65 V – 3.6 V	1 M Ω	15 pF	Open	N/A
t_{pd} Propagation (delay) time	1.1 V – 3.6 V	2 k Ω	15 pF	Open	N/A
	0.65 V – 0.95 V	20 k Ω	15 pF	Open	N/A
t_{en}, t_{dis} Enable time, disable time	3 V – 3.6 V	2 k Ω	15 pF	$2 \times V_{CCO}$	0.3 V
	1.65 V – 2.7 V	2 k Ω	15 pF	$2 \times V_{CCO}$	0.15 V
	1.1 V – 1.6 V	2 k Ω	15 pF	$2 \times V_{CCO}$	0.1 V
	0.65 V – 0.95 V	20 k Ω	15 pF	$2 \times V_{CCO}$	0.1 V
t_{en}, t_{dis} Enable time, disable time	3 V – 3.6 V	2 k Ω	15 pF	GND	0.3 V
	1.65 V – 2.7 V	2 k Ω	15 pF	GND	0.15 V
	1.1 V – 1.6 V	2 k Ω	15 pF	GND	0.1 V
	0.65 V – 0.95 V	20 k Ω	15 pF	GND	0.1 V





1. Illustrative purposes only. Enable Time is a calculation as described in the data sheet.
2. Output waveform on the condition that input is driven to a valid Logic Low.
3. Output waveform on the condition that input is driven to a valid Logic High.
4. V_{CCI} is the supply pin associated with the input port
5. V_{CCO} is the supply pin associated with the output port.
6. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

图 20. Disable and Enable Time

8 Detailed Description

8.1 Overview

The SN74AXCH1T45 is single-bit, dual-supply, noninverting voltage level translator. Pin A and the direction control pin are referenced to V_{CCA} logic levels and pin B is referenced to V_{CCB} logic levels, as depicted in . The A port can accept I/O voltages ranging from 0.65 V to 3.6 V, and the B port can accept I/O voltages from 0.65 V to 3.6 V. A logic high on the DIR pin enables data transmission from A to B and a logic low on the DIR pin enables data transmission from B to A.

8.2 Functional Block Diagram

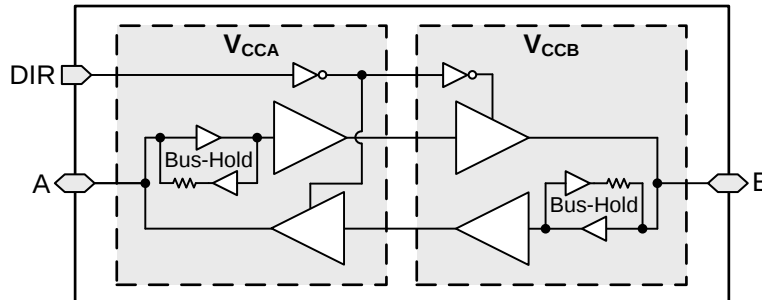


图 21. Functional Block Diagram

8.3 Feature Description

8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is $<100\text{mV}$.

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

Feature Description (接下页)

8.3.6 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in 图 22.

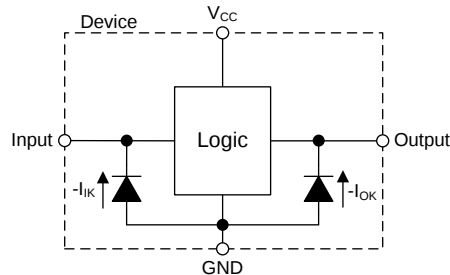
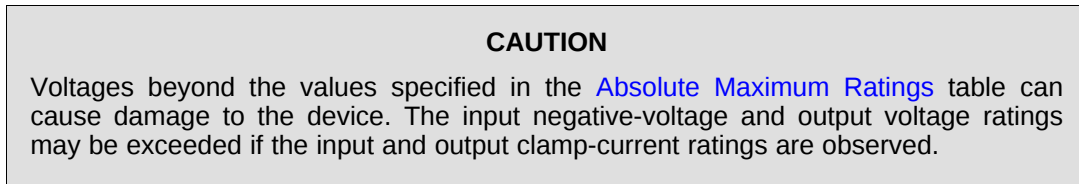


图 22. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.7 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

8.3.8 Supports High-Speed Translation

The SN74AXCH1T45 device can support high data-rate applications. The translated signal data rate can be up to 500 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.3.9 Bus-Hold Data Inputs

Each data input on this device includes a weak latch that maintains a valid logic level on the input. The state of these latches is unknown at startup and remains unknown until the input has been forced to a valid high or low state. After data has been sent through a channel, the latch then maintains the previous state on the input if the line is left floating. It is not recommended to use pull-up or pull-down resistors together with a bus-hold input, as it may cause undefined inputs to occur which leads to excessive current consumption.

Bus-hold data inputs prevent floating inputs on this device. The [Implications of Slow or Floating CMOS Inputs](#) application report explains the problems associated with leaving CMOS inputs floating.

These latches remain active at all times, independent of all control signals such as direction control or output enable.

The [Bus-Hold Circuit](#) application report has additional details regarding bus-hold inputs.

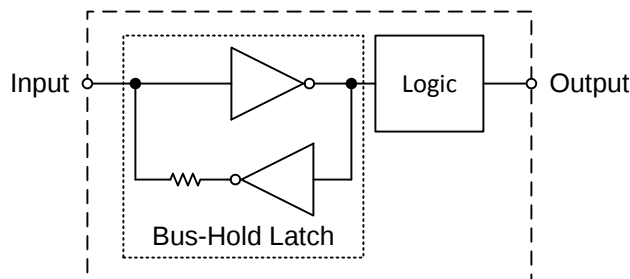


图 23. Simplified Schematic For Device With Bus-Hold Data Inputs

8.4 Device Functional Modes

表 10 lists the device functions for the DIR input.

表 10. Function Table

INPUT ⁽¹⁾ DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXCH1T45 device can be used in level-translation applications for interfacing devices or systems with one another when they are operating at different interface voltages. The maximum data rate can be up to 500 Mbps when the device translate signals from 1.8 V to 3.3 V.

9.1.1 Enable Times

Calculate the enable times for the SN74AXC1T45 using the following formulas:

$$t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \quad (1)$$

$$t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \quad (2)$$

$$t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \quad (3)$$

$$t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74AXCH1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

9.2 Typical Applications

9.2.1 Interrupt Request Application

图 24 shows an example of the SN74AXCH1T45 being used in an application where a system controller flags an interrupt request (IRQ) to the CPU. The system controller determines the direction of the IRQ line to either flag an interrupt to the CPU or allow the CPU to drive data on the line. In this application the controller is operating at 3.3 V while the CPU can be operating as low as 0.65 V.

The SN74AXCH1T45 device is used to ensure that these devices can communicate at the appropriate voltage levels. Because the SN74AXCH1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between the CPU and controller when changing directions.

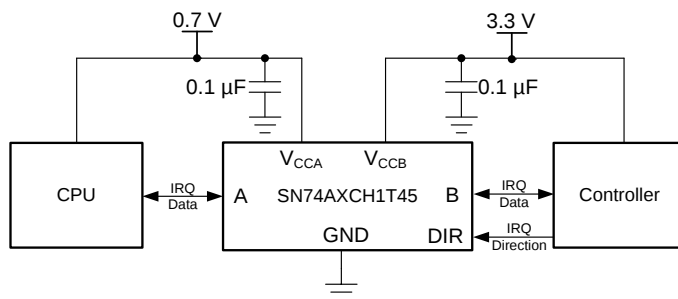


图 24. Interrupt Request Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 11.

Typical Applications (接下页)

表 11. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the SN74AXCH1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74AXCH1T45 device is driving to determine the output voltage range.

9.2.1.3 Application Curve

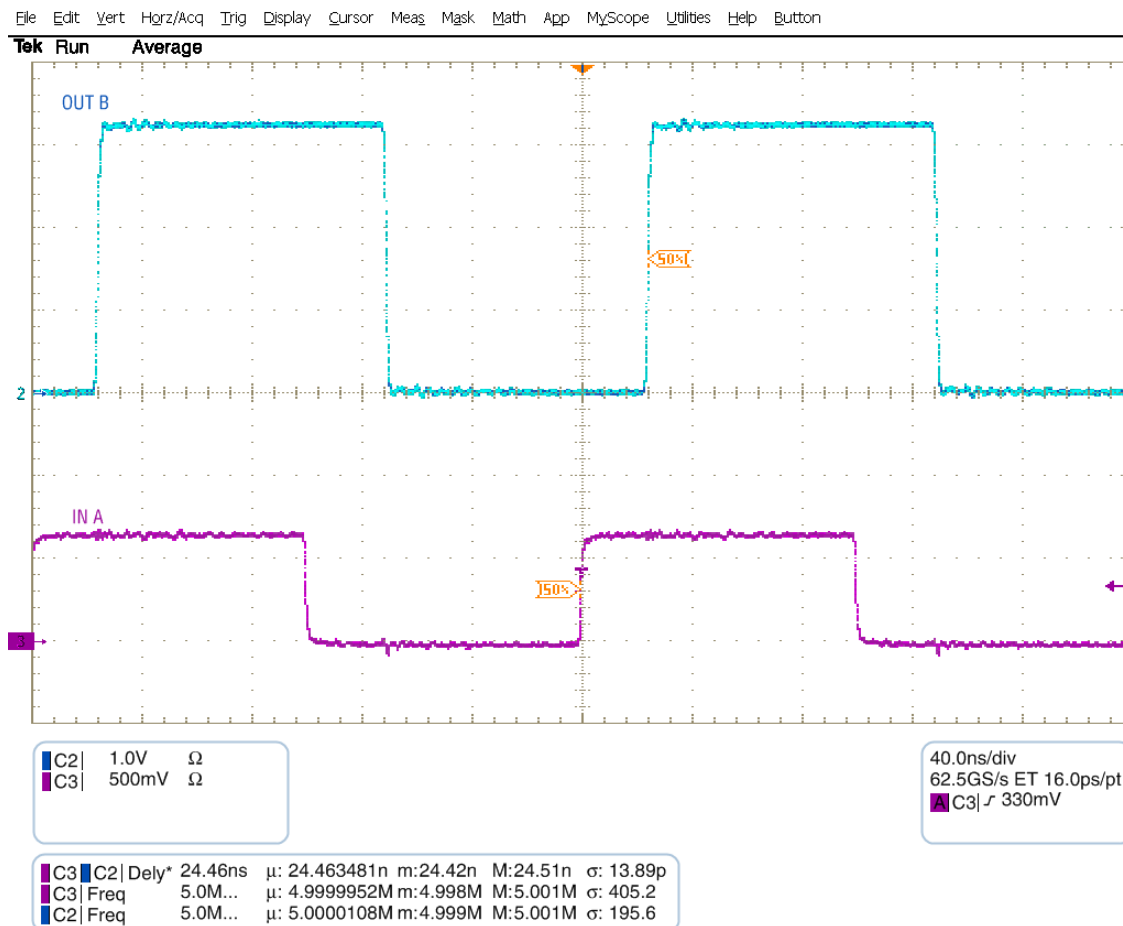


图 25. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

9.2.2 Universal Asynchronous Receiver-Transmitter (UART) Interface Application

图 26 shows the SN74AXCH1T45 being used for the two-bit UART interface application. One SN74AXCH1T45 device is used to level shift the voltage and drive the TX from the processor to the GPS Module while a second SN74AXCH1T45 device is used to drive the TX Data line from the GPS Module to the Processor. Devices with bus-hold inputs remove the requirement for external pullup resistors to maintain a valid logic level at the input.

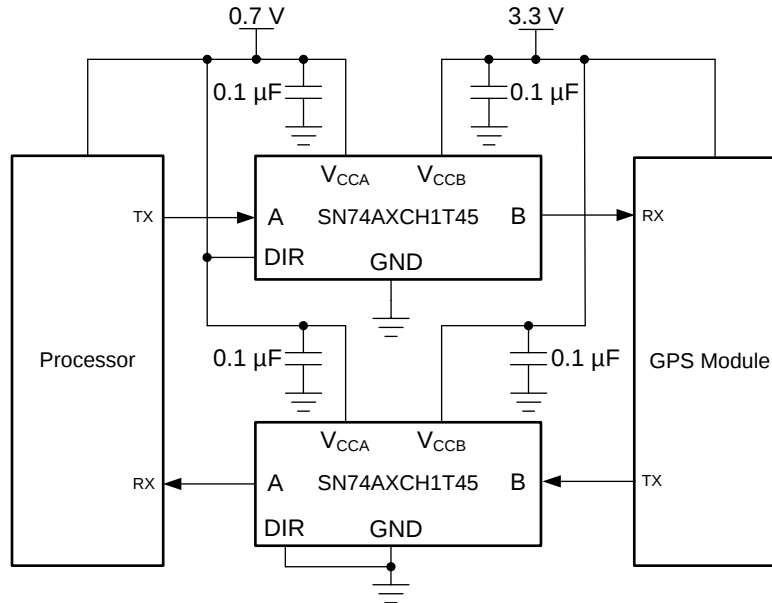


图 26. UART Interface Application

9.2.2.1 Design Requirements

Refer to [Design Requirements](#).

9.2.2.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#).

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the [Power Sequencing for AXC Family of Devices](#) application report

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- Use short trace lengths to avoid excessive loading.

11.2 Layout Example

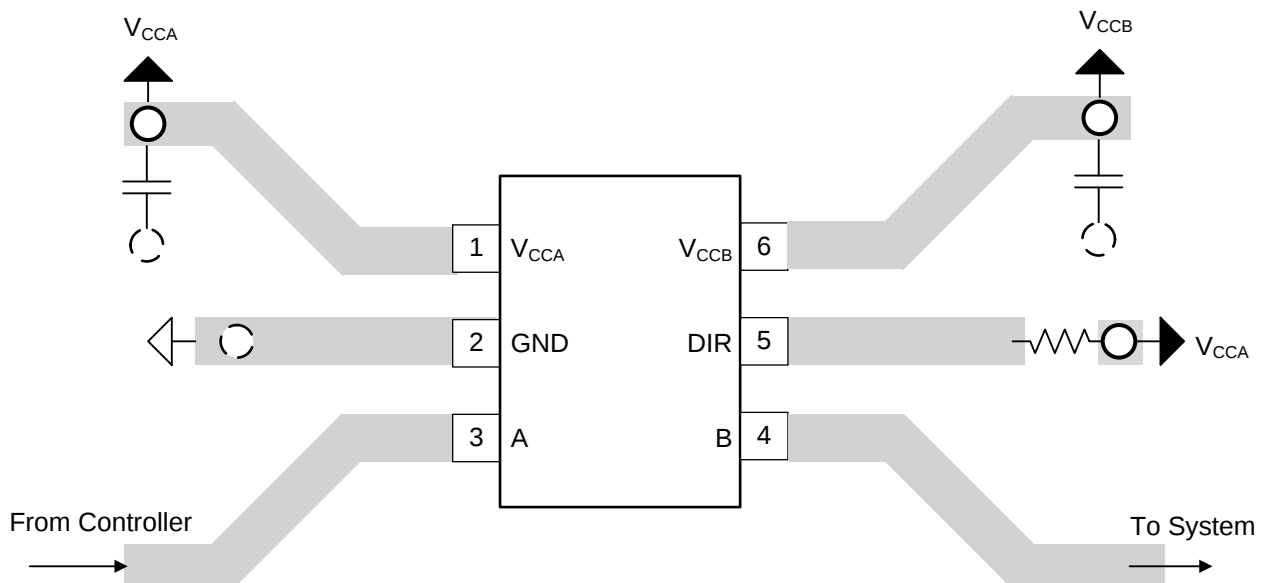
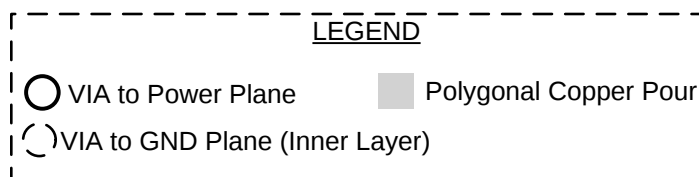


图 27. PCB Layout Example

12 器件和文档支持

12.1 文档支持

相关文档请参见以下部分：

- 德州仪器 (TI)，《使用通用 EVM 评估 SN74AXC1T45DRL》应用报告
- 德州仪器 (TI)，《利用总线保持电路避免浮点输入系统注意事项》应用报告
- 德州仪器 (TI)，《AXC 系列器件电源定序》应用报告
- 德州仪器 (TI)，《慢速或浮点 CMOS 输入的影响》应用报告

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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设计支持 TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXCH1T45DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PNL	Samples
SN74AXCH1T45DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1CC	Samples
SN74AXCH1T45DRY2	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IR	Samples
SN74AXCH1T45DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	II	Samples
SN74AXCH1T45DTQR	ACTIVE	X2SON	DTQ	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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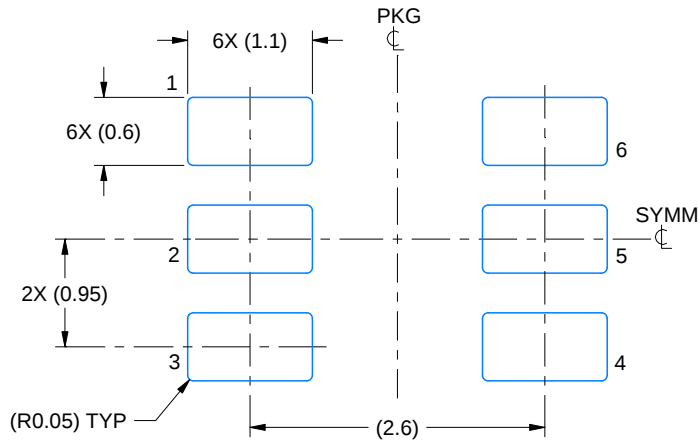
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EXAMPLE BOARD LAYOUT

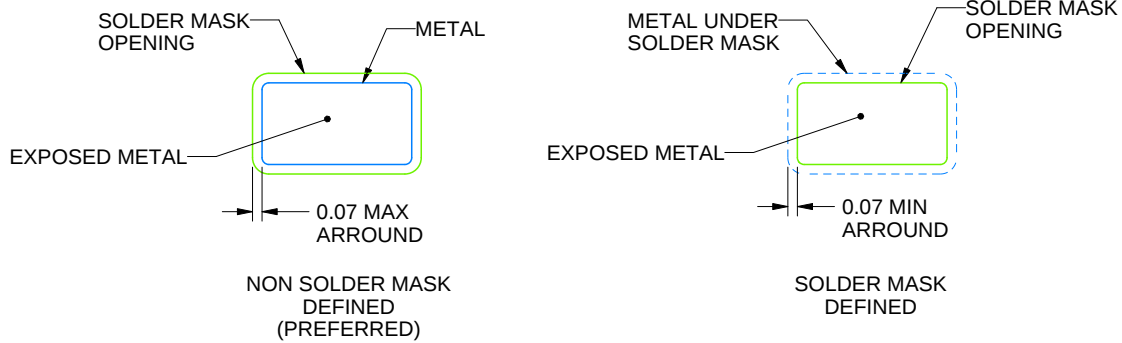
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

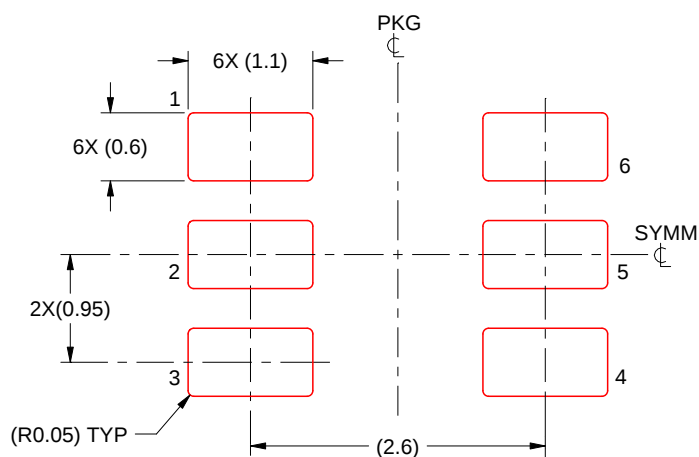
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

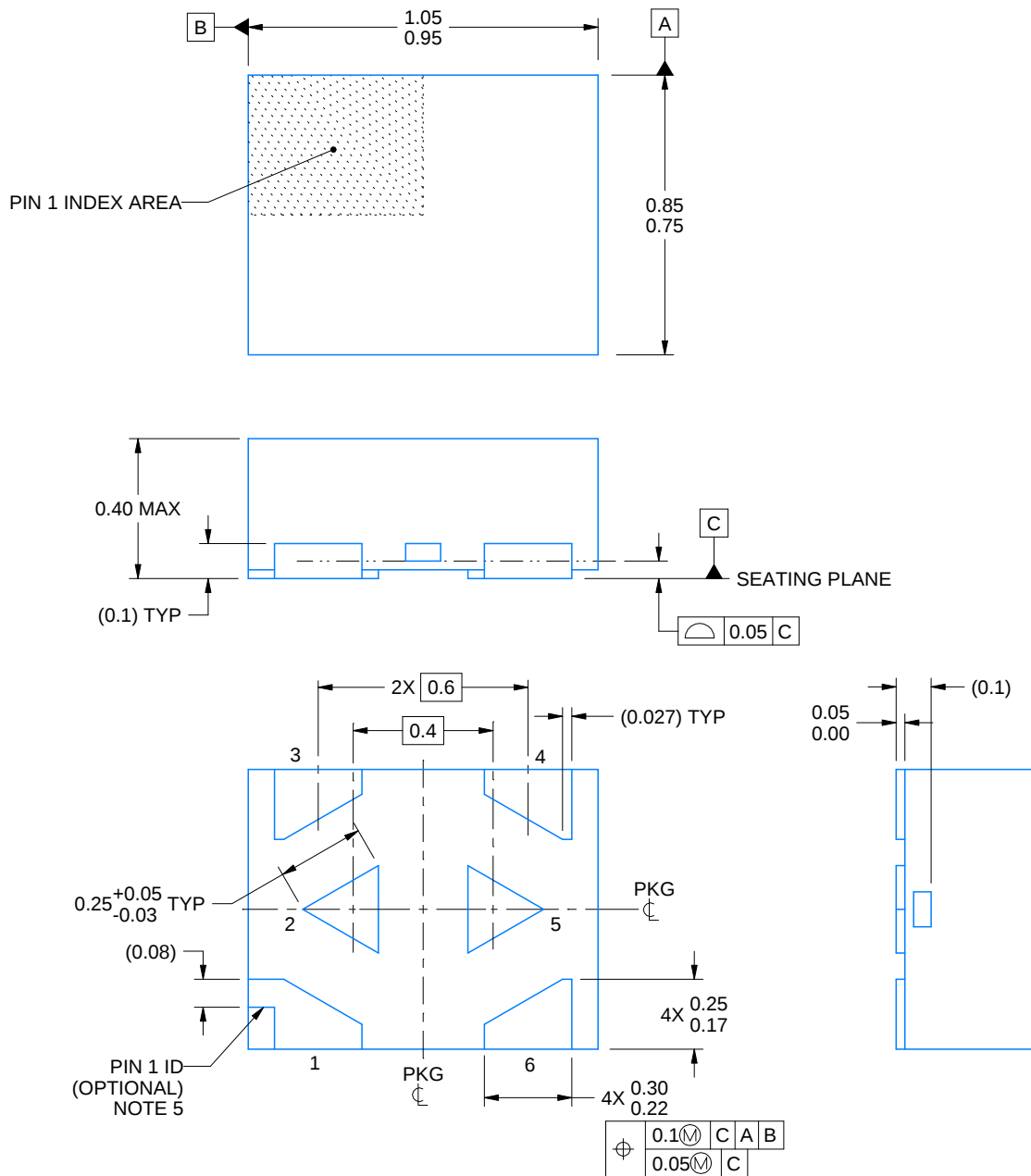


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4224056/A 11/2017

NOTES:

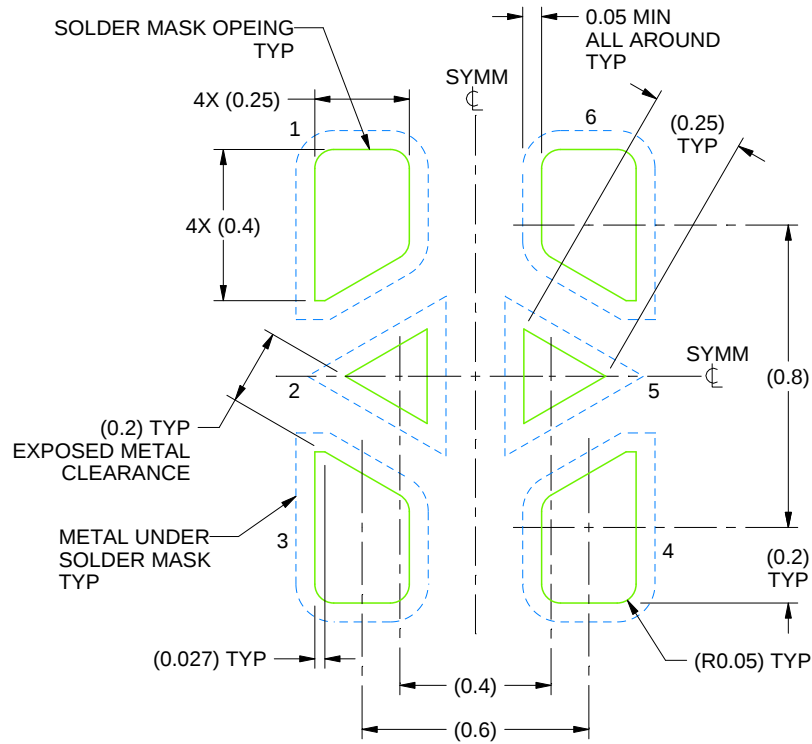
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

EXAMPLE BOARD LAYOUT

DTQ0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4224056/A 11/2017

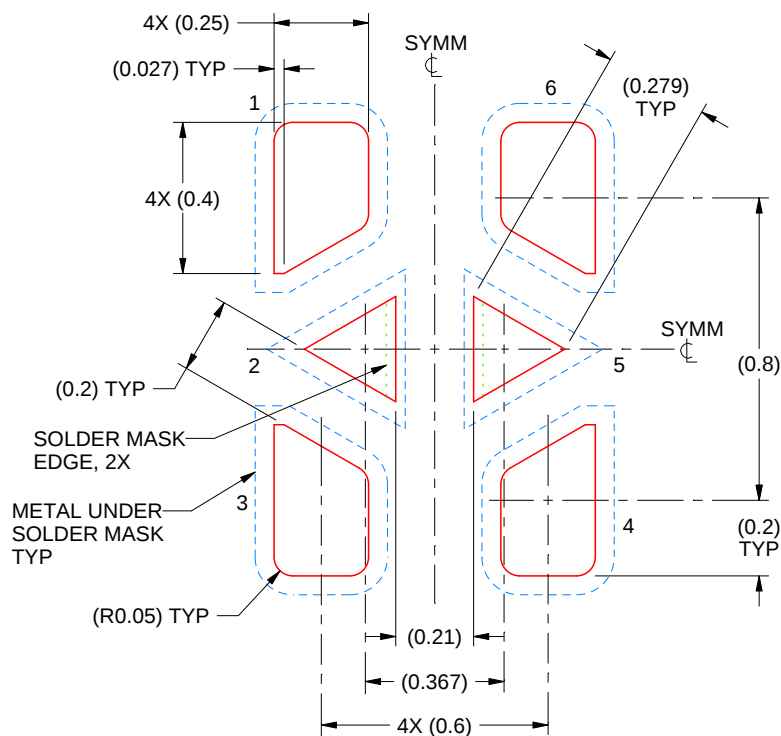
NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

DTQ0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

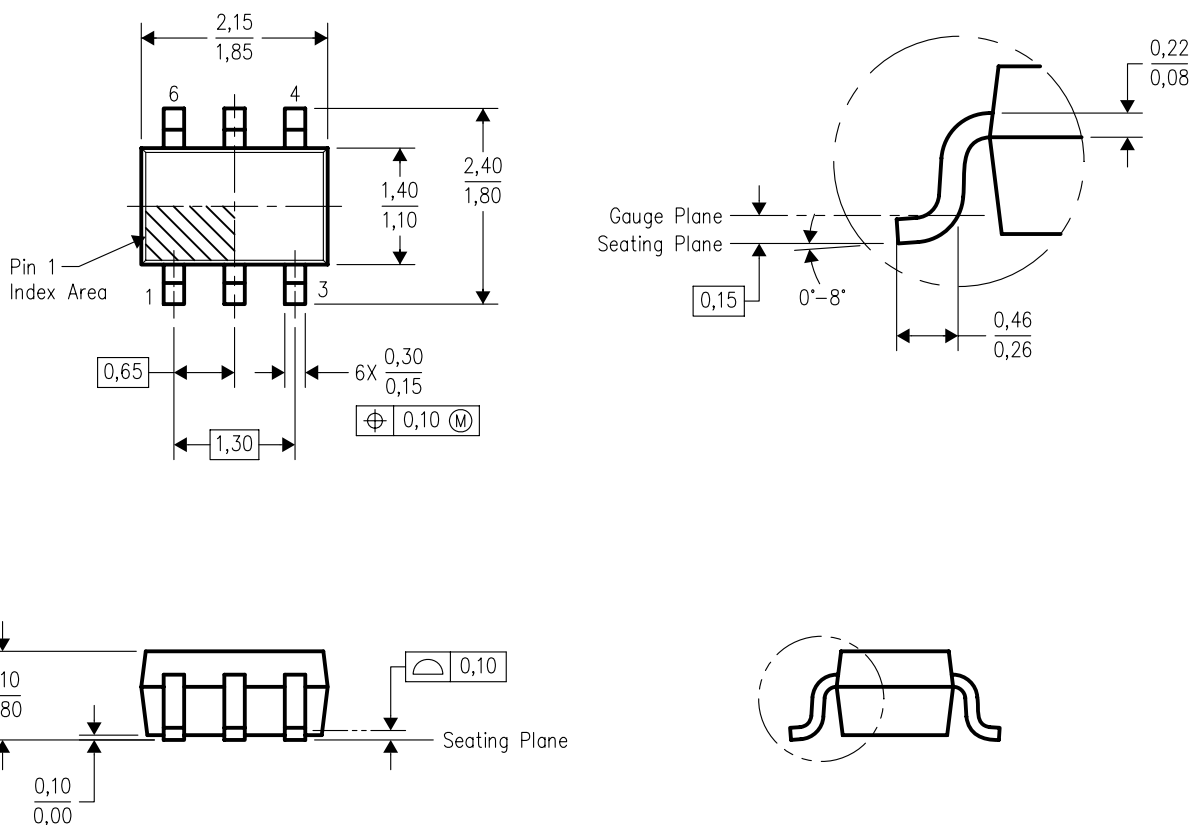
4224056/A 11/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

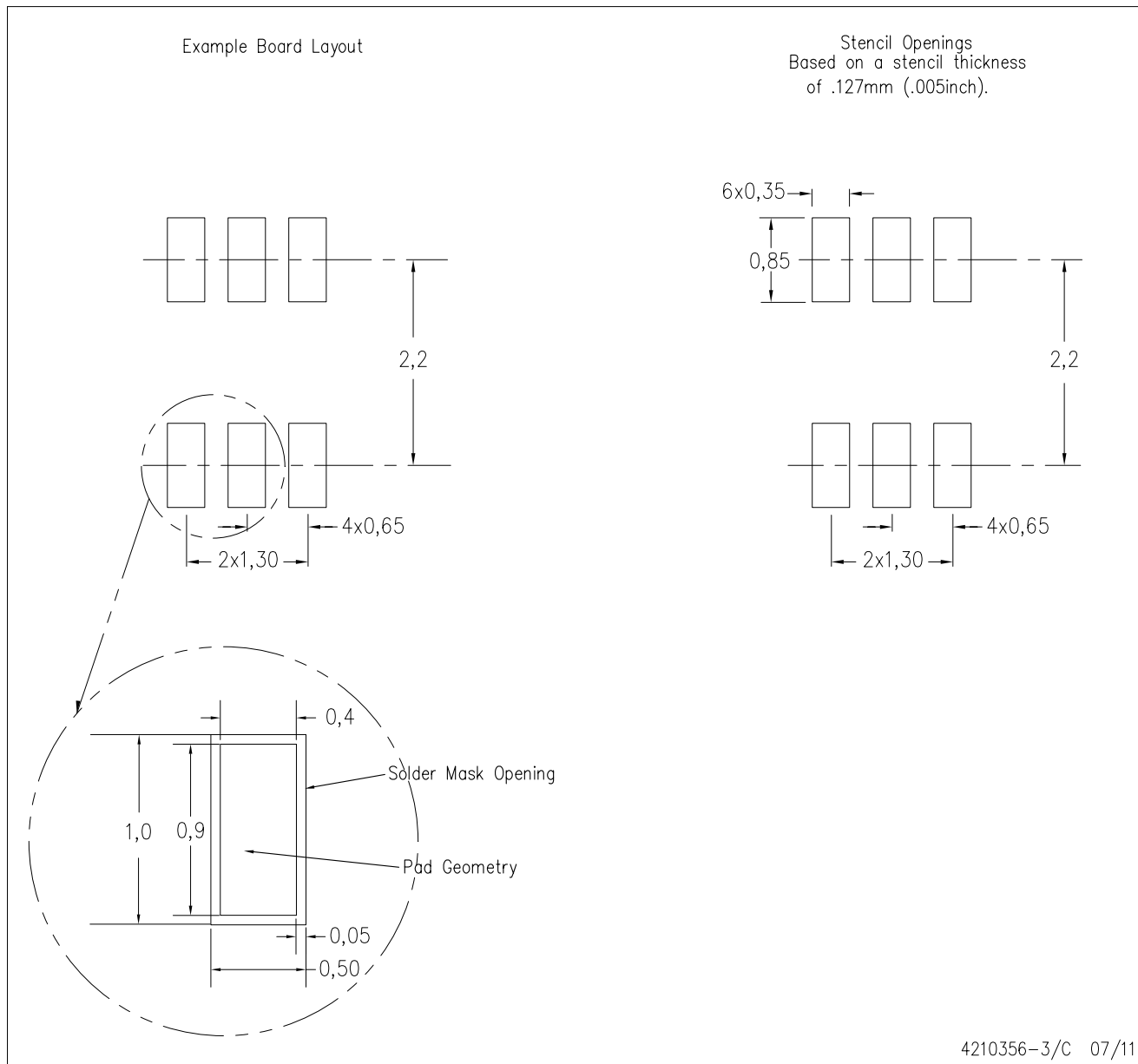


4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

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