ISOW7741 5000-V_{RMS} Reinforced Quad-Channel Digital Isolator with Integrated Low-Emissions, Low-Noise DC-DC Converter

1 Features

- 100 Mbps data rate
- Integrated DC-DC converter with low-emissions, low-noise
  - Emission optimized to meet CISPR 32 limits
  - Low frequency power converter at 25 MHz enabling low noise performance
  - Low output ripple: 24 mV
- High efficiency output power
  - Efficiency at max load: 45%
  - Up to 0.5-W output power
  - V_{isoout} accuracy of 5%
  - 5 V to 5 V: Available load current ≥ 110 mA
  - 5 V to 3.3 V: Available load current ≥ 110 mA
  - 3.3 V to 3.3 V: Available load current ≥ 60 mA
- Independent power supply for channel isolator & power converter
  - Logic supply (V_{IO}): 1.71-V to 5.5-V
  - Power converter supply (V_{DD}): 3-V to 5.5-V
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
- Reinforced isolation barrier:
  - >100-year projected lifetime at 1 kV_{RMS} working voltage
  - Up to 5000 V_{RMS} isolation rating
  - Up to 10 kV_{PK} surge capability
  - ±100 kV/µs typical CMTI
- Safety-Related Certifications (pending):
  - VDE reinforced insulation per DIN VDE V 0884-11:2017-01
  - UL 1577 component recognition program
  - IEC 60950-1, IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1-2011 certifications
- Extended temperature range: –40°C to +125°C
- 20-pin wide SOIC package

2 Applications

- Factory automation
- Motor control
- Grid infrastructure
- Medical equipment
- Test and measurement

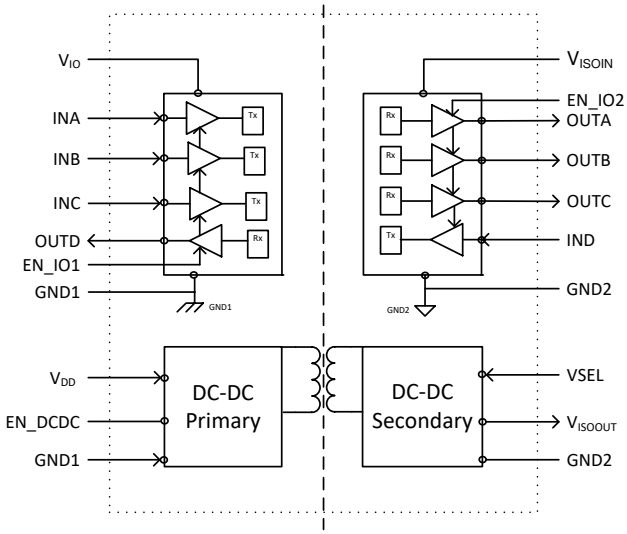
3 Description

The ISOW7741 device is a galvanically-isolated quad-channel digital isolator with an integrated high-efficiency power converter with low emissions. The integrated DC-DC converter provides up to 500 mW of isolated power, eliminating the need for a separate isolated power supply in space-constrained isolated designs.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
ISOW7741 ISOW7741F	DFM (20)	12.83 mm × 7.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial Release

5 Description (continued)

The high-efficiency of the power converter allows for operation at a wide operating ambient temperature range of –40°C to +125°C. This device provides improved emissions performance, allowing for simplified board design and has provisions for ferrite beads to further attenuate emissions. The ISOW7741 has been designed with enhanced protection features in mind, including soft-start to limit inrush current, over-voltage and under-voltage lock out, fault detection on the EN_DCDC pin, overload and short-circuit protection, and thermal shutdown.

The ISOW7741 device provides high electromagnetic immunity while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. This device has three channels in the forward and one channel in the reverse direction. If the input signal is lost, the default output is high for the ISOW7741 device without the F suffix and low for the ISOW7741F device with the F suffix. The ISOW7741 can operate from a single supply voltage of 3 V to 5.5 V by connecting V_{IO} and V_{DD} together on PCB. If lower logic levels are required, these devices support 1.71 V to 5.5 V logic supply (V_{IO}) that can be independent from the power converter supply (V_{DD}) of 3 V to 5.5 V. V_{ISOIN} and V_{ISOOUT} needs to be connected on board with either a ferrite bead or fed through a LDO.

This device helps prevent noise currents on data buses, such as UART, SPI, RS-485, RS-232, and CAN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the device has been significantly enhanced to ease system-level ESD, EFT, surge and emissions compliance. The device is available in a 20-pin SOIC wide-body (SOIC-WB) DFM package.

6 Pin Configuration and Functions

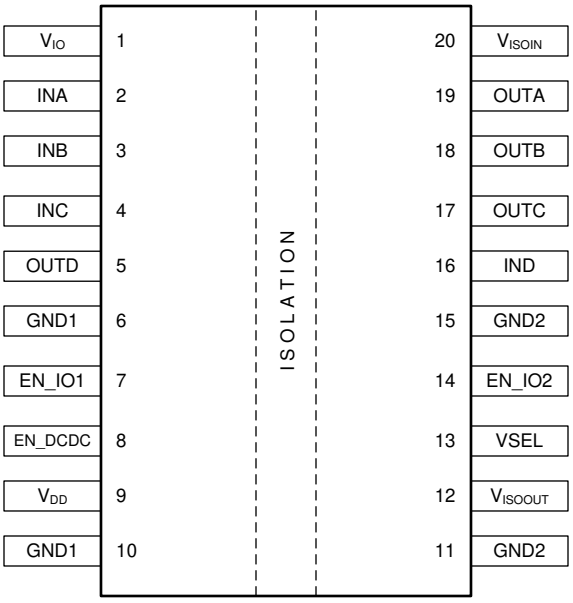


Figure 6-1. ISOW7741 DFM Package 20-Pin SOIC-WB Top View

ADVANCE INFORMATION

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
	ISOW7741		
GND1	6, 10	—	Ground connection for V_{DD} and V_{IO}. Both GND1 pins needs to be shorted on board.
GND2	11, 15	—	Ground connection for V_{ISOIN} and V_{ISOOUT}. GND2 pins can be shorted on board or connected through a ferrite bead. See the Layout Section for more information.
INA	2	I	Input channel A
INB	3	I	Input channel B
INC	4	I	Input channel C
IND	16	I	Input channel D
OUTA	19	O	Output channel A
OUTB	18	O	Output channel B
OUTC	17	O	Output channel C
OUTD	5	O	Output channel D
EN_IO1	7	I	Output Enable 1: When EN_IO1 is high or open then the channel output pins on side 1 are enabled. When EN_IO1 is low then the channel output pins on side 1 are in a high impedance state and the transmitter of the channel input pins on side 1 are disabled.
EN_IO2	14	I	Output Enable 2: When EN_IO2 is high or open then the channel output pins on side 2 are enabled. When EN_IO2 is low then the channel output pins on side 2 are in a high impedance state and the transmitter of the channel input pins on side 2 are disabled.
EN_DCDC	8	I/O	Multi-function power converter enable input pin or fault output pin. Can only be used as either an input pin or an output pin. Power converter enable input pin: enables and disables the integrated DC-DC power converter. Connect directly to microcontroller or through a series current limiting resistor to use as an enable input pin. DC-DC power converted is enabled when EN_DCDC is high and disabled when low. Fault output pin: Alert signal if power converter is not operating properly. This pin is active low. Connect to microcontroller through a 5 kΩ or greater pull-up resistor in order to use as a fault outpin pin. See Section 9.3.3 for more information
VSEL	13	I	V_{ISOOUT} selection pin. V_{ISOOUT} = 5 V when VSEL shorted to V_{ISOOUT}. V_{ISOOUT} = 3.3 V, when VSEL shorted to GND2 or when left floating. For more information see the Device Functional Modes.
V_{IO}	1	—	Side 1 logic supply.
V_{DD}	9	—	Side 1 DC-DC converter power supply.
V_{ISOIN}	20	—	Side 2 supply voltage for isolation channels. This pin and V_{ISOOUT} needs to be shorted on board.
V_{ISOOUT}	12	—	Isolated power converter output voltage. This pin and V_{ISOIN} needs to be shorted on board.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Power converter supply voltage	–0.5	6	V
V_{ISOIN}	Isolated supply voltage, input supply for secondary side isolation channels	–0.5	6	V
V_{ISOOUT}	Isolated supply voltage, Power converter output	–0.5	6	V
V_{IO}	Primary side logic supply voltage	–0.5	6	V
V	Voltage at INx, OUTx, EN_IOx	–0.5	V_{IO} + 0.5	V
	Voltage at EN_DCDC	–0.5	V_{IO} + 0.5	V
	Voltage at VSEL	–0.5	V_{ISOOUT} + 0.5	V
I_O	Maximum output current through data channels	–15	15	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) V_{DD}, V_{ISOIN} V_{ISOOUT}, and V_{IO} are with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	
		Contact discharge per IEC 61000-4-2(2) Isolation barrier withstand test	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.

ADVANCE INFORMATION

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
Power Converter						
V_{DD}	Power converter supply voltage	3.3 V operation	2.97	3.3	3.63	V
		5 V operation	4.5	5	5.5	V
$V_{DD(UVLO+)}$	Positive threshold when power converter supply is rising	Positive threshold when power converter supply is rising		2.7	2.95	V
$V_{DD(UVLO-)}$	Positive threshold when power converter supply is falling	Positive threshold when power converter supply is falling	2.40	2.55		V
$V_{DD(HYS)}$	Power converter supply voltage hysteresis	Power converter supply voltage hysteresis	0.15			V
Channel Isolation						
V_{IO}, V_{ISOIN}	Channel logic supply voltage	1.8 V operation	1.71		1.89	V
		2.5 V, 3.3 V, and 5 V operation	2.25		5.5	V
$V_{IO(UVLO+)}$	Rising threshold of logic supply voltage			1.55	1.7	V
$V_{IO(UVLO-)}$	Falling threshold of logic supply voltage		1.0	1.41		V
$V_{IO(HYS)}$	Logic supply voltage hysteresis		75			mV
I_{OH}	High level output current(1)	V_{ISOIN} = 5 V	–4			mA
		V_{ISOIN} = 3.3 V	–2			mA
		V_{ISOIN} = 2.5 V	–1			mA
		V_{ISOIN} = 1.8 V	–1			mA
I_{OL}	Low level output current(1)	V_{ISOIN} = 5 V			4	mA
		V_{ISOIN} = 3.3 V			2	mA
		V_{ISOIN} = 2.5 V			1	mA
		V_{ISOIN} = 1.8 V			1	mA
V_{IH}	High-level input voltage		0.7 × V_{SI}		V_{SI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{SI}	V
DR	Data rate				100	Mbps
t_{PWRUP}	Channel isolator ready after power up or EN_DCDC high	V_{ISOIN} > $V_{IO(UVLO+)}$		5		ms
T_A	Ambient temperature		–40		125	°C

(1) This current is for data output channel.

7.4 Thermal Information

THERMAL METRIC(1)		ISOW7741 DFM (SOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Power Ratings

V_{DD} = V_{IO} = 5.5 V, I_{ISO} = 110 mA, T_J = 150°C, T_A ≤ 80°C, C_L = 15 pF, input a 50-MHz 50% duty-cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{DD} = 5.5 V, V_{IO} = 5.5 V, V_{ISOOUT} = V_{ISOIN}, I_{ISOOUT} = 100 mA, T_J = 150°C, T_A ≤ 80°C, C_L = 15 pF, input a 50-MHz 50% duty-cycle square wave			1.48	W
P_{D1}	Maximum power dissipation (side-1)				0.74	W
P_{D2}	Maximum power dissipation (side-2)				0.74	W

ADVANCE INFORMATION

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	> 17	µm
		Minimum internal gap (internal clearance – transformer power isolation)	>120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$(qualification)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~3.5	pF
R_{IO}	Insulation resistance(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V, T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
$V_{ISO(UL)}$	Withstand isolation voltage	$V_{TEST} = V_{ISO(UL)}$= 5000 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO(UL)}$ = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1, and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 and EN 60950- 1:2006/A2:2013
Reinforced insulation; Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1500 V_{PK}; Maximum surge isolation voltage, 6250 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1:2014, 800 V_{RMS} maximum working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3+A1, 250 V_{RMS} maximum working voltage. Temperature rating is 90°C for reinforced insulation and 125°C for basic insulation; see certificate for details.	Single protection, 5000 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage;	5000 V_{RMS} Reinforced insulation per EN 61010-1:2010 up to working voltage of 600 V_{RMS}; 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A2:2013 up to working voltage of 800 V_{RMS}
Certification Planned	Certification Planned	Certification Planned	Certification Planned	Certification Planned

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 68.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			332	mA
		$R_{\theta JA}$ = 68.5°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			507	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 68.5°C/W, T_J = 150°C, T_A = 25°C			1825	mW
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Section 7.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use the following equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

ADVANCE INFORMATION

7.9 Electrical Characteristics - Power Converter

V_{DD} = 5 V ±10% or 3.3 V ±10% and V_{ISOIN} power externally (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} = 5 V, V_{ISOOUT} = 5 V, V_{SEL} = V_{ISOOUT}						
V_{ISOOUT}	Isolated supply voltage	External I_{ISOOUT} = 0 to 55 mA	4.75	5	5.25	V
V_{ISOOUT}	Isolated supply voltage	External I_{ISOOUT} = 0 to 110 mA	4.5	5	5.25	V
$V_{ISOOUT(LINE)}$	DC line regulation	I_{ISOOUT} = 55 mA, V_{DD} = 4.5 V to 5.5 V		2		mV/V
$V_{ISOOUT(LOAD)}$	DC load regulation	I_{ISOOUT} = 0 to 110 mA		1%		
EFF	Efficiency at maximum load current (1)	I_{ISOOUT} = 110 mA, C_{LOAD} = 0.01 µF || 10 µF; V_I = V_{DD} (ISOW7741); V_I =0 V (ISOW7741 with F suffix).		45%		
$V_{ISOOUT(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.01 µF || 20 µF, I_{ISOOUT} = 110 mA		24		mV
I_{ISOOUT_SC}	DC current from V_{DD} supply under short circuit on V_{ISOOUT}	V_{ISOOUT} shorted to GND2		250		mA
V_{DD} = 5 V, V_{ISOOUT} = 3.3 V, V_{SEL} = GND2						
V_{ISOOUT}	Isolated supply voltage	External I_{ISOOUT} = 0 to 55 mA	3.15	3.3	3.45	V
V_{ISOOUT}	Isolated supply voltage	External I_{ISOOUT} = 0 to 110 mA	3.15	3.3	3.45	V
$V_{ISOOUT(LINE)}$	DC line regulation	I_{ISOOUT} = 55 mA, V_{DD} = 4.5 V to 5.5 V		2		mV/V
$V_{ISOOUT(LOAD)}$	DC load regulation	I_{ISOOUT} = 0 to 110 mA		1%		
EFF	Efficiency at maximum load current (1)	I_{ISOOUT} = 110 mA, C_{LOAD} = 0.01 µF || 10 µF; V_I = V_{DD} (ISOW7741); V_I =0 V (ISOW7741 with F suffix).		38%		
$V_{ISOOUT(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth , C_{LOAD} = 0.01 µF || 20 µF, I_{ISOOUT} = 110 mA		30		mV
I_{ISOOUT_SC}	DC current from V_{DD} supply under short circuit on V_{ISOOUT}	V_{ISOOUT} shorted to GND2		250		mA
V_{DD} = 3.3 V, V_{ISOOUT} = 3.3 V, V_{SEL} = GND2						
V_{ISOOUT}	Isolated supply voltage	External I_{ISOOUT} = 0 to 30 mA	3.15	3.3	3.45	V
V_{ISOOUT}	Isolated supply voltage	External I_{ISOOUT} = 0 to 60 mA	3	3.3	3.45	V
$V_{ISOOUT(LINE)}$	DC line regulation	I_{ISOOUT} = 30 mA, V_{DD} = 3.0 V to 3.6 V		2		mV/V
$V_{ISOOUT(LOAD)}$	DC load regulation	I_{ISOOUT} = 0 to 60 mA		1%		
EFF	Efficiency at maximum load current (1)	I_{ISOOUT} = 60 mA, C_{LOAD} = 0.01 µF || 10 µF; V_I = V_{DD} (ISOW7741); V_I =0 V (ISOW7741 with F suffix).		42%		
$V_{ISOOUT(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.01 µF || 20 µF, I_{ISOOUT} = 60 mA		14		mV
I_{ISOOUT_SC}	DC current from V_{DD} supply under short circuit on V_{ISOOUT}	V_{ISOOUT} shorted to GND2		160		mA

(1) Power converter I_{LOAD} = current required to power the secondary side. I_{LOAD} does not take into account the channel isolator current. See Supply Current Characteristics Channel Isolator section for details.

7.10 Supply Current Characteristics - Power Converter

V_{DD} = 5 V ±10% or 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Power Converter Disabled							
Power converter supply current	EN_DCDC = GND1, V_{ISOOUT} = No I_{LOAD}		I_{DD}		0.28	0.45	mA
Logic supply current	EN_DCDC = GND1		I_{IO}		0.27	0.57	mA
Power Converter Enabled							
Power converter supply current input	V_{DD} = 5 V, V_{SEL} = V_{ISOOUT}	I_{LOAD} = 55 mA	I_{DD}		115	171	mA
	V_{DD} = 5 V, V_{SEL} = V_{ISOOUT}	I_{LOAD} = 110 mA			225	316	mA
	V_{DD} = 5 V, V_{SEL} = GND2	I_{LOAD} = 55 mA			96	130	mA
	V_{DD} = 5 V, V_{SEL} = GND2	I_{LOAD} = 110 mA			187	240	mA
	V_{DD} = 3.3 V, V_{SEL} = GND2	I_{LOAD} = 30 mA			74	112	mA
	V_{DD} = 3.3 V, V_{SEL} = GND2	I_{LOAD} = 60 mA			143	216	mA
Power converter output current (1)	V_{DD} = 5 V	V_{SEL} = V_{ISOOUT}	I_{ISOOUT}	110			mA
	V_{DD} = 5 V	V_{SEL} = GND2		110			mA
	V_{DD} = 3.3 V	V_{SEL} = GND2		60			mA

(1) Power converter I_{LOAD} = current required to power the secondary side. I_{LOAD} does not take into account the channel isolator current. See Supply Current Characteristics Channel Isolator section for details.

ADVANCE INFORMATION

ADVANCE INFORMATION

7.11 Electrical Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 5-V

V_{IO}, V_{ISOIN} = 5 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 x V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 x V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 x V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	–25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –4 mA, see TBD	V_{SO} (1) – 0.4			V
V_{OL}	Low level output voltage	I_O = 4 mA, see TBD			0.4	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see TBD		100		kV/us

(1) V_{SI} = input side supply; V_{SO} = output side supply

7.12 Supply Current Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 5-V

V_{IO}, V_{ISOIN} = 5 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW7741 Channel Supply Current							
Supply current - Disable	EN_IO1 = EN_IO2 = 0 V; V_I = V_{CCI} (1) (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.8	4.1	mA
			I_{ISOIN}		4.3	6.3	mA
	EN_IO1 = EN_IO2 = 0 V; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		2.8	4.1	mA
			I_{ISOIN}		4.3	6.3	mA
Channel Supply current - DC signal	EN_IO1 = EN_IO2 = V_{CCI}; V_I = V_{CCI} (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.8	4.1	mA
			I_{ISOIN}		4.3	6.3	mA
	EN_IO1 = EN_IO2 = V_{CCI}; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		6.1	8.4	mA
			I_{ISOIN}		5.5	7.9	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DD_IO}		4.4	6.3	mA
			I_{ISOIN}		4.9	7.1	mA
		10 Mbps	I_{DD_IO}		5	6.9	mA
			I_{ISOIN}		6.3	8.7	mA
		100 Mbps	I_{DD_IO}		11	12.9	mA
			I_{ISOIN}		21.4	32	mA

(1) V_{CCI} = V_{IO} or V_{ISOIN}

7.13 Electrical Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 3.3-V

V_{IO}, V_{ISOIN} = 3.3 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 x V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 x V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 x V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	-25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –4 mA, see TBD	V_{SO} (1) – 0.3			V
V_{OL}	Low level output voltage	I_O = 4 mA, see TBD			0.3	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see TBD		100		kV/us

(1) V_{SI} = input side supply; V_{SO} = output side supply

7.14 Supply Current Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 3.3-V

V_{IO}, V_{ISOIN} = 3.3 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW7741 Channel Supply Current							
Supply current - Disable	EN_IO1 = EN_IO2 = 0 V; V_I = V_{CCI} (1) (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.8	4	mA
			I_{ISOIN}		4.2	6.3	mA
	EN_IO1 = EN_IO2 = 0 V; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		2.8	4	mA
			I_{ISOIN}		4.2	6.3	mA
Channel Supply current - DC signal	EN_IO1 = EN_IO2 = V_{CCI}; V_I = V_{CCI} (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.8	4	mA
			I_{ISOIN}		4.2	6.3	mA
	EN_IO1 = EN_IO2 = V_{CCI}; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		6.1	8.3	mA
			I_{ISOIN}		5.5	7.9	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DD_IO}		4.4	6.3	mA
			I_{ISOIN}		4.9	7.1	mA
		10 Mbps	I_{DD_IO}		4.8	6.7	mA
			I_{ISOIN}		5.9	8.1	mA
		100 Mbps	I_{DD_IO}		8.4	10.8	mA
			I_{ISOIN}		15.1	24.3	mA

(1) V_{CCI} = V_{IO} or V_{ISOIN}

ADVANCE INFORMATION

7.15 Electrical Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 2.5-V

V_{IO}, V_{ISOIN} = 2.5 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 x V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 x V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 x V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	-25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –4 mA, see TBD	V_{SO} (1) – 0.1			V
V_{OL}	Low level output voltage	I_O = 4 mA, see TBD			0.1	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see TBD		100		kV/us

(1) V_{SI} = input side supply; V_{SO} = output side supply

7.16 Supply Current Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 2.5-V

V_{IO}, V_{ISOIN} = 2.5 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW7741 Channel Supply Current							
Supply current - Disable	EN_IO1 = EN_IO2 = 0 V; V_I = V_{CCI} (1) (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.7	4.3	mA
			I_{ISOIN}		4.2	6.3	mA
	EN_IO1 = EN_IO2 = 0 V; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		2.7	4.3	mA
			I_{ISOIN}		4.2	6.3	mA
Channel Supply current - DC signal	EN_IO1 = EN_IO2 = V_{CCI}; V_I = V_{CCI} (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.7	4.3	mA
			I_{ISOIN}		4.2	6.3	mA
	EN_IO1 = EN_IO2 = V_{CCI}; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		6.1	8.3	mA
			I_{ISOIN}		5.4	7.9	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DD_IO}		4.4	6.3	mA
			I_{ISOIN}		4.9	7.1	mA
		10 Mbps	I_{DD_IO}		4.7	8.3	mA
			I_{ISOIN}		5.6	7.9	mA
		100 Mbps	I_{DD_IO}		7.5	9.7	mA
			I_{ISOIN}		12.6	18.8	mA

(1) V_{CCI} = V_{IO} or V_{ISOIN}

7.17 Electrical Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 1.8-V

V_{IO}, V_{ISOIN} = 1.8 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 x V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 x V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 x V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	-25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –4 mA, see TBD	V_{SO} (1) – 0.1			V
V_{OL}	Low level output voltage	I_O = 4 mA, see TBD			0.1	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see TBD		100		kV/us

(1) V_{SI} = input side supply; V_{SO} = output side supply

7.18 Supply Current Characteristics Channel Isolator - V_{IO}, V_{ISOIN} = 1.8-V

V_{IO}, V_{ISOIN} = 1.8 V ±5% (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW7741 Channel Supply Current							
Supply current - Disable	EN_IO1 = EN_IO2 = 0 V; V_I = V_{CCI} (1) (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.4	3.6	mA
			I_{ISOIN}		3.8	4.6	mA
	EN_IO1 = EN_IO2 = 0 V; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		2.4	3.6	mA
			I_{ISOIN}		3.8	4.6	mA
Channel Supply current - DC signal	EN_IO1 = EN_IO2 = V_{CCI}; V_I = V_{CCI} (ISOW7741); V_I = 0 V (ISOW7741 with F suffix)		I_{DD_IO}		2.4	3.6	mA
			I_{ISOIN}		3.8	4.6	mA
	EN_IO1 = EN_IO2 = V_{CCI}; V_I = 0 V (ISOW7741); V_I = V_{CCI} (ISOW7741 with F suffix)		I_{DD_IO}		5.5	8	mA
			I_{ISOIN}		5	6	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DD_IO}		4.4	6.3	mA
			I_{ISOIN}		4.9	7.1	mA
		10 Mbps	I_{DD_IO}		4.6	6.5	mA
			I_{ISOIN}		5.4	7.6	mA
		100 Mbps	I_{DD_IO}		6.2	8.3	mA
			I_{ISOIN}		10	14.5	mA

(1) V_{CCI} = V_{IO} or V_{ISOIN}

ADVANCE INFORMATION

7.19 Switching Characteristics - 5-V Supply

V_{IO} = V_{ISOIN} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See TBD	6	10.7	15.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See TBD		1	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.4	ns
t_r	Output signal rise time	See TBD		1.9	4	ns
t_f	Output signal fall time	See TBD		1.9	4	ns
t_{PHZ}	Channel disable propagation delay, high-to-high impedance output	See TBD		24.5	33.2	ns
t_{PLZ}	Channel disable propagation delay, low-to-high impedance output	See TBD		24.5	33.2	ns
t_{PZH}	Channel enable propagation delay, high impedance-to-high output for ISOW7741	See TBD		26.2	33.1	ns
	Channel enable propagation delay, high impedance-to-high output for ISOW7741 with F suffix	See TBD		26.2	33.1	ns
t_{PZL}	Channel enable propagation delay, high impedance-to-low output for ISOW7741	See TBD		25.8	33.1	ns
	Channel enable propagation delay, high impedance-to-low output for ISOW7741 with F suffix	See TBD		25.8	33.1	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{IO} or V_{ISOIN} goes below 1.6 V at 10 mV/ns. See TBD		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.8		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

7.20 Switching Characteristics - 3.3-V Supply

V_{IO} = V_{ISOIN} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See TBD	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See TBD		0.1	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See TBD		0.62	4	ns
t_f	Output signal fall time	See TBD		0.62	4	ns
t_{PHZ}	Channel disable propagation delay, high-to-high impedance output	See TBD		29.3	42	ns
t_{PLZ}	Channel disable propagation delay, low-to-high impedance output	See TBD		29.3	39	ns
t_{PZH}	Channel enable propagation delay, high impedance-to-high output for ISOW7741	See TBD		29.9	40	ns
	Channel enable propagation delay, high impedance-to-high output for ISOW7741 with F suffix	See TBD		29.9	41	ns
t_{PZL}	Channel enable propagation delay, high impedance-to-low output for ISOW7741	See TBD		28.8	41	ns
	Channel enable propagation delay, high impedance-to-low output for ISOW7741 with F suffix	See TBD		28.8	41	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{IO} or V_{ISOIN} goes below 1.6 V at 10mV/ns. See TBD		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.9		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

7.21 Switching Characteristics - 2.5-V Supply

V_{IO} = V_{ISOIN} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See TBD	7.5	12	18	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.6	ns
t_r	Output signal rise time	See TBD		0.9	4	ns
t_f	Output signal fall time			0.9	4	ns
t_{PHZ}	Channel disable propagation delay, high-to-high impedance output	See TBD		36.2	54.6	ns
t_{PLZ}	Channel disable propagation delay, low-to-high impedance output			36.2	54.6	ns
t_{PZH}	Channel enable propagation delay, high impedance-to-high output for ISOW7741			35.9	49.2	ns
	Channel enable propagation delay, high impedance-to-high output for ISOW7741 with F suffix			35.9	49.2	ns
t_{PZL}	Channel enable propagation delay, high impedance-to-low output for ISOW7741			34.3	52.5	ns
	Channel enable propagation delay, high impedance-to-low output for ISOW7741 with F suffix			34.3	52.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{IO} or V_{ISOIN} goes below 1.6 V at 10 mV/ns. See TBD		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.7		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

7.22 Switching Characteristics - 1.8-V Supply

VIO = V_{ISOIN} = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See TBD	7.5	15	22.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	5.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.6	ns
t_r	Output signal rise time	See TBD		2.2	4	ns
t_f	Output signal fall time			2.2	4	ns
t_{PHZ}	Channel disable propagation delay, high-to-high impedance output	See TBD		53	80.2	ns
t_{PLZ}	Channel disable propagation delay, low-to-high impedance output			53	80.2	ns
t_{PZH}	Channel enable propagation delay, high impedance-to-high output for ISOW774x			52.6	69.5	ns
	Channel enable propagation delay, high impedance-to-high output for ISOW774x with F suffix			52.6	69.5	ns
t_{PZL}	Channel enable propagation delay, high impedance-to-low output for ISOW774x			49.6	76.7	ns
	Channel enable propagation delay, high impedance-to-low output for ISOW774x with F suffix			49.6	76.7	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{IO} or V_{ISOIN} goes below 1.6 V at 10mV/ns. See TBD		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.7		ns

(1) Also known as pulse skew.

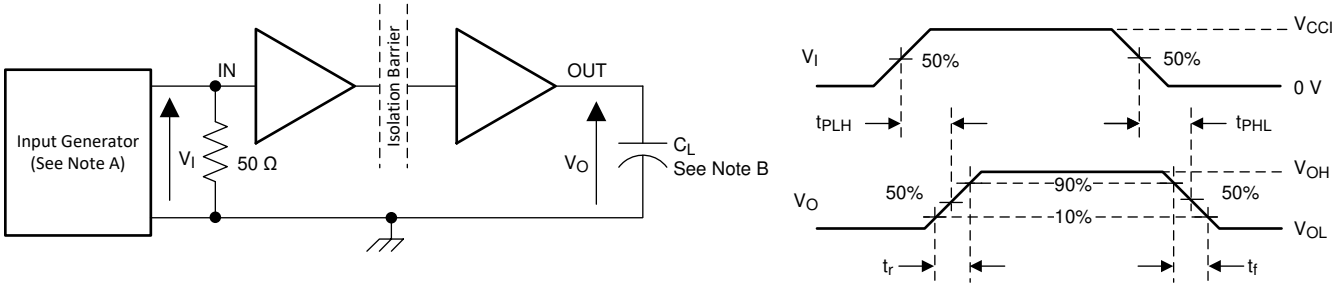
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

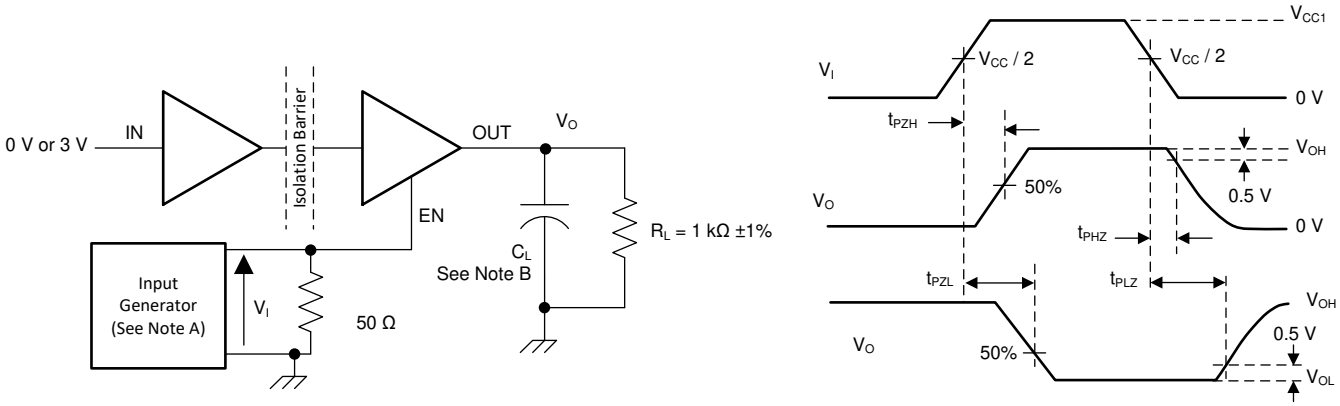
8 Parameter Measurement Information

In the below images, V_{CCI} and V_{CCO} refers to the power supplies V_{IO} and V_{ISOIN}, respectively.



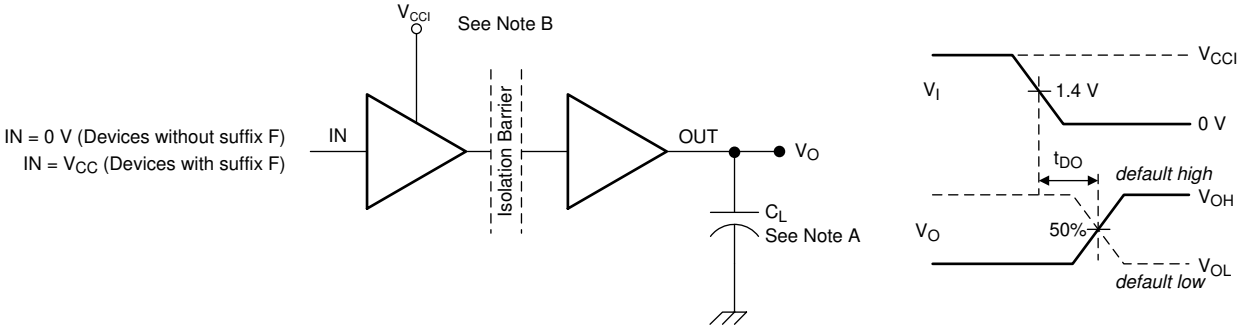
A. C_L = 15 pF and The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
B. B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
B. B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

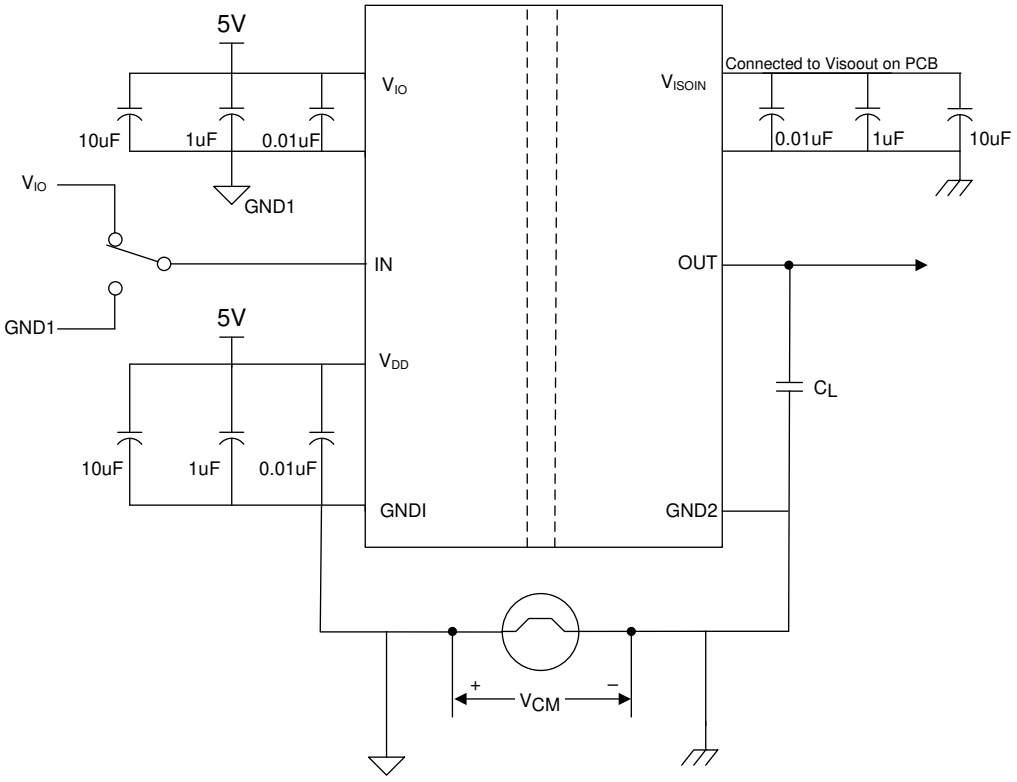
Figure 8-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



A. A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. B. Power Supply Ramp Rate = 10 mV/ns.

Figure 8-3. Default Output Delay Time Test Circuit and Voltage Waveforms

ADVANCE INFORMATION



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. Optional 100 µF capacitor can be added between V_{DD} and GND1; refer to *Section 11*.
C. Pass-fail criteria: Outputs must remain stable.

Figure 8-4. Common-Mode Transient Immunity Test Circuit

ADVANCE INFORMATION

9 Detailed Description

9.1 Overview

The ISOW7741 device has a low-noise, low-emissions isolated DC-DC converter, and four high- speed isolated data channels. Section 9.2 shows the functional block diagram of the ISOW7741 device.

9.1.1 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve upto 45% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. Output voltage of power converter can be controlled to 3.3 V or 5 V using V_{SEL} pin. The DC-DC converter can be switched off using the EN_DCDC (enable) pin to save power. The output voltage, V_{ISOOUT} , is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel. V_{ISOOUT} needs to be connected to V_{ISOIN} to ensure the feedback channel is properly powered to regulate the DC-DC converter. This can be achieved by connecting the pins directly or through an LDO that remains powered up at all times. A ferrite bead is recommended between Visoout and Visoin to further reduce emissions. See the Section 10.2 section. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{IO}, V_{DD} and V_{ISOIN} supplies which ensures robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

9.1.2 Signal Isolation

The integrated signal isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. Figure 9-1 shows a functional block diagram of a typical signal isolation channel. In order to keep any noise coupling from power converter away from signal path, power supplies on side 1 for power converter (V_{DD}) and signal path(V_{IO}) are kept separate. Similarly on side 2, power converter output (V_{ISOOUT}) needs to be connected to V_{ISOIN} externally on PCB. Emissions can be further improved by placing a ferrite bead between V_{ISOOUT} and V_{ISOIN} as well as between the GND2 pins. For more details, refer to the Layout Guidelines section.

9.2 Functional Block Diagram

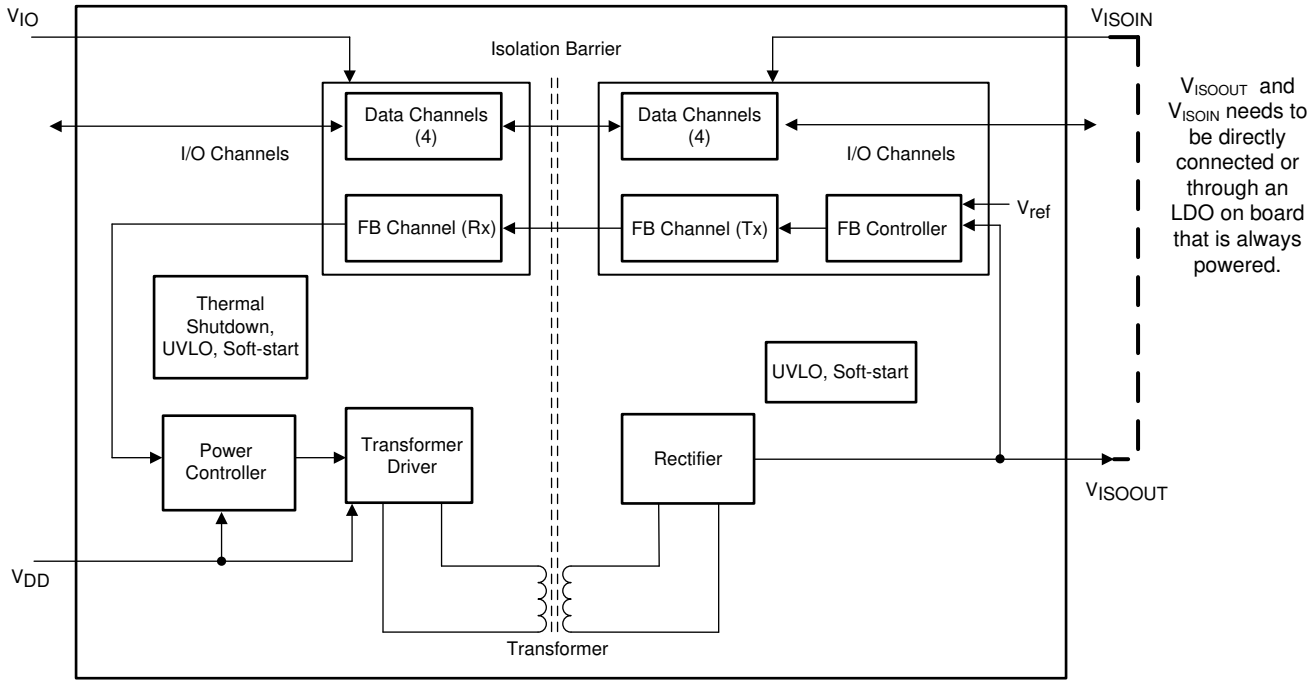


Figure 9-1. Block Diagram

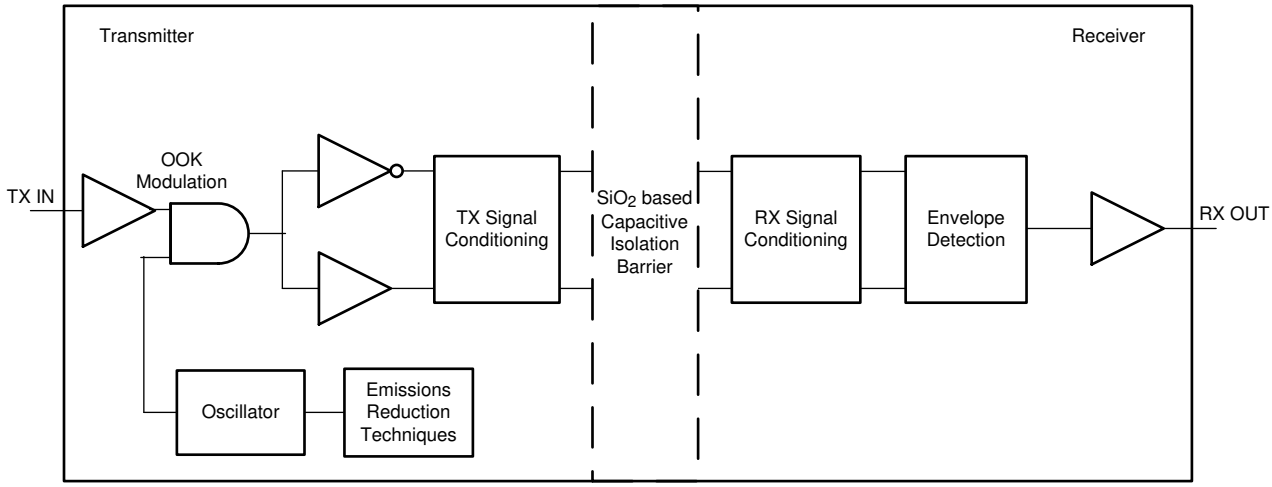


Figure 9-2. Conceptual Block Diagram of a Capacitive Data Channel

ADVANCE INFORMATION

Figure 9-3 shows a conceptual detail of how the OOK scheme works.

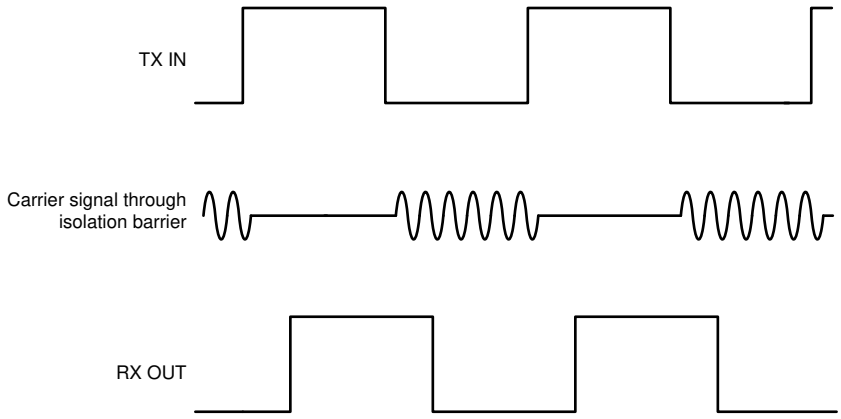


Figure 9-3. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

Table 9-1 shows an overview of the device features.

Table 9-1. Device Features

PART NUMBER 1	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT STATE	RATED ISOLATION 2
ISOW7741	3 forward, 1 reverse	100 Mbps	High	5 kV_{RMS} / 7071 V_{PK}
ISOW7741F			Low	

1. The F suffix is part of the orderable part number. See the *Section 14* section for the full orderable part number.
2. For detailed isolation ratings, see the Section 7.7 table.

9.3.1 Electromagnetic Compatibility (EMC) Considerations

The ISOW7741 device uses emissions reduction schemes for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISOW7741 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.
- Power path and signal path separated to minimize internal high frequency coupling and allowing for an external filtering knob using ferrite beads available to further reduce emissions
- Reduced power converter switching frequency to 25 Mhz to reduce strength of high frequency components in emissions spectrum

9.3.2 Power-Up and Power-Down Behavior

The ISOW7741 device has built-in UVLO on the V_{IO}, V_{DD}, and V_{ISOIN} supplies with positive-going and negative-going thresholds and hysteresis. Both the power converter supply (VDD) and logic supply (VIO) need to be present for the device to work. If either of them is below its UVLO, both the signal path and the power converter are disabled.

When the V_{DD} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{DD} supply and charges the V_{ISOOUT} output in a controlled manner, avoiding overshoots. Outputs of the isolated data channels are in an indeterminate state until the V_{IO} or V_{DD} voltage crosses the positive-going UVLO threshold. When the UVLO positive-going threshold is crossed on the secondary side V_{ISOOUT} pin, the feedback data channel starts providing feedback to the primary controller. The regulation loop takes over and the isolated data channels go to the normal state defined by the respective input channels or their default states. Design should consider a sufficient time margin (typically 10 ms with 10-µF load capacitance) to allow this power up sequence before valid data channels are accounted for system functionality.

When either V_{IO} or V_{DD} power is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISOOUT} capacitor then discharges depending on the external load. The isolated data outputs on the V_{ISOIN} side are returned to the default state for the brief time that the V_{ISOIN} voltage takes to discharge to zero.

9.3.3 Protection Features

The ISOW7741 devicehas multiple protection features to create a robust system level solution.

- The first feature is an Enable DC-DC /fault protection feature. This pin can be used as either an input pin to enable or disable the integrated DC-DC power converter or as an output pin which works as an alert signal if the power converter is not operating properly. In the /fault use case, a fault is reported if V_{DD} > 7 V, V_{DD} < 2.5 V, or if the junction temperature >170°C. When a fault is detected, this pin will go low, disabling the DC-DC converter to prevent any damage.

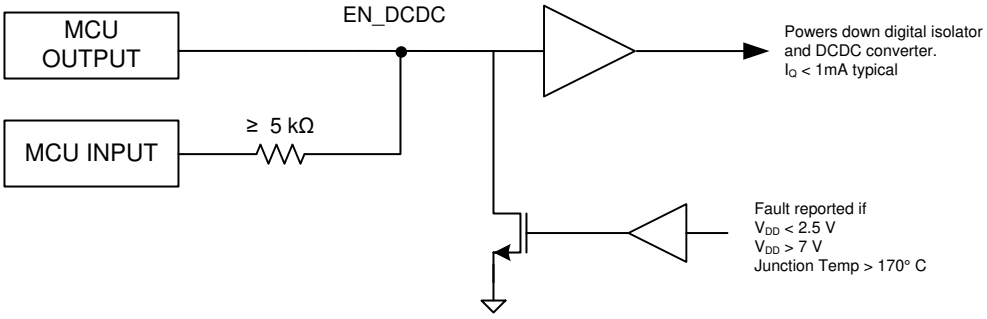


Figure 9-4. EN_DCDC Fault Pin Diagram

- Over-voltage lock out on V_{DD} will occur when a voltage higher than 7 V is seen. The device will go into a low power state and the EN_DCDC pin will go low. It is highly recommended that the V_{DD} abs max condition of 6V is not violated.
- An over-voltage clamp feature is present on V_{ISOOUT} which will clamp the voltage at 6V if there is an increase in voltage seen.
- The device is protected against output overload and short circuit. Output voltage starts dropping when the power converter is not able to deliver the current demanded during overload conditions. For a V_{ISO} short-circuit to ground, the duty cycle of the converter is limited to help protect against any damage.
- The device is protected against output overload and short circuit. Output voltage starts dropping when the power converter is not able to deliver the current demanded during overload conditions. For a V_{ISO} short-circuit to ground, the duty cycle of the converter is limited to help protect against any damage.
- The device is protected against output overload and short circuit. Output voltage starts dropping when the power converter is not able to deliver the current demanded during overload conditions. For a V_{ISO} short-circuit to ground, the duty cycle of the converter is limited to help protect against any damage.

ADVANCE INFORMATION

- Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the temperature goes above 165°C, thermal shutdown activates and the primary controller turns off which removes the energy supplied to the V_{ISO} load, which causes the device to cool off. When the junction temperature goes below 150°C, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the design to prevent the device junction temperatures from reaching such high values.

9.4 Device Functional Modes

The below table lists the supply configurations for these devices.

Table 9-2. Supply Configuration Function Table

V_{DD} (1)	V_{IO}	MODE	V_{ISOOUT} (3)
< $V_{DD(UVLO+)}$	>$V_{IO(UVLO+)}$	X	OFF
>$V_{DD(UVLO+)}$	<$V_{IO(UVLO+)}$	X	OFF
5 V	1.71 V to 5.5 V	High(shorted to V_{ISOOUT})	5 V
5 V or 3.3 V	1.71 V to 5.5 V	Low(shorted to GND2) or floating (2)	3.3 V

(1) V_{DD}= 3.3 V, MODE shorted to V_{ISOOUT}(essentially V_{ISOOUT} = 5 V) is not the recommended mode of operation
(2) The MODE pin has a weak pulldown internally. Therefore for V_{ISOOUT} = 3.3 V, the MODE pin should be strongly connected to the GND2 pin in noisy system scenarios.
(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB and both GND2 pins are shorted to each other and EN=High

Table 9-3 lists the channel isolators functional modes for these devices.

Table 9-3. Channel Isolator Function Table

INPUT SUPPLY (V_{IO}) (1)	OUTPUT SUPPLY (V_{ISOIN})	INPUT (INx)	IO ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or Open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or Open	L	
		Open	H or Open	Default	Default mode(2): When INx is open, the corresponding channel output goes to its default logic state.
		X	L	Z and Default	A low value of output enable causes the outputs of the same side to be high impedance. The output of opposite side will be Default if opposite side IO ENABLE is H or open.
PD	PU	X	H or Open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is High for ISOW7741 and Low for ISOW7741 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.

(1) PU = Powered up (V_{IO} > 1.7 V, V_{ISOIN} > 1.7 V); PD = Powered down (V_{IO} < 1 V, V_{ISOIN} < 1 V); X = Irrelevant; H = High level; L = Low level, V_{CC} = Input-side supply
(2) In the default condition, the output is high for the ISOW7741 device with the F suffix.

ADVANCE INFORMATION

9.4.1 Device I/O Schematics

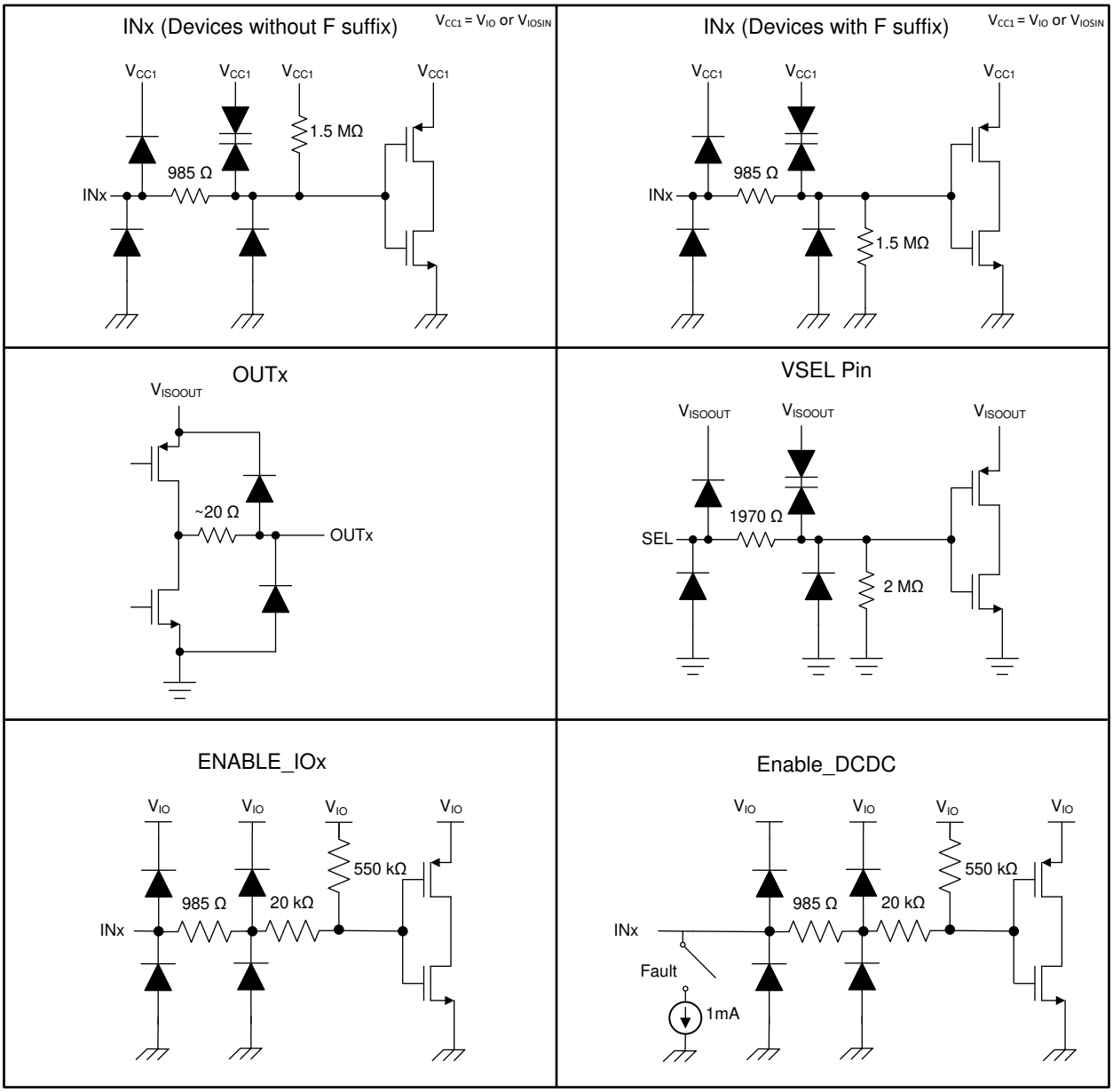


Figure 9-5. Device I/O Schematics

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The device is a high-performance, quad channel digital isolator with integrated DC-DC converter. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to the integrated DC-DC converter in the device, the isolated supply is generated inside the device that can be used to power isolated side of the device and peripherals on isolated side, thus saving board space. The device uses single-ended CMOS-logic switching technology. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is Microcontroller or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

The device is suitable for applications that have limited board space and desire more integration. The device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

10.2 Typical Application

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Design TIDA-01333, *Eight-Channel, Isolated, High-Voltage Analog Input Module With ISOW7841 Reference Design*.

Figure 10-1 shows the typical schematic for SPI isolation.

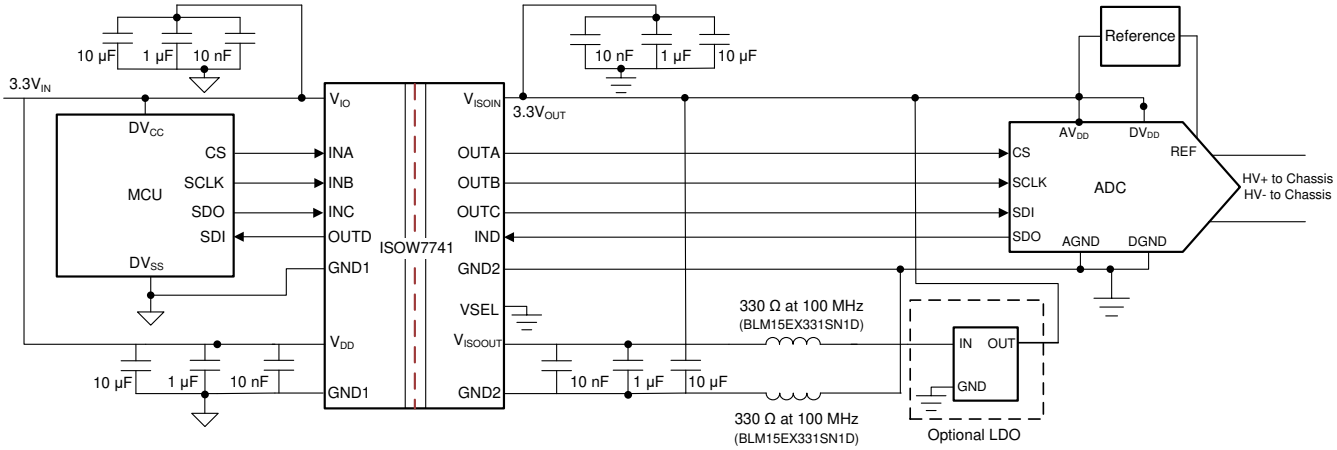


Figure 10-1. Isolated Power and SPI for ADC Sensing Application with ISOW7741

ADVANCE INFORMATION

10.2.1 Design Requirements

To design with this device, use the parameters listed in Table 10-1.

Table 10-1. Design Parameters

PARAMETER	VALUE
Input voltage	3 V to 5.5 V
Decoupling capacitor between V_{DD} and GND1	0.01 µF to 20 µF
Decoupling capacitor between V_{ISOOUT} and GND2	0.01 µF to 20 µF

Because of very-high current flowing through the ISOW7741 device device V_{DD} and V_{ISOOUT} supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10-µF capacitor is adequate, higher decoupling capacitors (such as 47 µF) on both the V_{DD} and V_{ISOOUT} pins to the respective grounds are strongly recommended to achieve the best performance.

10.2.2 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 10-2 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 10-3 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000 V_{RMS} with a lifetime of 1184 years.

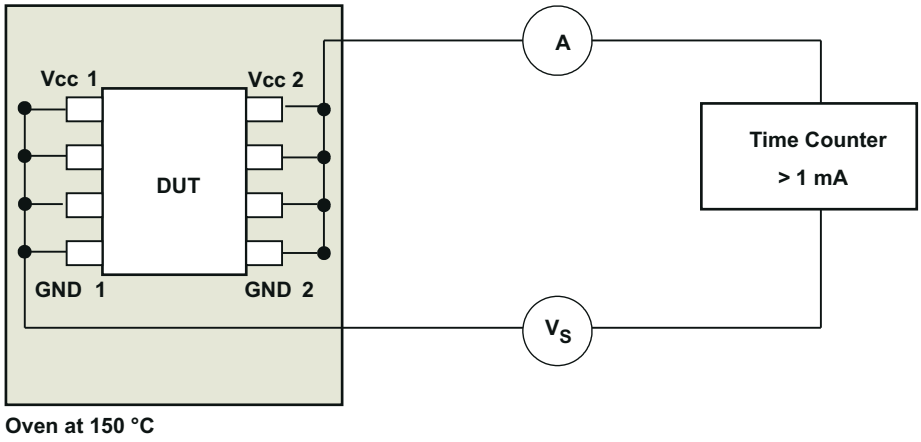


Figure 10-2. Test Setup for Insulation Lifetime Measurement

ADVANCE INFORMATION

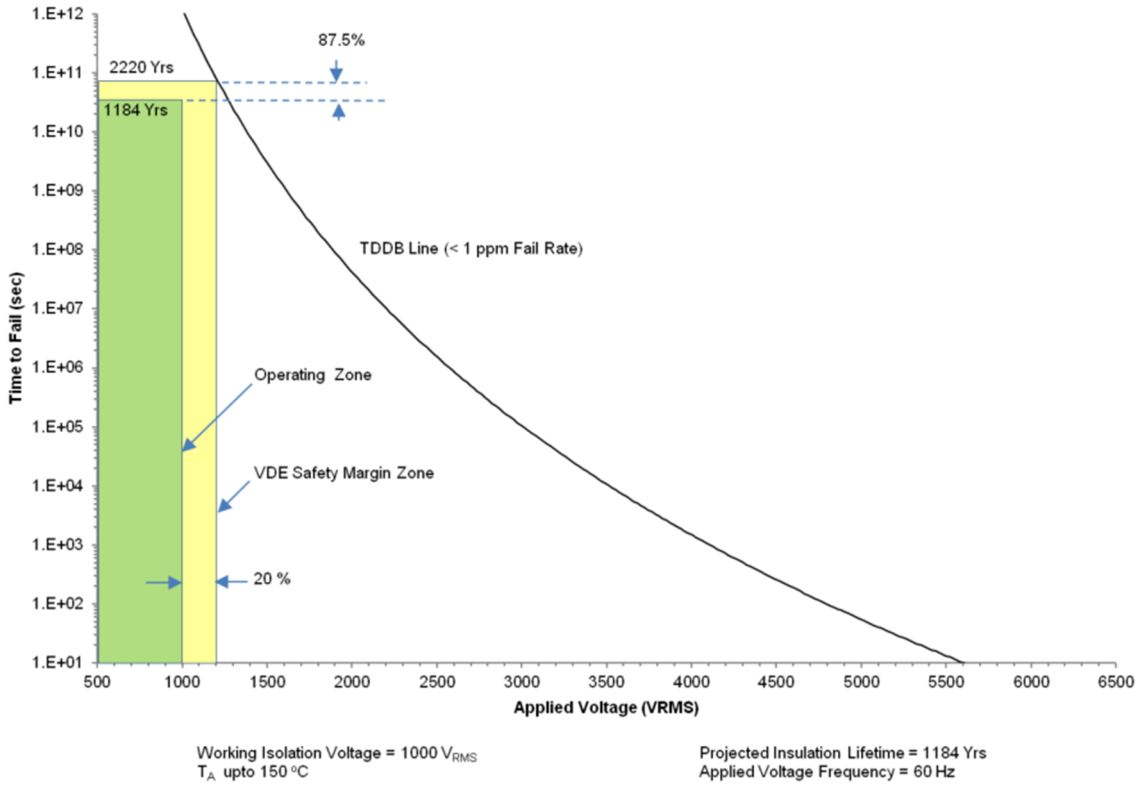


Figure 10-3. Insulation Lifetime Projection Data

11 Power Supply Recommendations

To help make sure that operation is reliable at data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. V_{ISOOUT} needs to be connected to V_{ISOIN} to ensure the feedback channel is properly powered to regulate the DC-DC converter. This can be achieved by connecting the pins directly or through an LDO that remains powered up at all times. A ferrite bead is recommended between V_{ISOOUT} and V_{ISOIN} to further reduce emissions. If $V_{ISOOUT}$and V_{ISOIN} are not connected, the DC-DC converter will run open loop and the V_{ISOOUT} voltage will drift until the over-voltage clamp clamps at 6 V. The input supply (V_{IO} and V_{DD}) must have an appropriate current rating to support output load and switching at the maximum data rate required by the end application. For more information, refer to the Section 10.2 section.

For an output load current of 110 mA, it is recommended to have >600 mA of input current limit and for lower output load currents, the input current limit can be proportionally lower.

ADVANCE INFORMATION

12 Layout

12.1 Layout Guidelines

A low cost two layer PCB should be sufficient to achieve good EMC performance:

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Because the device has no thermal pad to dissipate heat, the device dissipates heat through the respective GND pins. Ensure that enough copper is present on both GND pins to prevent the internal junction temperature of the device from rising to unacceptable levels.

Figure 12-1 shows the recommended placement and routing of device bypass capacitors. Below guidelines must be followed to meet application EMC requirements:

- High frequency bypass capacitors 10 nF must be placed close to V_{DD} and V_{ISOOUT} pins, less than 2 mm distance away from device pins. This is very essential for optimised radiated emissions performance. Ensure that these capacitors are 0402 size so that they offer least inductance (ESL).
- Bulk capacitors of atleast 10 µF must be placed on power converter input (V_{DD}) and output (V_{ISOOUT}) supply pins.
- Traces on V_{DD} and GND1 must be symmetric till bypass capacitors. Similarly traces on V_{ISOOUT} and GND2 must be symmetric.
- Place two 0402 size Ferrite beads (Part number: BLM15EX331SN1) on V_{ISOOUT} and GND2 path so that any high frequency noise from power converter output sees a high impedance before it goes to other components on PCB.
- Do not have any metal traces or ground pour within 4 mm of power converter output terminals V_{ISOOUT} pin12 and GND2 pin11. VSEL pin is also in V_{ISOOUT} domain and should be shorted to either pin 11 or pin 12 for output voltage selection.
- Following the layout guidelines of EVM as much as possible is highly recommended for a low radiated emissions design.

12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.2 Layout Example

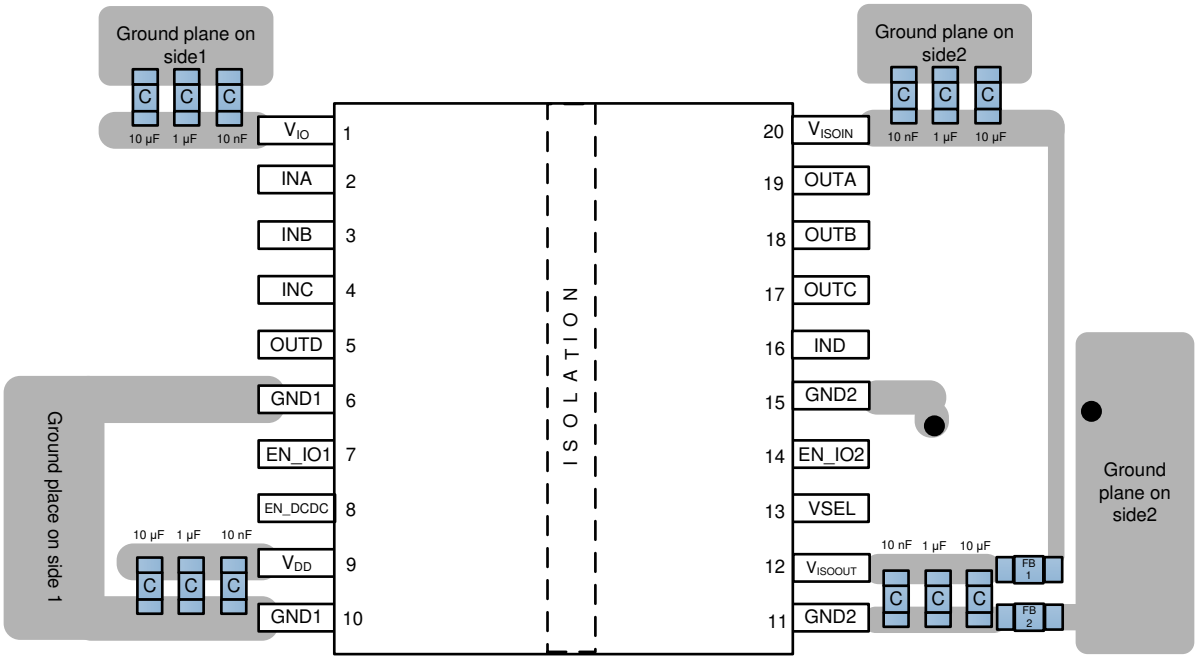


Figure 12-1. Layout Example

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

For development support, refer to:

- 8-ch Isolated High Voltage Analog Input Module with ISOW7841 Reference Design
- Isolated RS-485 With Integrated Signal and Power Reference Design
- Isolated RS-232 With Integrated Signal and Power Reference Design

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

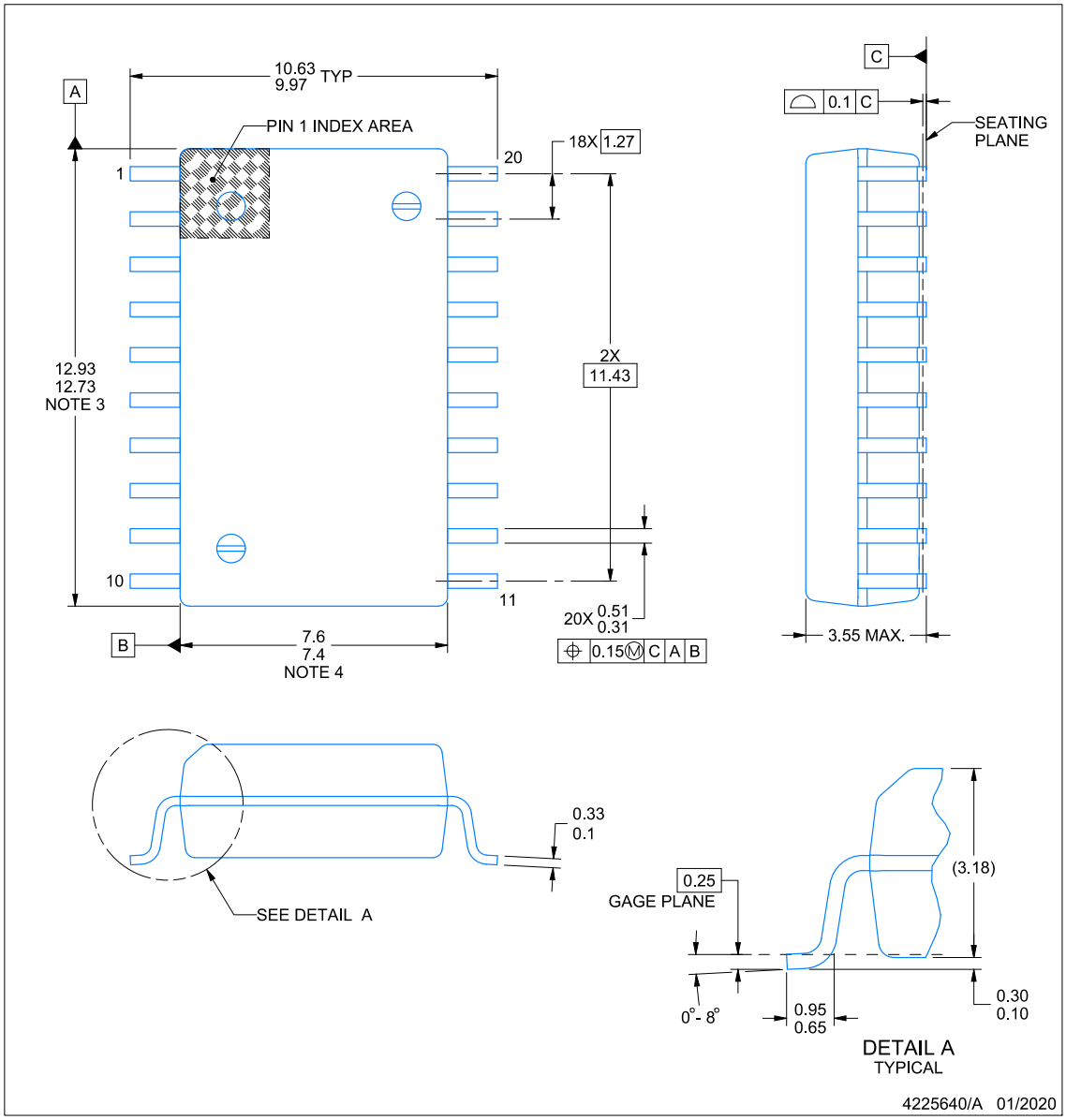
ADVANCE INFORMATION

PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES:

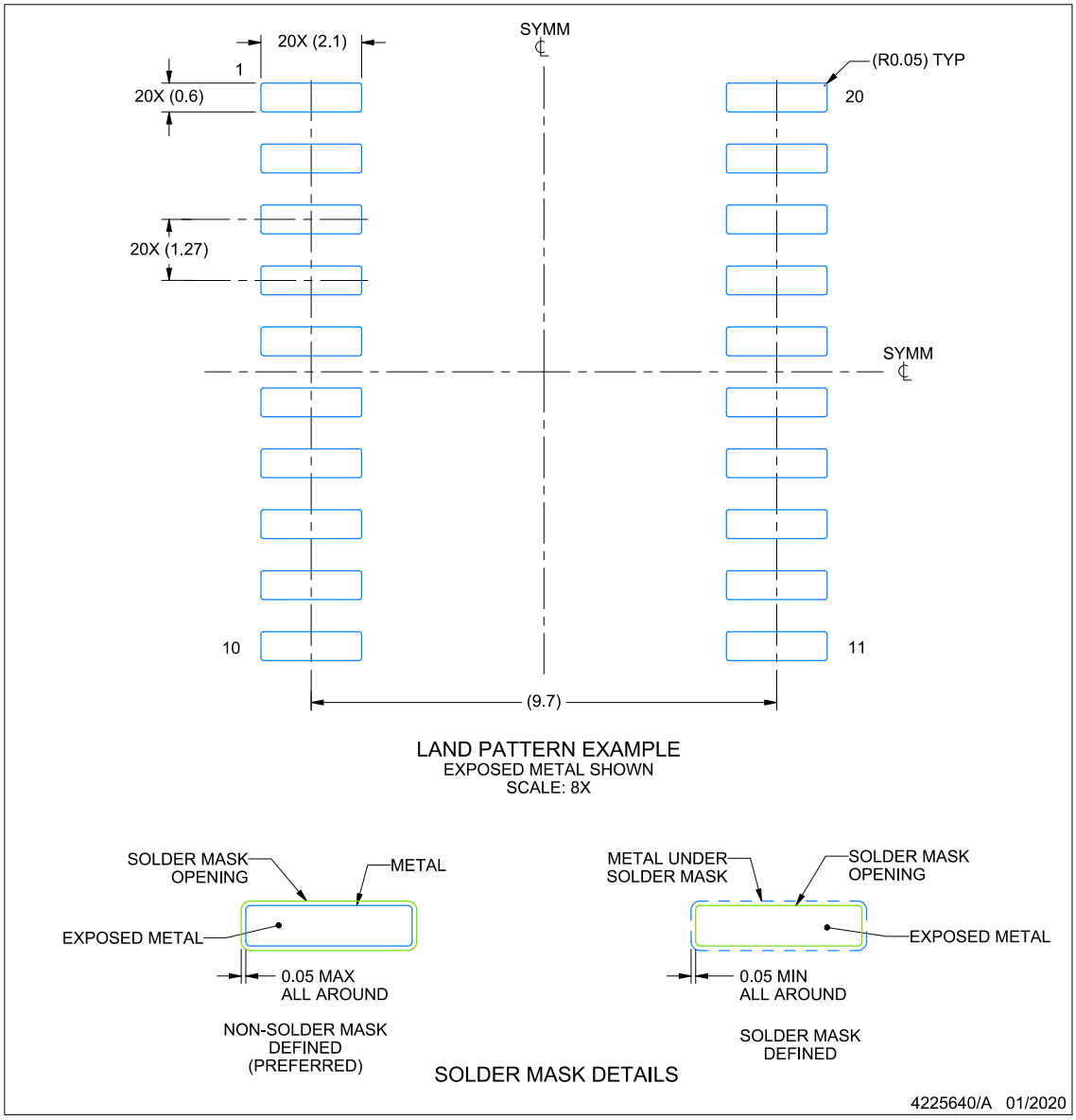
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

EXAMPLE BOARD LAYOUT

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

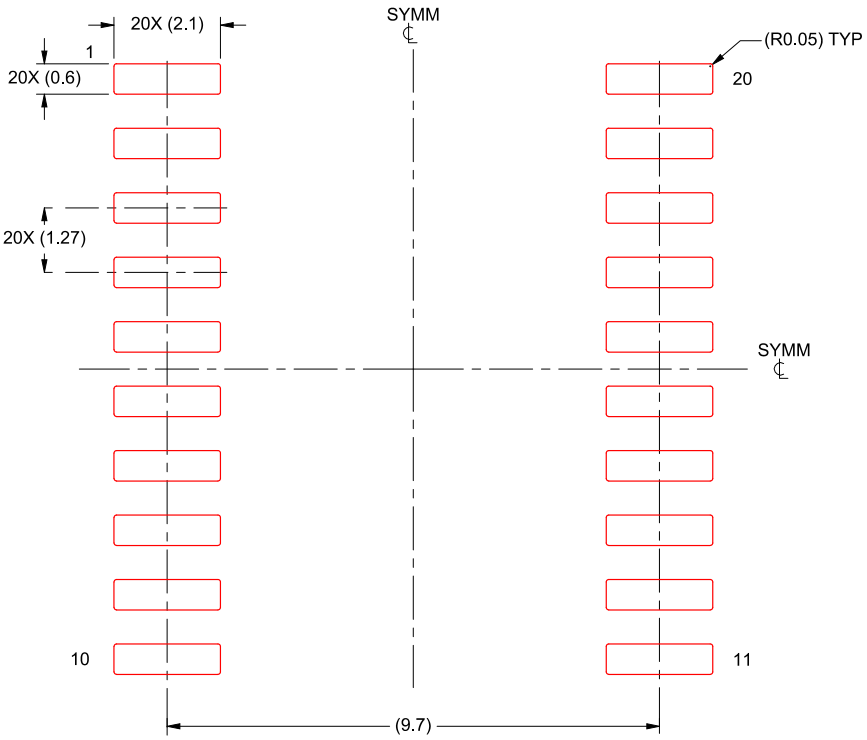
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DFM0020A — **SOIC - 3.55 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225640/A 01/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOW7741DFM	PREVIEW	SOIC	DFM	20	40	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		
ISOW7741DFMR	PREVIEW	SOIC	DFM	20	2000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		
ISOW7741FDFM	PREVIEW	SOIC	DFM	20	40	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		
ISOW7741FDFMR	PREVIEW	SOIC	DFM	20	2000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		
XISOW7741DFMR	ACTIVE	SOIC	DFM	20	2000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples
XISOW7741FDFMR	ACTIVE	SOIC	DFM	20	2000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265