DS100MB201 Dual Lane 2:1/1:2 Mux/Buffer with Equalization

Check for Samples: DS100MB201

FEATURES

- **Up to 10.3125 Gbps**
- **Dual Lane 2:1 Mux, 1.2 Switch or Fanout**
- **Adjustable Transmit Differential Output Voltage (V_{OD})**
- **<0.3 UI of Residual DJ at 10.3125 Gbps with 10” FR4 trace**
- **Adjustable Electrical IDLE Detect Threshold**
- **Signal Conditioning Programmable through SMBus I/F**
- **Single 2.5V Supply Operation**
- **>6 kV HBM ESD Rating**
- **3.3V Tolerant SMBus Interface**
- **High Speed Signal flow–thru Pinout**
- **Package: 54-pin WQFN (10 mm x 5.5 mm)**

APPLICATIONS

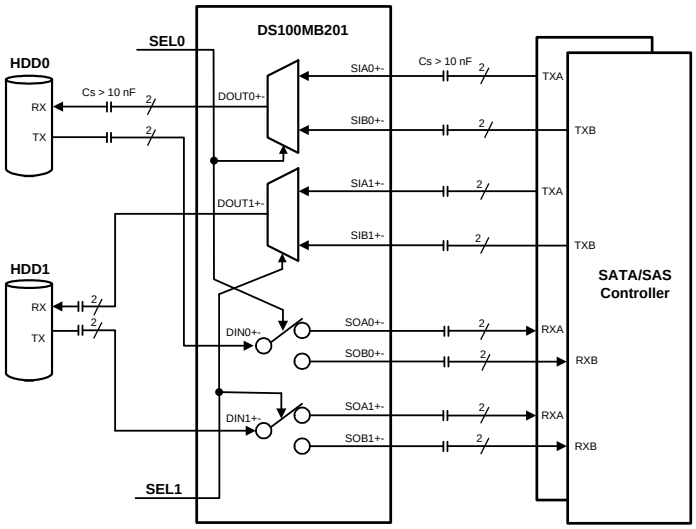
- **XAUI (3.125 Gbps), RXAUI (6.25 Gbps)**
- **sRIO – Serial Rapid I/O**
- **Fibre Channel (8.5 Gbps)**
- **10GBase-CX4, InfiniBand (QDR, SDR & DDR)**
- **FR4 Backplane Traces**

DESCRIPTION

The DS100MB201 is a dual lane 2:1 multiplexer and 1:2 switch or fan-out buffer with signal conditioning suitable for 10GE, Fibre Channel, Infiniband, SATA/SAS and other high-speed bus applications up to 10.31215 Gbps. The device performs receive equalization allowing maximum flexibility of physical placement within a system. The receiver's continuous time linear equalizer (CTLE) provides a boost to compensate for 10” of 4 mil FR4 stripline at 10.3125 Gbps. The DS100MB201 is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium. The transmitter features a programmable amplitude voltage levels to be selected from 600 mVp-p to 800 mVp-p. The signal conditioning settings are programmable with register control.

With a typical power consumption of 100 mW/channel at 10.3125 Gbps, and SMBus register control to turn-off unused lanes, the DS100MB201 is part of TI's PowerWise family of energy efficient devices.

Typical Application



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Pin Diagram

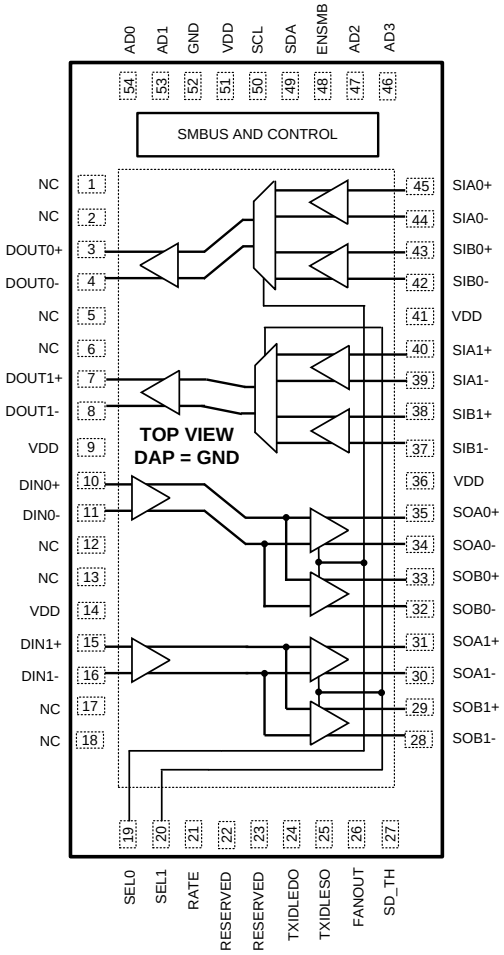


Figure 1. DS100MB201 Pin Diagram 54L WQFN Package
See Package Number NJY0054A

PIN DESCRIPTIONS(1)

Pin Name	Pin Number	I/O, Type(2)(3)(4)	Pin Description
Differential High Speed I/O's			
SIA0+, SIA0-, SIA1+, SIA1-	45, 44, 40, 39	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects SIA_n+ to VDD and SIA_n- to VDD when enabled.
SOA0+, SOA0-, SOA1+, SOA1-	35, 34, 31, 30	O	Inverting and non-inverting low power differential signaling 50Ω outputs. Fully compatible with AC coupled CML inputs.
SIB0+, SIB0-, SIB1+, SIB1-	43, 42, 38, 37	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects SIB_n+ to VDD and SIB_n- to VDD when enabled.
SOB0+, SOB0-, SOB1+, SOB1-	33, 32, 29, 28	O	Inverting and non-inverting low power differential signaling 50Ω outputs. Fully compatible with AC coupled CML inputs.
DIN0+, DIN0-, DIN1+, DIN1-	10, 11, 15, 16	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects SIB_n+ to VDD and SIB_n- to VDD when enabled.

(1) 1 = HIGH, 0 = LOW, FLOAT = 3rd input state.
(2) FLOAT condition; Do not drive pin; pin is internally biased to mid level with 50 kΩ pull-up/pull-down.
(3) Internal pulled-down = Internal 30 kΩ pull-down resistor to GND is present on the input.
(4) Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.

PIN DESCRIPTIONS[1] (continued)

Pin Name	Pin Number	I/O, Type[2][3][4]	Pin Description
DOUT0+, DOUT0-, DOUT1+, DOUT1-	3, 4, 7, 8	O	Inverting and non-inverting low power differential signaling 50Ω outputs. Fully compatible with AC coupled CML inputs.
Control Pins — (LVCMOS)			
ENSMB	48	I, LVCMOS w/ internal pull-down	System Management Bus (SMBus) enable pin. LOW = Reserved HIGH = Register Access: Provides access to internal digital registers to control such functions as equalization, VOD, channel powerdown, and idle detection threshold. Please refer to System Management Bus (SMBus) and Configuration Registers for detailed information.
SDA	49	I, LVCMOS	The SMBus bi-directional SDA pin. Data input or open drain output. External pull-up resistor is required. Refer to R_{term} in the SMBus specification.
SCL	50	I, LVCMOS	SMBUS clock input pin. External pull-up resistor maybe needed. Refer to R_{term} in the SMBus specification.
AD[3:0]	46, 47, 53, 54	I, LVCMOS w/ internal pull-down	SMBus Slave Address Inputs. These pins set the SMBus address.
Control Pins — (LVCMOS)			
RATE	21	I, Float, LVCMOS	LOW = Reserved HIGH = 10.3125 Gbps operation
TXIDLEDO	24	I, Float, LVCMOS	TXIDLEDO, 3–level input controls the driver output. LOW = disable the signal detect/squelch function for DOUT. FLOAT = enable the signal auto detect/squelch function for DOUT and the signal detect voltage threshold level can be adjusted using the SD_TH pin. HIGH = force the DOUT to be muted (electrical idle). See Table 1
TXIDLESO	25	I, Float, LVCMOS	TXIDLESO, 3–level input controls the driver output. LOW = disable the signal detect/squelch function for SOUT. FLOAT = enable the signal auto detect/squelch function for SOUT and the signal detect voltage threshold level can be adjusted using the SD_TH pin. HIGH = force the SOUT to be muted (electrical idle). See Table 1
FANOUT	26	I, LVCMOS w/ internal pull-down	LOW = disable one of the outputs depending on the SEL0, SEL1 pin. HIGH = enable both A/B outputs for broadcast mode. FANOUT = 0 See Table 3
SEL0, SEL1	19, 20	I, LVCMOS w/ internal pull-down	SEL0 is for lane 0, SEL1 is for lane 1 SEL0, SEL1 = 0 selects B input and B output. SEL0, SEL1 = 1 selects A input and A output. See Table 3
Reserved	52	I, LVCMOS	**Tie to GND**
Analog			
SD_TH	27	I, ANALOG	Threshold select pin for electrical idle detect threshold. Float pin for default 130 mVp-p (differential). See Table 2
Power			
VDD	9, 14, 36, 41, 51	Power	2.5V Power supply pins.
GND	DAP	Power	DAP is the large metal contact at the bottom side, located at the center of the 54 pin LLP package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.
Reserved	1, 2, 5, 6, 12, 13, 17, 18, 22, 23		No Connect — **Leave pin open**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (VDD)		-0.5V to +3.0V
LVCMOS Input/Output Voltage		-0.5V to +4.0V
Differential Input Voltage		-0.5V to (VDD+0.5V)
Differential Output Voltage		-0.5V to (VDD+0.5V)
Analog (SD_TH)		-0.5V to (VDD+0.5V)
Junction Temperature		+105°C
Storage Temperature		-40°C to +125°C
Maximum Package Power Dissipation at 25°C	NJY0054A Package	4.21 W
Derate NJY0054A Package		52.6mW/°C above +25°C
ESD Rating	HBM, STD - JESD22-A114C	≥±6 kV
	MM, STD - JESD22-A115-A	≥±250 V
	CDM, STD - JESD22-C101-C	≥±1250 V
Thermal Resistance	θ_{JC}	11.5°C/W
	θ_{JA}, No Airflow, 4 layer JEDEC	19.1°C/W

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions[1]

	Min	Typ	Max	Units
Supply Voltage, VDD to GND	2.375	2.5	2.625	V
Ambient Temperature[2]	-40	25	+85	°C
LVCMOS	0		2.625	V
SMBus (SDA, SCL)	0		3.6	V
CML Differential Input Voltage	0		2.0	Vp-p
Supply Noise Tolerance up to 50 MHz[3]		100		mV_{P-P}

(1) For soldering specifications: see product folder at: http://www.ti.com, http://www.ti.com/lit/SNOA549
(2) OOB signal pass-through limited to a minimum ambient temperature of -10°C.
(3) Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Electrical Characteristics[1]

Over recommended operating supply and temperature ranges with default register settings unless other specified.

Parameter		Test Conditions	Min	Typ	Max	Units
POWER						
PD	Power Dissipation 2.5V Operation	EQx = 0, K28.5 pattern, VOD = 700 mV p-p		900	1000	mW
		Channel powerdown[2]			11	mW
LVCMOS / LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		2.75	V
V_{IL}	Low Level Input Voltage		0		0.8	V
I_{IH}	Input High Current	V_{IN} = 2.5 V	-15		+15	µA
I_{IL}	Input Low Current	V_{IN} = 0V	-15		+15	µA
CML RECEIVER INPUTS (IN_n+, IN_n-)						
$RL_{RX-DIFF}$	Rx Differential Return Loss (SDD11), See[3]	150 MHz – 1.5 GHz		-20		dB
		150 MHz – 3.0 GHz		-13.5		
		150 MHz – 6.0 GHz		-8		
RL_{RX-CM}	Rx Common Mode Input Return Loss (SCC11)	150 MHz – 3.0 GHz, See[3]		-10		dB
R_{RX-IB}	Rx Impedance Balance (SCL11)	150 MHz – 3.0 GHz, See[3]		-27		dB
I_{IN}	Maximum current allowed at IN+ or IN- input pin.		−30		+30	mA
R_{IN}	Input Resistance	Single ended to V_{DD}, See[3]		50		Ω
R_{ITD}	Input Differential Impedance between IN+ and IN-	See[3]	85	100	115	Ω
R_{ITIB}	Input Differential Impedance Imbalance	See[3]			5	Ω
R_{ICM}	Input Common Mode Impedance	See[3]	20	25	40	Ω
$V_{RX-DIFF}$	Differential Rx peak to peak voltage	DC voltage, SD_TH = 20 kΩ to GND	0.1		1.2	V
V_{RX-SD_TH}	Electrical Idle detect threshold (differential)	SD_TH = Float, See[4] and Figure 6	40		175	mV_{p-p}

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) Measured with ENSMB = 1, all channels disabled using SMBus registers 0x01 and 0x02, and EQ in bypass (Default).
(3) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
(4) Measured at package pins of receiver. Less than 65 mVp-p is IDLE, greater than 175 mVp-p is ACTIVE. SD_TH pin connected with resistor to GND overrides this default setting.

Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified.

Parameter		Test Conditions	Min	Typ	Max	Units
DIFFERENTIAL OUTPUTS (OUT_n+, OUT_n-)						
V_{OD}	Output Differential Voltage Swing	R_L = 50 Ω ±1% to GND (AC coupled with 10 nF), 6.4 Gbps, See[5] VOD1–0 = 00	500	600	700	mV_{P-P}
V_{OCM}	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω termination, See[6]		V_{DD} – 1.4		V
T_{TX-RF}	Transmitter Rise/ Fall Time	20% to 80% of differential output voltage, measured within 1" from output pins, See[6][5] and Figure 2		65	85	ps
$T_{RF-DELTA}$	Tx rise/fall mismatch	20% to 80% of differential output voltage, See[6][5]			0.1	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss (SDD22), See[6]	Repeating 1100b (D24.3) pattern, VOD = 0.8 Vp-p, 150 MHz – 1.5 GHz		-11		dB
		1.5 GHz – 3.0 GHz		-10		
		3 GHz – 6.0 GHz		-5		
RL_{TX-CM}	Tx Common Mode Return Loss (SCC22)	Repeating 1100b (D24.3) pattern, VOD = 0.8 Vp-p, See[6] 50 MHz – 3.0 GHz		-10		dB
R_{TX-IB}	Tx Impedance Balance (SCL22)	Repeating 1100b (D24.3) pattern, VOD = 0.8 Vp-p, See[6] 50 MHz – 3.0 GHz		-30		dB
$I_{TX-SHORT}$	Tx Output Short Circuit Current Limit				90	mA
R_{OTD}	Output Differential Impedance between OUT+ and OUT-	See[6]	85	100	125	Ω
R_{OTIB}	Output Differential Impedance Imbalance	See[6]			5	Ω
R_{OCM}	Output Common Mode Impedance	See[6]	20	25	35	Ω
$V_{TX-CM-DELTA}$	Common Mode Voltage Delta between active burst and electrical Idle of an OOB signal	Minimum Temperature for OOB signal pass-through is -10C. VIN = 800 mVp-p, at 3 Gbps, See[7]			±40	mV
T_{PD}	Differential Propagation Delay (Low to High and High to Low Edge	Propagation delay measure at midpoint crossing between input to outputEQx[1:0] = 11 Figure 3	150	200	250	ps
		EQz[1:0] = OFF	120	170	220	ps
T_{LSK}	Lane to Lane Skew in a Single Part	V_{DD} = 2.5V, T_A = 25°C			27	ps
T_{PPSK}	Part to Part Propagation Delay Skew	V_{DD} = 2.5V, T_A = 25°C			35	ps
T_{SM}	Switch/Mux Time	Time to switch/mux between A and B input/output signals			150	ns

(5) Measured with clock-like {11111 00000} pattern.
(6) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
(7) Common-mode voltage (VCM) is expressed mathematically as the average of the two signal voltages with respect to local ground.VCM = (A + B) / 2, A = OUT+, B = OUT-.

Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified.

Parameter		Test Conditions	Min	Typ	Max	Units
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 8.5 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 10" 4–mil FR4 trace, VOD = 0.8 Vp-p, K28.5, SD_TH = float		0.1	0.25	UI_{P-P}
DJ2	Residual Deterministic Jitter at 10.3125 Gbps	Tx Launch Amplitude = 0.8 to 1.2 Vp–p, 10" 4–mil FR4 trace, VOD = 0.8 Vp-p, K28.5, SD_TH = float		0.1	0.3	UI_{P-P}
RJ	Random Jitter	Tx Launch Amplitude = 1.2 Vp–p, Repeating 1100b (D24.3) pattern		0.5		ps_{rms}

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Parameter		Test Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	See[1]	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	See[1][2]			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	$V_{DD3.3}$, See[1][2][3]		2000		Ω
		$V_{DD2.5}$, See[1][2][3]		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS. See Figure 5						
FSMB	Bus Operating Frequency	See[4]	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout	See[4]	25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period	See[4]	4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)	See[4]			2	ms
t_F	Clock/Data Fall Time	See[4]			300	ns
t_R	Clock/Data Rise Time	See[4]			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	See[4]			500	ms

(1) Recommended value. Parameter not tested in production.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Timing Diagrams

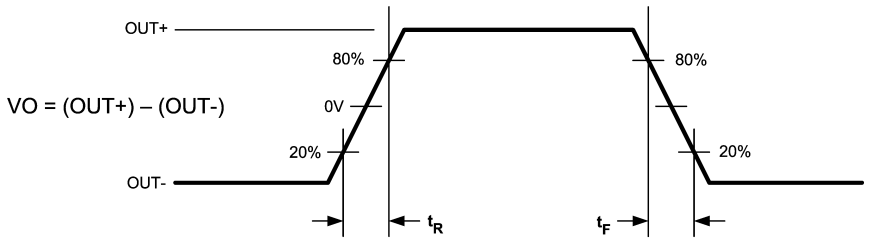


Figure 2. Output Transition Times

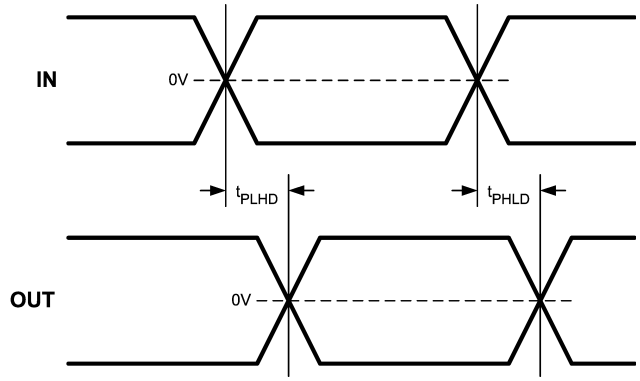


Figure 3. Propagation Delay Timing Diagram

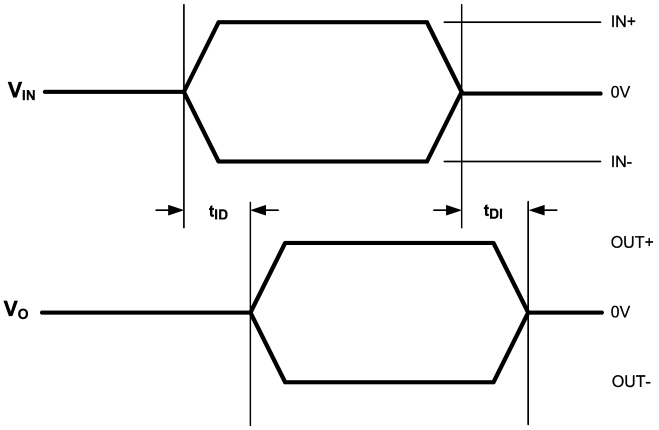


Figure 4. Idle Timing Diagram

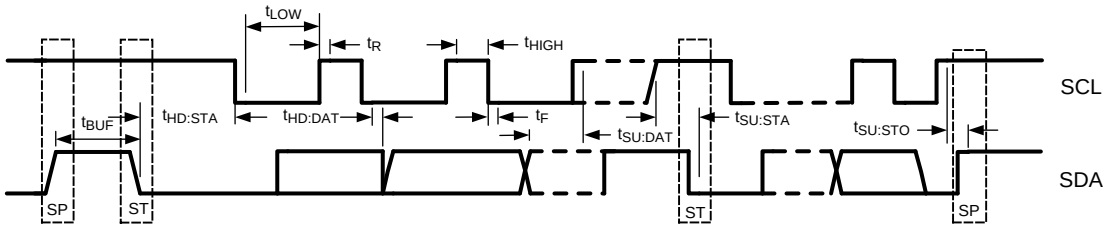


Figure 5. SMBus Timing Parameters

Functional Description

The DS100MB201 is a 2–lane signal conditioning 2:1 multiplexer and 1:2 switch or fan-out buffer optimized for PCB FR4 trace up to 10.3125 Gbps data rate. The DS100MB201 has direct register access through the SMBus. The ENSMB pin must be tied high to enable proper operation of the DS100MB201.

Pin Control Mode

The RATE pin must be forced HIGH to enable 10.3125 Gbps operation. The receiver electrical idle detect threshold is also programmable via an optional external resistor on the SD_TH pin.

SMBUS Register Programming

In SMBus mode the VOD amplitude level and equalization are all programmable on a individual lane basis. On power-up and when ENSMB is driven low all registers are reset to their default state.

Table 1. Idle Control (3–Level Input)

TXIDLEDO/SO	Function
0	This state is for lossy media, dedicated Idle threshold detect circuit disabled, output follows input based on EQ settings. Idle state not guaranteed.
Float	Float enables automatic idle detection. Idle on the input is passed to the output. Internal 50KΩ resistors hold TXIDLEDO/SO pin at a mid level - don't connect this pin if the automatic idle detect function is desired. This is the default state. Output in Idle if differential input signal less than value set by SD_TH pin.
1	Manual override, output in electrical Idle. Differential inputs are ignored.

Table 2. Receiver Electrical Idle Detect Threshold Adjust

SD_TH resistor value (Ω)	Receiver Electrical Idle Detect Threshold (DIFF p-p)
Float (no resistor required)	130 mV (default condition)
0	225 mV
80k	20 mV
SD_TH resistor value can be set from 0 through 80k ohms to achieve desired idle detect threshold, see Figure 6	

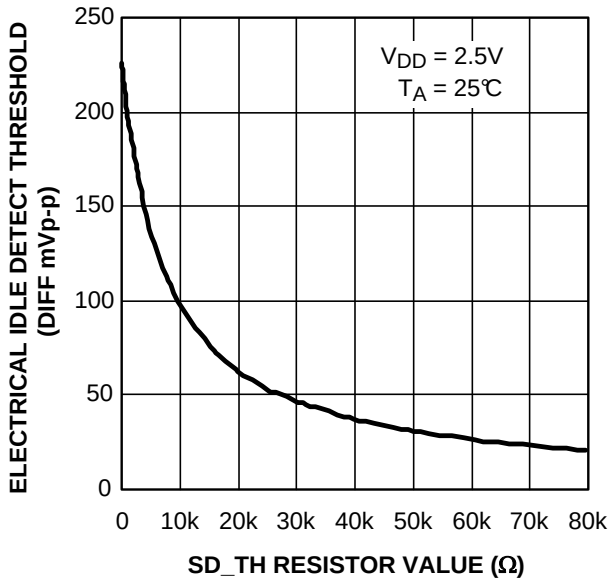


Figure 6. Typical Idle Threshold vs. SD_TH resistor value

Device Connection Paths

The lanes of the DS100MB201 can be configured either as a 2:1 multiplexer, 1:2 switch or fan-out buffer. The controller side is muxed to the disk drive side. The below table shows the logic for the multiplexer and switch functions.

Table 3. Logic Table of Switch and Mux Control

FANOUT	SEL0	SEL1	Function — connection path
0	0	0	DOUT0 connects to SIB0. DOUT1 connects to SIB1. DIN0 connects to SOB0. SOA0 is in idle (output muted). DIN1 connects to SOB1. SOA1 is in idle (output muted).
0	0	1	DOUT0 connects to SIB0. DOUT1 connects to SIA1. DIN0 connects to SOB0. SOA0 is in idle (output muted). DIN1 connects to SOA1. SOB1 is in idle (output muted).
0	1	0	DOUT0 connects to SIA0. DOUT1 connects to SIB1. DIN0 connects to SOA0. SOB0 is in idle (output muted). DIN1 connects to SOB1. SOA1 is in idle (output muted).
0	1	1	DOUT0 connects to SIA0. DOUT1 connects to SIA1. DIN0 connects to SOA0. SOB0 is in idle (output muted). DIN1 connects to SOA1. SOB1 is in idle (output muted).
1	0	0	DOUT0 connects to SIB0. DOUT1 connects to SIB1. DIN0 connects to SOB0 and SOA0. DIN1 connects to SOB1 and SOA1.
1	0	1	DOUT0 connects to SIB0. DOUT1 connects to SIA1. DIN0 connects to SOB0 and SOA0. DIN1 connects to SOA1 and SOB1.
1	1	0	DOUT0 connects to SIA0. DOUT1 connects to SIB1. DIN0 connects to SOA0 and SOB0. DIN1 connects to SOB1 and SOA1.
1	1	1	DOUT0 connects to SIA0. DOUT1 connects to SIA1. DIN0 connects to SOA0 and SOB0. DIN1 connects to SOA1 and SOB1.

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB must be pulled high to enable SMBus mode and allow access to the configuration registers.

The DS100MB201 has the AD[3:0] inputs in SMBus mode. These pins set the SMBus slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is A0'h. Based on the SMBus 2.0 specification, the DS100MB201 has a 7-bit slave address of 1010000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 101**0 000**0'b or A0'h. The bold bits indicate the AD[3:0] pin map to the slave address bits [4:1]. The device address byte can be set with the use of the AD[3:0] inputs. Below are some examples.

AD[3:0] = 0001'b, the device address byte is A2'h

AD[3:0] = 0010'b, the device address byte is A4'h

AD[3:0] = 0100'b, the device address byte is A8'h

AD[3:0] = 1000'b, the device address byte is B0'h

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

TRANSFER OF DATA VIA THE SMBUS

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBUS TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

When SMBus is enabled, all outputs of the DS100MB201 **must write VOD2 register to 0x01 (hex).** See Table 4 for more information. Each channel must be set to the value of 0x01 (hex) through each register (0x18, 0x26, 0x2E, 0x35, 0x3C, 0x43) to ensure a proper output waveform. The driver Vout voltage is set on a per lane basis using 6 different registers. Each register (0x17, 0x25, 0x2D, 0x34, 0x3B, 0x43) controls the VOD to 600 mV and 800 mV.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1” indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

RECOMMENDED SMBUS REGISTER SETTINGS

Upon power-up, the default register settings are not configured to an appropriate level. Below is the recommended settings to configure the EQ and VOD to a medium level that supports interconnect length of 10 inches FR4 trace. Please refer to Table 4, Table 5 for additional information and recommended settings.

1. Reset the SMBus registers to default values:
   - **Write 01'h to 0x00.**
2. Set output voltage for all lanes:
   - **Write 01'h to 0x18, 0x26, 0x2E, 0x35, 0x3C, 0x43.**
3. Set equalization ~6 dB at 5GHz for all lanes:
   - **Write 30'h to 0x0F, 0x16, 0x1D, 0x24, 0x2C, 0x3A.**
4. Set VOD = 0.8 Vp-p for all lanes:
   - **Write 07'h to 0x17, 0x25, 0x2D, 0x34, 0x3B, 0x42.**

Table 4. Output Driver Register Settings (must write when in SMBus mode)

Output Value	VOD Control 1 Register Setting (800 mV)	VOD Control 2 Register Setting (must set)	10.3125 Gbps Operation
1V dB	0x07	0x01	10” trace

Table 5. SMBus Register Map

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x00	Reset	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Reset			SMBus Reset 1: Reset registers to default value
0x01	PWDN lanes	7:0	PWDN CHx	R/W	0x00	Power Down per lane [7]: NC — SOB1 [6]: DIN1 — SOA1 [5]: NC — SOB0 [4]: DIN0 — SOA0 [3]: SIB1 — DOUT1 [2]: SIA1 — NC [1]: SIB0 — DOUT0 [0]: SIA0 — NC 00'h = all lanes enabled FF'h = all lanes disabled
0x02	PWDN Control	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	PWDN Control			0: Normal operation 1: Enable PWDN control in Register 0x01
0x03	SEL / FANOUT Control	7:3	Reserved	R/W	0x00	Set bits to 0.
		2	SEL1			0: Selects B input and output 1: Selects A input and output
		1	SEL0			0: Selects B input and output 1: Selects A input and output
		0	FANOUT			0: Enable only A or B output depends on SEL1 and SEL0 1: Enable both A and B output
0x08	Pin Control Override	7:5	Reserved	R/W	0x00	Set bits to 0.
		4	Override IDLE			0: Allow IDLE pin control 1: Block IDLE pin control
		3	Reserved			Set bit to 0.
		2	Reserved			Set bit to 0.
		1	Override SEL			0: Allow SEL pin control 1: Block SEL pin control
		0	Override FANOUT			0: Allow FANOUT pin control 1: Block FANOUT pin control

Table 5. SMBus Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x0F	SIA0 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	SIA0 EQ			SIA0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Register [EN] [GST] [BST] = Hex Value 100000 = 20'h = Bypass (Default) 101010 = 2A'h = 5 dB at 3 GHz 110000 = 30'h = 9 dB at 3 GHz 110010 = 32'h = 11.7 dB at 3 GHz 111001 = 39'h = 14.6 dB at 3 GHz 110101 = 35'h = 18.4 dB at 3 GHz 110111 = 37'h = 20 dB at 3 GHz 111011 = 3B'h = 21.2 dB at 3 GHz 111101 = 3D'h = 28.4 dB at 3 GHz
0x12	SIA0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x15	DOUT0 IDLE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:0	Reserved			Set bits to 0.
0x16	SIB0 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	SIB0 EQ			SIB0 Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Register [EN] [GST] [BST] = Hex Value 100000 = 20'h = Bypass (Default) 101010 = 2A'h = 5 dB at 3 GHz 110000 = 30'h = 9 dB at 3 GHz 110010 = 32'h = 11.7 dB at 3 GHz 111001 = 39'h = 14.6 dB at 3 GHz 110101 = 35'h = 18.4 dB at 3 GHz 110111 = 37'h = 20 dB at 3 GHz 111011 = 3B'h = 21.2 dB at 3 GHz 111101 = 3D'h = 28.4 dB at 3 GHz
0x17	DOUT0 VOD Control 1	7	Reserved	R/W	0x03	Set bit to 0.
		6:0	DOUT0 VOD 1			DOUT0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV
0x18	DOUT0 VOD Control 2	7:0	DOUT0 VOD 2	R/W	0x03	DOUT0 VOD Control VOD Level Control Register [TYPE] [Level Control] = Hex Value 00000001 = 01'h
0x19	SIB0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Table 5. SMBus Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x1D	SIA1 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	SIA1 EQ			SIA1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Register [EN] [GST] [BST] = Hex Value 100000 = 20'h = Bypass (Default) 101010 = 2A'h = 5 dB at 3 GHz 110000 = 30'h = 9 dB at 3 GHz 110010 = 32'h = 11.7 dB at 3 GHz 111001 = 39'h = 14.6 dB at 3 GHz 110101 = 35'h = 18.4 dB at 3 GHz 110111 = 37'h = 20 dB at 3 GHz 111011 = 3B'h = 21.2 dB at 3 GHz 111101 = 3D'h = 28.4 dB at 3 GHz
0x20	SIA1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x23	DOUT1 IDLE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:0	Reserved			Set bits to 0.
0x24	SIB1 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	SIB1 EQ			SIB1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Register [EN] [GST] [BST] = Hex Value 100000 = 20'h = Bypass (Default) 101010 = 2A'h = 5 dB at 3 GHz 110000 = 30'h = 9 dB at 3 GHz 110010 = 32'h = 11.7 dB at 3 GHz 111001 = 39'h = 14.6 dB at 3 GHz 110101 = 35'h = 18.4 dB at 3 GHz 110111 = 37'h = 20 dB at 3 GHz 111011 = 3B'h = 21.2 dB at 3 GHz 111101 = 3D'h = 28.4 dB at 3 GHz
0x25	DOUT1 VOD Control 1	7	Reserved	R/W	0x03	Set bit to 0.
		6:0	DOUT1 VOD 1			DOUT1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV
0x26	DOUT1 VOD Control 2	7:0	DOUT1 VOD 2	R/W	0x03	DOUT1 VOD Control VOD Level Control Register [TYPE] [Level Control] = Hex Value 00000001 = 01'h
0x27	SIB1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV

Table 5. SMBus Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x2B	SOA0 IDLE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:0	Reserved			Set bits to 0.
0x2C	DIN0 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	DIN0 EQ			DIN0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Register [EN] [GST] [BST] = Hex Value 100000 = 20'h = Bypass (Default) 101010 = 2A'h = 5 dB at 3 GHz 110000 = 30'h = 9 dB at 3 GHz 110010 = 32'h = 11.7 dB at 3 GHz 111001 = 39'h = 14.6 dB at 3 GHz 110101 = 35'h = 18.4 dB at 3 GHz 110111 = 37'h = 20 dB at 3 GHz 111011 = 3B'h = 21.2 dB at 3 GHz 111101 = 3D'h = 28.4 dB at 3 GHz
0x2D	SOA0 VOD Control 1	7	Reserved	R/W	0x03	Set bit to 0.
		6:0	SOA0 VOD 1			SOA0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = TBD mV 3F'h = TBD mV
0x2E	SOA0 VOD Control 2	7:0	SOA0 VOD 2	R/W	0x03	SOA0 VOD Control VOD Level Control Register [TYPE] [Level Control] = Hex Value 00000001 = 01'h
0x2F	DIN0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x32	SOB0 IDLE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:0	Reserved			Set bits to 0.
0x34	SOB0 VOD Control 1	7	Reserved	R/W	0x03	Set bit to 0.
		6:0	SOB0 VOD 1			SOB0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV
0x35	SOB0 VOD Control 2	7:0	SOB0 VOD 2	R/W	0x03	SOB0 VOD Control VOD Level Control Register [TYPE] [Level Control] = Hex Value 00000001 = 01'h
0x39	SOA1 IDLE Select	7:6	Reserve	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:0	Reserved			Set bits to 0.

Table 5. SMBus Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x3A	DIN1 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	DIN1 EQ			DIN1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Register [EN] [GST] [BST] = Hex Value 100000 = 20'h = Bypass (Default) 101010 = 2A'h = 5 dB at 3 GHz 110000 = 30'h = 9 dB at 3 GHz 110010 = 32'h = 11.7 dB at 3 GHz 111001 = 39'h = 14.6 dB at 3 GHz 110101 = 35'h = 18.4 dB at 3 GHz 110111 = 37'h = 20 dB at 3 GHz 111011 = 3B'h = 21.2 dB at 3 GHz 111101 = 3D'h = 28.4 dB at 3 GHz
0x3B	SOA1 VOD Control 1	7	Reserved	R/W	0x03	Set bit to 0.
		6:0	SOA1 VOD 1			SOA1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV
0x3C	SOA1 VOD Control 2	7:0	SOA1 VOD 2	R/W	0x03	SOA1 VOD Control VOD Level Control Register [TYPE] [Level Control] = Hex Value 00000001 = 01'h
0x3D	DIN1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x40	SOB1 IDLE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:0	Reserved			Set bits to 0.
0x42	SOB1 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		6:0	SOB1 VOD			SOB1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV
0x43	SOB1 VOD Control 2	7:0	SOB1 VOD 2	R/W	0x03	DOUT0 VOD Control VOD Level Control Register [TYPE] [Level Control] = Hex Value 00000001 = 01'h
0x47	Global VOD Adjust	7:2	Reserved	R/W	0x02	Set bits to 0.
		1:0	VOD Adjust			00 = -25.0% 01 = -12.5% 10 = +0.0% (Default) 11 = +12.5%

APPLICATIONS INFORMATION

GENERAL RECOMMENDATIONS

The DS100MB201 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and CML compatible outputs must have a controlled differential impedance of 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 (SNOA401) for additional information on WQFN packages.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS100MB201 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS100MB201. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS100MB201SQ/NOPB	ACTIVE	WQFN	NJY	54	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	DS100MB201 SQ	Samples
DS100MB201SQE/NOPB	ACTIVE	WQFN	NJY	54	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	DS100MB201 SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

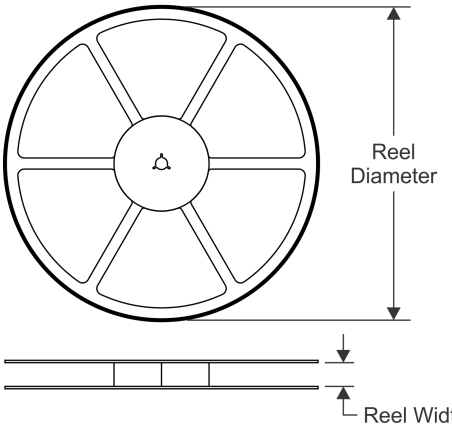
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

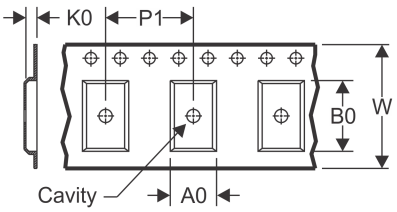
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

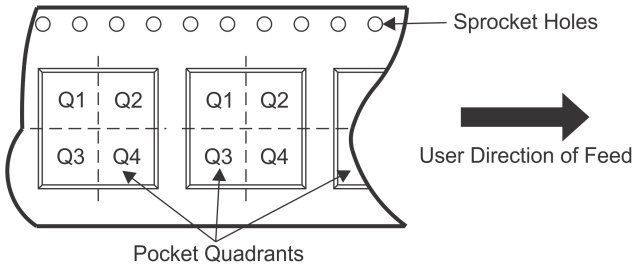


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

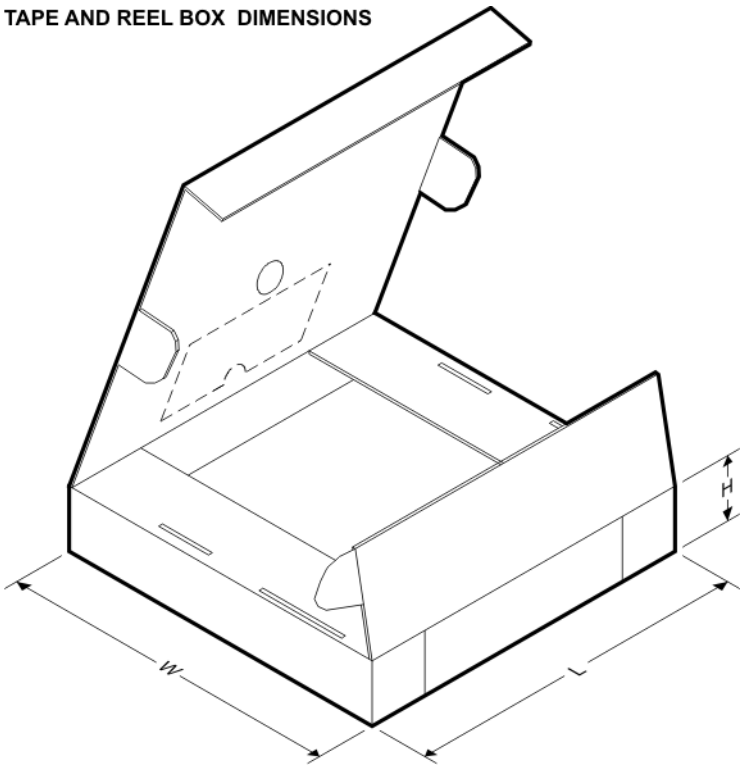
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

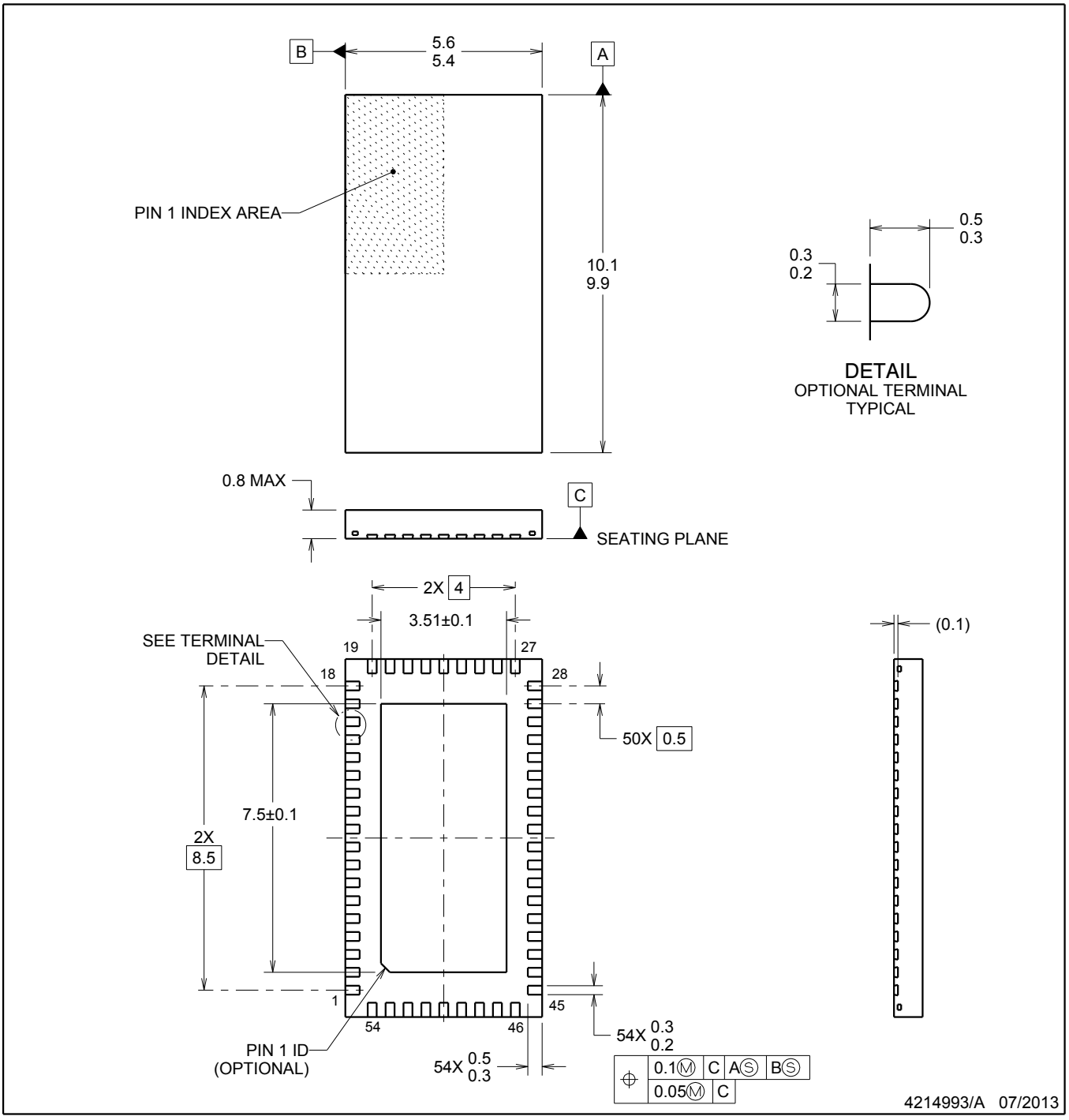
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS100MB201SQ/NOPB	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
DS100MB201SQE/NOPB	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



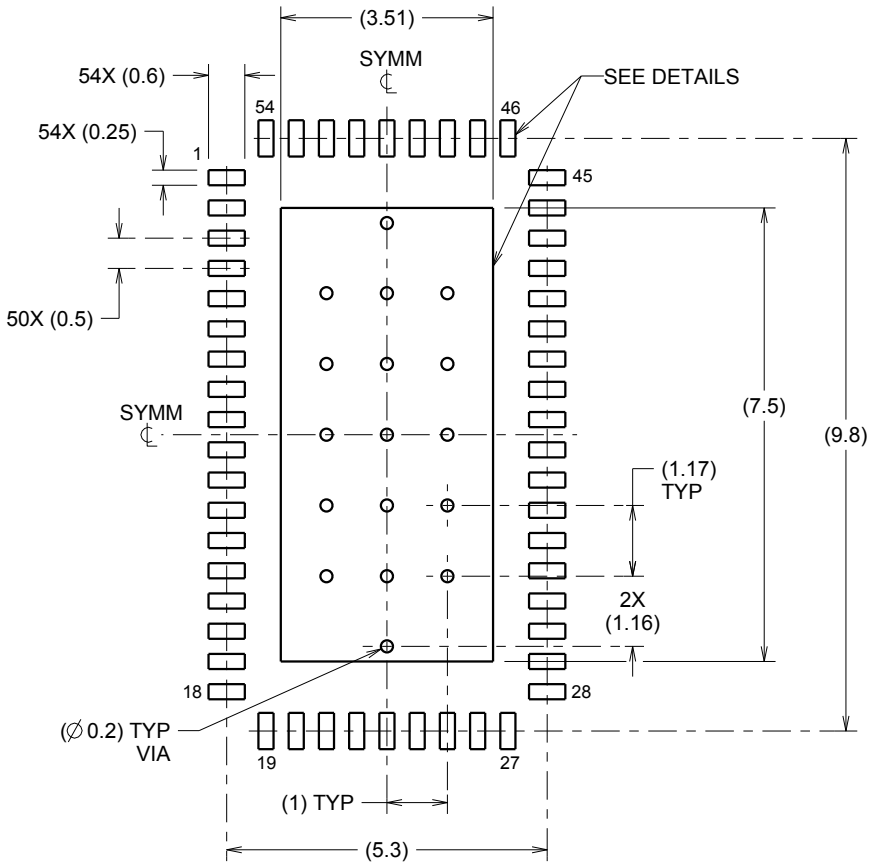
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS100MB201SQ/NOPB	WQFN	NJY	54	2000	367.0	367.0	38.0
DS100MB201SQE/NOPB	WQFN	NJY	54	250	210.0	185.0	35.0

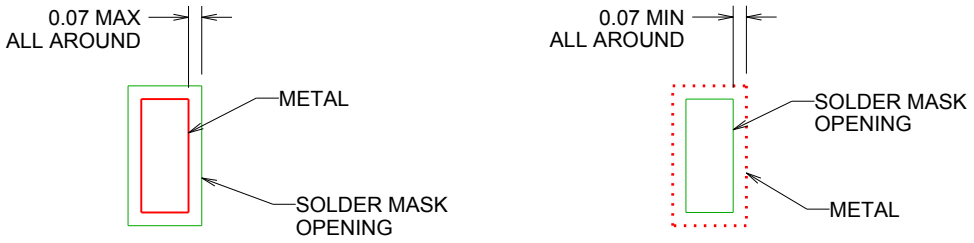


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

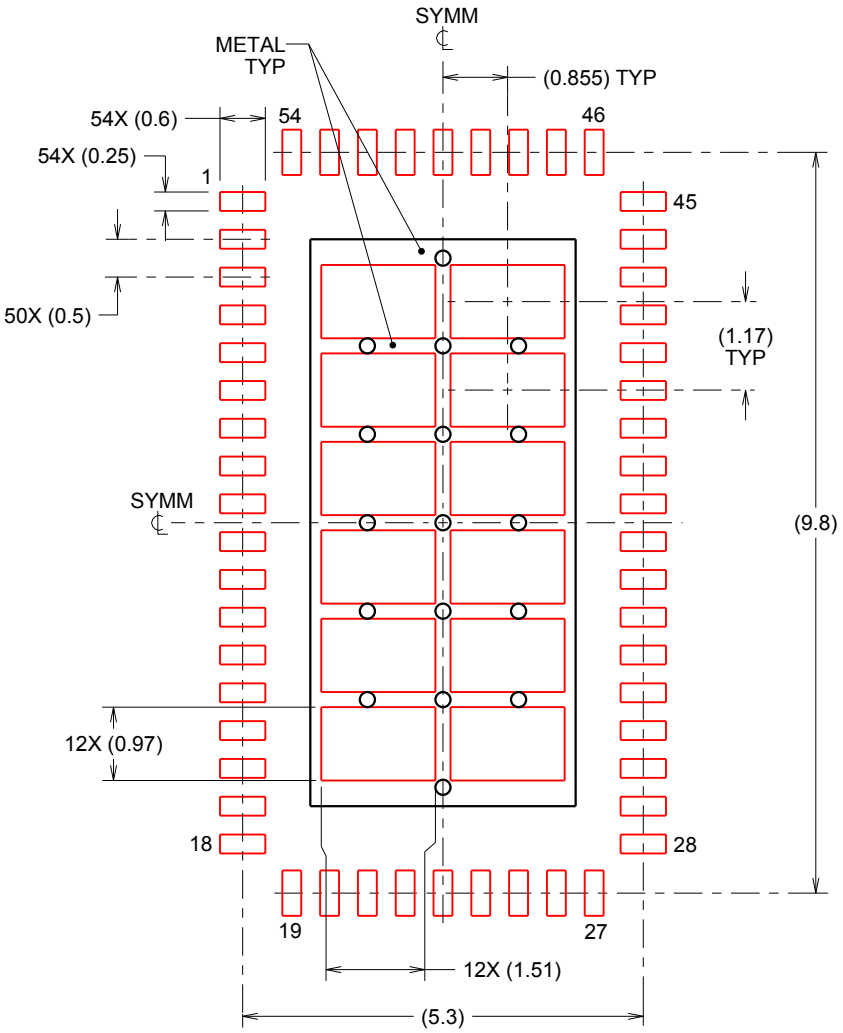
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214993/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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