

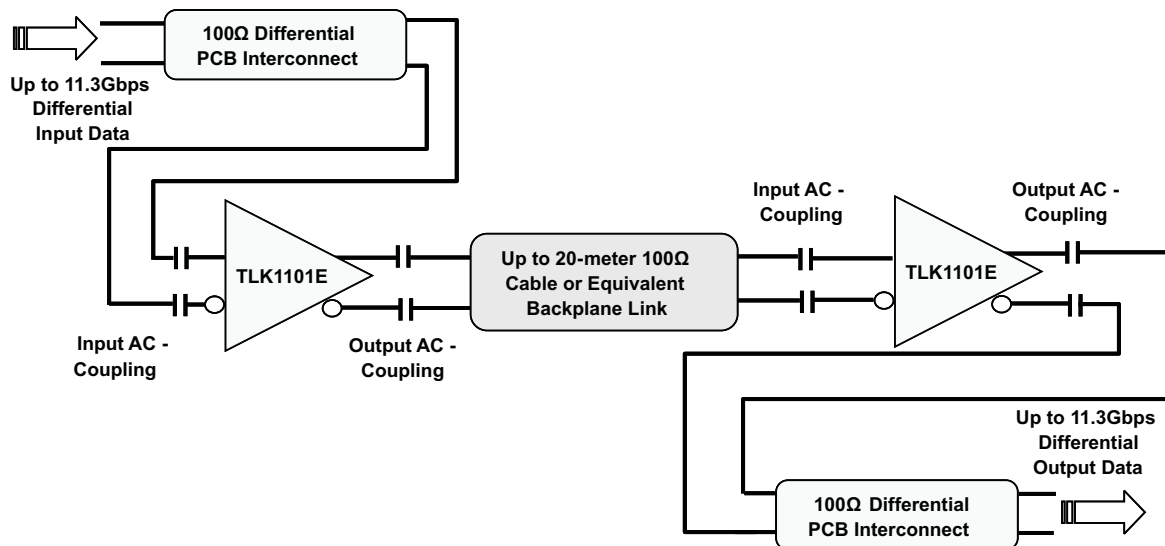
## 11.3-Gbps Cable and PC Board Equalizer

### FEATURES

- Multi-Rate Operation up to 11.3Gbps
- Compensates for up to 30dB Loss on the Receive Side and up to 7dB Loss on the Transmit Side at 5.65GHz
- Input Offset Cancellation
- Output Disable/Squelch Function
- Loss Of Signal Detection
- Adjustable Output Swing
- Adjustable Output De-Emphasis
- Two-Wire Serial Interface
- Single 3.3V Supply
- Surface Mount Small Footprint 4-mm × 4-mm 20-Pin QFN Package

### APPLICATIONS

- High-Speed Links In Communication And Data Systems
- SFP+ and XFP Active Cables
- Backplane, Daughtercard, and Cable Interconnects for 10GE, 8GFC, 10GFC, 10G SONET, SAS, SATA



### DESCRIPTION

The TLK1101E is a versatile and flexible high-speed equalizer for applications in digital high-speed links with data rates up to 11.3Gbps.

The TLK1101E can be configured in many ways to optimize its performance. It provides output de-emphasis adjustable from 0dB to 7dB using pins DE0 and DE1.

The output differential voltage swing can be set to 300mV<sub>p-p</sub>, 600mV<sub>p-p</sub>, or 900mV<sub>p-p</sub> using the SWG pin. A controlling voltage on pin VTH can be used to adjust the input threshold voltage.

Pins LN0 and LN1 can be used to optimize the device performance for various interconnect lengths, e.g. from 0 to 20 meters of 24-AWG twinaxial cable.

The LOS (loss of signal) assert level can be set to a desired level through a controlling voltage connected to pin LOSL. The LOS assert levels can be chosen from two LOS assert level ranges selectable with the LOSR pin.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

The output can be disabled using the DIS pin. The DIS and the LOS pin can be connected together to implement a squelch function.

The de-emphasis, the output voltage swing, the input threshold voltage, the output disable, and the LOS assert levels and ranges can alternatively be set using the two-wire serial interface through the SCL and SDA pins. The external pin configuration is the default device setup method. The active device control method is selected through register address 0 bit 0 (see [Table 4](#) and [Table 20](#)). The two-wire serial interface also allows for the control of the input bandwidth to optimize the device performance for various data rates.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1600mV<sub>p-p</sub> differential.

The low-frequency cut-off is low enough to support low-frequency control signals such as SAS and SATA out-of-band (OOB) signals.

## BLOCK DIAGRAM

A simplified block diagram of the TLK1101E is shown in [Figure 1](#). This compact, low power, 11.3-Gbps equalizer consists of a high-speed data path with offset cancellation block combined with an analog input threshold selection circuitry, a loss of signal detection block, a two-wire interface with a control-logic block, a bandgap voltage reference, and a bias current generation block.

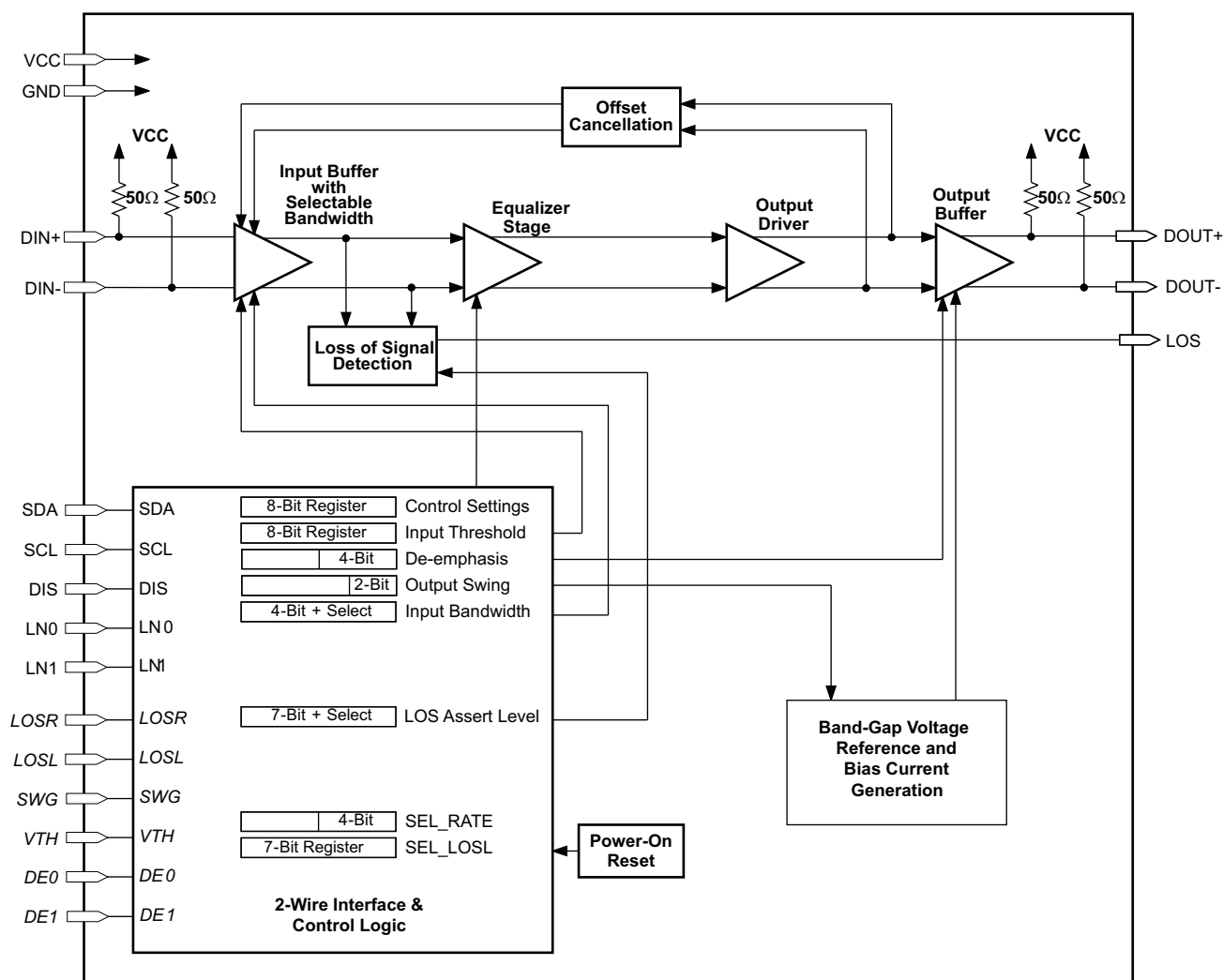
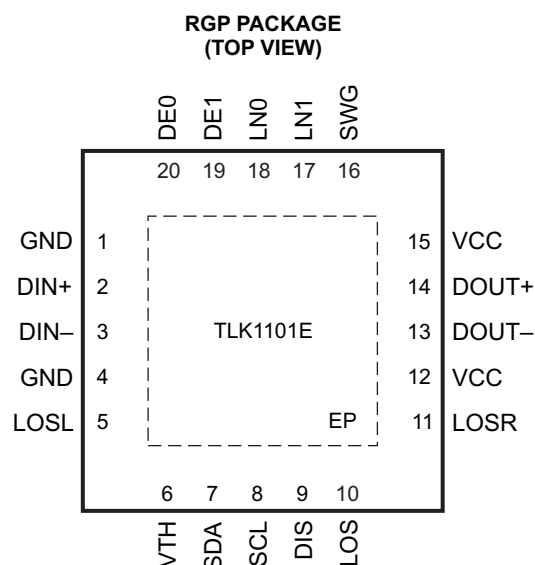


Figure 1. Simplified Block Diagram of the TLK1101E

## PACKAGE

For the TLK1101E a small footprint 4-mm × 4-mm 20-pin QFN package is used, with a lead pitch of 0.5mm. The pin-out is shown in [Figure 2](#).



**Figure 2. Pin-Out of the TLK1101E in a 4-mm × 4-mm 20-Pin QFN Package**

## TERMINAL FUNCTIONS

PIN	SYMBOL	TYPE	DESCRIPTION
1, 4	GND	supply	Circuit ground.
2	DIN+	analog-in	Non-inverted data input. On-chip 50Ω terminated to VCC.
3	DIN–	analog-in	Inverted data input. On-chip 50Ω terminated to VCC.
5	LOSL	analog-in	LOS threshold control. A controlling voltage on this pin adjusts the LOS assert and de-assert levels.
6	VTH	analog-in	Input signal threshold control. A controlling voltage of 0V to 1V on this pin adjusts the input signal threshold. Leave open for the default 0V differential threshold.
7	SDA	digital-in/out	Bidirectional serial data pin for the SDA/SCL interface. Open drain. Always connect to a pull-up resistor.
8	SCL	digital-in	Serial clock pin for the SDA/SCL interface. Always connect to a pull-up resistor.
9	DIS	digital-in	Disables CML output stage when set to high level. Internally pulled down.
10	LOS	digital-out	High level indicates that the input signal amplitude is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
11	LOSR	digital-in	LOS range select. Set to high level or leave open for upper range, or set to low level for lower range.
12, 15	VCC	supply	3.3V ± 10% supply voltage.
13	DOUT–	CML-out	Inverted data output. On-chip 50Ω back-terminated to VCC.
14	DOUT+	CML-out	Non-inverted data output. On-chip 50Ω back-terminated to VCC.
16	SWG	three-state	Output voltage swing control. Set to high level for high swing, set to low level for low swing, or leave open for medium swing.
17	LN1	digital-in	Interconnect length select. Supports two logic levels: high and low. (see <a href="#">Table 2</a> )
18	LN0	digital-in	
19	DE1	three-state	Output signal de-emphasis control. Supports three logic levels: high, low, and open. (see <a href="#">Table 1</a> )
20	DE0	three-state	
EP	EP		Exposed die pad (EP) must be grounded.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE	UNIT
$V_{CC}$	Supply voltage <sup>(2)</sup>	–0.3 to 4.0	V
$V_{DIN+}$ , $V_{DIN-}$	Voltage at DIN+, DIN– <sup>(2)</sup>	0.5 to 4.0	V
$V_{DIS}$ , $V_{LOSL}$ , $V_{LOSR}$ , $V_{TH}$ , $V_{DE0}$ , $V_{DE1}$ , $V_{LN0}$ , $V_{LN1}$ , $V_{SWG}$ , $V_{SCL}$ , $V_{SDA}$	Voltage at DIS, LOSL, LOSR, VTH, DE0, DE1, LN0, LN1, SWG, SCL, SDA <sup>(2)</sup>	–0.3 to 4.0	V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±2.5	V
$I_{DIN+}$ , $I_{DIN-}$ , $I_{DOUT+}$ , $I_{DOUT-}$	Continuous current at inputs and outputs	–25 to 25	mA
ESD	ESD Rating at all pins	2.5	kV (HBM)
$T_{J,max}$	Maximum junction temperature	125	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2.95	3.3	3.6	V
$T_A$	Operating lead temperature	–40		100	°C
$V_{IH}$	CMOS Input high voltage	2.0			V
$V_{IL}$	CMOS Input low voltage			0.8	V

## DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	Supply voltage	2.95	3.3	3.6	V
$I_{CC}$	Supply current SWG = Open (CML output current included)		76	110	mA
			83	120	
	LOS High voltage $I_{SOURCE} = 50\mu A$ ; 10k $\Omega$ Pull-up to $V_{CC}$ on LOS pin	2.4			V
	LOS Low voltage $I_{SINK} = 10mA$ ; 10k $\Omega$ Pull-up to $V_{CC}$ on LOS pin			0.4	V

## AC ELECTRICAL CHARACTERISTICS

Typical operating condition is at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$ . Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency –3dB bandwidth With 0.1 $\mu F$ input AC-coupling capacitors		30	50	kHz
$V_{IN,MIN}$	Data input sensitivity <sup>(1)</sup> BER < 10 <sup>–12</sup> , K28.5 Pattern at 11.3Gbps over a 15-m 24-AWG cable including two SMA connectors, SWG = Open, No de-emphasis, Maximum interconnect length setting. Voltage measured at the input of the cable			250	mV <sub>p-p</sub>
$V_{IN,MAX}$	Data input overload BER < 10 <sup>–12</sup> , K28.5 Pattern at 11.3Gbps, K28.5 pattern at 11.3Gbps over a 15-m 24-AWG cable including two SMA connectors, SWG = Open, No de-emphasis, Maximum interconnect length setting. Voltage measured at the input of the cable	1600			mV <sub>p-p</sub>
	High frequency boost $f = 5.65GHz$	20	24		dB
$V_{OD}$	Differential data output voltage swing DIS = Low, SWG = Low, $V_{IN} = 400mV_{p-p}$ , No de-emphasis, No interconnect line	225	300	450	mV <sub>p-p</sub>
	DIS = Low, SWG = Open, $V_{IN} = 400mV_{p-p}$ , No de-emphasis, No interconnect line	450	600	800	
	DIS = Low, SWG = High, $V_{IN} = 400mV_{p-p}$ , No de-emphasis, No interconnect line	600	900	1200	

- (1) The given differential input signal swing is valid for the low-frequency components of the input signal. The high frequency components may be attenuated by up to 24dB at 5.65GHz.

## AC ELECTRICAL CHARACTERISTICS (continued)

Typical operating condition is at  $V_{CC} = 3.3V$  and  $T_A = 25^{\circ}C$ . Over recommended operating conditions (unless otherwise noted)

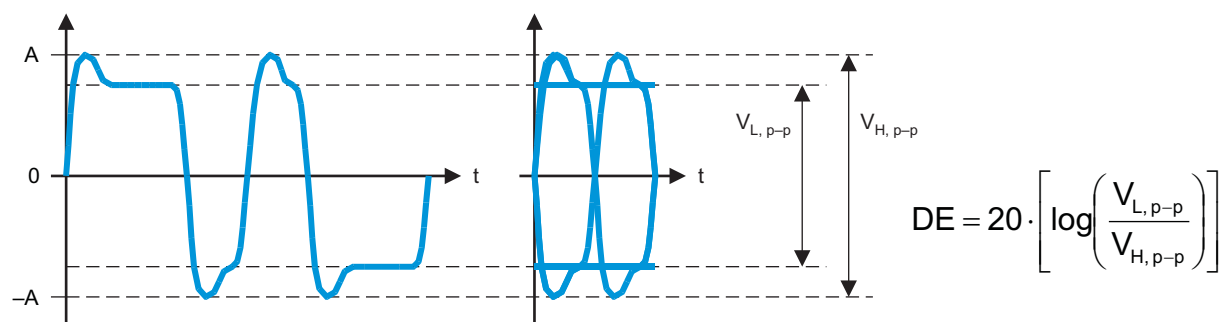
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CM,OUT}$ Data output common-mode voltage	DIS = Low, SWG = Low, $V_{IN} = 400mV_{p-p}$ , No de-emphasis, No interconnect line	$V_{CC}-0.113$	$V_{CC}-0.075$	$V_{CC}-0.056$	V
	DIS = Low, SWG = Open, $V_{IN} = 400mV_{p-p}$ , No de-emphasis, No interconnect line	$V_{CC}-0.2$	$V_{CC}-0.15$	$V_{CC}-0.113$	
	DIS = Low, SWG = High, $V_{IN} = 400mV_{p-p}$ , No de-emphasis, No interconnect line	$V_{CC}-0.3$	$V_{CC}-0.225$	$V_{CC}-0.15$	
$V_{RIP}$ Differential output ripple	DIS = High, 50% Transitions of K28.5 pattern at 11.3Gbps, No interconnect line, $V_{IN} = 1600mV_{p-p}$		1.5	5	mV <sub>RMS</sub>
DE Output de-emphasis <sup>(2)</sup>	K28.5 Pattern at 11.3Gbps, No interconnect line, $V_{IN} = 400mV_{p-p}$ , SWG = Open, Output de-emphasis off: DE0 = Low, DE1 = Low		0		dB
	K28.5 Pattern at 11.3Gbps, No interconnect line, $V_{IN} = 400mV_{p-p}$ , SWG = Open, Maximum output de-emphasis: DE0 = High, DE1 = High		7		
DJ Deterministic jitter	K28.5 Pattern at 11.3Gbps, 10-m 28-AWG Cable, $V_{IN} = 400mV_{p-p}$ , SWG = Open, No de-emphasis, Maximum interconnect length setting		12		ps <sub>p-p</sub>
	K28.5 Pattern at 11.3Gbps, 15-m 24-AWG Cable, $V_{IN} = 400mV_{p-p}$ , SWG = Open, No de-emphasis, Maximum interconnect length setting		12		
RJ Random jitter	K28.5 Pattern at 11.3Gbps, 10-m 28-AWG Cable, $V_{IN} = 400mV_{p-p}$ , SWG = Open, No de-emphasis, Maximum interconnect length setting		1.0		ps <sub>RMS</sub>
	K28.5 Pattern at 11.3Gbps, 15-m 24-AWG Cable, $V_{IN} = 400mV_{p-p}$ , SWG = Open, No de-emphasis, Maximum interconnect length setting		1.0		
$t_R$ Output rise time	20% to 80%, No interconnect line, $V_{IN} = 400mV_{p-p}$ , SWG = Open, No de-emphasis	20	28		ps
$t_F$ Output fall time	20% to 80%, No interconnect line, $V_{IN} = 400mV_{p-p}$ , SWG = Open, No de-emphasis	20	28		
SDD11 Differential input return loss	0.01GHz < f < 3.9GHz		16		dB
	3.9GHz < f < 12.1GHz		See <sup>(3)</sup>		
SDD22 Differential output return loss	0.01GHz < f < 3.9GHz		16		dB
	3.9GHz < f < 12.1GHz		See <sup>(3)</sup>		
SCD11 Input differential to common-mode conversion	0.01GHz < f < 7.5GHz		25		dB
	7.5GHz < f < 12.1GHz		20		
SCC22 Common-mode output return loss	0.01GHz < f < 2.5GHz		13		dB
	2.5GHz < f < 12.1GHz		7		
$V_{AS}$ LOS Assert threshold voltage	K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = Open	25	60		mV <sub>p-p</sub>
	K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = 1.0V	75	180		
$V_{DAS}$ LOS De-assert threshold voltage	K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = Open		100	150	mV <sub>p-p</sub>
	K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = 1.0V		300	450	
LOS Hysteresis	$20\log(V_{DAS} / V_{AS})$	2.5	4.5		dB
$T_{AS/DAS}$ LOS Assert/de-assert time		2.5		50	μs
$T_{DIS}$ Disable response time			20		ns
Latency	From DIN+/DIN– to DOUT+/DOUT–		150		ps

(2) See Table 1 and Figure 3 for output de-emphasis settings

(3) Differential Return Loss given by SDD11, SDD22 =  $19.3 + 26.66 \log_{10}(f/8.25)$ , f in GHz

**Table 1. Available Output De-emphasis Settings**

		DE0		
		LOW	OPEN	HIGH
DE1	LOW	0dB	0.875dB	1.75dB
	OPEN	2.625dB	3.5dB	4.375dB
	HIGH	5.25dB	6.125dB	7dB



T0157-01

**Figure 3. Output De-emphasis****Table 2. Available Interconnect Length Settings (24-AWG Twinaxial Cable Used as Reference)**

		LN0	
		LOW	HIGH
LN1	LOW	0–5 meters	10–15 meters
	HIGH	5–10 meters	15–20 meters

## TWO-WIRE SERIAL INTERFACE AND CONTROL LOGIC

### FUNCTIONAL DESCRIPTION

The TLK1101E uses a two-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. Both inputs include 100kΩ pull-up resistors to VCC. For driving these inputs, an open-drain output is recommended.

The two-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The TLK1101E is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCL signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (0101000) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8-bit register address
4. 8-bit register data
5. STOP command

Regarding timing, the TLK1101E is I<sup>2</sup>C-compatible. The typical timing is shown in Figure 4 and a complete data transfer is shown in Figure 5. Parameters for Figure 4 are defined in Table 3.

**Bus Idle:** Both SDA and SCL lines remain HIGH

**Start Data Transfer:** A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

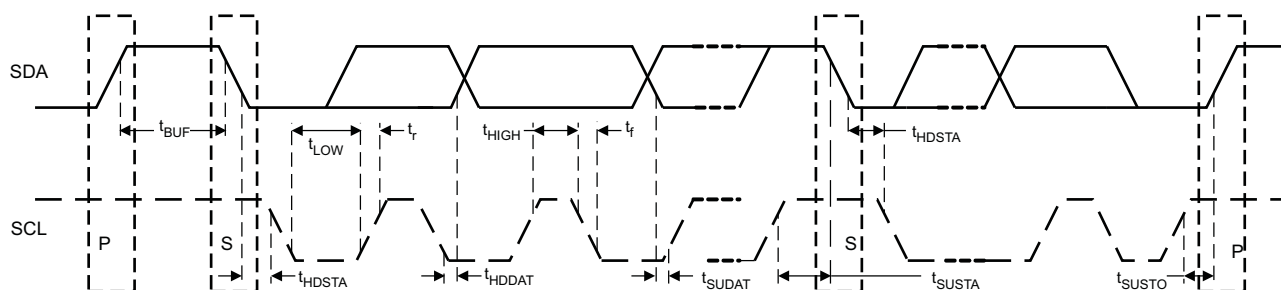
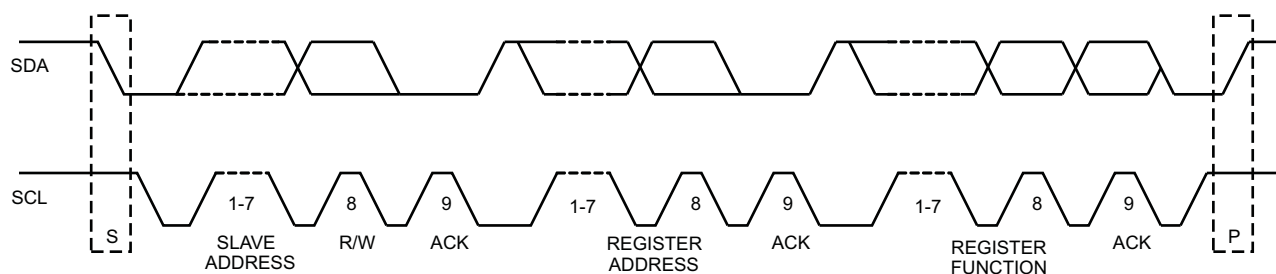


Figure 4. Two-Wire Serial Interface Timing Diagram.

**Table 3. Two-Wire Serial Interface Timing Diagram Definitions**

SYMBOL	PARAMETER	MIN	MAX	UNIT
$f_{SCL}$	SCL Clock frequency		400	kHz
$t_{BUF}$	Bus free time between START and STOP conditions	1.3		$\mu$ s
$t_{HDSTA}$	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		$\mu$ s
$t_{LOW}$	Low period of the SCL clock	1.3		$\mu$ s
$t_{HIGH}$	High period of the SCL clock	0.6		$\mu$ s
$t_{SUSTA}$	Setup time for a repeated START condition	0.6		$\mu$ s
$t_{HDDAT}$	Data HOLD time	0		$\mu$ s
$t_{SUDAT}$	Data setup time	100		ns
$t_R$	Rise time of both SDA and SCL signals		300	ns
$t_F$	Fall time of both SDA and SCL signals		300	ns
$t_{SUSTO}$	Setup time for STOP condition	0.6		$\mu$ s

**Figure 5. Two-Wire Serial Interface Data Transfer**



## REGISTER MAPPING

The register mapping for read/write register addresses 0 (0x00) through 13 (0x0D) are shown in [Table 4](#) through [Table 17](#). The register mapping for the read only register addresses 14 (0x0E) and 15 (0x0F) are shown in [Table 18](#) and [Table 19](#). [Table 20](#) describes the circuit functionality based on the register settings.

**Table 4. Register 0 (0x00) Mapping – Control Settings**

register address 0 (0x00)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REG11OFF	REG3OFF	REG2OFF	REG1OFF	DISABLE	LOS_RNG	OCOFF	I2CMODE

**Table 5. Register 1 (0x01) Mapping – Input Threshold Adjust**

register address 1 (0x01)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
THRESH7	THRESH6	THRESH5	THRESH4	THRESH3	THRESH2	THRESH1	THRESH0

**Table 6. Register 2 (0x02) Mapping – De-emphasis Setting**

register address 2 (0x02)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	DEEM3	DEEM2	DEEM1	DEEM0

**Table 7. Register 3 (0x03) Mapping – Output Swing Control**

register address3 (0x03)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	AMP1	AMP0

**Table 8. Register 4 (0x04) Mapping**

register address 4 (0x04)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 9. Register 5 (0x05) Mapping**

register address 5 (0x05)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 10. Register 6 (0x06) Mapping**

register address 6 (0x06)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 11. Register 7 (0x07) Mapping – Maximum Data Rate Setting**

register address 7 (0x07)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RATE_7	–	–	–	RATE_3	RATE_2	RATE_1	RATE_0

**Table 12. Register 8 (0x08) Mapping**

register address 8 (0x08)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 13. Register 9 (0x09) Mapping**

register address 9 (0x09)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 14. Register 10 (0x0A) Mapping**

register address 10 (0x0A)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 15. Register 11 (0x0B) Mapping – LOS Level Setting**

register address 11 (0x0B)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LOSLVL_7	LOSLVL_6	LOSLVL_5	LOSLVL_4	LOSLVL_3	LOSLVL_2	LOSLVL_1	LOSLVL_0

**Table 16. Register 12 (0x0C) Mapping**

register address 12 (0x0C)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 17. Register 13 (0x0D) Mapping**

register address 13 (0x0D)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

**Table 18. Register 14 (0x0E) Mapping – Selected Rate Setting (Read Only)**

register address 14 (0x0E)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	SEL_RATE3	SEL_RATE2	SEL_RATE1	SEL_RATE0

**Table 19. Register 15 (0x0F) Mapping – Selected LOS Level (Read Only)**

register address 15 (0x0F)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	SEL_LOSL6	SEL_LOSL5	SEL_LOSL4	SEL_LOSL3	SEL_LOSL2	SEL_LOSL1	SEL_LOSL0

**Table 20. Register Functionality**

NAME	REGISTER DESCRIPTION	FUNCTION																						
REG11OFF	Address 0 bit 7: Register address 11 control	<b>Register address 11 control bit:</b> 1 = External LOS level (LOSL) control active 0 = Register address 11 settings active (default)																						
REG3OFF	Address 0 bit 6: Register address 3 control	<b>Register address 3 control bit:</b> 1 = External output swing (SWG) control active 0 = Register address 3 settings active (default)																						
REG2OFF	Address 0 bit 5: Register address 2 control	<b>Register address 2 control bit:</b> 1 = External output de-emphasis (DE) control active 0 = Register address 2 settings active (default)																						
REG1OFF	Address 0 bit 4: Register address 1 control	<b>Register address 1 control bit:</b> 1 = External input threshold (VTH) control active 0 = Register address 1 settings active (default)																						
DISABLE	Address 0 bit 3: Output disable	<b>Output disable bit:</b> 1 = Output disabled 0 = Output enabled (default)																						
LOS_RNG	Address 0 bit 2: LOS Range	<b>LOS Range bit:</b> 1 = High LOS assert voltage range 0 = Low LOS assert voltage range (default)																						
OCOFF	Address 0 bit 1: Offset cancellation disable	<b>Offset cancellation disable bit:</b> 1 = Offset cancellation is disabled 0 = Offset cancellation is enabled (default)																						
I2CMODE	Address 0 bit 0: Two-wire interface disable	<b>Two-wire interface disable bit:</b> 1 = Register settings active 0 = External control active (default)																						
THRESH7	Address 1 bit 7: Input threshold adjust bit 7 (MSB)	<b>Input threshold adjustment setting:</b> Maximum positive shift for 00000001 (1) Minimum positive shift for 01111111 (127) Zero shift for 10000000 (128) or 00000000 (0) (default) Minimum negative shift for 10000001 (129) Maximum negative shift for 11111111 (255)																						
THRESH6	Address 1 bit 6: Input threshold adjust bit 6																							
THRESH5	Address 1 bit 5: Input threshold adjust bit 5																							
THRESH4	Address 1 bit 4: Input threshold adjust bit 4																							
THRESH3	Address 1 bit 3: Input threshold adjust bit 3																							
THRESH2	Address 1 bit 2: Input threshold adjust bit 2																							
THRESH1	Address 1 bit 1: Input threshold adjust bit 1																							
THRESH0	Address 1 bit 0: Input threshold adjust bit 0 (LSB)																							
DEEM3	Address 2 bit 3: De-emphasis adjust bit 3 (MSB)	<table><tr><th colspan="2">De-emphasis setting:</th></tr><tr><th>De-emphasis (dB)</th><th>Register Setting</th></tr><tr><td>0</td><td>0000 (default)</td></tr><tr><td>0.875</td><td>0001</td></tr><tr><td>1.75</td><td>0011</td></tr><tr><td>2.625</td><td>0100</td></tr><tr><td>3.5</td><td>0101</td></tr><tr><td>4.375</td><td>0111</td></tr><tr><td>5.25</td><td>1100</td></tr><tr><td>6.125</td><td>1101</td></tr><tr><td>7</td><td>1111</td></tr></table>	De-emphasis setting:		De-emphasis (dB)	Register Setting	0	0000 (default)	0.875	0001	1.75	0011	2.625	0100	3.5	0101	4.375	0111	5.25	1100	6.125	1101	7	1111
De-emphasis setting:																								
De-emphasis (dB)	Register Setting																							
0	0000 (default)																							
0.875	0001																							
1.75	0011																							
2.625	0100																							
3.5	0101																							
4.375	0111																							
5.25	1100																							
6.125	1101																							
7	1111																							
DEEM2	Address 2 bit 2: De-emphasis adjust bit 2																							
DEEM1	Address 2 bit 1: De-emphasis adjust bit 1																							
DEEM0	Address 2 bit 0: De-emphasis adjust bit 0 (LSB)																							

**Table 20. Register Functionality (continued)**

NAME	REGISTER DESCRIPTION	FUNCTION
AMP1	Address 3 bit 1: Output swing control bit 1 (MSB)	<b>Output swing control:</b> 00 = 300mV <sub>p-p</sub> 01 = 600mV <sub>p-p</sub> (default) 10 = 600mV <sub>p-p</sub> 11 = 900mV <sub>p-p</sub>
AMP0	Address 3 bit 0: Output swing control bit 0 (LSB)	
RATE_7	Address 7 bit 7: Bandwidth selection bit 7 (MSB)	<b>Input filter bandwidth selection control bit:</b> 1 = Contents of register address 7 bits 3 to 0 are used to select the input filter bandwidth 0 = Bandwidth of 9.1GHz is used (default)
RATE_3	Address 7 bit 3: Bandwidth selection bit 3	<b>Input filter bandwidth selection bits:</b> Register 7 bits 3 to 0 are used to set the input filter bandwidth: 0000 = Maximum bandwidth 1111 = Minimum bandwidth
RATE_2	Address 7 bit 2: Bandwidth selection bit 2	
RATE_1	Address 7 bit 1: Bandwidth selection bit 1	
RATE_0	Address 7 bit 0: Bandwidth selection bit 0 (LSB)	
LOSLVL_7	Address 11 bit 7: LOS assert level bit 7 (MSB)	<b>LOS Assert level control bit:</b> 1 = Contents of register address 11 bits 6 to 0 are used to select the LOS assert level 0 = LOS Assert level of 50mV <sub>p-p</sub> is used (default)
LOSLVL_6	Address 11 bit 6: LOS assert level selection bit 6	<b>LOS Assert level selection bits:</b> Register 11 bits 6 to 0 are used to select the LOS assert level: 0000000 = Minimum LOS assert level 1111111 = Maximum LOS assert level
LOSLVL_5	Address 11 bit 5: LOS assert level selection bit 5	
LOSLVL_4	Address 11 bit 4: LOS assert level selection bit 4	
LOSLVL_3	Address 11 bit 3: LOS assert level selection bit 3	
LOSLVL_2	Address 11 bit 2: LOS assert level selection bit 2	
LOSLVL_1	Address 11 bit 1: LOS assert level selection bit 1	
LOSLVL_0	Address 11 bit 0: LOS assert level selection bit 0 (LSB)	
SEL_RATE3	Address 14 bit 3: Selected rate setting bit 3	<b>Selected rate setting (read only)</b>
SEL_RATE2	Address 14 bit 2: Selected rate setting bit 2	
SEL_RATE1	Address 14 bit 1: Selected rate setting bit 1	
SEL_RATE0	Address 14 bit 0: Selected rate setting bit 0	

**Table 20. Register Functionality (continued)**

NAME	REGISTER DESCRIPTION	FUNCTION
SEL_LOSL6	Address 15 bit 6: Selected LOS assert level bit 6 (MSB)	Selected LOS assert level (read only)
SEL_LOSL5	Address 15 bit 5: Selected LOS assert level bit 5	
SEL_LOSL4	Address 15 bit 4: Selected LOS assert level bit 4	
SEL_LOSL3	Address 15 bit 3: Selected LOS assert level bit 3	
SEL_LOSL2	Address 15 bit 2: Selected LOS assert level bit 2	
SEL_LOSL1	Address 15 bit 1: Selected LOS assert level bit 1	
SEL_LOS_0	Address 15 bit 0: Selected LOS assert level bit 0 (LSB)	

## TYPICAL CHARACTERISTICS

Typical operating condition is at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$ ,  $V_{IN} = 400mV_{p-p}$ ,  $DE0 = DE1 = low$ ,  $SWG = open$ ,  $LN0 = LN1 = high$ , and no interconnect line at the output (unless otherwise noted). Differential S-parameter characteristics of Spectra-Strip SkewClear EXD twinaxial cables and a 36-inch FR-4 stripline used for the measurements captured in this document are as shown in Figure 6.

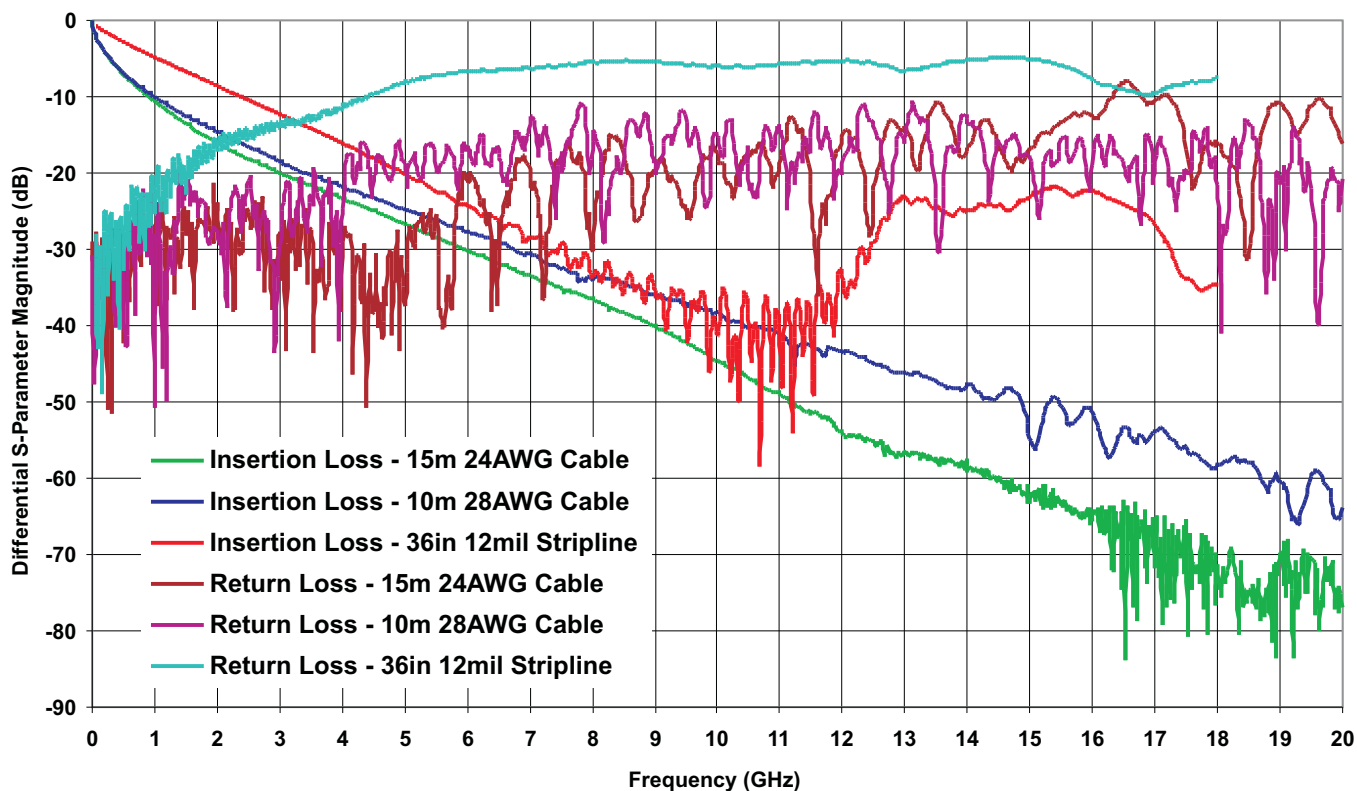
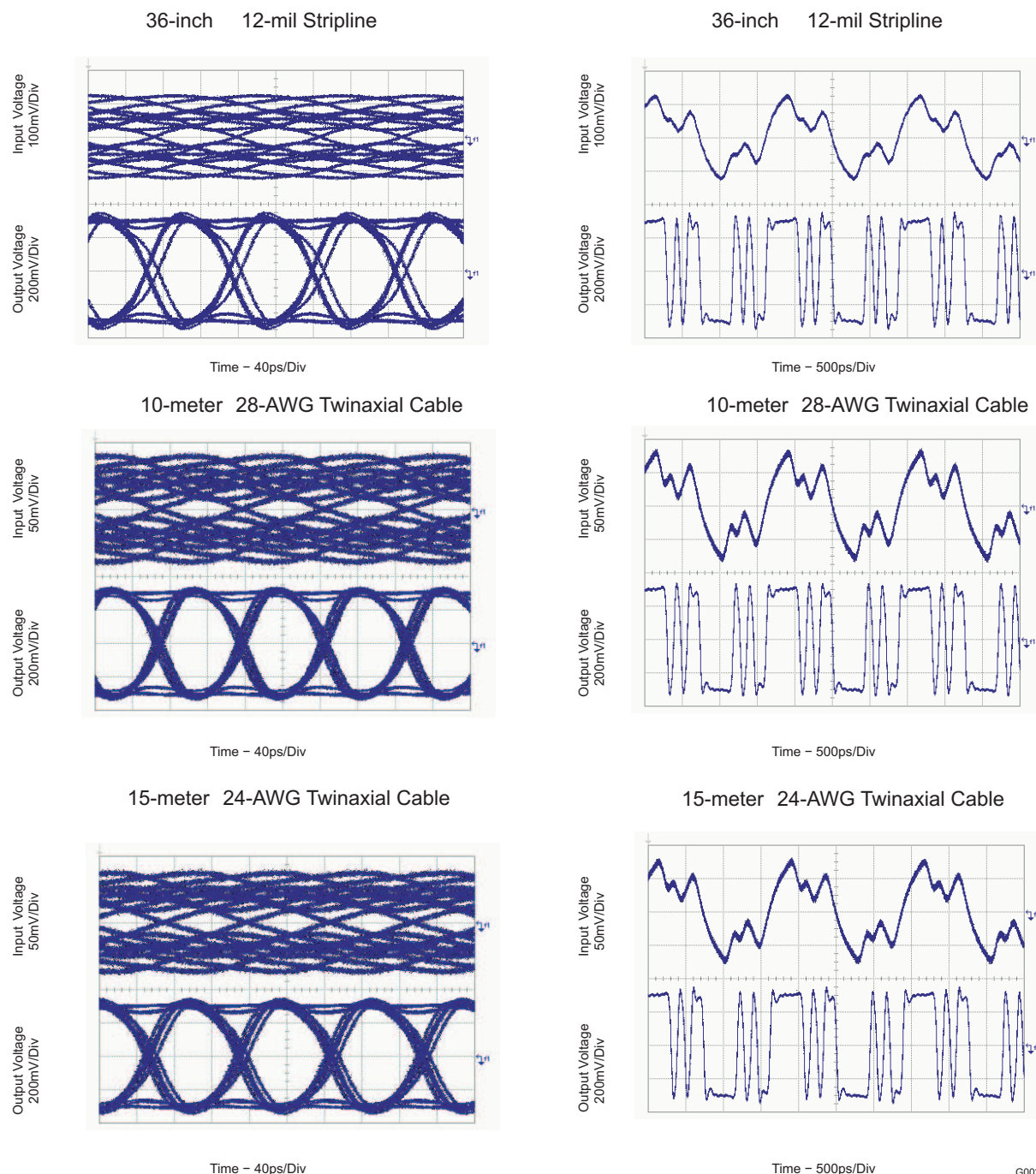


Figure 6. Typical Differential S-Parameter Characteristics of Interconnect Lines

## TYPICAL CHARACTERISTICS (continued)

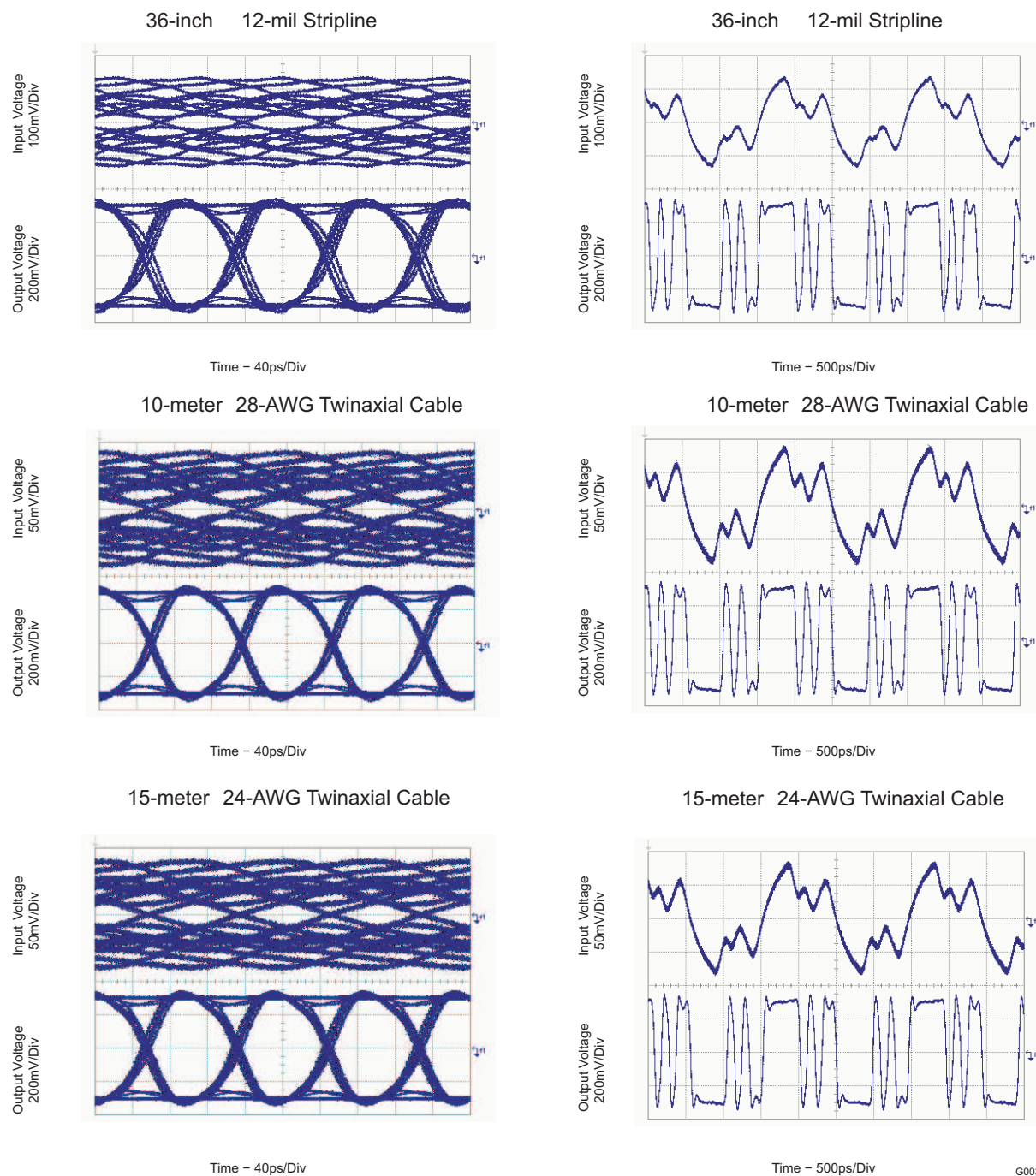
### DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 11.3Gbps USING A K28.5 PATTERN



G002

**Figure 7. Equalizer Input and Output Signals with Different Interconnect Lines at 11.3Gbps**



**TYPICAL CHARACTERISTICS (continued)****DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 10.3125Gbps USING A K28.5 PATTERN****Figure 8. Equalizer Input and Output Signals with Different Interconnect Lines at 10.3125Gbps**



## TYPICAL CHARACTERISTICS (continued)

### DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 8.5Gbps USING A K28.5 PATTERN

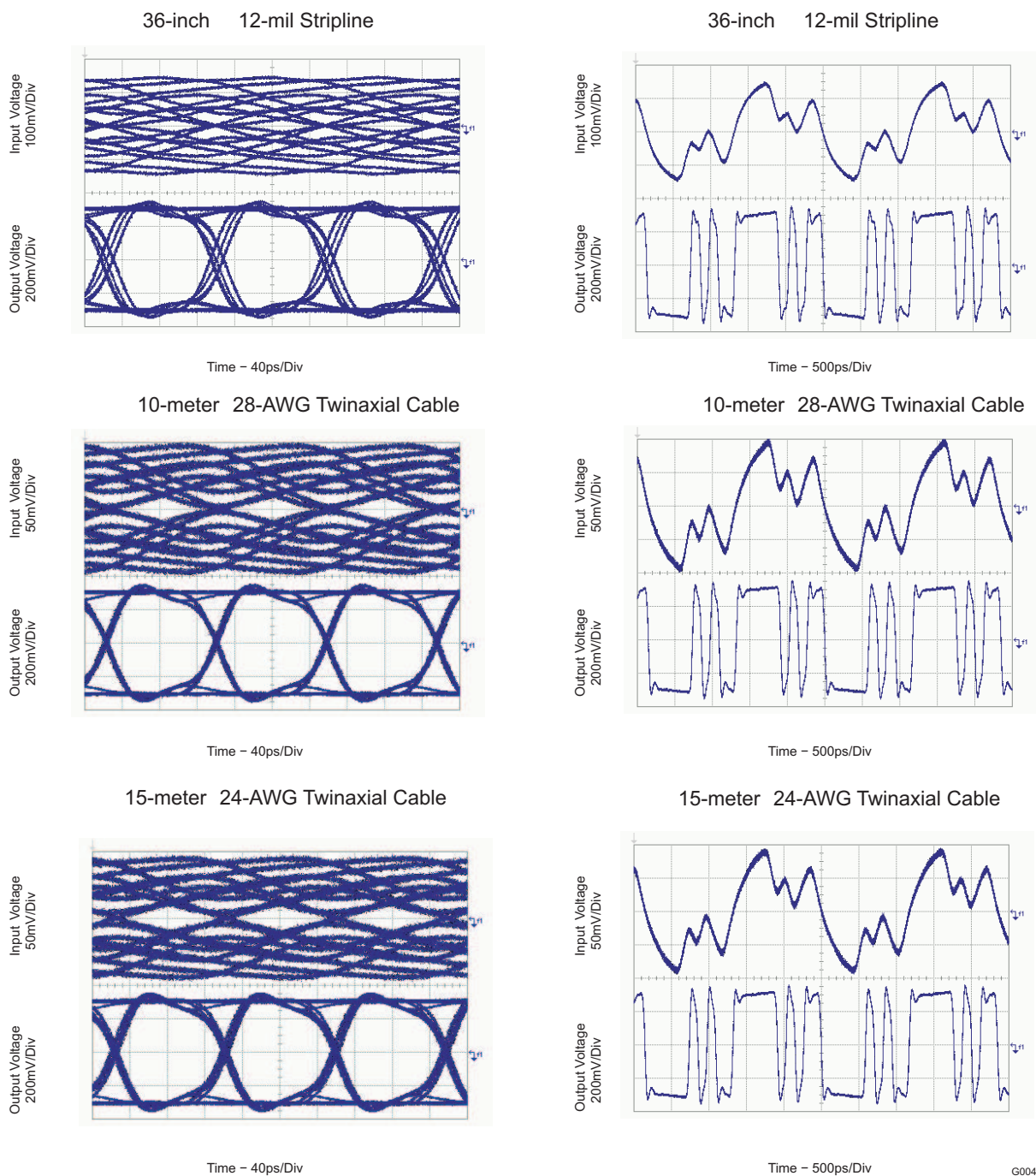


Figure 9. Equalizer Input and Output Signals with Different Interconnect Lines at 8.5Gbps.

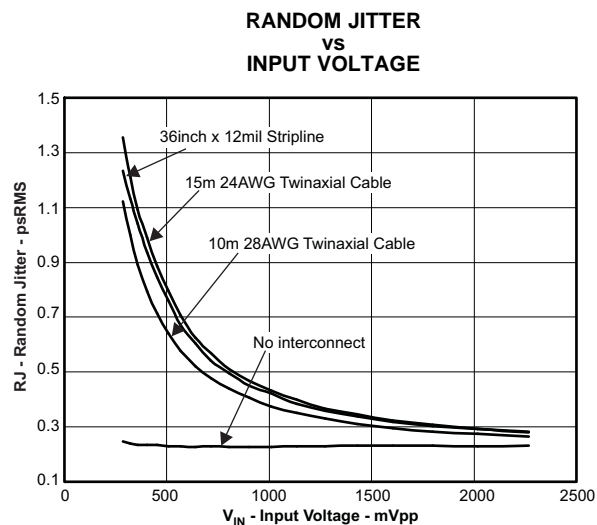
**TYPICAL CHARACTERISTICS (continued)**

Figure 10.

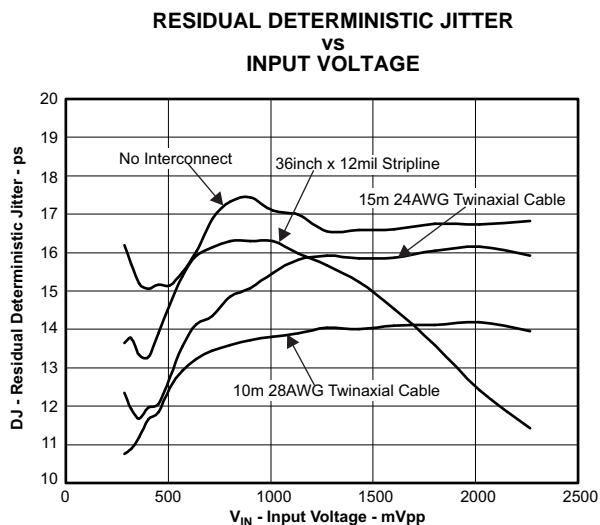


Figure 11.

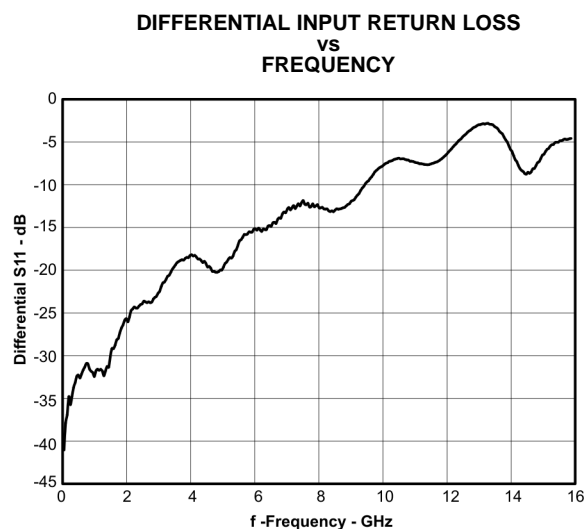


Figure 12.

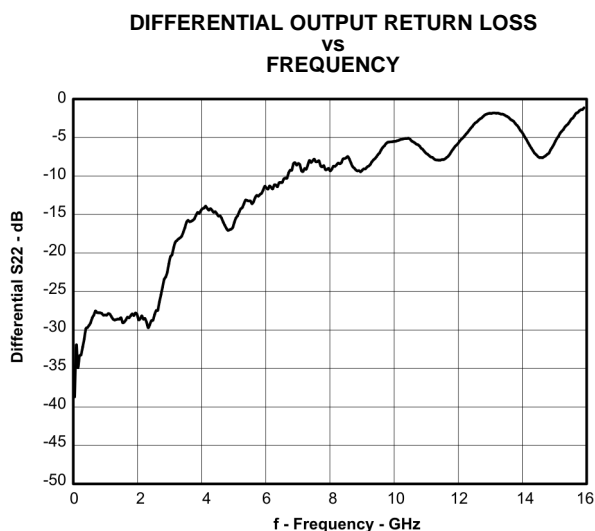


Figure 13.

## TYPICAL CHARACTERISTICS (continued)

LOS THRESHOLD VOLTAGE  
vs  
LOSL VOLTAGE (LOSR = LOW)

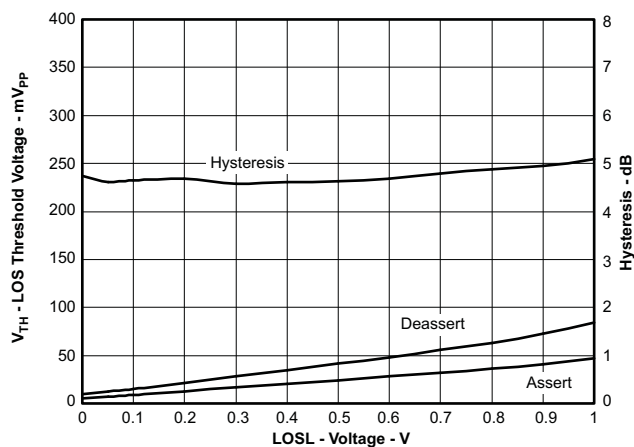


Figure 14.

LOS THRESHOLD VOLTAGE  
vs  
LOSL VOLTAGE (LOSR = HIGH)

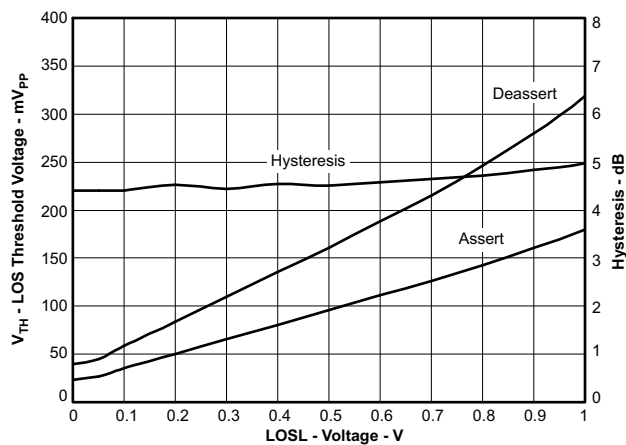


Figure 15.

LOS THRESHOLD VOLTAGE  
vs  
REGISTER 11 (0x0B) SETTING (LOSR = LOW)

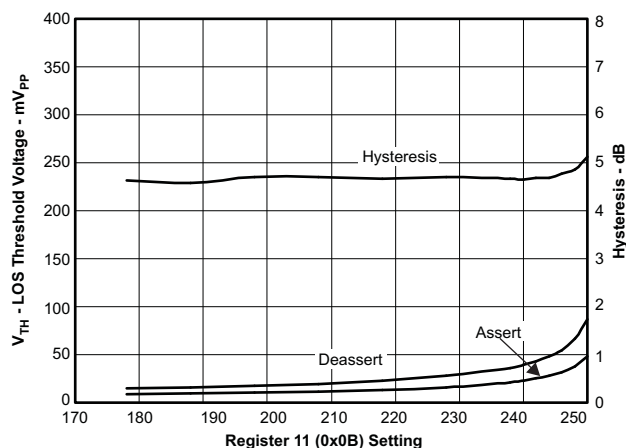


Figure 16.

LOS THRESHOLD VOLTAGE  
vs  
REGISTER 11 (0x0B) SETTING (LOSR = HIGH)

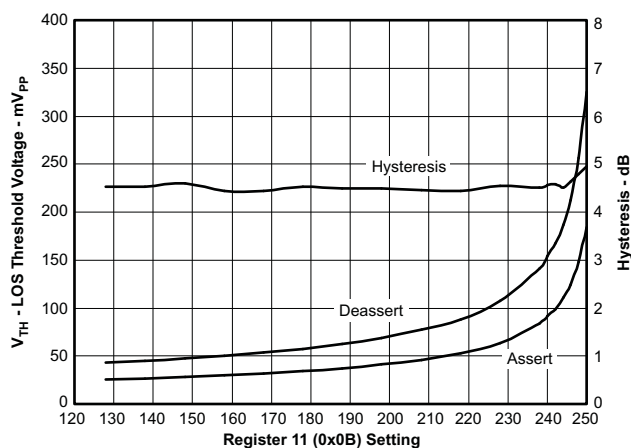
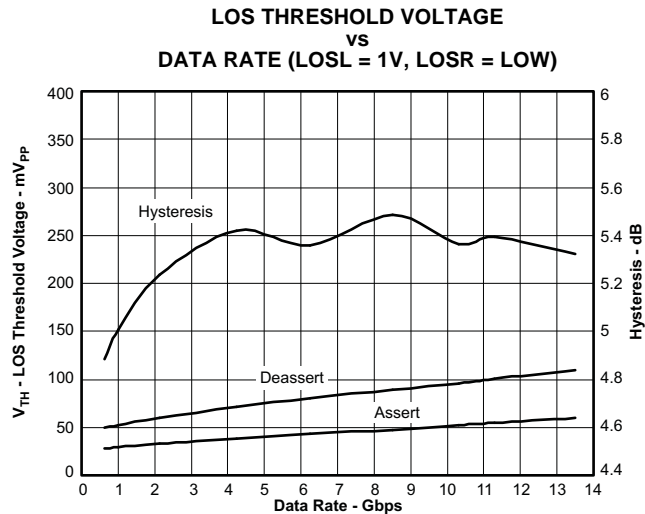
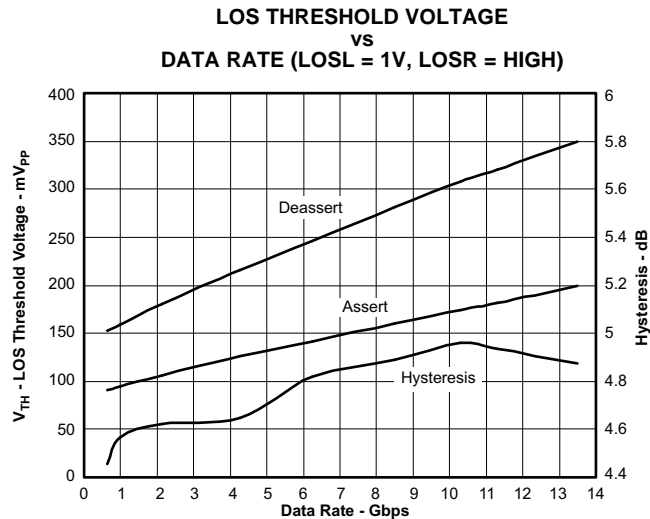


Figure 17.

**TYPICAL CHARACTERISTICS (continued)****Figure 18.****Figure 19.**

## Revision History

Changes from Original (August 2007) to Revision A	Page
• Added external pin configuration information - default device setup method to description .....	2
• Changed LN0 to LN1 in terminal functions table .....	3
• Changed LN1 to LN0 in terminal functions table .....	3
• Changed DE0 to DE1 in terminal functions table .....	3
• Changed DE1 to DE0 in terminal functions table .....	3
• Deleted fixed input equalizer in high frequency boost test conditions.....	4
• Added Twinaxial to <a href="#">Table 2</a> title.....	6
• Changed scale on <a href="#">Figure 7</a> .....	15
• Changed scale on <a href="#">Figure 8</a> .....	16
• Changed scale on <a href="#">Figure 9</a> .....	17

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK1101ERGPR	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	TLK 1101E	<a href="#">Samples</a>
TLK1101ERGPT	ACTIVE	QFN	RGP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	TLK 1101E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK1101ERGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLK1101ERGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK1101ERGPR	QFN	RGP	20	3000	853.0	449.0	35.0
TLK1101ERGPT	QFN	RGP	20	250	210.0	185.0	35.0

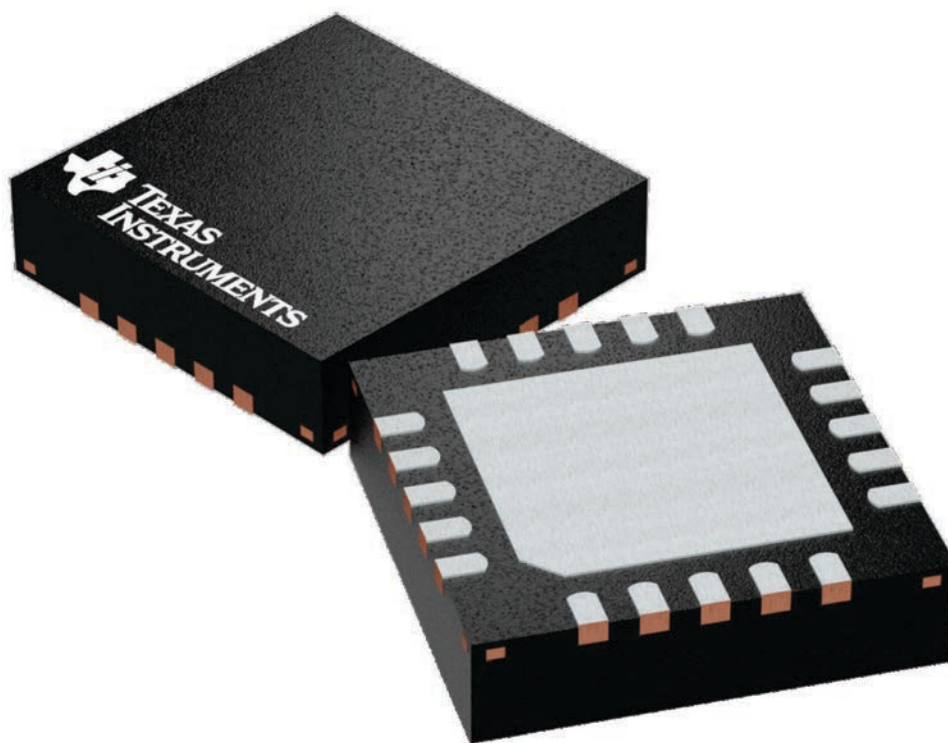
## GENERIC PACKAGE VIEW

**RGP 20**

**VQFN - 1 mm max height**

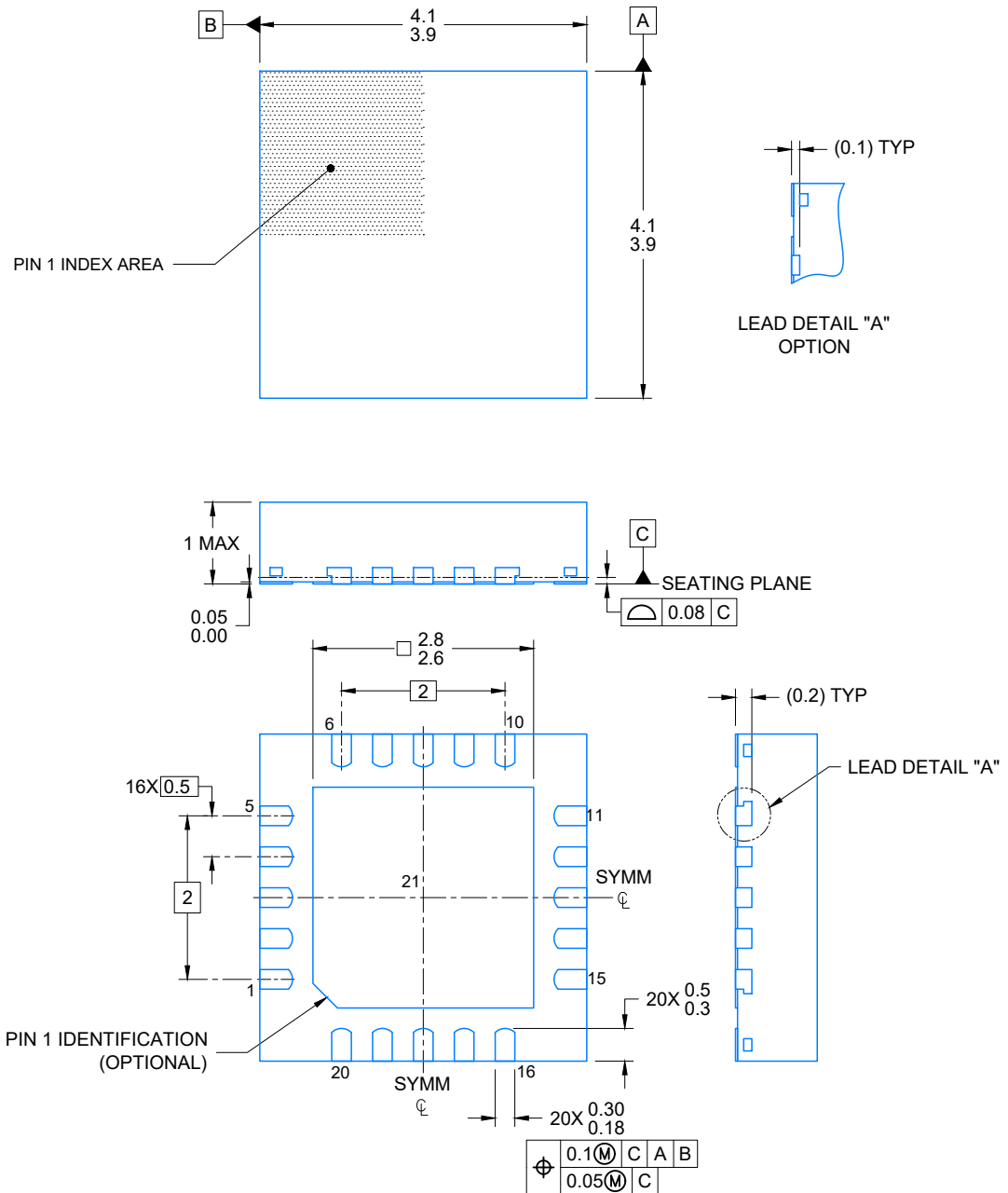
4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

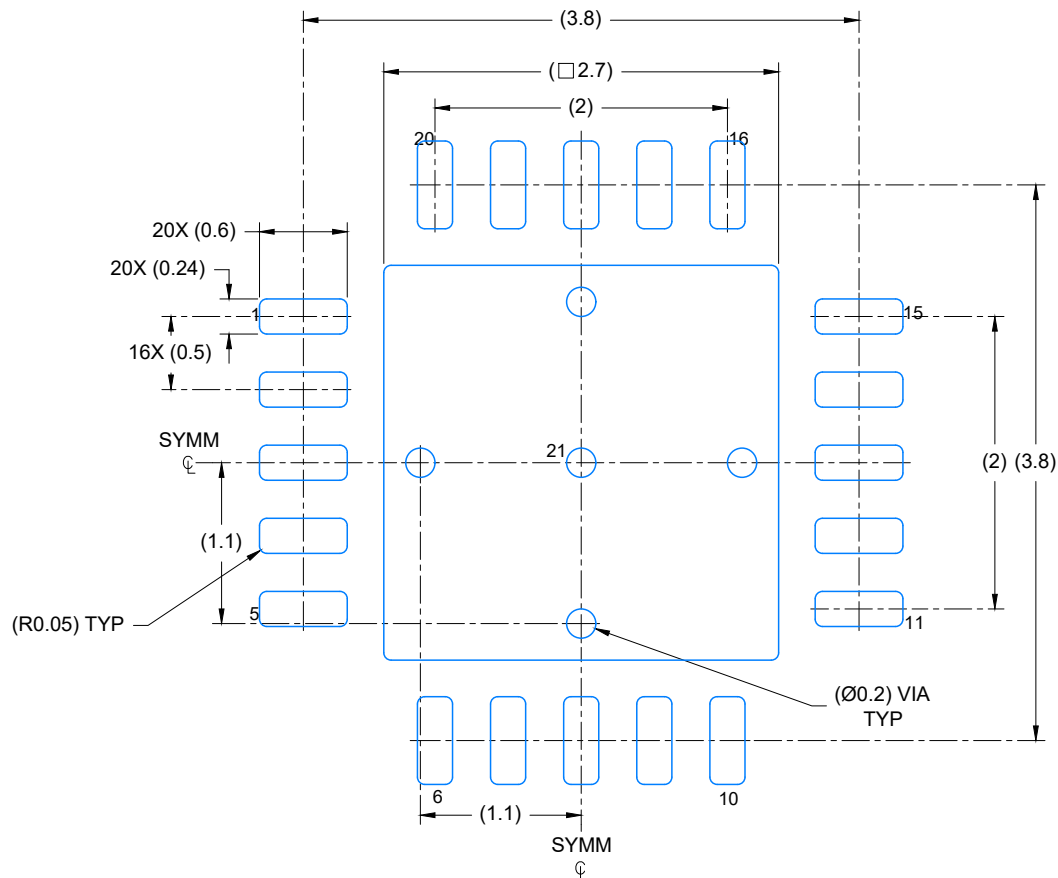
4224735/A



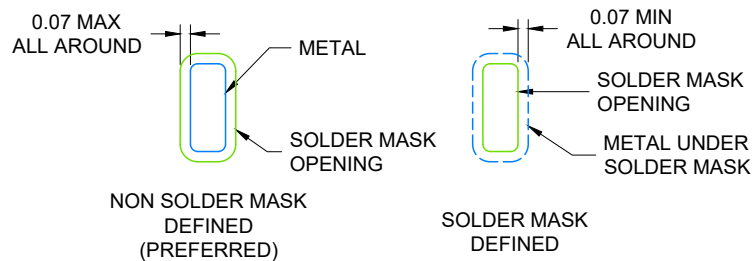
4219028/A 12/2018

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

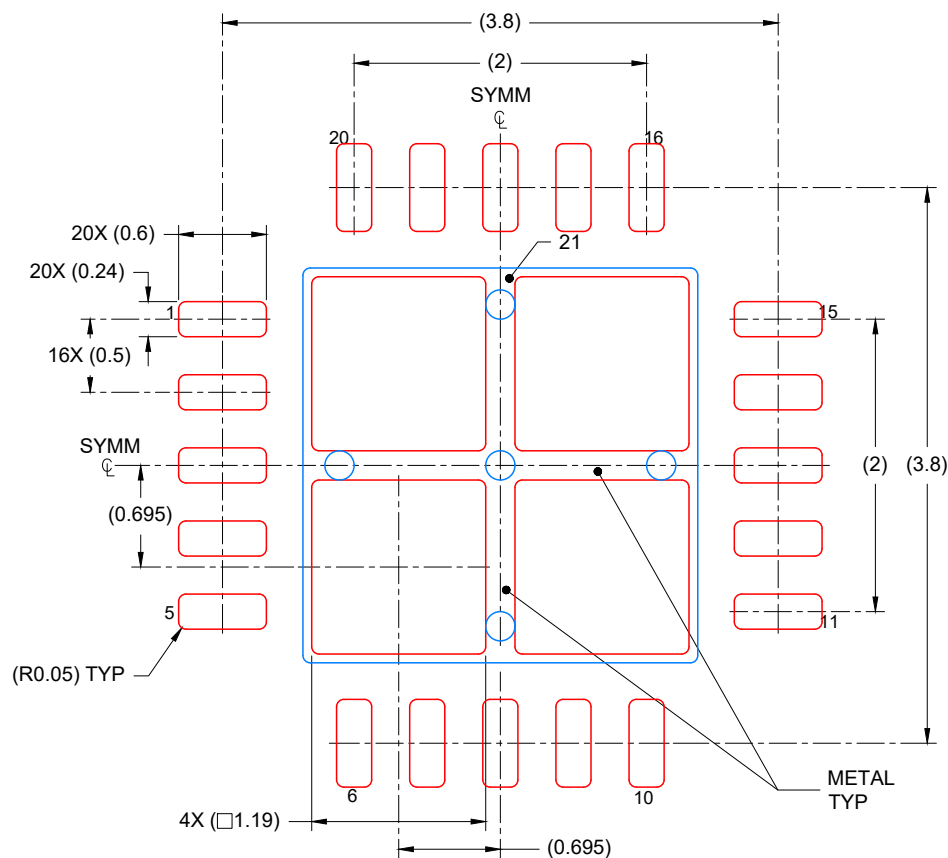


SOLDER MASK DETAILS

4219028/A 12/2018

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 77% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4219028/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated