DS90UB913A-Q1 25MHz 至 100MHz 10/12 位 FPD-Link III 串行器

1 特性

- 符合AEC-Q100 车规认证
  - 器件温度等级 2：环境工作温度范围为 -40℃ 至 +105℃
- 25MHz 至 100MHz 输入像素时钟支持
- 可编程数据有效载荷：
  - 10 位有效载荷，高达 100MHz
  - 12 位有效载荷，高达 75MHz
- 连续低延迟双向控制接口通道，带有 I2C 接口，支持 400kHz 传输速率
- 嵌入式时钟具有 DC 均衡编码，用于支持 AC 耦合互连
- 可驱动长达 15m 的同轴电缆或 20m 的屏蔽双绞线电缆
- 稳健的同轴电缆供电 (PoC) 运行
- 4 个专用通用输入/输出
- 串行器上提供 1.8V、2.8V 或 3.3V 兼容并行输入
- 1.8V 单电源
- 符合 ISO 10605 和 IEC 61000-4-2 ESD 标准
- 小尺寸串行器 (5mm × 5mm)

2 应用

- 汽车
  - 环视系统 (SVS)
  - 前置摄像头 (FC)
  - 后视摄像头 (RVC)
  - 传感器融合
  - 驾驶员监视摄像头 (DMS)
  - 远距卫星雷达、ToF 和激光雷达传感器
- 安防和监控
- 机器视觉 应用

3 说明

DS90UB913A-Q1 器件提供一个具有高速正向通道和双向控制通道的 FPD-Link III 接口，用来实现单一同轴电缆或差分对上的数据传输。DS90UB913A-Q1 器件的高速正向通道和双向控制通道数据路径上均包含差分信令。串行器/解串器对主要用于电子控制单元 (ECU) 中成像器与视频处理器的连接。该器件非常适用于驱动需要高达 12 位像素深度、2 个同步信号以及双向控制通道总线的视频数据。

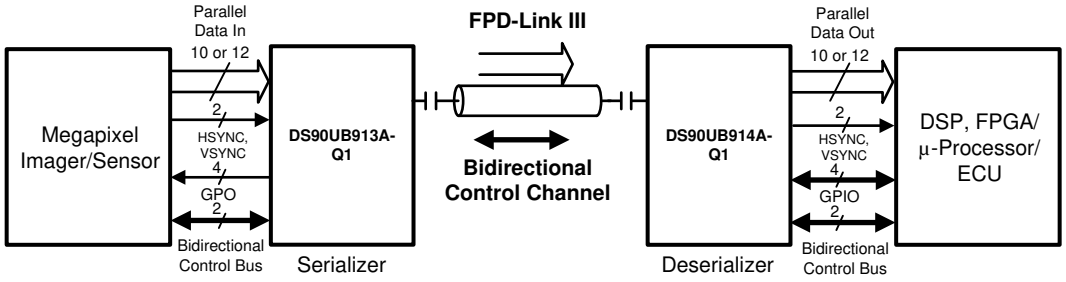
凭借德州仪器 (TI) 的嵌入式时钟技术，可在单一差分对上进行透明的全双工通信，从而运载不对称的双向控制通道信息。这个单个串行数据流通过消除并行数据与时钟路径间的偏差，简化了印刷电路板 (PCB) 走线和电缆上的宽数据总线传输。这样，通过限制数据路径的宽度，大大节省了系统成本，相应地减少了 PCB 层数、电缆宽度以及连接器尺寸和引脚数量。内部 DC 均衡编码/解码用于支持 AC 耦合互连。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DS90UB913A-Q1	WQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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- Added Power Over Coax supply noise to the recommended operating conditions table ... 8
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- Added strap pin input current specification for MODE and IDX pins ... 9
- Updated T_{JIT1} PCLK input jitter in the external oscillator mode ... 11
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- Revised coax connection diagram to include pulldown resistor for GPO2 40
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Changes from Revision C (April 2016) to Revision D **Page**

- Added back channel line rate = 5.5 MHz as test condition; also added footnote for clarification between MHz and Mbps distinction. 10
- Removed 'ns' unit from specifications referencing period in units of T. 11
- Updated test condition specs for jitter bandwidth regarding t_{JIT0}, t_{JIT1}, and t_{JIT2}. 11
- Added input external oscillator frequency range for pin/freq. 11
- Added parameter for typical external oscillator frequency stability. 11
- Added test conditions to t_{JIND}, t_{JINR}, and t_{JINT}. 15
- Added DOUT± as measured output pins for jitter parameters. 15
- Added note (6) for "Serializer output peak-to-peak total jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input". 15
- Added jitter tolerance curve for typical system IJT configuration with DS90UB913A linked to DS90UB914A. 16
- Added device functional mode table for external oscillator operation with example XCLKIN = 48MHz. 21

Changes from Revision B (December 2014) to Revision C **Page**

- 将文档拆分为有关器件 DS90UB913A-Q1 和 DS90UB914A-Q1 的两个独立文档 1
- 已修改汽车 特性 1
- Updated pin description for DIN to include active/inactive outputs corresponding to MODE setting. 5
- Added pin description to GPO pins to leave open if unused. 6
- Changed Air Discharge ESD Rating (IEC61000-4-2: RD = 330 Ω, CS = 150 pF) to minimum ±25000 V. 7
- Added RTV text to Thermal Information table 8
- Added GPO[3:0] typical pin capacitances. 9
- Changed Differential Output Voltage minimum specification. 9
- Changed Single-Ended Output Voltage minimum specification. 9
- Added Back Channel Differential Input Voltage minimum specification. 10
- Added Back Channel Single-Ended Input Voltage minimum specification. 10
- Updated IDDT for V_{DD_n}=1.89V, V_{DDIO}=3.6V, RL=100Ω, Random Pattern with f=100 MHz, 10-bit mode to typical value of 65 mA; value is currently 54 mA. 10
- Updated IDDT for V_{DD_n}=1.89V, V_{DDIO}=3.6V, RL=100Ω, Random Pattern with f=75 MHz, 12-bit high freq mode to typical value of 64 mA; value is currently 54 mA. 10
- Updated IDDT for V_{DD_n}=1.89V, V_{DDIO}=3.6V, RL=100Ω, Random Pattern with f=50 MHz, 12-bit low freq mode to typical value of 63 mA; value is currently 54 mA. 10
- Updated frequency ranges for MODE settings and also revised with correct maximum clock periods. Added footnote and nominal clock period to be in terms of 'T'.(5) 11
- Deleted Revised jitter freq. test conditions to be > f/20 and also updated typical values for $t_{jit0}$and t_{jit2}. 11
- Updated V_{OL} Output Low Level row with revised I_{OL} currents and max V_{OL} voltages, dependent upon V_{DDIO} voltage. 12
- Updated Figure 2 title to state '"Worst-Case" Test Pattern for Power Consumption'. 13
- Added footnote that states the following: "UI – Unit Interval is equivalent to one serialized data bit width. The UI scales with PCLK frequency." Add below calculations to footnote. 12-bit LF mode 1 UI = 1 / (PCLK_Freq. x 28) 12-bit HF mode 1 UI = 1 / (PCLK_Freq. x 2/3 x 28) 10-bit mode 1 UI = 1 / (PCLK_Freq. /2 x 28) 15
- Updated frequency requirements for 10-bit and 12-bit HF modes. 10-bit mode – 50 MHz to 100 MHz; 12-bit HF

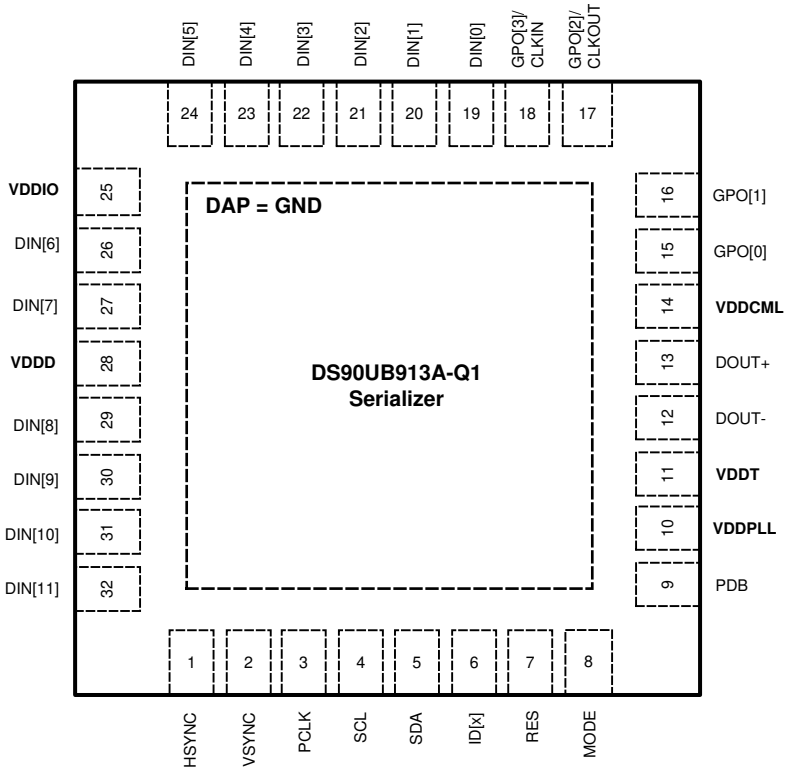
Changes from Revision A (June 2013) to Revision B **Page**

5 Device Comparison Table

PART NUMBER	FPD-III FUNCTION	PACKAGE	TRANSMISSION MEDIA	PCLK FREQUENCY
DS90UB913Q-Q1	Serializer	WQFN RTV (32)	STP	10 to 100 MHz
DS90UB913A-Q1	Serializer	WQFN RTV (32)	Coax or STP	25 to 100 MHz

6 Pin Configuration and Functions

32-Pin WQFN
Package RTV
Top View



Pin Functions: DS90UB913A-Q1 Serializer

PIN		I/O	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
DIN[0:11]	19,20,21,22, 23,24,26,27, 29,30,31,32	Inputs, LVCMOS w/ pulldown	Parallel Data Inputs. For 10-bit MODE, parallel inputs DIN[0:9] are active. DIN[10:11] are inactive and should not be used. Any unused inputs (including DIN[10:11]) should be No Connect. For 12-bit MODE (HF or LF), parallel inputs DIN[0:11] are active. Any unused inputs should be No Connect.
HSYNC	1	Input, LVCMOS w/ pulldown	Horizontal SYNC Input. Note: HS transition restrictions: 1. 12-bit Low-Frequency mode: No HS restrictions (raw) 2. 12-bit High-Frequency mode: No HS restrictions (raw) 3. 10-bit mode: HS restricted to no more than one transition per 10 PCLK cycles. Leave open if unused.
VSYNC	2	Input, LVCMOS w/ pulldown	Vertical SYNC Input. Note: VS transition restrictions: 1. 12-bit Low-Frequency mode: No VS restrictions (raw) 2. 12-bit High-Frequency mode: No VS restrictions (raw) 3. 10-bit High-Frequency mode: VS restricted to no more than one transition per 10 PCLK cycles. Leave open if unused.
PCLK	3	Input, LVCMOS w/ pulldown	Pixel Clock Input Pin. Strobe edge set by TRFB control register 0x03[0].

Pin Functions: DS90UB913A-Q1 Serializer (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GENERAL PURPOSE OUTPUT (GPO)			
GPO[1:0]	16,15	Output, LVCMOS	General-purpose output pins can be configured as outputs; used to control and respond to various commands. GPO[1:0] can be configured to be the outputs for input signals coming from GPIO[1:0] pins on the Deserializer or can be configured to be outputs of the local register on the Serializer. Leave open if unused.
GPO[2]/ CLKOUT	17	Output, LVCMOS	GPO[2] pin can be configured to be the output for input signal coming from the GPIO[2] pin on the Deserializer or can be configured to be the output of the local register on the Serializer. It can also be configured to be the output clock pin when the DS90UB913A-Q1 device is used in the External Oscillator mode. See *Device Functional Modes* section for a detailed description of External Oscillator Mode. It is recommended to pull GPO2 to GND with a minimum 40-kΩ resistor to ensure GPO2=LOW when PDB transitions from LOW to HIGH.
GPO[3]/ CLKIN	18	Input/Output, LVCMOS	GPO[3] can be configured to be the output for input signals coming from the GPIO[3] pin on the Deserializer or can be configured to be the output of the local register setting on the Serializer. It can also be configured to be the input clock pin when the DS90UB913A-Q1 Serializer is working with an external oscillator. See *Device Functional Modes* section for a detailed description of External Oscillator Mode. Leave open if unused.
BIDIRECTIONAL CONTROL BUS - I2C-COMPATIBLE			
SCL	4	Input/Output, Open Drain	Clock line for the bidirectional control bus communication SCL requires an external pullup resistor to V_{DDIO}.
SDA	5	Input/Output, Open Drain	Data line for the bidirectional control bus communication SDA requires an external pullup resistor to V_{DDIO}.
MODE	8	Input, analog	Device Mode Select Resistor (Rmode) to Ground and 10-kΩ pullup to 1.8 V rail. MODE pin on the Serializer can be used to select whether the system is running off the PCLK from the imager or an external oscillator. See details in Table 2.
ID[x]	6	Input, analog	Device ID Address Select The ID[x] pin on the Serializer is used to assign the I2C device address. Resistor (RID) to Ground and 10-kΩ pullup to 1.8 V rail. See Table 6.
CONTROL AND CONFIGURATION			
PDB	9	Input, LVCMOS w/ pulldown	Power Down Mode Input Pin PDB = H, Serializer is enabled and is ON. PDB = L, Serializer is in Power Down mode. When the Serializer is in Power Down, the PLL is shutdown, and IDD is minimized. Programmed control register data is NOT retained and reset to default values.
RES	7	Input, LVCMOS w/ pulldown	Reserved **This pin MUST be tied LOW.**
FPD–Link III INTERFACE			
DOUT+	13	Input/Output, CML	Non-inverting differential output, bidirectional control channel input. The interconnect must be AC Coupled with a 0.1-µF capacitor.
DOUT-	12	Input/Output, CML	Inverting differential output, bidirectional control channel input. The interconnect must be AC Coupled with a 0.1-µF capacitor. For applications using single-ended coaxial interconnect, a 0.047-µF AC coupling capacitor should be placed in series with a 50Ω resistor before terminating to GND.
POWER AND GROUND (1)			
VDDPLL	10	Power, Analog	PLL Power, 1.8 V ±5%.
VDDT	11	Power, Analog	Tx Analog Power, 1.8 V ±5%.
VDDCML	14	Power, Analog	CML & Bidirectional Channel Driver Power, 1.8 V ±5%.
VDDD	28	Power, Digital	Digital Power, 1.8 V ±5%.
VDDIO	25	Power, Digital	Power for I/O stage. The single-ended inputs and SDA, SCL are powered from V_{DDIO}. VDDIO can be connected to a 1.8 V ±5% or 2.8 V ±10% or 3.3 V ±10%.

(1) See *Power-Up Requirements and PDB Pin*.

Pin Functions: DS90UB913A-Q1 Serializer (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 9 vias.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage – V_{DD_n} (V_{DDPLL}, V_{DDT}, V_{DDCML}, V_{DDD})	−0.3	2.5	V
Supply Voltage – V_{DDIO}	−0.3	4.0	V
LVCMOS Input Voltage	−0.3	V_{DDIO} + 0.3	V
CML Driver I/O Voltage – (V_{DD_n})	-0.3	V_{DD_n} + 0.3	V
Junction Temperature		150	°C
Storage temperature range, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3B		±8000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	Corner pins (1, 8, 9, 16, 17, 24, 25, 32)	±1000	
			Other pins		
		(IEC 61000-4-2) R_D = 330 Ω, C_s = 150pF	Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	±25000	
			Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	±7000	
		(ISO10605) R_D = 330 Ω, C_s = 150/330 pF R_D = 2 KΩ, C_s = 150/330 pF	Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	±15000	
			Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply Voltage (V_{DD_n})		1.71	1.8	1.89	V
LVCMOS Supply Voltage	V_{DDIO}= 1.8 V	1.71	1.8	1.89	V
	V_{DDIO}= 3.3 V	3	3.3	3.6	
	V_{DDIO}= 2.8 V	2.52	2.8	3.08	
Supply Noise(1)	V_{DD_n} = 1.8 V			25	mVp-p
	V_{DDIO} = 1.8 V			25	
	V_{DDIO} = 3.3 V			50	

(1) Supply noise testing was done with minimum capacitors (as shown on Figure 36, Figure 32 on the PCB. A sinusoidal signal is AC coupled to the V_{DD_n} (1.8 V) supply with amplitude = 25 mVp-p measured at the device V_{DD_n} pins. Bit error rate testing of input to the Ser and output of the Des with 10-meter cable shows no error when the noise frequency on the Ser is less than 1 MHz. The Des on the other hand shows no error when the noise frequency is less than 750 kHz.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Power-Over-Coax Supply Noise	f = 30 Hz - 1 KHz, t_{rise} > 100 µs Measured differentially between DOUT+ and DOUT– (coax mode only)		10		mVp-p
	f = 1 KHz - 50 MHz Measured differentially between DOUT+ and DOUT- (coax mode only)		10		mVp-p
Operating Free Air Temperature (T_A)		–40	25	105	°C
PCLK Clock Frequency	10-bit mode	50		100	MHz
	12-bit HF mode	37.5		75	MHz
	12-bit LF mode	25		50	MHz
External Clock Input Frequency to GPO3	10-bit mode	25		50	MHz
	12-bit HF mode	25		50	MHz
	12-bit LF mode	25		50	MHz

7.4 Thermal Information

THERMAL METRIC(1)		DS90UB913A-Q1 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics(1)(2)(3)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS 3.3 V I/O (SER INPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 3 V to 3.6 V		2		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 3 V to 3.6 V		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or 3.6 V, V_{IN} = 3 V to 3.6 V		–20	±1	20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3 V to 3.6 V, I_{OH} = −4 mA		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3 V to 3.6 V, I_{OL} = 4 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	Serializer GPO Outputs		–15		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0 V, V_{OUT} = 0 V or V_{DDIO}	Serializer GPO Outputs	–20		20	µA

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD and ΔVOD which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified.

Electrical Characteristics[1][2][3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{GPO}	Pin Capacitance	GPO [3:0]			1.5		pF
LVCMOS DC SPECIFICATIONS 1.8 V I/O (SER INPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 1.71 V to 1.89 V		0.65 V_{IN}		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 1.71 V to 1.89 V		GND		0.35 V_{IN}	V
I_{IN}	Input Current	V_{IN} = 0 V or 1.89 V, V_{IN} = 1.71 V to 1.89 V		–20	±1	20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71 V to 1.89 V, I_{OH} = −4 mA		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 1.71 V to 1.89 V I_{OL} = 4 mA		GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	Serializer GPO Outputs		–11		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0 V, V_{OUT} = 0 V or V_{DDIO}	Serializer GPO Outputs	-20		20	µA
C_{GPO}	Pin Capacitance	GPO [3:0]			1.5		pF
$I_{IN-STRAP}$	Strap pin input current	V_{IN} = 0 V to V_{DD_n}		-1		1	µA
LVCMOS DC SPECIFICATIONS 2.8 V I/O (SER INPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 2.52 V to 3.08 V		0.7 V_{IN}		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 2.52 V to 3.08 V		GND		0.3 V_{IN}	V
I_{IN}	Input Current	V_{IN} = 0 V or 3.08 V, V_{IN} = 2.52 V to 3.08 V		–20	±1	20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 2.52 V to 3.08 V, I_{OH} = −4 mA		V_{DDIO} - 0.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} =2.52 V to 3.08V I_{OL} = 4 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	Serializer GPO Outputs		–11		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0 V, V_{OUT} = 0 V or V_{DDIO}	Serializer GPO Outputs	–20		20	µA
C_{GPO}	Pin Capacitance	GPO [3:0]			1.5		pF
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT-)							
V_{OD}	Differential Output Voltage	R_L = 100 Ω (Figure 6), Back Channel Disabled		640		824	mV
V_{OUT}	Single-Ended Output Voltage	R_L = 50 Ω (Figure 6), Back Channel Disabled		320		412	mV
ΔV_{OD}	Differential Output Voltage Unbalance	R_L = 100 Ω			1	50	mV
V_{OS}	Output Offset Voltage	R_L = 100 Ω (Figure 6)			V_{DD_n} - $V_{OD/2}$		V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100 Ω			1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+ = 0 V or DOUT– = 0 V			–26		mA
R_T	Differential Internal Termination Resistance	Differential across DOUT+ and DOUT–		80	100	120	Ω
	Single-ended Termination Resistance	DOUT+ or DOUT–		40	50	60	Ω

Electrical Characteristics[1][2][3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ID-BC}	Back Channel Differential Input Voltage	Back Channel Frequency = 5.5 MHz[4]		260			mV
V_{IN-BC}	Back Channel Single-Ended Input Voltage			130			mV
SERIALIZER SUPPLY CURRENT							
I_{DDT}	Serializer (Tx) V_{DD_n} Supply Current (includes load current)	R_L = 100 Ω WORST CASE pattern (Figure 2)	V_{DD_n} = 1.89 V V_{DDIO} = 3.6 V f = 100 MHz, 10-bit mode Default Registers		61	80	mA
			V_{DD_n} = 1.89 V V_{DDIO} = 3.6 V f = 75 MHz, 12-bit high frequency mode Default Registers		61	80	mA
			V_{DD_n} = 1.89 V V_{DDIO} = 3.6 V f = 50 MHz, 12-bit low frequency mode Default Registers		61	80	
I_{DDT}	Serializer (Tx) V_{DD_n} Supply Current (includes load current)	R_L = 100 Ω RANDOM PRBS-7 pattern	V_{DD_n} = 1.89 V V_{DDIO} = 3.6 V f = 100 MHz, 10-bit mode Default Registers		65		mA
			V_{DD_n} = 1.89 V V_{DDIO} = 3.6 V f = 75 MHz, 12-bit high frequency mode Default Registers		64		
			V_{DD_n} = 1.89 V V_{DDIO} = 3.6 V f = 50 MHz, 12-bit low frequency mode Default Registers		63		
I_{DDIOT}	Serializer (Tx) V_{DDIO} Supply Current (includes load current)	R_L = 100 Ω WORST CASE pattern (Figure 2)	V_{DDIO} = 1.89 V f = 75 MHz, 12-bit high frequency mode Default Registers		1.5	3	mA
			V_{DDIO} = 3.6 V f = 75 MHz, 12-bit high frequency mode Default Registers		5	8	
I_{DDTZ}	Serializer (Tx) Supply Current Power Down	PDB = 0V; All other LVCMOS Inputs = 0 V	V_{DDIO}=1.89 V Default Registers		300	1000	µA
			V_{DDIO} = 3.6 V Default Registers		300	1000	µA
I_{DDIOTZ}	Serializer (Tx) V_{DDIO} Supply Current Power Down	PDB = 0V; All other LVCMOS Inputs = 0 V	V_{DDIO} = 1.89 V Default Registers		15	100	µA
			V_{DDIO} = 3.6 V Default Registers		15	100	µA

(4) The back channel frequency (MHz) listed is the frequency of the internal clock used to generate the encoded back channel data stream. The data rate (Mbps) of the encoded back channel stream is the back channel frequency divided by 2.

7.6 Recommended Serializer Timing For PCLK(1) (2)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN / FREQ	MIN	NOM	MAX	UNIT
t_{TCP}	Transmit Clock Period	10-bit mode 50 MHz – 100 MHz		10	T	20	ns
		12-bit high frequency mode 37.5 MHz - 75MHz		13.33	T	26.67	ns
		12-bit low frequency mode 25 MHz - 50MHz		20	T	40	ns
t_{TCIH}	Transmit Clock Input High Time			0.4T	0.5T	0.6T	
t_{TCIL}	Transmit Clock Input Low Time			0.4T	0.5T	0.6T	
t_{CLKT}	PCLK Input Transition Time (Figure 7)	10-bit mode 50 MHz – 100 MHz		0.05T	0.25T	0.3T	
		12-bit high frequency mode 37.5 MHz - 75MHz		0.05T	0.25T	0.3T	
		12-bit low frequency mode 25 MHz - 50MHz		0.05T	0.25T	0.3T	
t_{JIT0}	PCLK Input Jitter (PCLK from imager mode)(3)	LPF = f/20, CDR PLL Loop BW = f/15, BER = 1E-10	f_{PCLK} = 25 – 100 MHz(4)			0.3	UI
t_{JIT1}	PCLK Input Jitter (External Oscillator mode)(3)	LPF = f/20, CDR PLL Loop BW = f/15, BER = 1E-10	f_{PCLK} = 25 – 100 MHz(4)		1T		
t_{JIT2}	External Oscillator Jitter(3)	LPF = f/20, CDR PLL Loop BW = f/15, BER = 1E-10	f_{OSC} = 25 – 50 MHz(5)			0.3	UI
Δ_{OSC}	External Oscillator Frequency Stability		f_{OSC} = 25 – 50 MHz(5)		±50		ppm

(1) Recommended Input Timing Requirements are input specifications and not tested in production.
(2) T is the period of the PCLK.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified.
(4) f_{PCLK} denotes input PCLK frequency to the device.
(5) f_{OSC} denotes input external oscillator frequency to the device (GPO3/CLKIN).

7.7 AC Timing Specifications (SCL, SDA) - I2C-Compatible

Over recommended supply and temperature ranges unless otherwise specified. (Figure 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD:DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
$t_{SU:DAT}$	Data Set Up Time	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU:STO}$	Set Up Time for STOP Condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free time between Stop and Start	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time	Standard Mode			300	ns
		Fast Mode			300	ns

7.8 Bidirectional Control Bus DC Timing Specifications (SCL, SDA) - I2C-Compatible(1)

Over recommended supply and temperature ranges unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
V_{IH}	Input High Level	SDA and SCL	0.7*V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level	SDA and SCL	GND		0.3*V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}	Output Low Level(2)	SDA, V_{DDIO} = 1.8 V, I_{OL}= 0.9 mA	0		0.36	V
		SDA, V_{DDIO} = 3.3 V, I_{OL}= 1.6 mA	0		0.4	
I_{IN}	Input Current	SDA or SCL, V_{IN}= V_{DDIO} OR GND	−10		10	µA
t_R	SDA Rise Time-READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF (Figure 1)		430		ns
t_F	SDA Fall Time-READ			20		ns
C_{IN}		SDA or SCL		<5		pF

(1) Specification is verified by design.
(2) FPD-Link device was designed primarily for point-to-point operation and a small number of attached slave devices. As such the Minimum I_{OL} pullup current is targeted to lower value than the minimum I_{OL} in the I2C specification.

7.9 Timing Diagrams

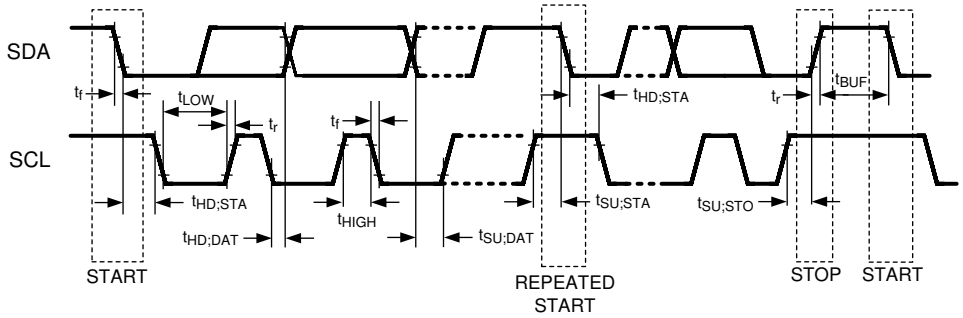


Figure 1. Bi-directional Control Bus Timing

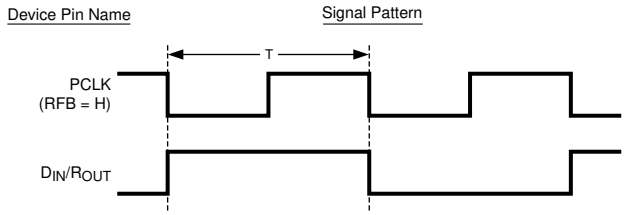


Figure 2. "Worst Case" Test Pattern for Power Consumption

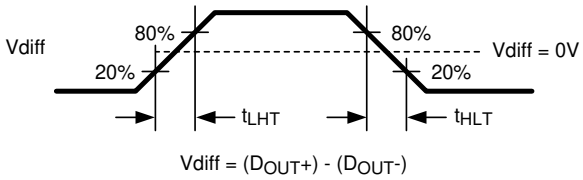


Figure 3. Serializer CML Output Load and Transition Times

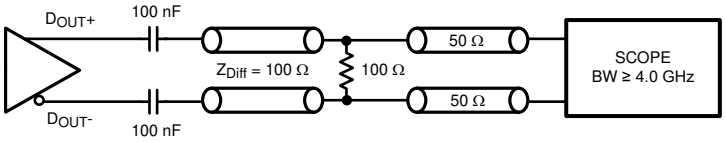


Figure 4. Serializer CML Output Load and Transition Times

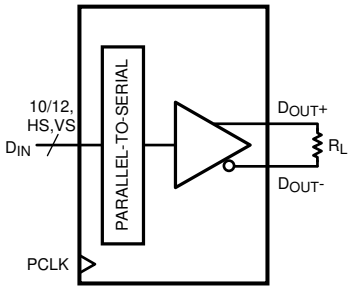


Figure 5. Serializer VOD Setup

Timing Diagrams (continued)

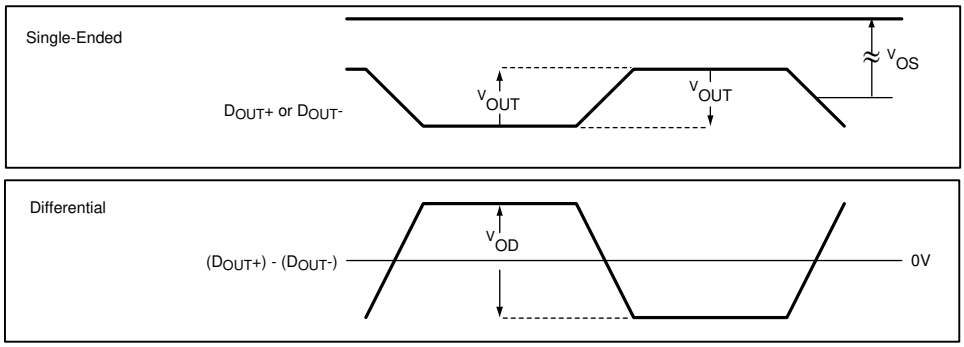


Figure 6. Serializer VOD Diagram

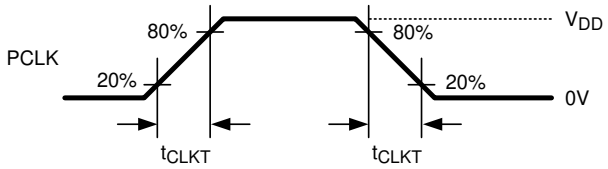


Figure 7. Serializer Input Clock Transition Times

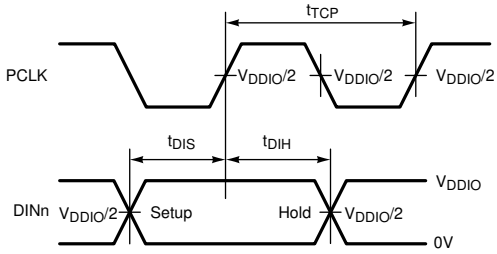


Figure 8. Serializer Setup/Hold Times

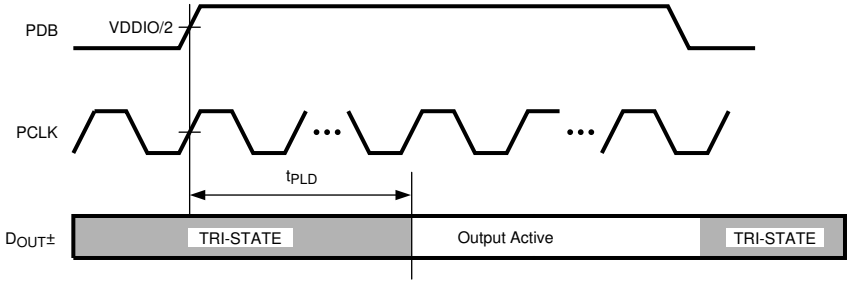


Figure 9. Serializer PLL Lock Time

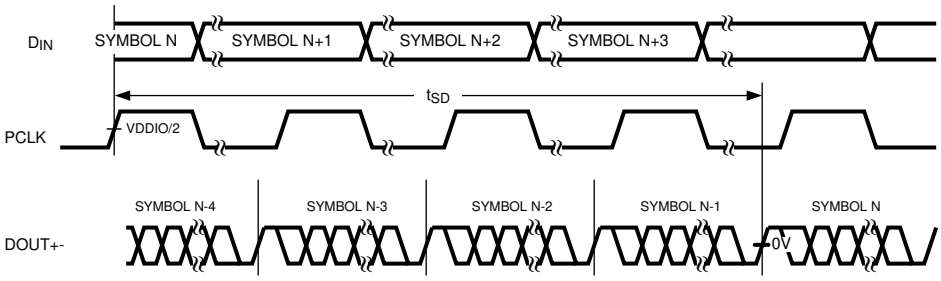


Figure 10. Serializer Delay

7.10 Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{LHT}	CML Low-to-High Transition Time	R_L = 100 Ω (Figure 3)			150	330	ps
t_{HLT}	CML High-to-Low Transition Time	R_L = 100 Ω (Figure 3)			150	330	ps
t_{DIS}	Data Input Setup to PCLK	Serializer Data Inputs (Figure 8)		2			ns
t_{DIH}	Data Input Hold from PCLK			2			ns
t_{PLD}	Serializer PLL Lock Time (1)(2)	R_L = 100 Ω (Figure 9)			1	2	ms
t_{SD}	Serializer Delay (2)	R_T = 100 Ω, 10–bit mode Register 0x03h b[0] (TRFB = 1) (Figure 10)		32.5T	38T	44T	
		R_T = 100 Ω, 12–bit mode Register 0x03h b[0] (TRFB = 1) (Figure 10)		11.75T	13T	15T	
t_{JIND}	Serializer Output Deterministic Jitter (3)(4)(5)	PRBS-7 test pattern, CDR PLL Loop BW = ƒ/15, BER = 1E-10	DOUT±		0.17	0.26	UI
t_{JINR}	Serializer Output Random Jitter (3)(4)(5)	PRBS-7 test pattern, CDR PLL Loop BW = ƒ/15, BER = 1E-10	DOUT±		0.016		UI
t_{JINT}	Peak-to-Peak Serializer Output Total Jitter (3)(5)(6)	PRBS-7 test pattern, CDR PLL Loop BW = ƒ/15, BER = 1E-10	DOUT±		0.4	0.52	UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth	10–bit mode PCLK = 100 MHz. Default Registers			2.20		MHz
		12–bit high frequency mode PCLK = 75 MHz. Default Registers			2.20		
		12–bit low frequency mode PCLK = 50 MHz. Default Registers			2.20		
δ_{STX}	Serializer Jitter Transfer Function (Peaking)	10–bit mode PCLK = 100 MHz. Default Registers			1.06		dB
		12–bit high frequency mode PCLK = 75 MHz. Default Registers			1.09		
		12–bit low frequency mode PCLK = 50 MHz. Default Registers			1.16		
δ_{STXf}	Serializer Jitter Transfer Function (Peaking Frequency)	10–bit mode PCLK = 100 MHz. Default Registers			400		kHz
		12–bit high frequency mode PCLK = 75 MHz. Default Registers			500		
		12–bit low frequency mode PCLK = 50 MHz. Default Registers			600		

(1) t_{PLD} is the time required by the serializer to obtain lock when exiting power-down state with an active PCLK.
(2) Specification is verified by design.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified.
(4) Specification is verified by characterization and is not tested in production.
(5) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.
10-bit mode: 1 UI = 1 / (PCLK_Freq. /2 x 28)
12-bit HF mode: 1 UI = 1 / (PCLK_Freq. x 2/3 x 28)
12-bit LF mode: 1 UI = 1 / (PCLK_Freq. x 28)
(6) Serializer output peak-to-peak total jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input.

7.11 Typical Characteristics

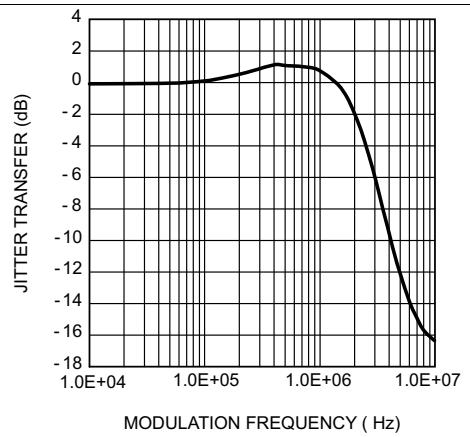


Figure 11. Typical Serializer Jitter Transfer Function

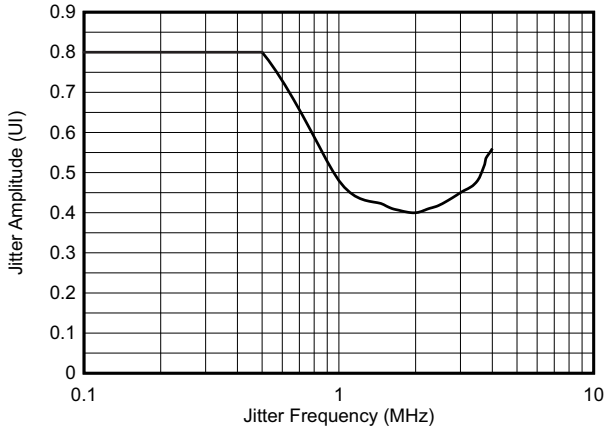


Figure 12. Typical System Input Jitter Tolerance Curve - DS90UB913A Linked to DS90UB914A

8 Detailed Description

8.1 Overview

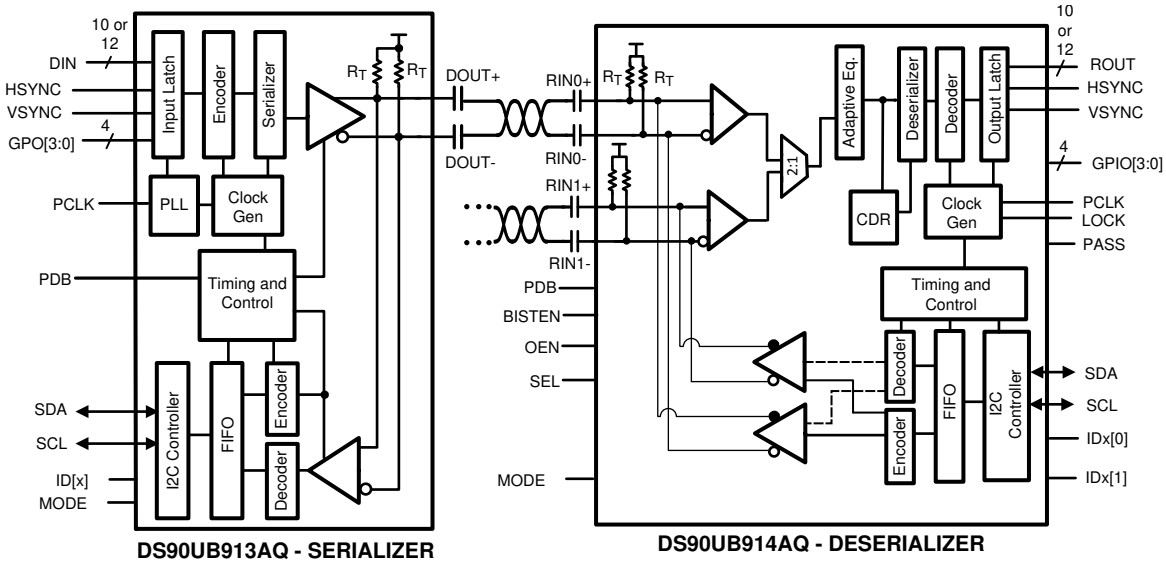
The DS90UB913A-Q1 is optimized to interface with the DS90UB914A-Q1 using a 50-Ω coax interface. The DS90UB913A-Q1 will also work with the DS90UB914A-Q1 using an STP interface.

The DS90UB913A/914A FPD- Link III chipsets are intended to link mega-pixel camera imagers and video processors in ECUs. The Serializer/Deserializer chipset can operate from 25 MHz to 100 MHz pixel clock frequency. The DS90UB913A-Q1 device transforms a 10/12-bit wide parallel LVCMOS data bus along with a bidirectional control channel control bus into a single high-speed differential pair. The high speed serial bit stream contains an embedded clock and DC-balanced information which enhances signal quality to support AC coupling. The DS90UB914A-Q1 device receives the single serial data stream and converts it back into a 10/12-bit wide parallel data bus together with the control channel data bus. The DS90UB913A/914A chipsets can accept up to:

- 12-bits of DATA + 2 bits SYNC for an input PCLK range of 25 MHz to 50 MHz in the 12-bit low frequency mode. Note: No HS/VS restrictions (raw).
- 12-bits of DATA + 2 SYNC bits for an input PCLK range of 37.5 MHz to 75 MHz in the 12-bit high frequency mode. Note: No HS/VS restrictions (raw).
- 10-bits of DATA + 2 SYNC bits for an input PCLK range of 50 MHz to 100 MHz in the 10-bit mode. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles.

The DS90UB913A/914A chipset offer customers the choice to work with different clocking schemes. The DS90UB913A/914A chipsets can use an external oscillator as the reference clock source for the PLL (see section *DS90UB913A/914A Operation with External Oscillator as Reference Clock*) or PCLK from the imager as primary reference clock to the PLL (see section *DS90UB913A/914A Operation with Pixel Clock from Imager as Reference Clock*).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Serial Frame Format

The High Speed Forward Channel is composed of 28 bits of data containing video data, sync signals, I2C and parity bits. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. The 28-bit frame structure changes in the 12-bit low frequency mode, 12-bit high frequency mode and the 10-bit mode internally and is seamless to the customer. The bidirectional control channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex low speed forward and backward path across the serial link together with a high speed forward channel without the dependence on the video blanking phase.

8.3.2 Line Rate Calculations for the DS90UB913A/914A

The DS90UB913A-Q1 device divides the clock internally by divide-by-1 in the 12-bit low frequency mode, by divide-by-2 in the 10-bit mode and by divide-by-1.5 in the 12-bit high frequency mode. Conversely, the DS90UB914A-Q1 multiplies the recovered serial clock to generate the proper pixel clock output frequency. Thus the maximum line rate in the three different modes remains 1.4 Gbps. The following are the formulae used to calculate the maximum line rate in the different modes:

- For the 12-bit low frequency mode, Line rate = f_{PCLK}*28; for example, f_{PCLK} = 50 MHz, line rate = 50*28 = 1.4 Gbps
- For the 12-bit high frequency mode, Line rate = f_{PCLK}*(2/3)*28; for example, f_{PCLK} = 75 MHz, line rate = (75)*(2/3)*28 = 1.4 Gbps
- For the 10-bit mode, Line rate = f_{PCLK}/2*28; for example, f_{PCLK} = 100 MHz, line rate = (100/2)*28 = 1.4 Gbps

8.3.3 Error Detection

The chipset provides error detection operations for validating data integrity in long distance transmission and reception. The data error detection function offers users flexibility and usability of performing bit-by-bit data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bidirectional control channel data across the serial link
- Parallel video/sync data across the serial link

The chipset provides 1 parity bit on the forward channel and 4 cyclic redundancy check (CRC) bits on the back channel for error detection purposes. The DS90UB913A/914A chipset checks the forward and back channel serial links for errors and stores the number of detected errors in two 8-bit registers in the Serializer and the Deserializer respectively.

To check parity errors on the forward channel, monitor registers 0x1A and 0x1B on the DS90UB914A. If there is a loss of LOCK, then the counters on registers 0x1A and 0x1B are reset. ***Whenever there is a parity error on the forward channel, the PASS pin will go low.***

To check CRC errors on the back-channel, monitor registers 0x0A and 0x0B on the Serializer.

Feature Description (continued)

8.3.4 Synchronizing Multiple Cameras

For applications requiring multiple cameras for frame-synchronization, it is recommended to utilize the General Purpose Input/Output (GPIO) pins to transmit control signals to synchronize multiple cameras together. To synchronize the cameras properly, the system controller needs to provide a field sync output (such as a vertical or frame sync signal) and the cameras must be set to accept an auxiliary sync input. The vertical synchronize signal corresponds to the start and end of a frame and the start and end of a field. Note this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the bidirectional control channel, there will be a time variation of the GPIO signals arriving at the different target devices (between the parallel links). The maximum latency delta (t1) of the GPIO data transmitted across multiple links is 25 µs.

NOTE

The user must verify that the timing variations between the different links are within their system and timing specifications.

See Figure 13 for an example of this function.

The maximum time (t1) between the rising edge of GPIO (that is, sync signal) to the time the signal arrives at Camera A and Camera B is 25 µs.

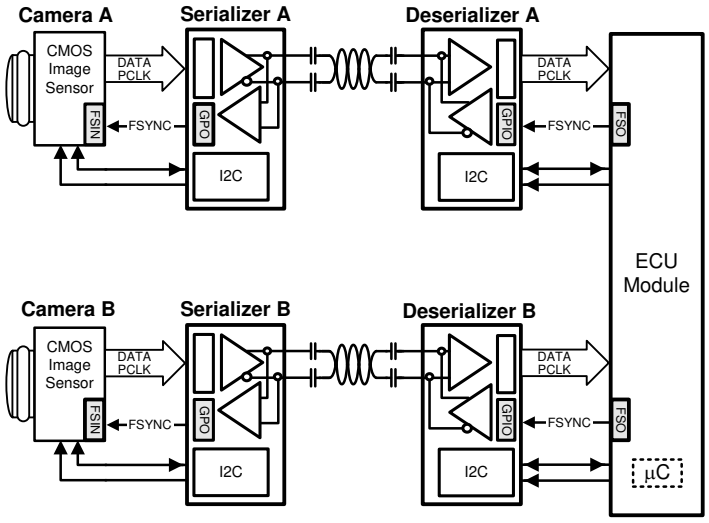


Figure 13. Synchronizing Multiple Cameras

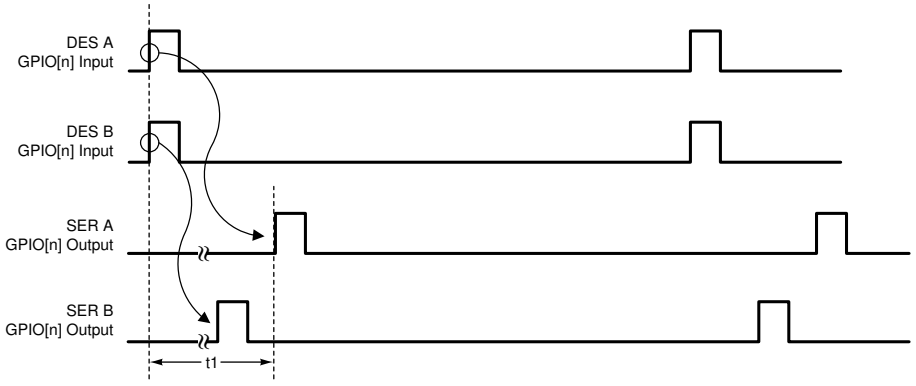


Figure 14. GPIO Delta Latency

Feature Description (continued)

8.3.5 General Purpose I/O (GPIO) Descriptions

There are 4 GPOs on the Serializer and 4 GPIOs on the Deserializer when the DS90UB913A/914A chipsets are run off the pixel clock from the imager as the reference clock source. The GPOs on the Serializer can be configured as outputs for the input signals that are fed into the Deserializer GPIOs. In addition, the GPOs on the Serializer can behave as outputs of the local register on the Serializer. The GPIOs on the Deserializer can be configured to be the input signals feeding the GPOs (configured as outputs) on the Serializer. In addition the GPIOs on the Deserializer can be configured to behave as outputs of the local register on the Deserializer. The DS90UB913A Serializer GPOs cannot be configured as inputs for remote communication with Deserializer. If the DS90UB913A/914A chipsets are run off the external oscillator source as the reference clock, then GPO3 on the Serializer is automatically configured to be the input for the external clock and GPO2 is configured to be the output of the divide-by-2 clock which is fed into the imager as its reference clock. In this case, the GPIO2 and GPIO3 on the Deserializer can only behave as outputs of the local register on the Deserializer. The GPIO maximum switching rate is up to 66 kHz when configured for communication between Deserializer GPIO to Serializer GPO.

8.3.6 LVCMOS V_{DDIO} Option

1.8 V/2.8 V/3.3 V Serializer inputs are user configurable to provide compatibility with 1.8 V, 2.8 V and 3.3 V system interfaces.

8.3.7 Pixel Clock Edge Select (TRFB / RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the falling edge of the PCLK.

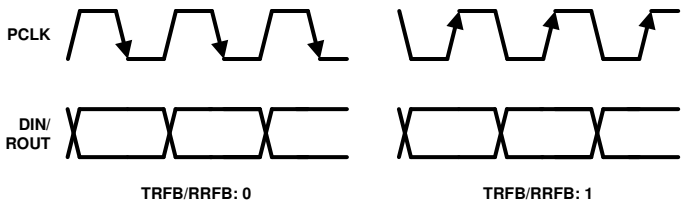


Figure 15. Programmable PCLK Strobe Select

8.3.8 Power Down

The SER has a PDB input pin to ENABLE or power down the device. Enabling PDB on the SER will disable the link to save power. If PDB = HIGH, the SER will operate at its internal default oscillator frequency when the input PCLK stops. When the PCLK starts again, the SER locks to the valid input PCLK and transmit the data to the DES. When PDB = LOW, the high-speed driver outputs are static HIGH. Please refer to *Power-Up Requirements and PDB Pin* for power-up requirements.

8.4 Device Functional Modes

8.4.1 DS90UB913A/914A Operation with External Oscillator as Reference Clock

In some applications, the pixel clock that comes from the imager can have jitter which exceeds the tolerance of the DS90UB913A/914A chipsets. In this case, the DS90UB913A-Q1 device should be operated by using an external clock source as the reference clock for the DS90UB913A/914A chipsets. **This is the recommended operating mode.** The external oscillator clock output goes through a divide-by-2 circuit in the DS90UB913A-Q1 Serializer and this divided clock output is used as the reference clock for the imager. The output data and pixel clock from the imager are then fed into the DS90UB913A-Q1 device. Figure 16 shows the operation of the DS90UB13A/914A chipsets while using an external automotive grade oscillator.

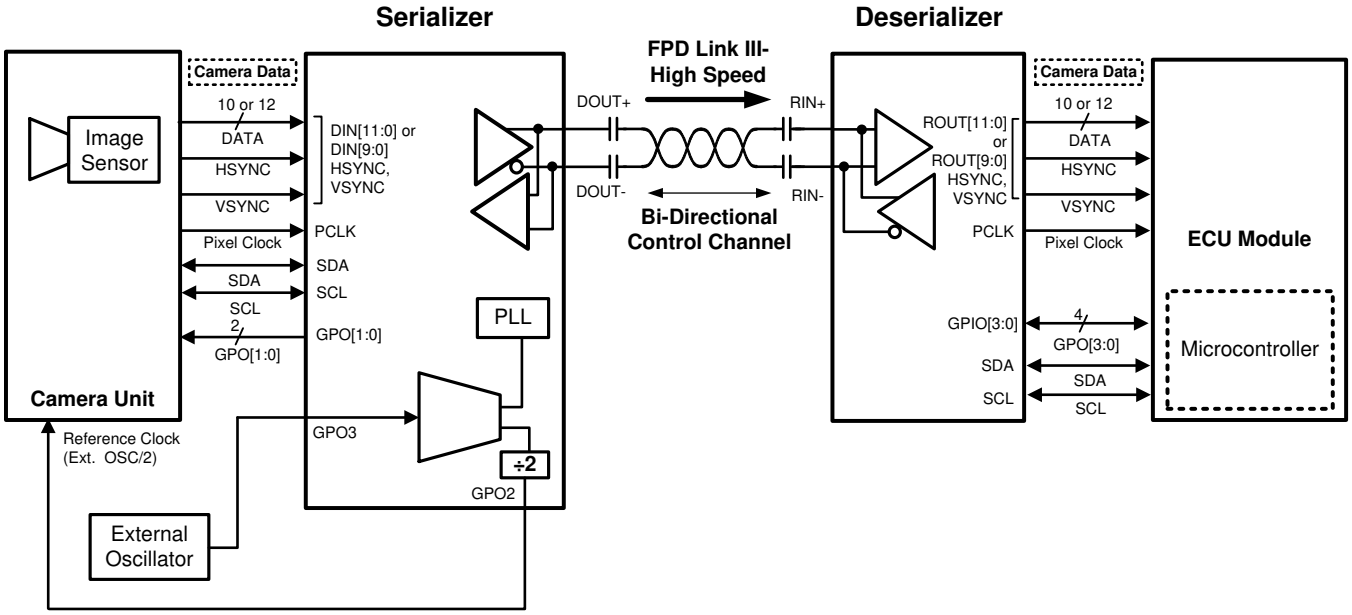


Figure 16. DS90UB913A-Q1/914A-Q1 Operation in the External Oscillator Mode

When the DS90UB913A-Q1 device is operated using an external oscillator, the GPO3 pin on the DS90UB913A-Q1 is the input pin for the external oscillator. In applications where the DS90UB913A-Q1 device is operated from an external oscillator, the divide-by-2 circuit in the DS90UB913A-Q1 device feeds back the divided clock output to the imager device through GPO2 pin. The pixel clock to external oscillator ratios needs to be fixed for the 12–bit high frequency mode and the 10–bit mode. **In the 10-bit mode, the pixel clock frequency divided by the external oscillator frequency must be 2. In the 12-bit high frequency mode, the pixel clock frequency divided by the external oscillator frequency must be 1.5.** For example, if the external oscillator frequency is 48 MHz in the 10–bit mode, the pixel clock frequency of the imager needs to be twice of the external oscillator frequency, that is, 96 MHz. If the external oscillator frequency is 48MHz in the 12-bit high frequency mode, the pixel clock frequency of the imager needs to be 1.5 times of the external oscillator frequency, that is, 72 MHz.

When PCLK signal edge is detected, and 0x03[1] = 0, the DS90UB913A will switch from internal oscillator mode to an external PCLK. Upon removal of PCLK input, the device will switch back into internal oscillator mode. In external oscillator mode, GPO2 and GPO3 on the Serializer cannot act as the output of the input signal coming from GPIO2 or GPIO3 on the Deserializer.

Table 1. Device Functional Mode w/ Example XCLKIN = 48 MHz

MODE	GPIO3 XCLKIN	GPIO2 XCLKOUT = XCLKIN / 2	Ratio	Input PCLK Frequency = XLCKIN * Ratio
10-bit	48 MHz	24 MHz	2	96 MHz
12-bit High Frequency (HF)	48 MHz	24 MHz	1.5	72 MHz
12-bit Low Frequency (LF)	48 MHz	24 MHz	1	48 MHz

8.4.2 DS90UB913A/914A Operation with Pixel Clock from Imager as Reference Clock

The DS90UB913A/914A chipsets can be operated by using the pixel clock from the imager as the reference clock. Figure 17 shows the operation of the DS90UB913A/914A chipsets using the pixel clock from the imager. If the DS90UB913A-Q1 device is operated using the pixel clock from the imager as the reference clock, then the imager uses an external oscillator as its reference clock. There are 4 GPIOs available in this mode (PCLK from imager mode).

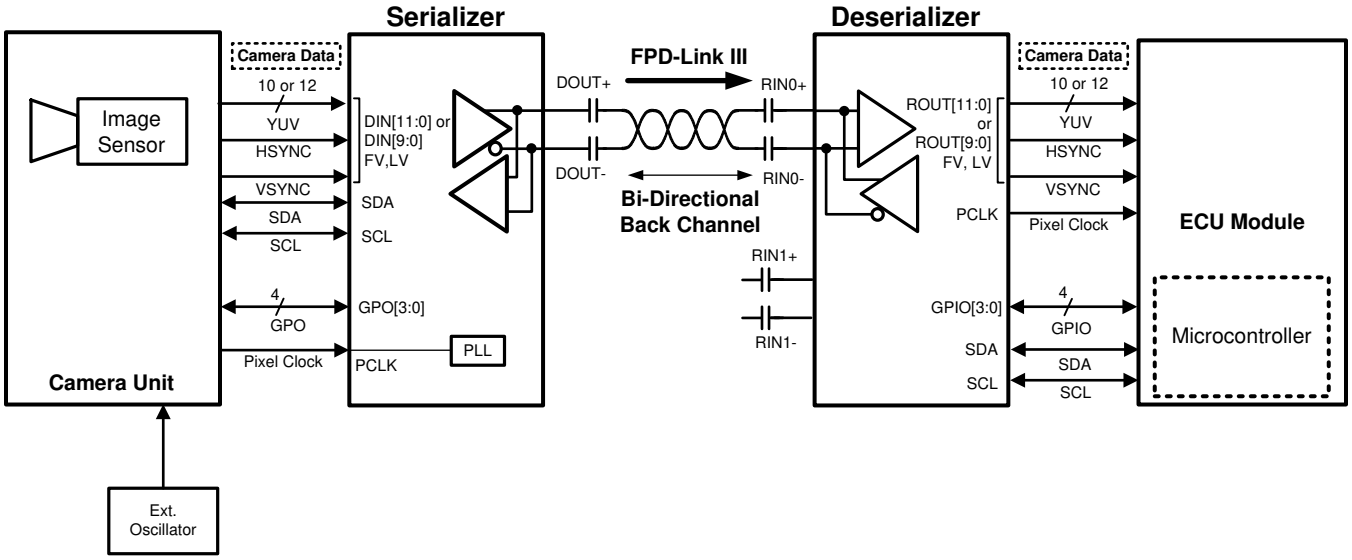


Figure 17. DS90UB913A-Q1/914A-Q1 Operation in PCLK mode

8.4.3 MODE Pin on Serializer

The MODE pin on the Serializer can be configured to select if the DS90UB913A-Q1 device is to be operated from the external oscillator or the PCLK from the imager. The pin must be pulled to V_{DD_n}(1.8 V, not V_{DDIO}) with a resistor R1 and a pulldown resistor R2 for external oscillator mode to create the ratio shown in Figure 18. If the device is to be operated from PCLK from imager mode, MODE pin can be pulled up to V_{DD_n} (1.8V) with a 10-kΩ resistor directly or use the ratio shown in Figure 18 and Table 2. The recommended maximum resistor tolerance is 1%.

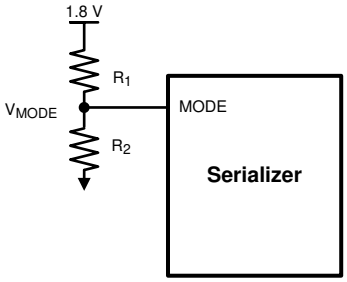


Figure 18. MODE Pin Configuration on DS90UB913A-Q1

Table 2. DS90UB913A-Q1 Serializer MODE Setting

MODE SELECT	MINIMUM RATIO ($V_{MODE}/V_{(VDD\_n)}$)	MAXIMUM RATIO ($V_{MODE}/V_{(VDD\_n)}$)	SUGGESTED R_1 RESISTOR VALUE (kΩ)	SUGGESTED R_2 RESISTOR VALUE (kΩ)
PCLK from Imager mode	0.750	1.000	10	100
External Oscillator mode	0.292	0.339	10	4.7

8.4.4 Internal Oscillator

When a PCLK is not applied to the DS90UB913A, the serializer will establish the FPD-III link using an internal oscillator. During normal operation (not BIST) the frequency of the internal oscillator can be adjusted from DS90UB913A register 0x14[2:1] according to Table 3. In BIST mode, the internal oscillator frequency should only be adjusted from the DS90UB914A. The BIST frequency can be set by either pin strapping (Table 4) or register (Table 5). In BIST DS90UB913A register 0x14[2:1] is automatically loaded from the DS90UB914A through the bi-directional control channel.

Table 3. Clock Sources for Forward Channel Frame on the Serializer During Normal Operation

DS90UB913A-Q1 Reg 0x14 [2:1]	10–BIT MODE	12–BIT HIGH-FREQUENCY MODE	12–BIT LOW-FREQUENCY MODE
00	50 MHz	37.5 MHz	25 MHz
01	100 MHz	75 MHz	50 MHz
10	50 MHz	37.5 MHz	25 MHz
11	Reserved	Reserved	Reserved

8.4.5 Built In Self Test

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link and low-speed back channel. This is useful in the prototype stage, equipment production, and in-system test and also for system diagnostics.

8.4.6 BIST Configuration and Status

The chipset can be programmed into BIST mode using either pins or registers on the DES only. By default, BIST configuration is controlled through pins. BIST can be configured via registers using BIST Control register (0x24). Pin-based configuration is defined as follows:

- BISTEN = HIGH: Enable the BIST mode, BISTEN = LOW: Disable the BIST mode.
- Deserializer GPIO0 and GPIO1: Defines the BIST clock source (PCLK vs. various frequencies of internal OSC)

Table 4. BIST Pin Configuration

DESERIALIZER GPIO[0:1]	OSCILLATOR SOURCE	BIST FREQUENCY
00	External PCLK	PCLK or External Oscillator
01	Internal	~50 MHz
10	Internal	~25 MHz

Table 5. BIST Register Configuration

DS90UB914A-Q1 Reg 0x24 [2:1]	10–BIT MODE	12–BIT HIGH-FREQUENCY MODE	12–BIT LOW-FREQUENCY MODE
00	PCLK	PCLK	PCLK
01	100 MHz	75 MHz	50 MHz
10	50 MHz	37.5 MHz	25 MHz
11	Reserved	Reserved	Reserved

BIST mode provides various options for the PCLK source. Either external pins (GPIO0 and GPIO1) or registers can be used to program the BIST to use external PCLK or various OSC frequencies. Refer to Table 4 for pin settings. The BIST status can be monitored real-time on the PASS pin. For every frame with error(s), the PASS pin toggles low for one-half PCLK period. If two consecutive frames have errors, PASS will toggle twice to allow counting of frames with errors. Once the BIST is done, the PASS pin reflects the pass/fail status of the last BIST run only for one PCLK cycle. The status can also be read through I2C for the number of frames in errors. BIST status register retains results until it is reset by a new BIST session or a device reset. To evaluate BIST in external oscillator mode, both the external oscillator and PCLK need to be present. For all practical purposes, the BIST status can be monitored from the BIST Error Count register 0x25 on the DS90UB914A Deserializer.

8.4.7 Sample BIST Sequence

Step 1. For the DS90UB913A/914A FPD-Link III chipset, BIST Mode is enabled via the BISTEN pin of DS90UB914A-Q1 FPD-Link III deserializer. The desired clock source is selected through the deserializer GPIO0 and GPIO1 pins as shown in Table 4.

Step 2. The DS90UB913A-Q1 Serializer BIST pattern is enabled through the back channel. The BIST pattern is sent through the FPD-Link III to the deserializer. Once the serializer and deserializer are in the BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking FPD-Link III serial stream. If an error in the payload is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3. To stop the BIST mode, the deserializer BISTEN pin is set LOW. The deserializer stops checking the data. The final test result is not maintained on the PASS pin. To monitor the BIST status, check the BIST Error Count register, 0x25 on the Deserializer.

Step 4. The link returns to normal operation after the deserializer BISTEN pin is low. Figure 20 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, or by reducing signal condition enhancements (Rx equalization).

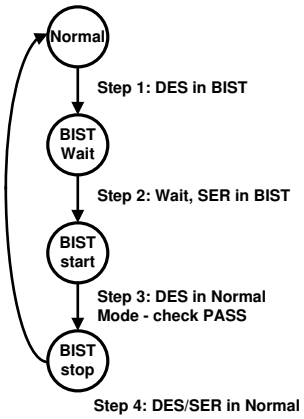


Figure 19. AT-Speed BIST System Flow Diagram

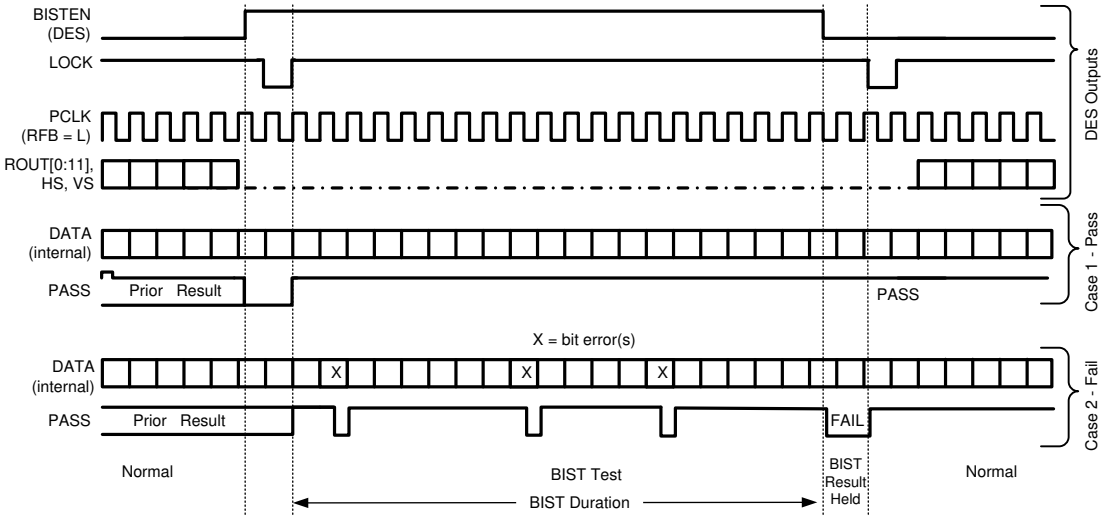


Figure 20. BIST Timing Diagram

8.5 Programming

8.5.1 Programmable Controller

An integrated I2C slave controller is embedded in the DS90UB913A-Q1 Serializer. It must be used to configure the extra features embedded within the programmable registers or it can be used to control the set of programmable GPIOs.

8.5.2 Description of Bidirectional Control Bus and I2C Modes

The I2C-compatible interface allows programming of the DS90UB913A-Q1, DS90UB914A-Q1, or an external remote device (such as image sensor) through the bidirectional control channel. Register programming transactions to/from the DS90UB913A-Q1/914A-Q1 chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and both lines must be pulled-up to V_{DDIO} by an external resistor. Pullup resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic LOW is transmitted by driving the output low. Logic HIGH is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pullup resistor values will depend upon the total bus capacitance and operating speed. The DS90UB913A I2C bus data rate supports up to 400 kbps according to I2C fast mode specifications.

For further description of general I2C communication, please refer to application note *Understanding the I2C Bus* (SLVA704). For more information on choosing appropriate pullup resistor values, please refer to application note *I2C Bus Pullup Resistor Calculation* (SLVA689).

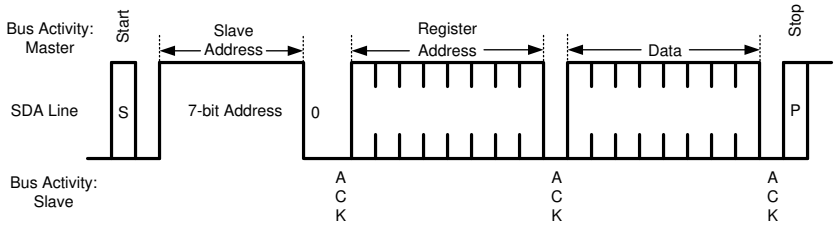


Figure 21. Write Byte

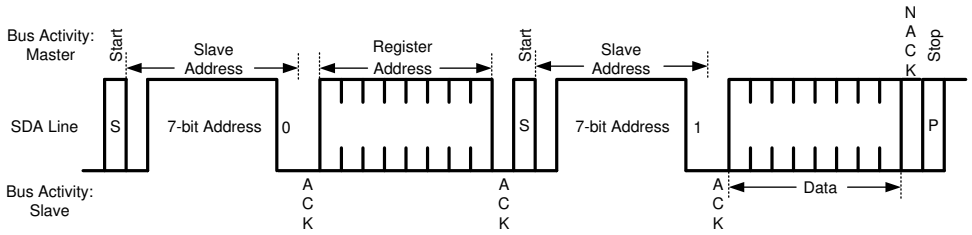


Figure 22. Read Byte

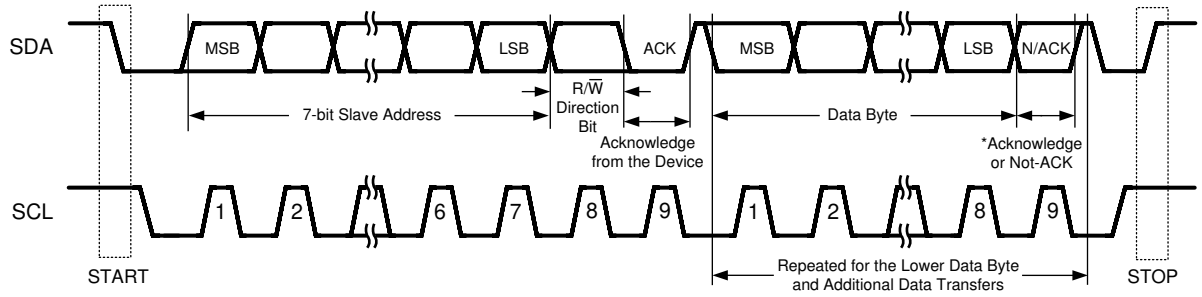


Figure 23. Basic Operation

Programming (continued)

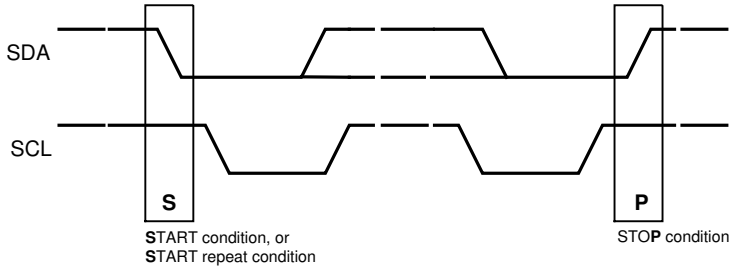


Figure 24. Start and Stop Conditions

8.5.3 I2C Pass-Through

I2C pass-through provides a way to access remote devices at the other end of the FPD-Link III interface. This option is used to determine if an I2C instruction is transferred over to the remote I2C bus. For example, when the I2C master is connected to the deserializer and I2C pass-through is enabled on the deserializer, any I2C traffic targeted for the remote serializer or remote slave will be allowed to pass through the deserializer to reach those respective devices.

See Figure 25 for an example of this function and refer to application note *I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel* (SNLA222).

If master controller transmits I2C transaction for address 0xA0, the DES A with I2C pass-through enabled will transfer I2C commands to remote Camera A. The DES B with I2C pass-through disabled, any I2C commands will NOT be passed on the I2C bus to Camera B.

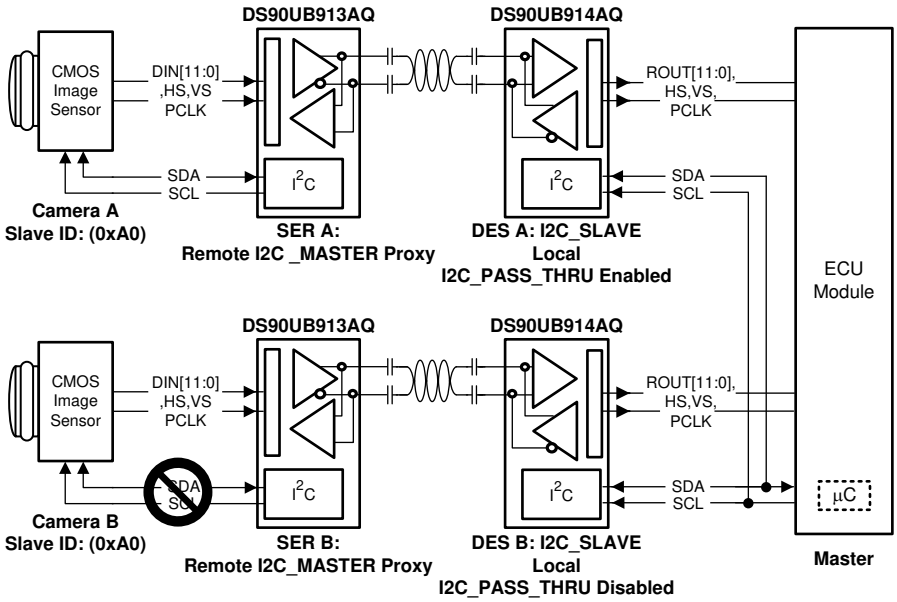


Figure 25. I2C Pass-Through

Programming (continued)

8.5.4 Slave Clock Stretching

The I2C-compatible interface allows programming of the DS90UB913A-Q1, DS90UB914A-Q1, or an external remote device (such as image sensor) through the bidirectional control. To communicate and synchronize with remote devices on the I2C bus through the bidirectional control channel/MCU, **the chipset utilizes bus clock stretching (holding the SCL line low) during data transmission**; where the I2C slave pulls the SCL line low on the 9th clock of every I2C transfer (before the ACK signal). The slave device will not control the clock and only stretches it until the remote peripheral has responded. The I2C master must support clock stretching to operate with the DS90UB913A/914A chipset.

8.5.5 ID[x] Address Decoder on the Serializer

The ID[x] pin on the Serializer is used to decode and set the physical slave address of the Serializer (I2C only) to allow up to five devices on the bus connected to the Serializer using only a single pin. The pin sets one of the 6 possible addresses for each Serializer device. The pin must be pulled to V_{DD_n} (1.8 V, not V_{DDIO}) with a 10-kΩ resistor and a pull-down resistor (R_{ID}) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 1%.

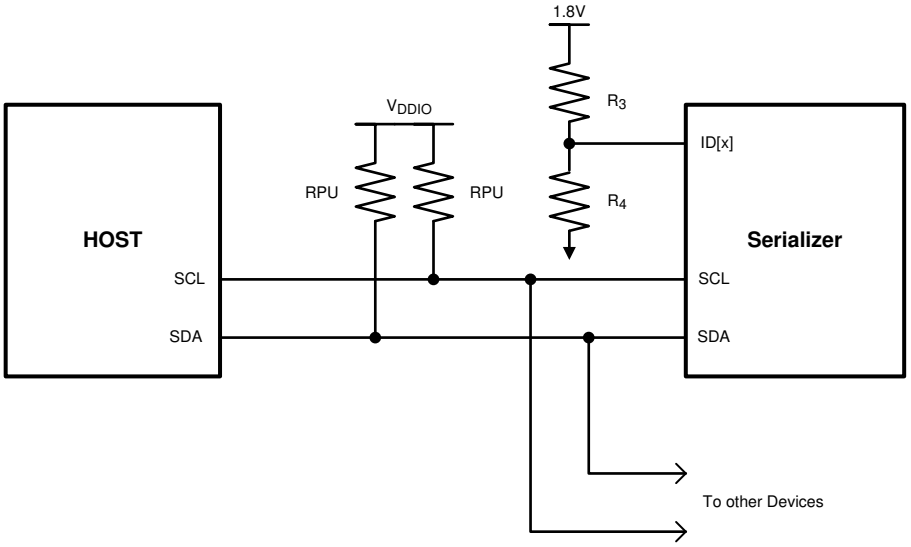


Figure 26. ID[x] Address Decoder on the Serializer

Table 6. IDX Setting for DS90UB913A-Q1 Serializer

IDX Setting — DS90UB913A-Q1 SERIALIZER					
MINIMUM RATIO ($V_{IDX}/V_{(VDD\_n)}$)	MAXIMUM RATIO ($V_{IDX}/V_{(VDD\_n)}$)	SUGGESTED R_3 RESISTOR VALUE (kΩ)	SUGGESTED R_4 RESISTOR VALUE (kΩ)	Address 7-bit	Address 8-bit 0 appended (WRITE)
0	0	Open	0	0x58	0xB0
0.114	0.186	10	2	0x59	0xB2
0.297	0.347	10	4.7	0x5A	0xB4
0.436	0.464	10	8.2	0x5B	0xB6
0.564	0.608	10	14	0x5C	0xB8
0.742	1.0	10	100	0x5D	0xBA

8.5.6 Multiple Device Addressing

Some applications require multiple camera devices with the same fixed address to be accessed on the same I2C bus. The DS90UB913A provides slave ID matching/aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming of the Slave alias register on Deserializer. This will remap the Slave alias address to the target SLAVE_ID address; up to 8 ID Alias's are supported in sensor mode when slaves are attached to the DS90UB913A serializer. In display mode, when the external slaves are at the deserializer the DS90UB913A supports one ID Alias. The ECU Controller must keep track of the list of I2C peripherals in order to properly address the target device.

See Figure 27 for an example of this function.

- ECU is the I2C master and has an I2C master interface
- The I2C interfaces in DES A and DES B are both slave interfaces
- The I2C protocol is bridged from DES A to SER A and from DES B to SER B
- The I2C interfaces in SER A and SER B are both master interfaces

If master controller transmits I2C slave 0xA0, DES A (address 0xC0), with pass through enabled, will forward the transaction to remote Camera A. If the controller transmits slave address 0xA4, the DES B 0xC2 will recognize that 0xA4 is mapped to 0xA0 and will be transmitted to the remote Camera B. If controller sends command to address 0xA6, the DES B (address 0xC2), with pass through enabled, will forward the transaction to slave device 0xA2.

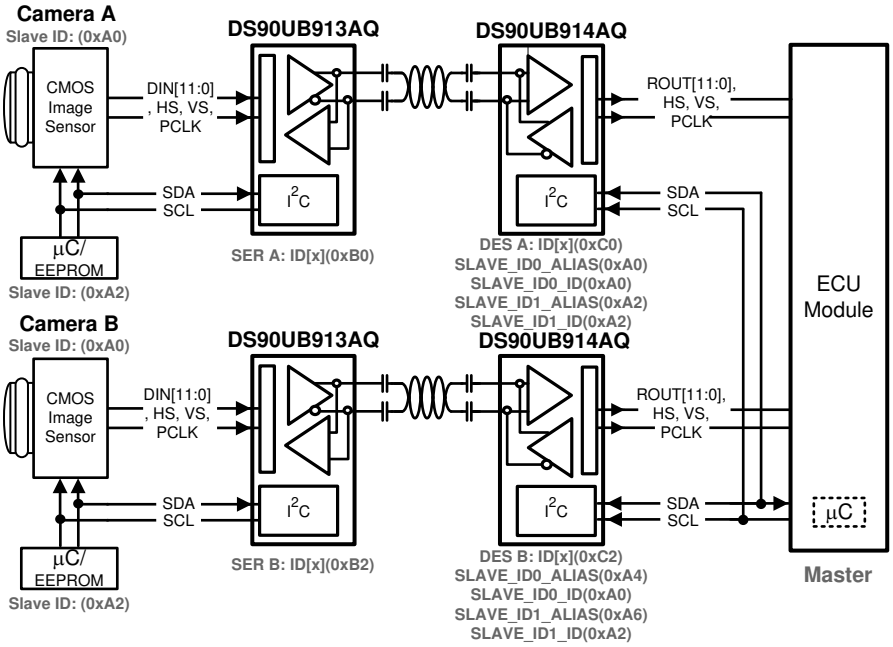


Figure 27. Multiple Device Addressing

8.6 Register Maps

In the register definitions under the *TYPE* and *DEFAULT* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access
- R/RC = Read only access, Read to Clear
- (R/W)/SC = Read / Write access, Self-Clearing bit
- (R/W)/S = Read / Write access, Set based on strap pin configuration at startup
- LL = Latched Low and held until read
- LH = Latched High and held until read
- S = Set based on strap pin configuration at startup

Table 7. DS90UB913A-Q1 Control Registers(1)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x00	I2C Device ID	7:1	DEVICE ID	R/W	0xB0'h (1011_0000'b)	7-bit address of Serializer (0x58'h default). This field does not auto update IDX strapped address.
		0	Serializer ID SEL			0: Device ID is from ID[x]. 1: Register I2C Device ID overrides ID[x].
0x01	Power and Reset	7	RSVD	R/W	0	Reserved.
		6	RDS	R/W	0	Digital Output Drive Strength. 1: High Drive Strength. 0: Low Drive Strength.
		5	V_{DDIO} Control	R/W	1	Auto Voltage Control. 1: Enable. 0: Disable.
		4	V_{DDIO} MODE	R/W	1	V_{DDIO} Voltage set. 1: V_{DDIO} = 3.3 V. 0: V_{DDIO} = 1.8 V.
		3	ANAPWDN	R/W	0	This register can be set only through local I2C access. 1: Analog power down. Powers down the analog block in the Serializer. 0: No effect.
		2	RSVD	R/W	0	Reserved.
		1	DIGITAL RESET1	R/W	0	1: Resets the digital block except for register values. Does not affect device I2C Bus or Device ID. This bit is self-clearing. 0: Normal Operation.
		0	DIGITAL RESET0	R/W	0	1: Digital Reset, resets the entire digital block including all register values. This bit is self-clearing. 0: Normal Operation.
0x02	**Reserved**					

(1) **To ensure optimum device functionality, It is recommended to NOT write to any RESERVED registers.**

Register Maps (continued)

Table 7. DS90UB913A-Q1 Control Registers(1) (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x03	General Configuration	7	RX CRC Checker Enable	R/W	1	Back-channel CRC checker enable 1: Enable 0: Disable
		6	TX Parity Generator Enable	R/W	1	Forward channel parity generator enable. 1: Enable 0: Disable
		5	CRC Error Reset	R/W	0	Clear CRC error counters This bit is NOT self-clearing. 1: Clear counters 0: Normal operation
		4	I2C Remote Write Auto Acknowledge	R/W	0	Automatically acknowledge I2C remote write The mode works when the system is LOCKed. 1: Enable: When enabled, I2C writes to the deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the deserializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. 0: Disable
		3	I2C Pass-Through All	R/W	0	1: Enable Forward Control Channel pass-through of all I2C accesses to I2C IDs that *do not match* the serializer I2C ID. *The I2C accesses are then remapped to address specified in register 0x06.* 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C IDs *matching* either the remote deserializer ID or the remote I2C IDs.
		2	I2C Pass-Through	R/W	1	I2C Pass-through mode 1: Pass-through enabled. DES alias 0x07 and slave alias 0x09 0: Pass-through disabled
		1	OV_CLK2PLL	R/W	0	1:Enabled : When enabled this register overrides the clock to PLL mode (External Oscillator mode or Direct PCLK mode) defined through MODE pin and allows selection through register 0x35 in the serializer. 0: Disabled : When disabled, Clock to PLL mode (External Oscillator mode or Direct PCLK mode) is defined through MODE pin on the Serializer.
		0	TRFB	R/W	1	Pixel clock edge select 1: Parallel interface data is strobed on the rising clock edge 0: Parallel interface data is strobed on the falling clock edge
0x04	**Reserved.**					

Register Maps (continued)

Table 7. DS90UB913A-Q1 Control Registers(1) (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x05	Mode Select	7	RSVD	R/W	0	Reserved.
		6	RSVD	R/W	0	Reserved.
		5	MODE_ OVERRIDE	R/W	0	Allows overriding mode select bits coming from back-channel. 1: Overrides MODE select bits. 0: Does not override MODE select bits.
		4	MODE_UP_ TO_DATE	R	0	1: Status of mode select from Deserializer is up-to-date. 0: Status is NOT up-to-date.
		3	Pin_MODE_ 12–bit High Frequency	R	0	1: 12-bit high frequency mode is selected. 0: 12-bit high frequency mode is not selected.
		2	Pin_MODE_ 10–bit mode	R	0	1: 10-bit mode is selected. 0: 10-bit mode is not selected.
		1	TX_MODE_12b	R/W	0	Selects 12 bit data-bus. This bit changes the Tx mode settings if MODE_OVERRIDE is SET 0x05[5] = 1. 1: Enables 12 bit HF mode 0: Disables 12 bit HF mode Note: This bit changes mode settings on TX. When TX_MODE_12b is set TX_MODE_10b must be cleared; 0x05[1:0] = 10.
		0	TX_MODE_10b	R/W	0	Selects 10 bit data-bus. This bit changes the Tx mode settings if MODE_OVERRIDE is SET 0x05[5] = 1. 1: Enables 10b mode 0: Disables 10b mode Note: This bit changes mode settings on TX. When TX_MODE_10b is set TX_MODE_12b must be cleared; 0x05[1:0] = 01.
0x06	DES ID	7:1	Deserializer Device ID	R/W	0x00'h	7-bit **Deserializer** Device ID Configures the I2C Slave ID of the remote **Deserializer**. A value of 0 in this field disables I2C access to the remote **Deserializer**. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
		0	Freeze Device ID	R/W	0	1: Prevents auto-loading of the **Deserializer** Device ID by the bidirectional control channel. The ID will be frozen at the value written. 0: Update.
0x07	DES Alias	7:1	Deserializer ALIAS ID	R/W	0x00	7-bit remote *deserializer* device alias ID Configures the decoder for detecting transactions designated for an I2C *deserializer* device. The transaction is remapped to the address specified in the DES ID register. A value of 0 in this field disables access to the remote *deserializer.*
		0	RSVD	R/W	0	Reserved
0x08	SlaveID	7:1	SLAVE ID	R/W	0x00'h	7-bit Remote Slave Device ID Configures the physical I2C address of the remote I2C Slave device attached to the remote **Deserializer**. If an I2C transaction is addressed to the Slave Alias ID, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the **Deserializer** and then to remote slave. A value of 0 in this field disables access to the remote I2C slave.
		0	RSVD	R/W	0	Reserved.

Register Maps (continued)

Table 7. DS90UB913A-Q1 Control Registers(1) (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x09	Slave Alias	7:1	SLAVE ALIAS ID	R/W	0x00'h	7-bit Remote Slave Device Alias ID Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote **Deserializer**. The transaction will be remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I2C Slave.
		0	RSVD	R/W	0	Reserved.
0x0A	CRC Errors	7:0	CRC Error Byte 0	R	0x00'h	Number of back-channel CRC errors during normal operation. Least Significant byte.
0x0B	CRC Errors	7:0	CRC Error Byte 1	R	0x00'h	Number of back-channel CRC errors during normal operation. Most Significant byte.
0x0C	General Status	7:5	Rev-ID	R	0x0'h	Revision ID. 0x0: Production Revision ID.
		4	RX Lock Detect	R	0	1: RX LOCKED. 0: RX not LOCKED.
		3	BIST CRC Error Status	R	0	1: CRC errors in BIST mode. 0: No CRC errors in BIST mode.
		2	PCLK Detect	R	0	1: Valid PCLK detected. 0: Valid PCLK not detected.
		1	DES Error	R	0	1: CRC error is detected during communication with Deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x03[5]. 0: No effect.
		0	LINK Detect	R	0	1: Cable link detected. 0: Cable link not detected. This includes any of the following faults: — Cable Open. — '+' and '-' shorted. — Short to GND. — Short to battery.
0x0D	GPO[0] and GPO[1] Configuration	7	GPO1 Output Value	R/W	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO1 Remote Enable	R/W	1	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		5	RSVD	R/W	0	Reserved.
		4	GPO1 Enable	R/W	1	1: GPIO enable. 0: Tri-state.
		3	GPO0 Output Value	R/W	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO0 Remote Enable	R/W	1	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		1	RSVD	R/W	0	Reserved.
		0	GPO0 Enable	R/W	1	1: GPIO enable. 0: Tri-state.

Register Maps (continued)

Table 7. DS90UB913A-Q1 Control Registers(1) (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x0E	GPO[2] and GPO[3] Configuration	7	GPO3 Output Value	R/W	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO3 Remote Enable	R/W	0	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		5	GPO3 Direction	R/W	1	1: Input. 0: Output.
		4	GPO3 Enable	R/W	1	1: GPIO enable. 0: Tri-state.
		3	GPO2 Output Value	R/W	0	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled. The local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO2 Remote Enable	R/W	1	Remote GPIO Control. 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		1	RSVD	R/W	0	Reserved.
		0	GPO2 Enable	R/W	1	1: GPIO enable. 0: Tri-state.
0x0F	I2C Master Config	7:5	RSVD	R	0x0'h	Reserved.
		4:3	SDA Output Delay	R/W	00	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00: ~350 ns 01: ~400 ns 10: ~450 ns 11: ~500 ns
		2	Local Write Disable	R/W	0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer.
		1	I2C Bus Timer Speed up	R/W	0	Speed up I2C Bus Watchdog Timer. 1: Watchdog Timer expires after approximately 50 microseconds. 0: Watchdog Timer expires after approximately 1 second.
		0	I2C Bus Timer Disable	R/W	0	1. Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL. 0: No effect.

Register Maps (continued)

Table 7. DS90UB913A-Q1 Control Registers(1) (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x10	I2C Control	7	RSVD	R/W	0	Reserved.
		6:4	SDA Hold Time	R/W	0x1'h	Internal SDA Hold Time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 ns.
		3:0	I2C Filter Depth	R/W	0x7'h	I2C Glitch Filter Depth. This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10 ns.
0x11	SCL High Time	7:0	SCL High Time	R/W	0x82'h	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4 µs + 1 µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x12	SCL LOW Time	7:0	SCL Low Time	R/W	0x82'h	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7 µs + 0.3 µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x13	General Purpose Control	7:0	GPCR[7:0]	R/W	0x00'h	1: High. 0: Low.
0x14	BIST Control	7:5	RSVD	R	0x0'h	Reserved.
		4:3	RSVD	R/W	0x0'h	Reserved.
		2:1	Clock Source	R/W	0x0'h	Allows choosing different OSC clock frequencies for forward channel frame. OSC Clock Frequency in Functional Mode when OSC mode is selected or when the selected clock source is not present, for example, missing PCLK/ External Oscillator. See Table 3 for oscillator clock frequencies when PCLK/ External Clock is missing.
		0	RSVD	R/W	0	Reserved.
0x15 - 0x1D	**Reserved.**					
0x1E	BCC Watchdog Control	7:1	BCC Watchdog Timer	R/W	0x7F'h (111_1111'b)	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	R/W	0	1: Disables BCC Watchdog Timer operation. 0: Enables BCC Watchdog Timer operation.
0x1F - 0x26	**Reserved**					
0x27	Analog Power Down Control	7:6	Reserved	R	0	Reserved
		5	Power Down PLL	RW	0	1: Power down forward channel PLL 0: Normal operation
		4:0	Reserved	RW	0	Reserved
0x28	**Reserved**					

Register Maps (continued)

Table 7. DS90UB913A-Q1 Control Registers(1) (continued)

Addr (Hex)	Name	Bits	Field	TYPE	Default	Description
0x29	OSC Divider	7:6	RSVD	R/W	0x0	Reserved
		5	OSC Divider	R/W	0	Selects the OSC frequency to drive out on GPO2 in external oscillator mode. 0: Divide by 2 (default) 1: Divide by 4
		4:0	RSVD	R/W	0x06	Reserved
0x2A	CRC Errors	7:0	BIST Mode CRC Errors Count	R	0x00'h	Number of CRC Errors in the back channel when in BIST mode.
0x2B - 0x2C	**Reserved.**					
0x2D	Inject Forward Channel Error	7	Force Forward Channel Error	R/W	0	1: Forces 1 (one) error over forward channel frame in normal operating mode. Self clearing bit. 0: No error.
		6:0	Force BIST Error	R/W	0x00'h	N: Forces N number of errors in BIST mode. This register MUST be set BEFORE BIST mode is enabled. BIST Error Count Register on the deserializer (i.e. 0x25 on 914A device) should be read AFTER BIST mode is disabled for the correct number of errors incurred while in BIST mode. 0: No error.
0x2E - 0x34	**Reserved.**					
0x35	PLL Clock Overwrite	7:4	RSVD	R/W	0x0'h	Reserved.
		3	PIN_LOCK to External Oscillator	R	0	Status of mode select pin. 1: Indicates External Oscillator mode is selected by mode-resistor. 0: External Oscillator mode is not selected by mode-resistor.
		2	RSVD	R	0	Reserved.
		1	LOCK to External Oscillator	R/W	0	Affects only when 0x03[1]=1 (OV_CLK2PLL) and 0x35[0]=0. 1: Routes GPO3 directly to PLL. 0: Allows PLL to lock to PCLK.
		0	LOCK2OSC	R/W	1	Affects only when 0x03[1]=1 (OV_CLK2PLL). 1: Allows internal OSC clock to feed into PLL. 0: Allows PLL to lock to either PCLK or external clock from GPO3.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90UB913A was designed as a serializer to support automotive camera designs. Automotive cameras are often located in remote positions such as bumpers or trunk lids, and a major component of the system cost is the wiring. For this reason it is desirable to minimize the wiring to the camera. This chipset allows the video data, along with a bidirectional control channel, and power to all be sent over a single coaxial cable. The chipset is also able to transmit over STP and is pin-to-pin/backwards compatible with the DS90UB913Q.

9.1.1 Power Over Coax

See application report *Sending Power over Coax in DS90UB913A Designs* for more details.

9.1.2 Power-Up Requirements and PDB Pin

Transition of the PDB pin from LOW to HIGH must occur after the V_{VDDIO} and V_{VDD_n} supplies have reached their required operating voltage levels. Direct control of the PDB timing by processor GPIO is recommended if possible. When direct control of PDB is not available, the PDB pin can be tied to the power supply rail with an RC filter network to help ensure proper power up timing. GPO2 should be low when PDB goes high. Timing constraints are noted in Figure 28 and Table 8. Please refer to *Power Down* for device operation when powered down.

If GPO2 state is not determined when PDB goes high, DS90UB913A registers must be programmed to configure the transmission mode. Mode Select register 0x05[5] must be set to 1 and register 0x05 bit 1 and 0 are to be selected based on desired 12-bit or 10-bit transmit data format.

Common applications will tie the V_{DDIO} and V_{DD_n} supplies to the same power source of 1.8 V typically. This is an acceptable method for ramping the V_{DDIO} and V_{DD_n} supplies. The main constraint here is that the V_{DD_n} supply does not lead in ramping before the V_{DDIO} system supply. This is noted in Figure 28 with the requirement of $t_1 \geq 0$. V_{DDIO} should reach the expected operating voltage earlier than V_{DD_n} or at the same time.

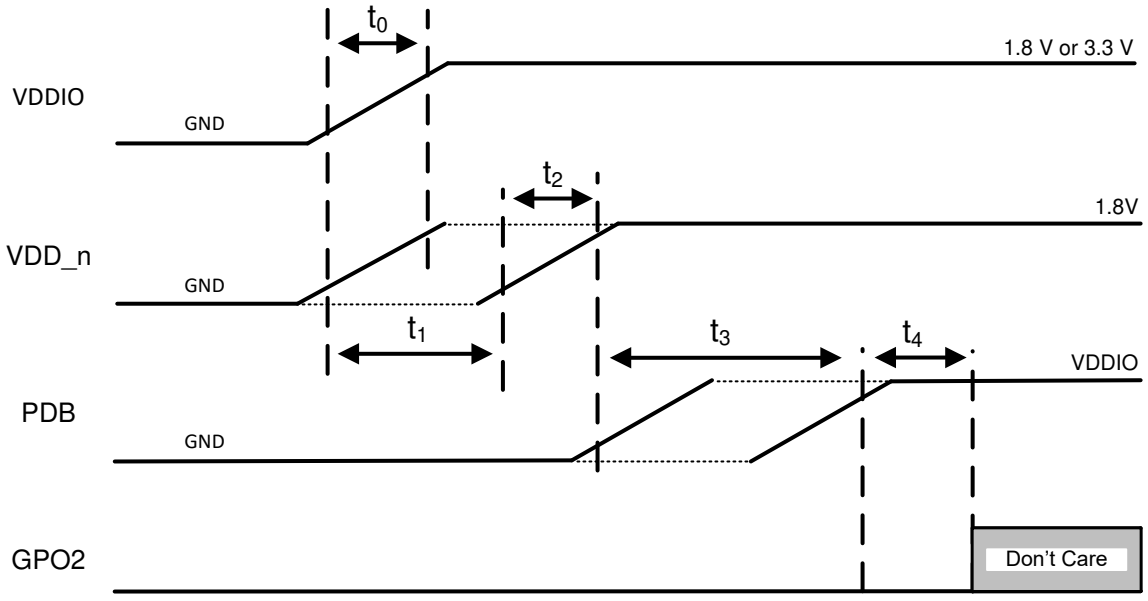


Figure 28. Suggested Power-Up Sequencing

Application Information (continued)

Table 8. Power-Up Sequencing Constraints for DS90UB913A-Q1

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	Units
t_0	$V_{(VDDIO)}$ rise time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required	0.05		5	ms
t_1	$V_{(VDDIO)}$ to $V_{(VDD\_n)}$ delay	10% of rising edge ($V_{(VDDIO)}$) to 10% of rising edge ($V_{(VDD\_n)}$)	0			ms
t_2	$V_{(VDD\_n)}$ rise time	10% to 90% of nominal voltage on rising edge. Monotonic signal ramp is required. V_{PDB} < 10% of $V_{(VDDIO)}$	0.05		5	ms
t_3*	$V_{(VDD\_n)}$ to V_{PDB} delay	90% rising edge ($V_{(VDD\_n)}$) to 90% rising edge (V_{PDB})	0		16	ms
t_4	PDB to GPO2 delay	90% of rising edge (PDB) to 10% of rising edge (GPO2)	1.3			ms

* If timing constraint t_3 can not be assured, the following programming steps should be issued to the 913A via local I2C control (not via remote back channel) >= 10ms after the power sequence is complete. This step will cause a brief restart of the forward channel output:

- Write Register 0x27 = 0x20
- Wait >= 20ms
- Write Register 0x27 = 0x00

9.1.3 AC Coupling

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in Figure 29. For applications utilizing single-ended 50-Ω coaxial cable, the unused data pin (DOUT–, RIN–) should utilize a 0.047-µF capacitor and should be terminated with a 50-Ω resistor. For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

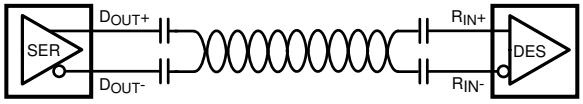


Figure 29. AC-Coupled Connection (STP)

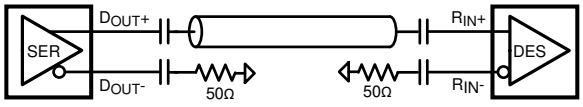


Figure 30. AC-Coupled Connection (Coaxial)

9.1.4 Transmission Media

The DS90UB913A/914A chipset is intended to be used in a point-to-point configuration through a shielded coaxial cable. The Serializer and Deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connectors) should have a differential impedance of 100 Ω, or a single-ended impedance of 50 Ω. The maximum length of cable that can be used is dependent on the quality of the cable (gauge, impedance), connector, board(discontinuities, power plane), the electrical environment (for example, power stability, ground noise, input clock jitter, PCLK frequency, etc). The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. A differential probe should be used to measure across the termination resistor at the CMLOUTP/N pins.

Please refer to *Cable Requirements for the DS90UB913A & DS90UB914A* or contact TI for a channel specification regarding cable loss parameters and further details on adaptive equalizer loss compensation.

9.2 Typical Applications

9.2.1 Coax Application

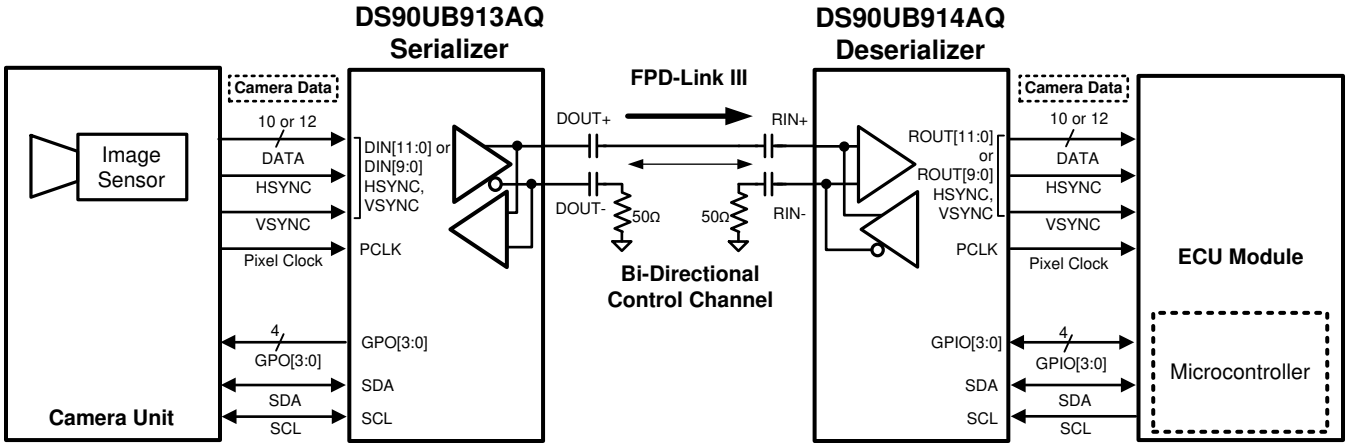


Figure 31. Coax Application Block Diagram

Typical Applications (continued)

9.2.1.1 Design Requirements

For the typical coax design applications, use the following as input parameters:

Table 9. Coax Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8 V, 2.8 V, or 3.3 V
V_{DD_n}	1.8 V
AC Coupling Capacitors for DOUT±	0.1 µF, 0.047 µF (For the unused data pin, DOUT–)
PCLK Frequency	50 MHz (12-bit low frequency), 75 MHz (12-bit high frequency), 100 MHz (10-bit)

9.2.1.2 Detailed Design Procedure

Figure 32 shows the typical connection of a DS90UB913A-Q1 Serializer using a **coax** interface.

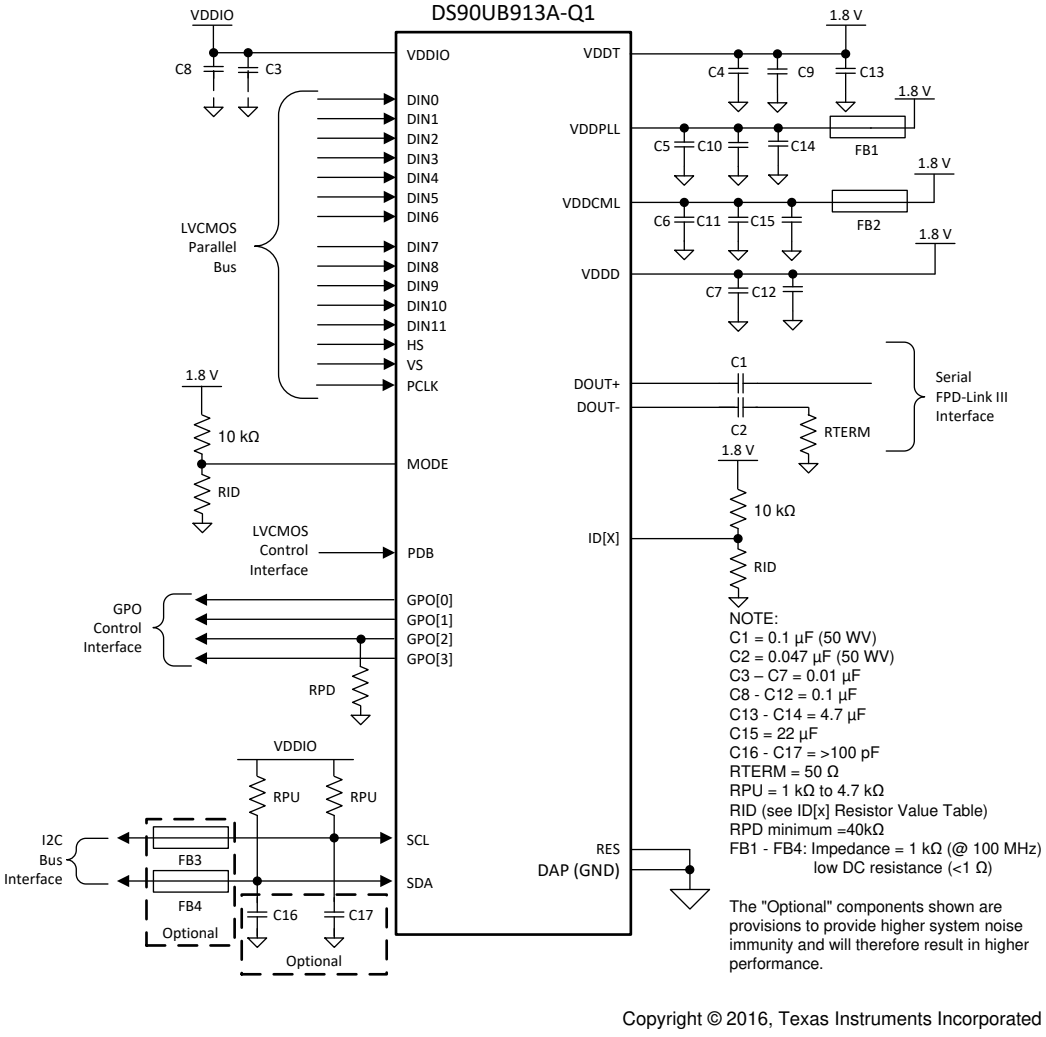


Figure 32. DS90UB913A-Q1 Typical Connection Diagram — Pin Control (Coax)

9.2.1.3 Application Curves

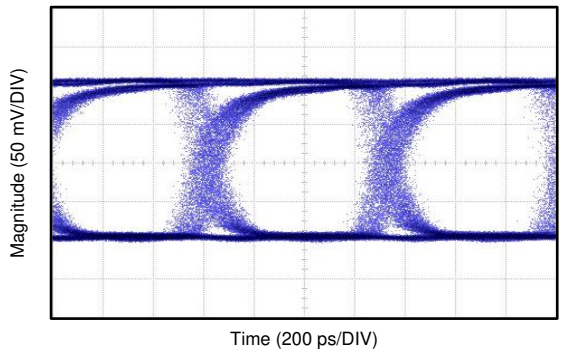


Figure 33. Coax Eye Diagram at 1.4-Gbps Line Rate (100-MHz Pixel Clock) from Deserializer CML Loop-through Output (CMLOUT±)

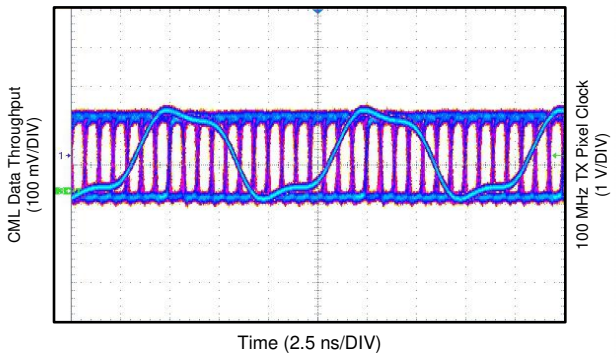


Figure 34. Coax Eye Diagram with 100-MHz TX Pixel Clock Overlay from Deserializer CML Loop-through Output (CMLOUT±)

9.2.2 STP Application

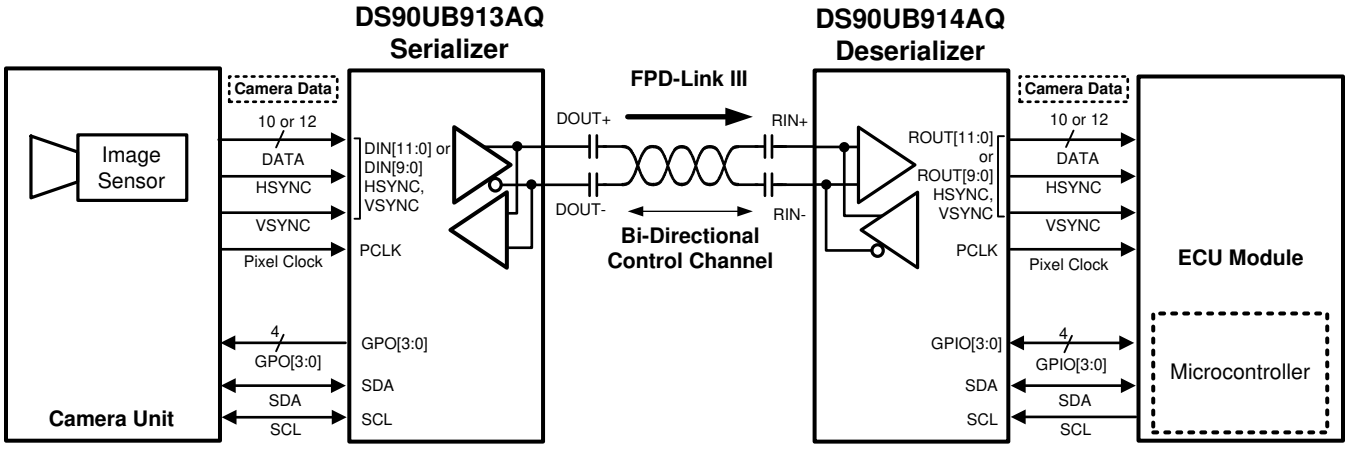


Figure 35. STP Application Block Diagram

9.2.2.1 Design Requirements

For the typical STP design applications, use the following as input parameters

Table 10. STP Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8 V, 2.8 V, or 3.3 V
V_{DD_n}	1.8 V
AC Coupling Capacitors for DOUT±	0.1 µF
PCLK Frequency	50 MHz (12-bit low frequency), 75 MHz (12-bit high frequency), 100 MHz (10-bit)

9.2.2.2 Detailed Design Procedure

Figure 36 shows a typical connection of a DS90UB913A-Q1 Serializer using an **STP** interface.

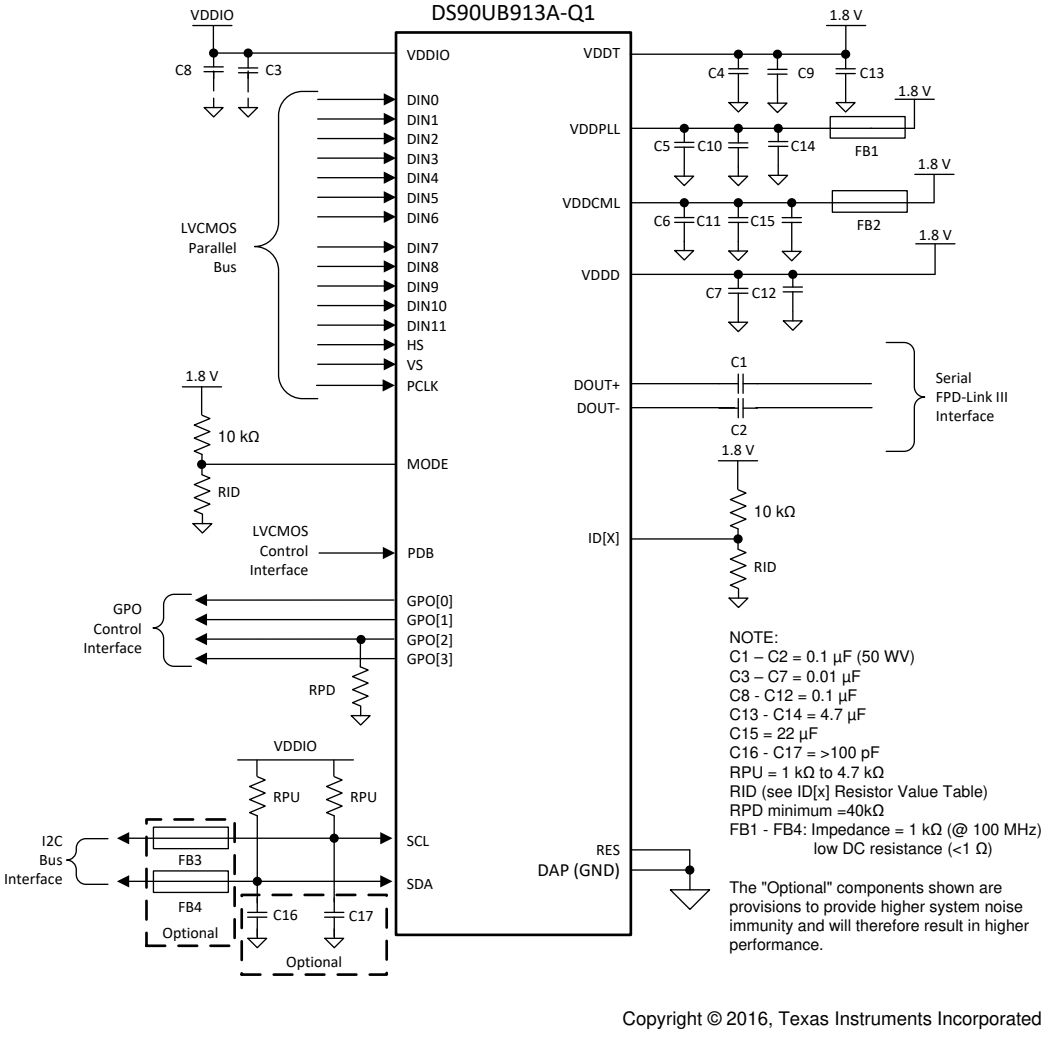


Figure 36. DS90UB913A-Q1 Typical Connection Diagram — Pin Control (STP)

9.2.2.3 Application Curves

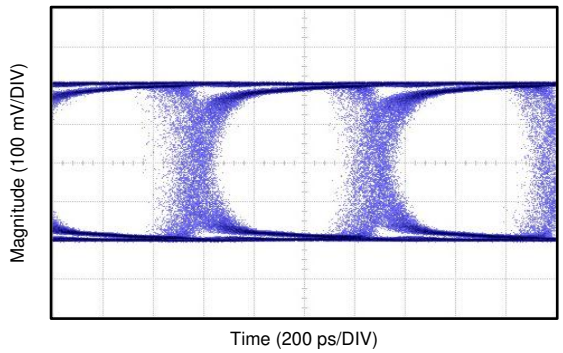


Figure 37. STP Eye Diagram at 1.4-Gbps Line Rate (100-MHz Pixel Clock) from Deserializer CML Loop-through Output (CMLOUT±)

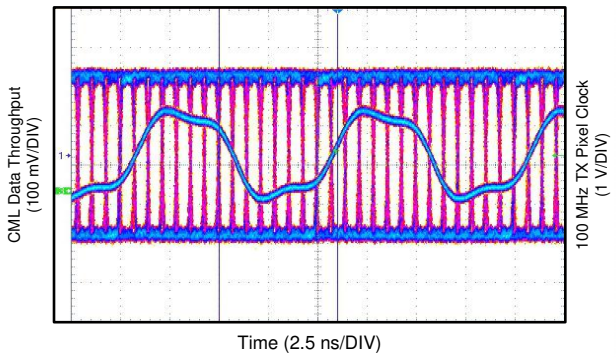


Figure 38. STP Eye Diagram with 100-MHz TX Pixel Clock Overlay from Deserializer CML Loop-through Output (CMLOUT±)

10 Power Supply Recommendations

This device is designed to operate from an input core voltage supply of 1.8 V. Some devices provide separate power and ground terminals for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Terminal description tables typically provide guidance on which circuit blocks are connected to which power terminal pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs. The voltage applied on V_{DDIO} (1.8 V, 2.8 V, 3.3 V) or other power supplies making up V_{DD_n} (1.8 V) should be at the input pin - any board level DC drop should be compensated (i.e. ferrite beads in the path of the power supply rails).

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in TI Application Note: *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

11.1.1 Interconnect Guidelines

See *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) for full details.

- Use 100 Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instrument web site at: www.ti.com/lvds.

11.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown below:

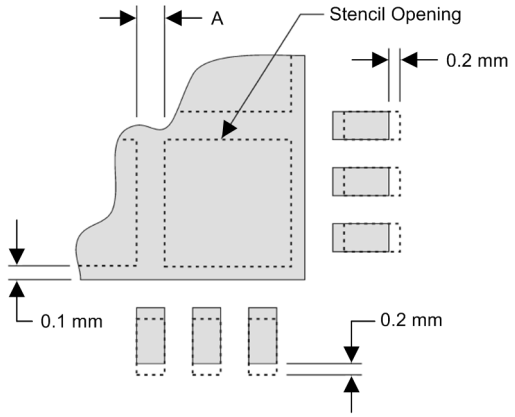


Figure 39. No Pullback WQFN, Single Row Reference Diagram

Table 11. No Pullback WQFN Stencil Aperture Summary for DS90UB913A-Q1

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE(mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS90UB913A-Q1	32	RTV	0.25 x 0.6	0.5	3.1 x 3.1	0.25 x 0.7	1.4 x 1.4	4	0.2

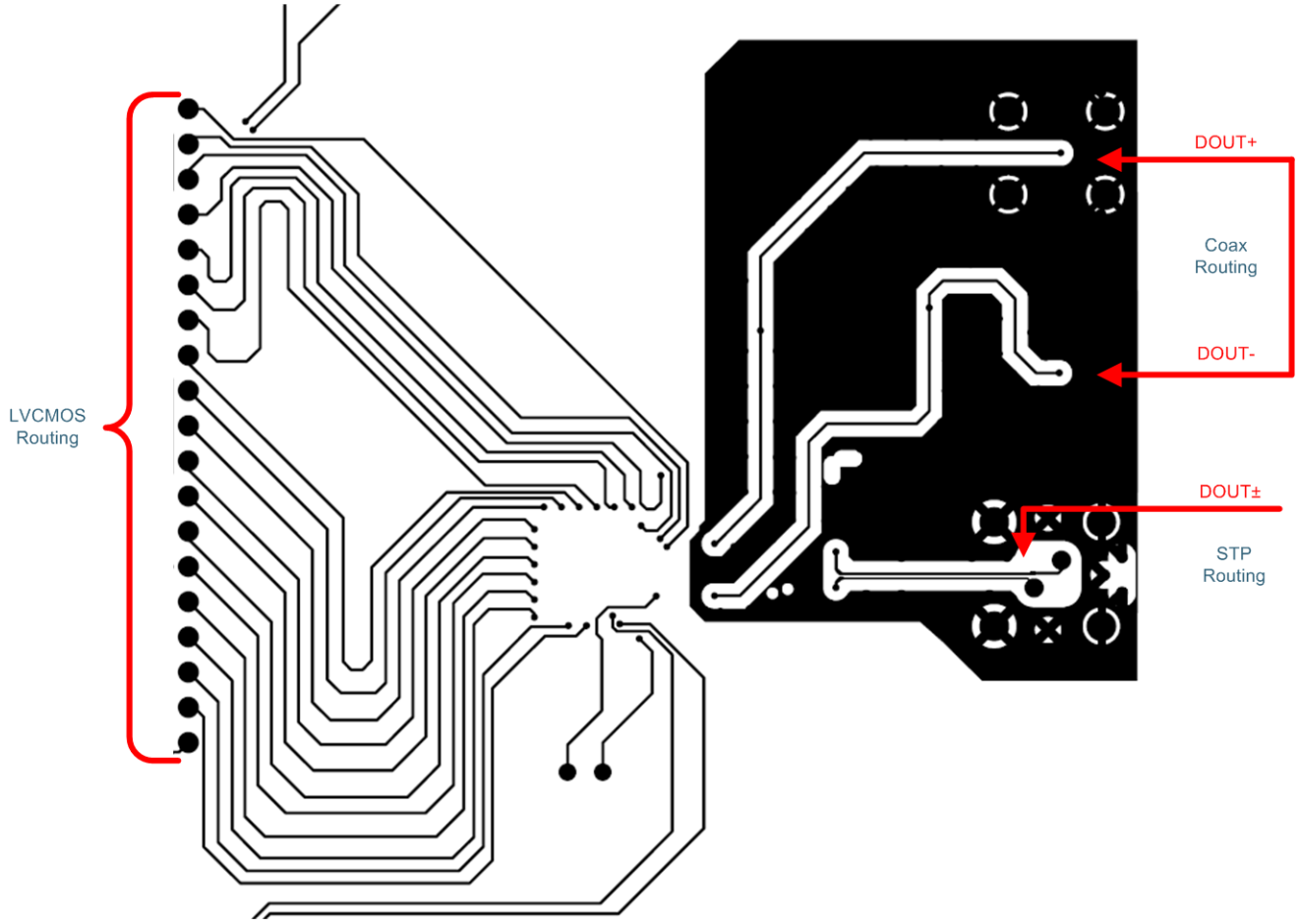


Figure 40. DS90UB913A-Q1 Serializer Example Layout

The following PCB layout examples are derived from the layout design of the DS90UB913A-Q1 Evaluation Module (DS90UB913A-CXEVM and DS90UB914A-CXEVM REV A User's Guide). These graphics and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in this Serializer.

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《DS90UB913A-CXEVM 和 DS90UB914A-CXEVM 修订版 A 用户指南》* (SNLU135)
- *《通过具有双向控制通道的 DS90UB913/4 FPD-Link III 进行 I2C 通信》* (SNLA222)
- *《在 DS90UB913A 设计中进行同轴电缆供电》* (SNOA549)
- *FPD-Link 学习中心*
- *《I2C 总线上拉电阻器计算》* (SLVA689)
- *《焊接规格应用报告》* (SNOA549)
- *《IC 封装热度量指标应用报告》* (SPRA953)
- *《无引线框架封装 (LLP) 应用报告》* (SNOA401)
- *《LVDS 用户手册》* (SNLA187)
- *《DS90UB913A 和 DS90UB914A 的电缆要求》* (SNLA229)
- *《一种适用于 FPD-Link III SerDes 的 EMC/EMI 系统设计和测试方法》* (SLYT719)
- *《按照车用 EMC/EMI 要求进行成功设计的 10 个技巧》* (SLYT636)

12.2 接收文档更新通知

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12.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商标

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12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB913ATRTVJQ1	ACTIVE	WQFN	RTV	32	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB913AQ	Samples
DS90UB913ATRTVRQ1	ACTIVE	WQFN	RTV	32	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB913AQ	Samples
DS90UB913ATRTVTQ1	ACTIVE	WQFN	RTV	32	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB913AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

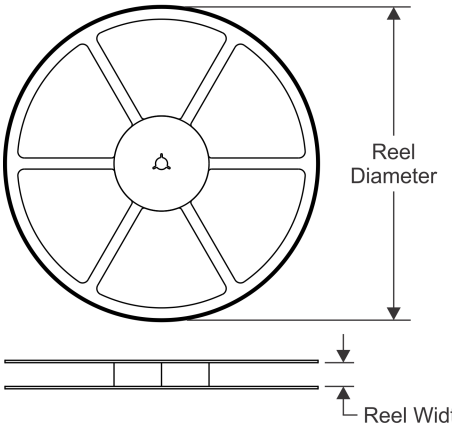
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

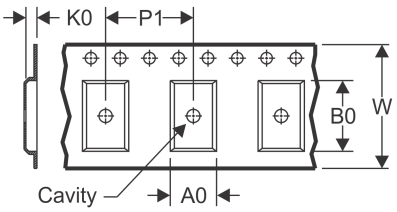
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

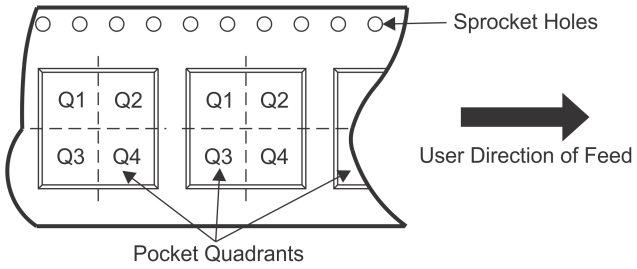


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

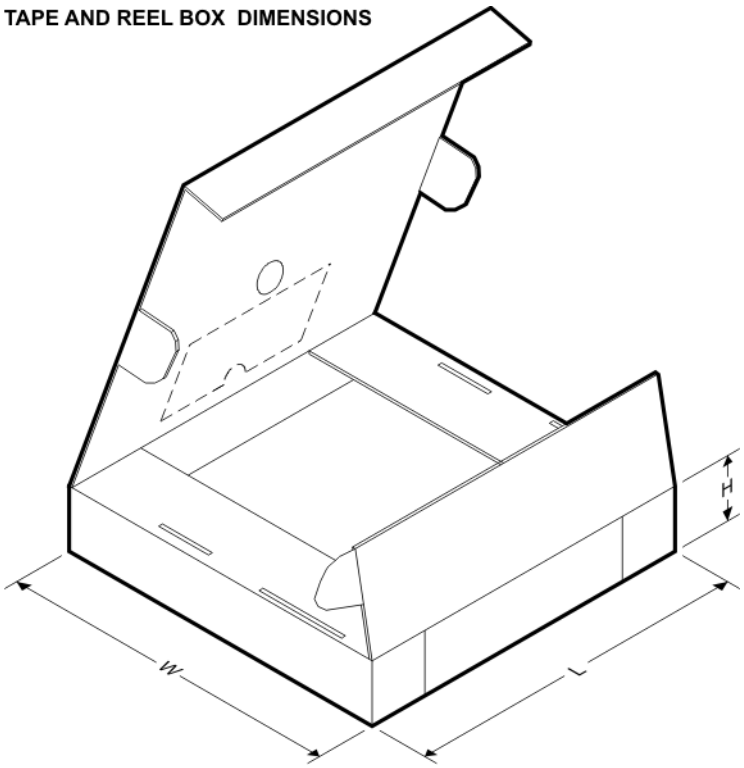
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB913ATRTVJQ1	WQFN	RTV	32	2500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90UB913ATRTVRQ1	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90UB913ATRTVTQ1	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

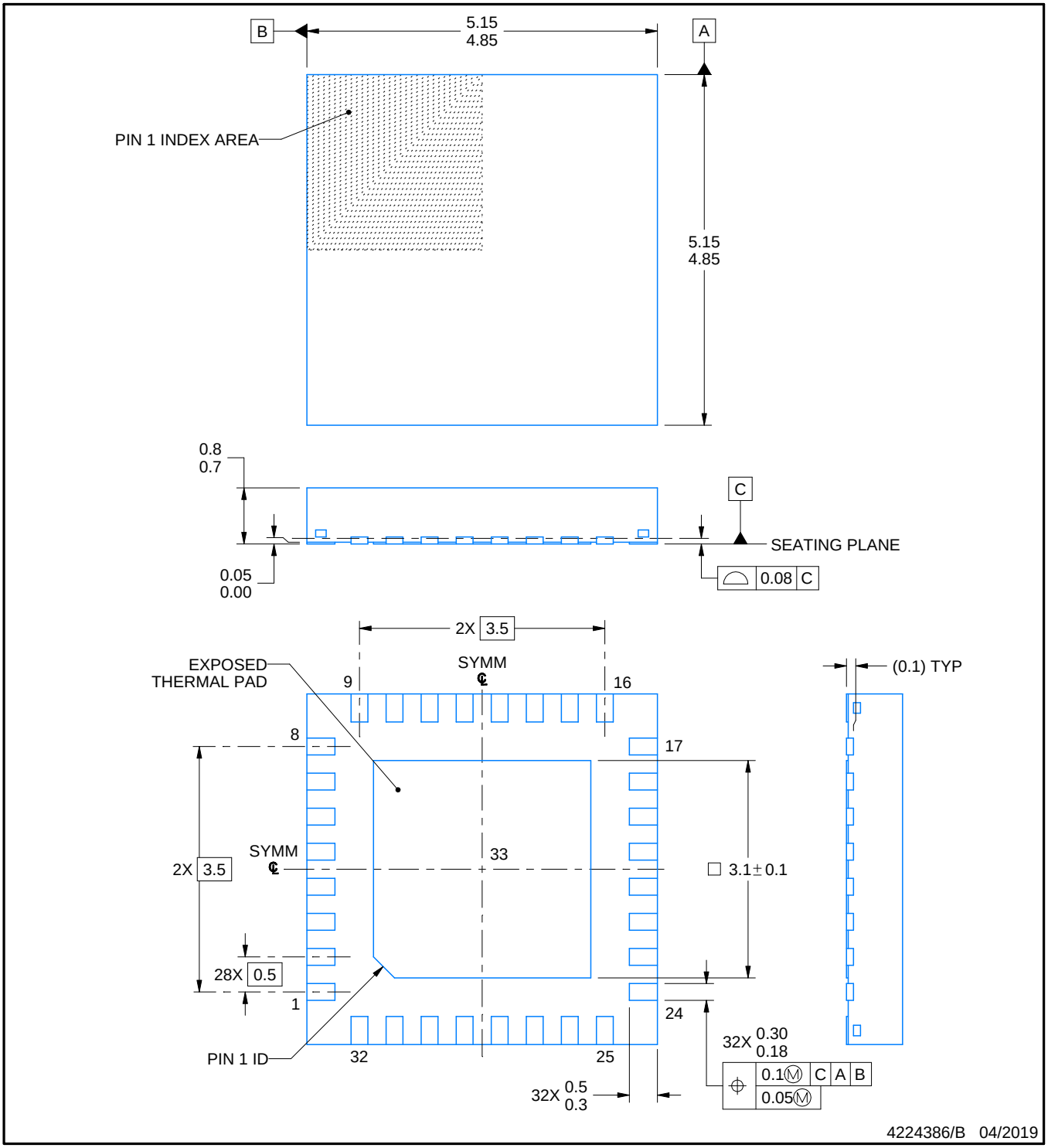
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB913ATRTVJQ1	WQFN	RTV	32	2500	367.0	367.0	35.0
DS90UB913ATRTVRQ1	WQFN	RTV	32	1000	210.0	185.0	35.0
DS90UB913ATRTVTQ1	WQFN	RTV	32	250	210.0	185.0	35.0

PACKAGE OUTLINE

RTV0032A

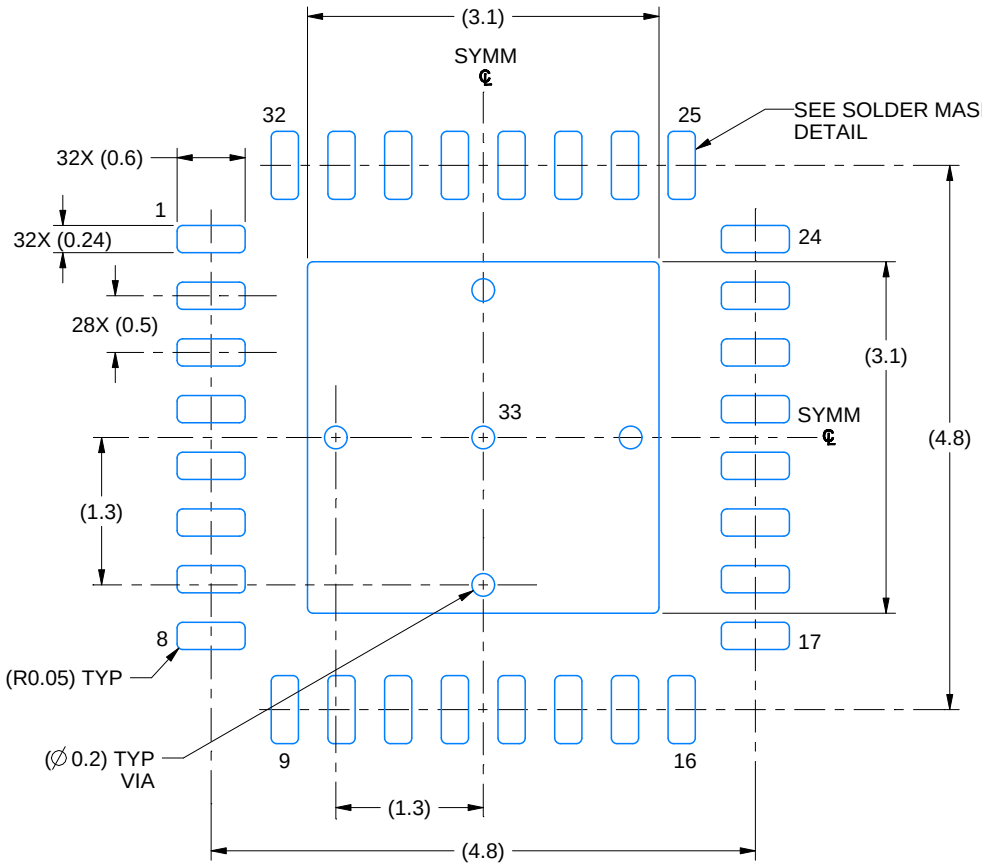
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

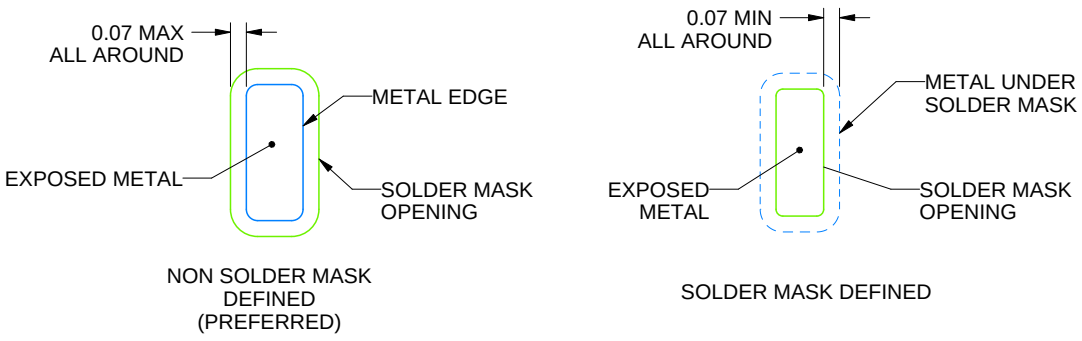


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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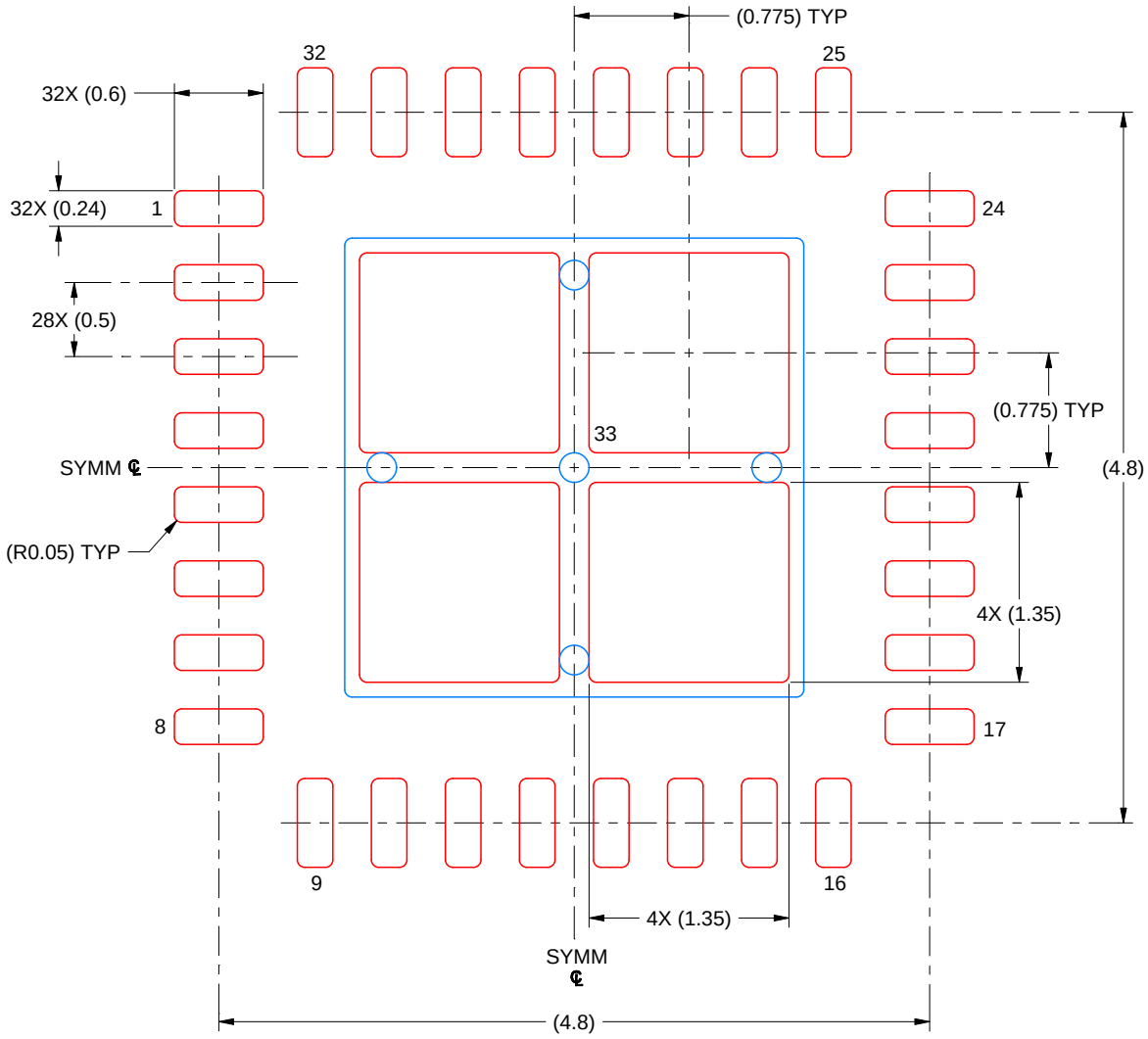
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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