TCA9517-Q1 电平转换 I2C 总线中继器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度范围：–40°C 至 125°C T_A
  - 器件 HBM 分类等级：±5500V
  - 器件 CDM 分类等级：±1000V
- 两通道双向缓冲器
- 与 I^2C 总线和系统管理总线 (SMBus) 兼容
- 在 A 侧上，工作电源电压范围为 0.9V 至 5.25V
- 在 B 侧上，工作电源电压范围为 2.7V 至 5.25V
- 可将电压电平从 0.9V - 5.25V 转换到 2.7V - 5.25V
- 高电平有效中继器启用输入
- 漏极开路 I^2C I/O
- 5.25V 耐压 I^2C 和使能输入支持混合模式信号操作
- 适用于标准模式和快速模式 I^2C 器件和多重主器件
- 器件断电时 I^2C 引脚呈高阻态
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 服务器
- 路由器（电信交换设备）
- 工业设备
- 具有多个 I^2C 从器件和/或印刷电路板 (PCB) 走线较长的产品

3 说明

TCA9517-Q1 是一款具有电平转换功能的双向缓冲器，适用于 I^2C 和 SMBus 系统。此器件可在混合模式应用中提供低电压（低至 0.9V）和较高电压（2.7V 至 5.25V）间的双向电压电平转换（上行转换/下行转换）。该器件能够扩展 I^2C 和 SMBus 系统，甚至在电平转换期间也不会降低系统性能。

TCA9517-Q1 可缓冲 I^2C 总线上的串行数据 (SDA) 和串行时钟 (SCL) 信号，因此允许在 I^2C 应用中连接两条总线电压高达 400pF 的总线。

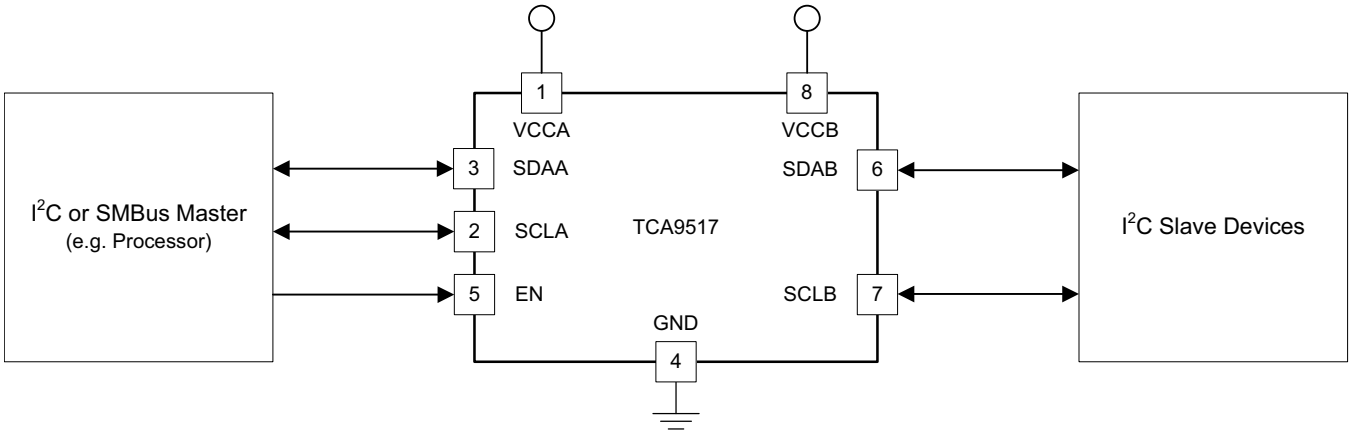
TCA9517-Q1 具有两类驱动器：A 侧驱动器和 B 侧驱动器。所有输入和 I/O 都能够承受 5.25V 的过压，即使器件未通电时也是如此（V_{CCB} 和/或 V_{CCA} = 0V）。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCA9517-Q1	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2018 年 6 月	*	初始发行版。

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5 说明（续）

B 侧上的缓冲器设计使其无法与使用静态电压偏移的器件串联使用。器件并不将经缓冲的低电平信号识别为有效低电平，并且不再将它作为经缓冲的低电平进行传送。

B 侧驱动器的运行电压介于 2.7V 至 5.25V 之间。此内部缓冲器的输出低电平大约为 0.5V。当输出在内部被驱动为低电平时，输出电压必须比输出低电平低 70mV 或者更多。更高的电压低信号被称为经缓冲的低电平。当 B 侧 I/O 被内部驱动为低电平时，输入并不将此低电平识别为低电平。当输入低电平状态被释放时，这一特性防止了锁定情况的发生。

A 侧驱动器运行电压介于 0.9V 至 5.25V 之间并且能够驱动更大电流。它们不需要经缓冲的低电平特性（或者静态失调电压）。B 侧低电平信号在 A 侧转换为接近 0V 的低电平。它可以适应低电压逻辑更小的电压摆幅。A 侧输出下拉驱动硬低电平。输入电平设置为 0.3 × V_{CCA} 以满足低电压侧电源低至 0.9V 的系统中对较低电平的需求。

两个或多个 TCA9517-Q1 器件的 A 侧可以连接在一起。将 A 侧作为公共总线可以实现多个拓扑结构（请参阅 图 8 和 图 9）。可以将 A 侧直接连接至任意具有静态或动态失调电压的其他缓冲器。可以将多个 TCA9517-Q1 串联在一起（相邻器件间通过 A 侧和 B 侧相连），失调电压不会增大，只是需要考虑飞行时间延迟。由于 B 侧缓冲低电压的原因，TCA9517-Q1 不能通过 B 侧相连。B 侧不能连接配有上升时间加速器的器件。

VCCA 只能用于为 A 侧输入比较器提供 0.3 × V_{CCA} 参考电压，或者用于电源正常状态检测电路。TCA9517-Q1 逻辑和所有 I/O 均由 VCCB 引脚供电。

当与标准 I^2C 系统一同工作时，需要用上拉电阻在经缓冲的总线上提供逻辑高电平。TCA9517-Q1 具有 I^2C 总线的标准开漏配置。这些上拉电阻器的尺寸由系统决定，然而，中继器的每一侧都必须有一个上拉电阻器。此器件专为与标准模式及快速模式 I^2C 器件（而不单是 SMBus 器件）一起工作而设计。在可以接受标准模式器件和多个主控器的通用型 I^2C 系统中，标准模式 I^2C 器件的额定值只为 3mA。在某些情况下，可以采用更高的结束电流。

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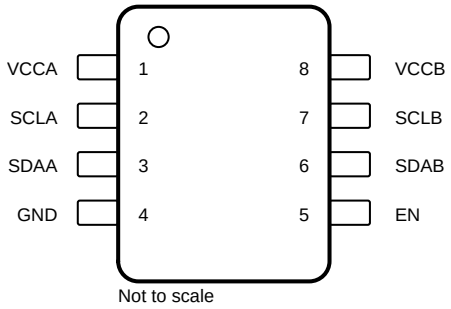
6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCA	Supply	A-side supply voltage (0.9 V to 5.25 V)
2	SCLA	Input/Output	Serial clock bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
3	SDAA	Input/Output	Serial data bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
4	GND	Ground	Ground
5	EN	Input	Active-high repeater enable input
6	SDAB	Input/Output	Serial data bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
7	SCLB	Input/Output	Serial clock bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
8	VCCB	Supply	B-side and device supply voltage (2.7 V to 5.25 V)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	7	V
V_{CCA}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

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7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±5500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9 (1)	5.25	V
V_{CCB}	Supply voltage, B-side bus	$V_{CCA} \le V_{CCB}$	2.7	5.25	V
		$V_{CCA} > V_{CCB}$	2.9	5.25	
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	5.25	V
		SDAB, SCLB	0.7 × V_{CCB}	5.25	
		EN	0.7 × V_{CCB}	5.25	
V_{IL}	Low-level input voltage	SDAA, SCLA		0.3 × V_{CCA}	V
		SDAB, SCLB (2)		0.3 × V_{CCB}	
		EN		0.3 × V_{CCB}	
I_{OL}	Low-level output current			6	mA
T_A	Operating free-air temperature		–40	125	°C

(1) Low-level supply voltage
(2) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines. See *V_{ILC} and Pullup Resistor Sizing* for V_{ILC} application information

7.4 Thermal Information

THERMAL METRIC (1)		TCA9517-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

V_{CCB} = 2.7 V to 5.25 V, GND = 0 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	2.7 V to 5.25 V			–1.2	V
V_{OL}	Low-level output voltage	SDAB, SCLB	I_{OL} = 100 μA or 6 mA, V_{ILA} = V_{ILB} = 0 V	2.7 V to 5.25 V	0.45	0.52	0.6	V
		SDAA, SCLA	I_{OL} = 6 mA			0.1	0.2	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SDAB, SCLB	ensured by design	2.7 V to 5.25 V		70		mV
V_{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB		2.7 V to 5.25 V		0.4		V
I_{CC}	Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I_{CC}	Quiescent supply current		Both channels high, SDAA = SCLA = V_{CCA} and SDAB = SCLB = V_{CCB} and EN = V_{CCB}	5.25 V		1.5	5	mA
			Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open			1.5	5	
			In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			3	5	
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.7 V to 5.25 V			±1	μA
			V_I = 0.2 V				10	
		SDAA, SCLA	V_I = V_{CCB}				±1	
			V_I = 0.2 V				10	
		EN	V_I = V_{CCB}				±1	
			V_I = 0.2 V			–10	–30	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V	2.7 V to 5.25 V			10	μA
		SDAA, SCLA					10	
C_I	Input capacitance	EN	V_I = 3 V or 0 V	3.3 V		6	10	pF
		SCLA, SCLB	V_I = 3 V or 0 V	3.3 V		8	13	
				0 V		7	11	
C_{IO}	Input/output capacitance	SDAA, SDAB	V_I = 3 V or 0 V	3.3 V		8	13	pF
				0 V		7	11	

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

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7.7 I²C Interface Switching Characteristics

V_{CCB} = 2.7 V to 5.25 V, GND = 0 V, T_A = –40°C to 125°C (unless otherwise noted)(1) (2)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP(3)	MAX	UNIT
t_{PLZ}	Propagation delay		SDAB, SCLB(4) (see 图 6)	SDAA, SCLA(4) (see 图 6)			141	250	ns
			SDAA, SCLA(5) (see 图 5)	SDAB, SCLB(5) (see 图 5)			74	110	
t_{PZL}	Propagation delay		SDAB, SCLB	SDAA, SCLA	V_{CCA} ≤ 2.7 V (see 图 4)		76(6)	110	ns
					V_{CCA} ≥ 3 V (see 图 4)		95	290	
			SDAA, SCLA(5) (see 图 5)	SDAB, SCLB(5) (see 图 5)			107	230	
t_{TLH}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see 图 5)		12		ns
					V_{CCA} ≥ 3 V (see 图 5)		42		
		A side to B-side (see 图 4)					125		
t_{THL}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see 图 5)		67(6)	200	ns
					V_{CCA} ≥ 3 V (see 图 5)		86	240	
		A side to B-side (see 图 4)					48	120	

(1) Times are specified with loads of 1.35-kΩ pull-up resistance and 50-pF load capacitance on the B-side. On the A side, for 0.9-V ≤ V_{CCA} ≤ 2.7-V, a 167-Ω pull-up and 57-pF load capacitance. For V_{CCA} ≥ 3.0-V, a 450-Ω pull-up and 57-pF load capacitance. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
(2) pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B-side.
(3) Typical values were measured with V_{CCA} = V_{CCB} = 3.3 V at T_A = 25°C, unless otherwise noted.
(4) The t_{PLH} delay data from B to A side is measured at 0.4 V on the B-side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
(5) The proportional delay data from A to B-side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B-side.
(6) Typical value measured with V_{CCA} = 2.7 V at T_A = 25°C

7.8 Typical Characteristics

V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

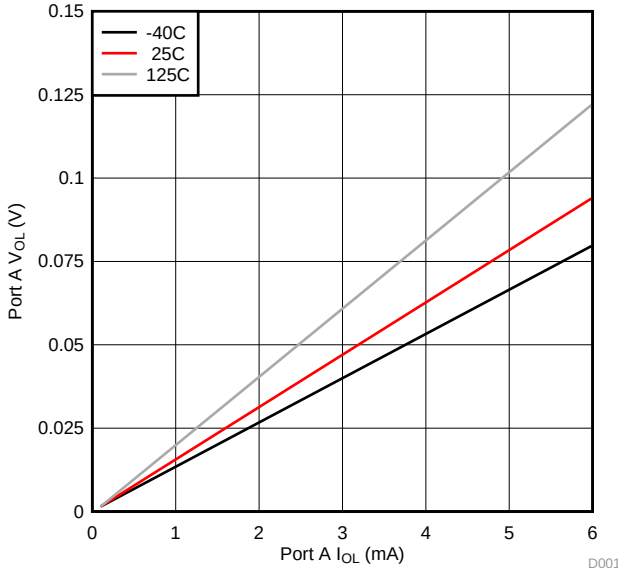


图 1. Port A V_{OL} vs I_{OL}

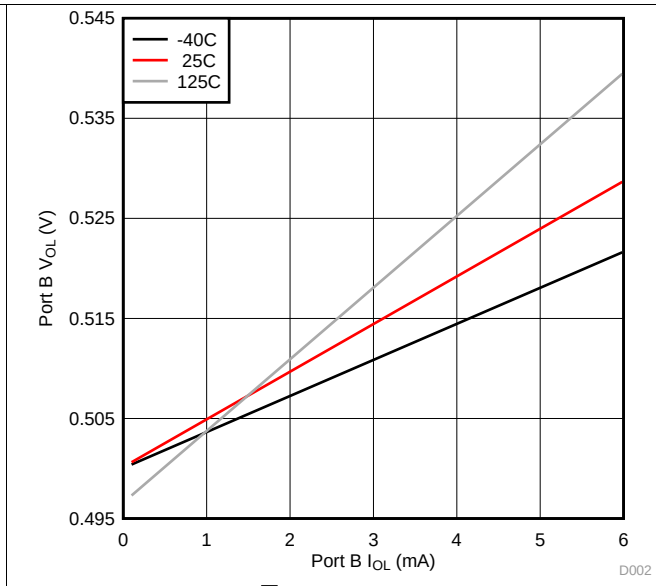
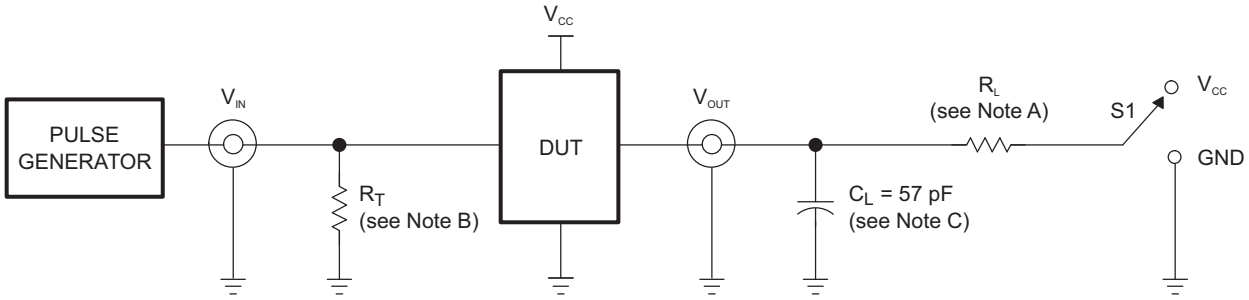


图 2. Port B V_{OL} vs I_{OL}

8 Parameter Measurement Information



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

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A. R_L = 167 Ω (0.9 V to 2.7 V) and R_L = 450 Ω (3.0 V to 5.25 V) on the A side and 1.35 kΩ on the B-side

B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

C. C_L includes probe and jig capacitance. C_L = 50 pF when on the B-side.

D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

E. The outputs are measured one at a time, with one transition per measurement.

F. t_{PLH} and t_{PHL} are the same as t_{pd}.

G. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

H. t_{PZL} and t_{PZH} are the same as t_{en}.

图 3. Test Circuit

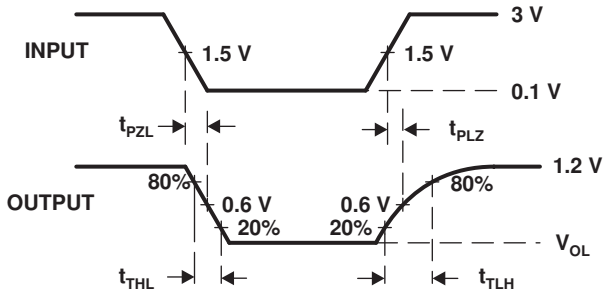

图 4. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side

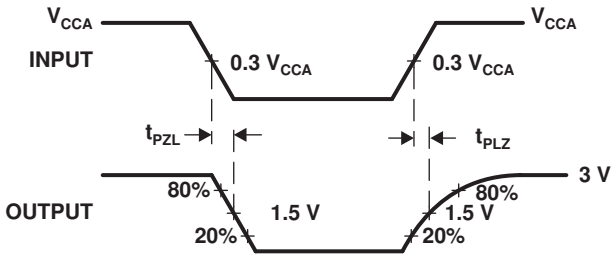

图 5. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side

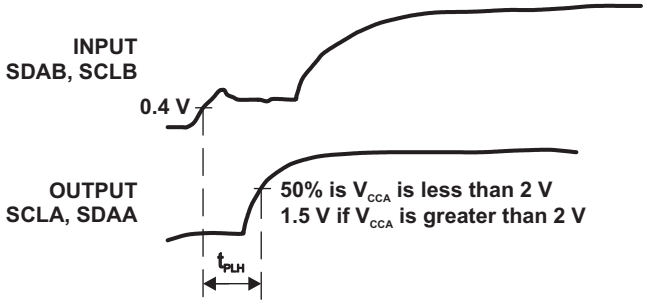

图 6. Waveform 3 – Propagation Delay for B-side to A-side

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9 Detailed Description

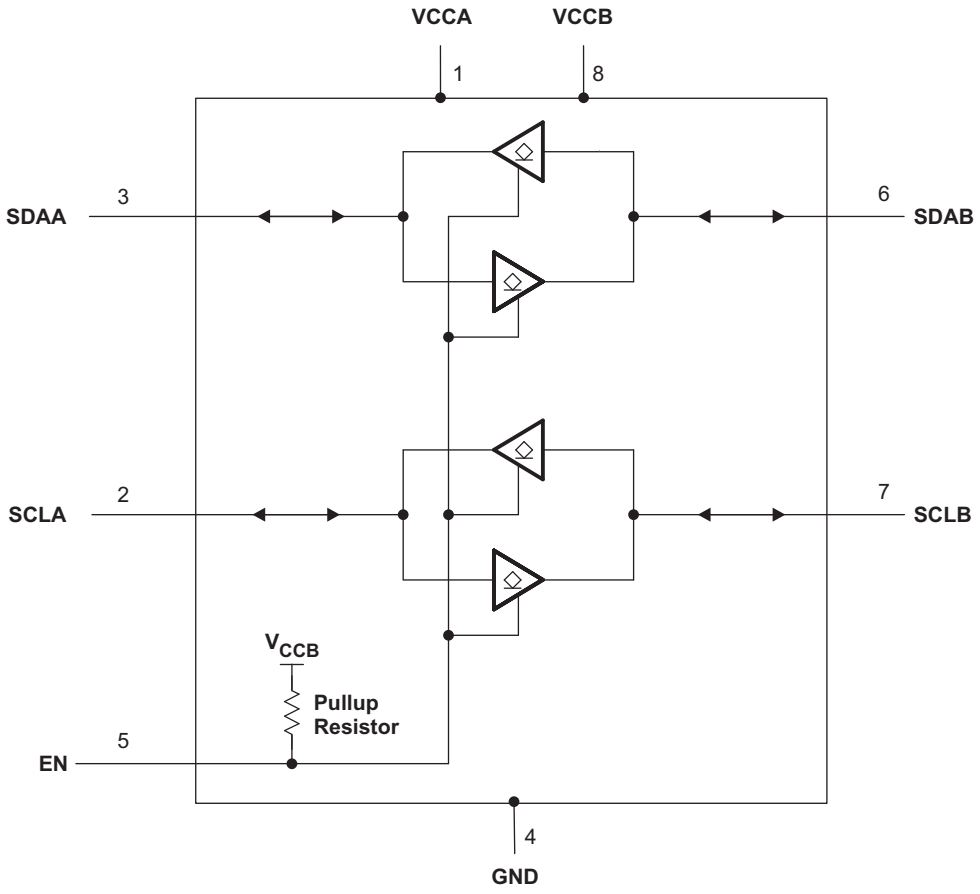
9.1 Overview

The TCA9517-Q1 is a bidirectional buffer with level shifting capabilities for I^2C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.25 V) in mixed-mode applications. This device enables I^2C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517-Q1 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I^2C bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an I^2C application.

The TCA9517-Q1 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.25 V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9517-Q1 is a two-channel bidirectional buffer with level-shifting capabilities

9.3.2 Active-High Repeater-Enable Input

The TCA9517-Q1 has an active-high enable (EN) input with an internal pull-up to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

9.3.3 V_{OL} B-Side Offset Voltage

The B-side drivers operate from 2.7 V to 5.25 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

9.3.4 Standard Mode and Fast Mode Support

The TCA9517-Q1 supports standard mode as well as fast mode I^2C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

9.3.5 Clock Stretching Support

The TCA9517-Q1 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

9.4 Device Functional Modes

表 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

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10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A typical application is shown in 图 7. In this example, the system master is running on a 3.3 V I^2C bus, and the slave is connected to a 1.2 V I^2C bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The TCA9517-Q1 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.25 V bus voltages and 2.7 V to 5.25 V bus voltages.

When the A side of the TCA9517-Q1 is pulled low by a driver on the I^2C bus, a comparator detects the falling edge when it goes below 0.3 × V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the TCA9517-Q1 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to 图 9 and 图 10. If the bus master in 图 7 were to write to the slave through the TCA9517-Q1, waveforms shown in 图 9 would be observed on the A bus. This looks like a normal I^2C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517-Q1, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9517-Q1. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517-Q1 for a short delay, while the A-bus side rises above 0.3 × V_{CCA} and then continues high.

10.2 Typical Application

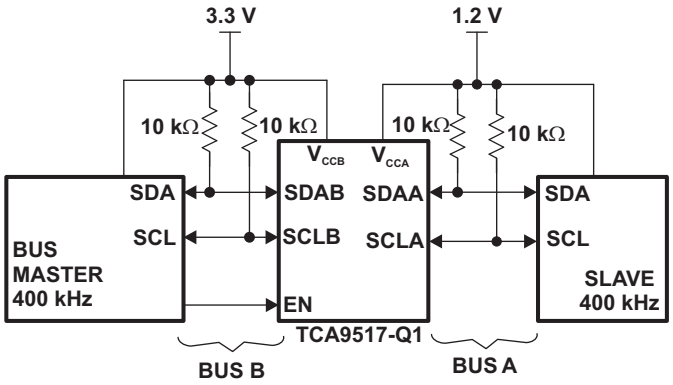

图 7. Typical Application Schematic

10.2.1 Design Requirements

For the level translating application, the following should be true:

- V_{CCA} = 0.9 V to 5.25 V
- V_{CCB} = 2.7 to 5.25 V
- B-side ports must not be connected together

Typical Application (接下页)

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support

The TCA9517-Q1 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

10.2.2.2 V_{ILC} and Pullup Resistor Sizing

For the TCA9517-Q1 to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the B-side must be below 0.4 V.

V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

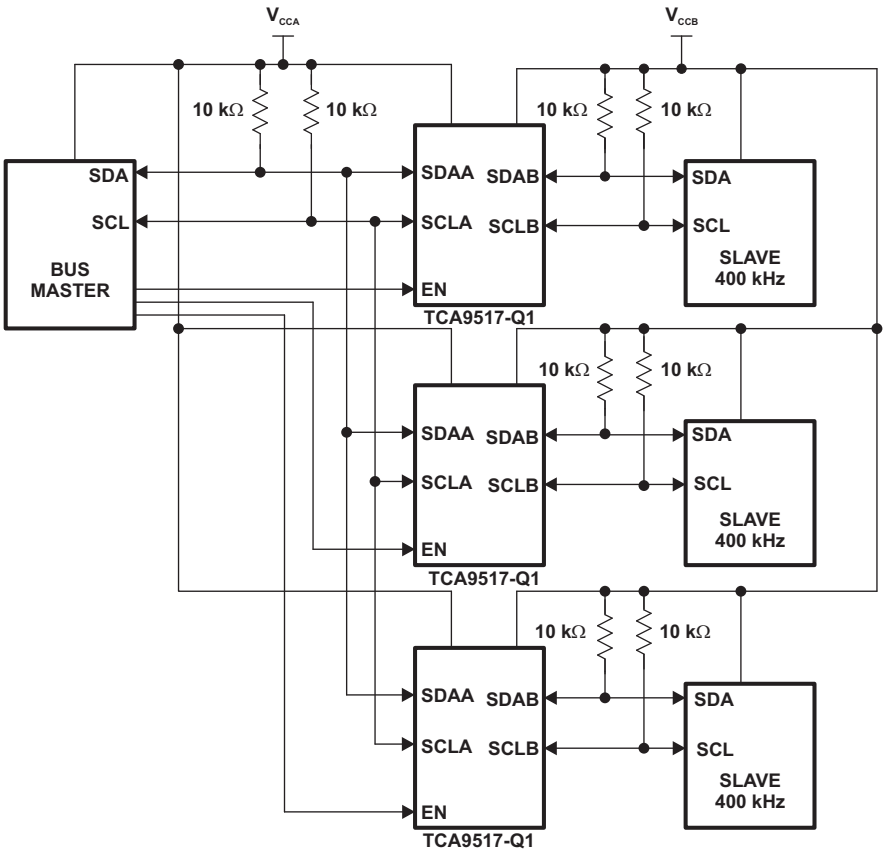

图 8. Typical Star Application

Multiple A sides of TCA9517-Q1s can be connected in a star configuration, allowing all nodes to communicate with each other.

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Typical Application (接下页)

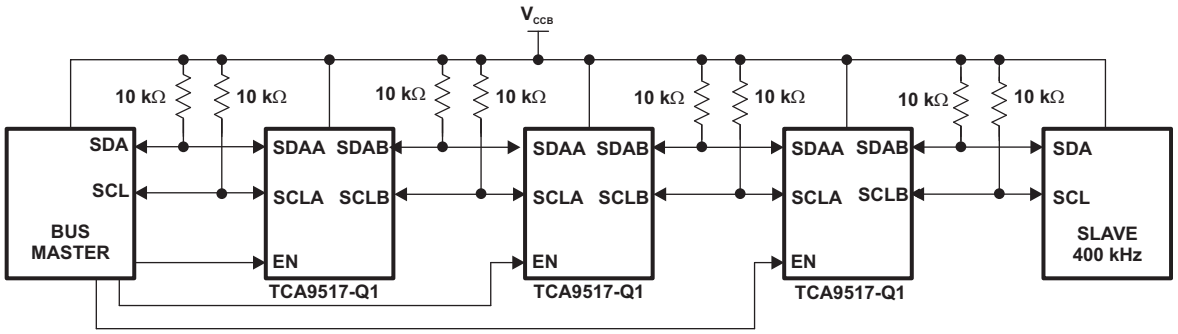

图 9. Typical Series Application

To further extend the I^2C bus for long traces/cables, multiple TCA9517-Q1s can be connected in series as long as the A-side is connected to the B-side. I^2C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

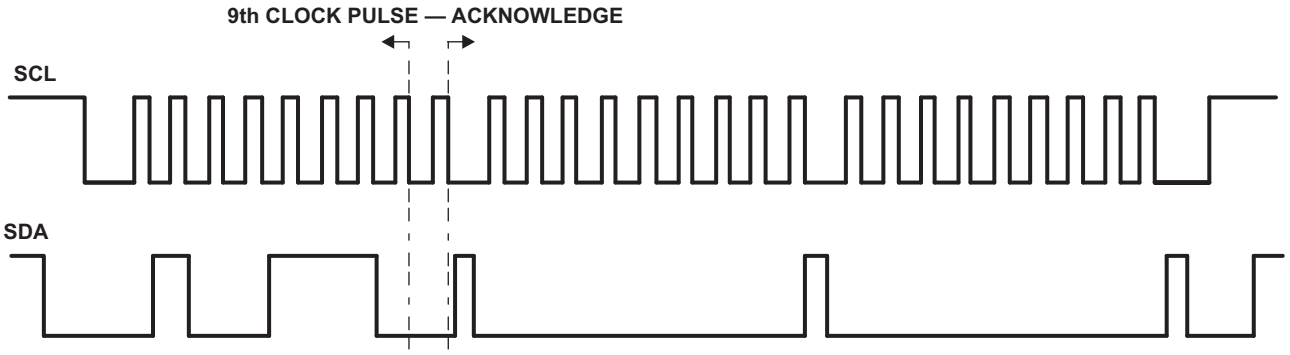

图 10. Bus A (0.9 V to 5.25 V Bus) Waveform

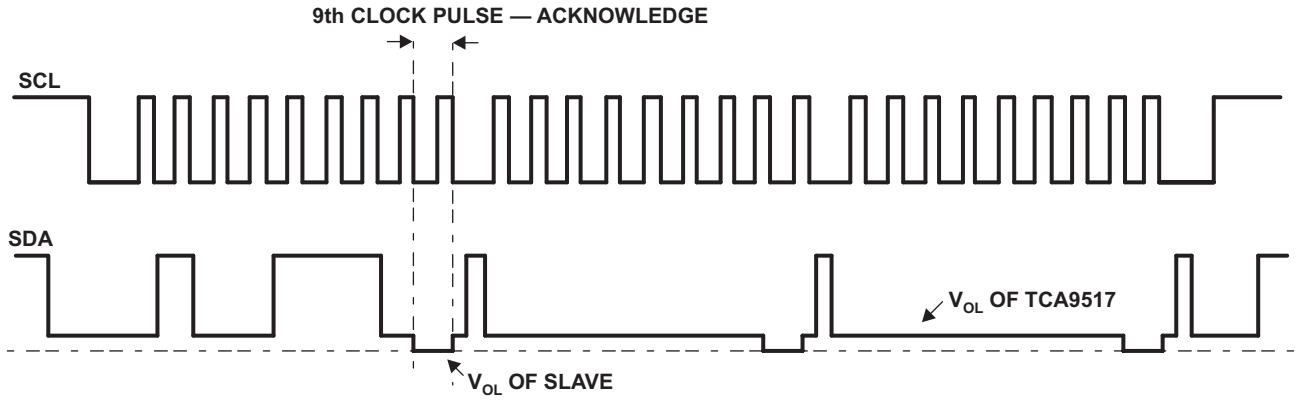

图 11. Bus B (2.7 V to 5.25 V Bus) Waveform

Typical Application (接下页)

10.2.3 Application Curve

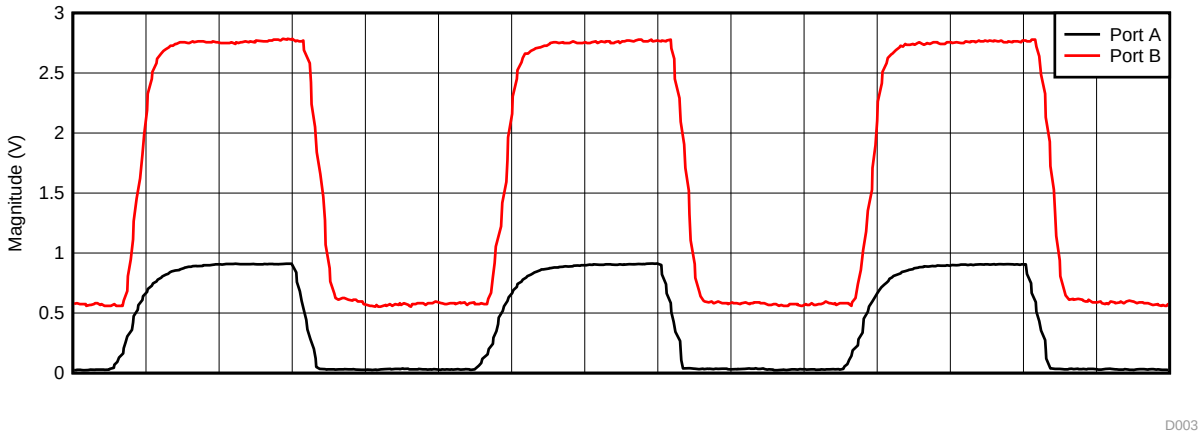

图 12. Voltage Translation at 400 kHz, V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

11 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9517-Q1 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the A-side (below 0.3 × V_{CCA}) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5 V. When the A-side rises above 0.3 × V_{CCA}, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below 0.3 × V_{CCB}, the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above 0.7 × V_{CCB}. If the B-side low voltage goes below 0.4 V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5 V until the A-side rises above 0.3 × V_{CCA}.

TI recommends using a decoupling capacitor and placing it close to the VCCA and VCCB pins of a value of about 100 nF.

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12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9517-Q1.

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example

图 13 shows an example layout of the DGK package.

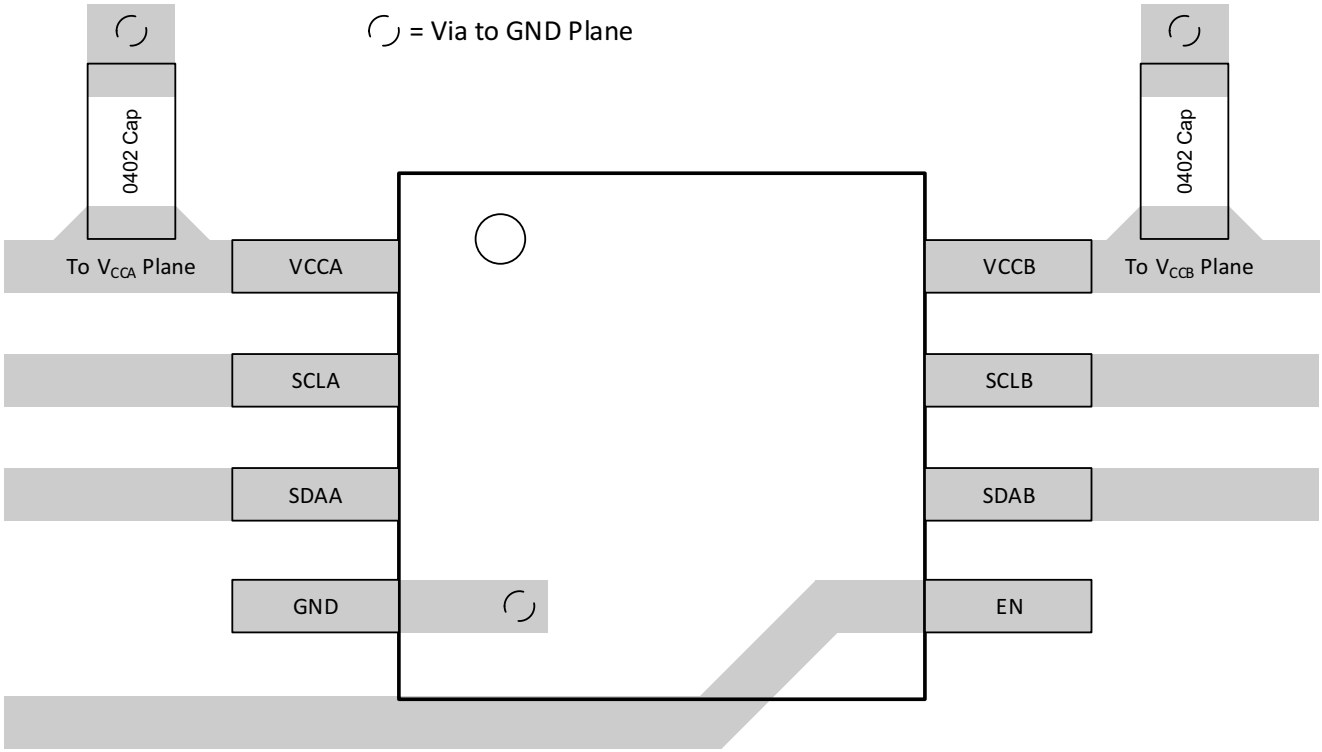

图 13. TCA9517-Q1A Layout Example

13 器件和文档支持

13.1 器件支持

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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14 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9517DGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1N2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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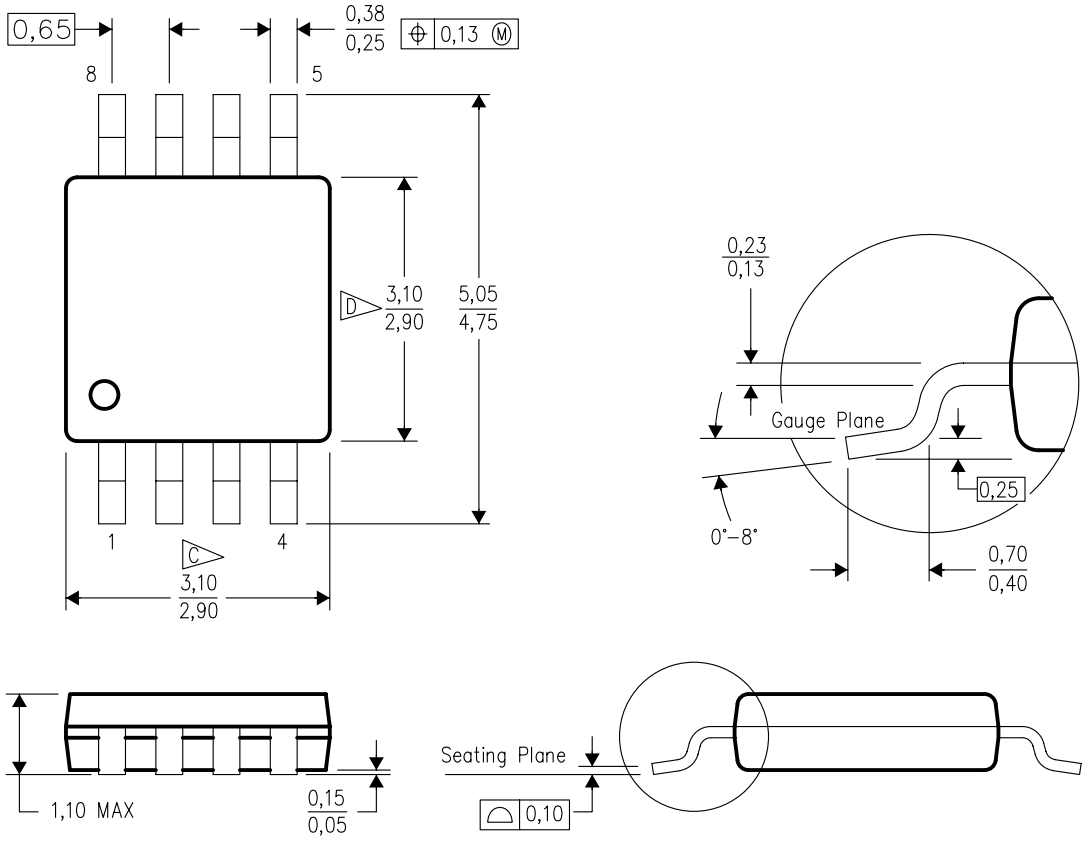
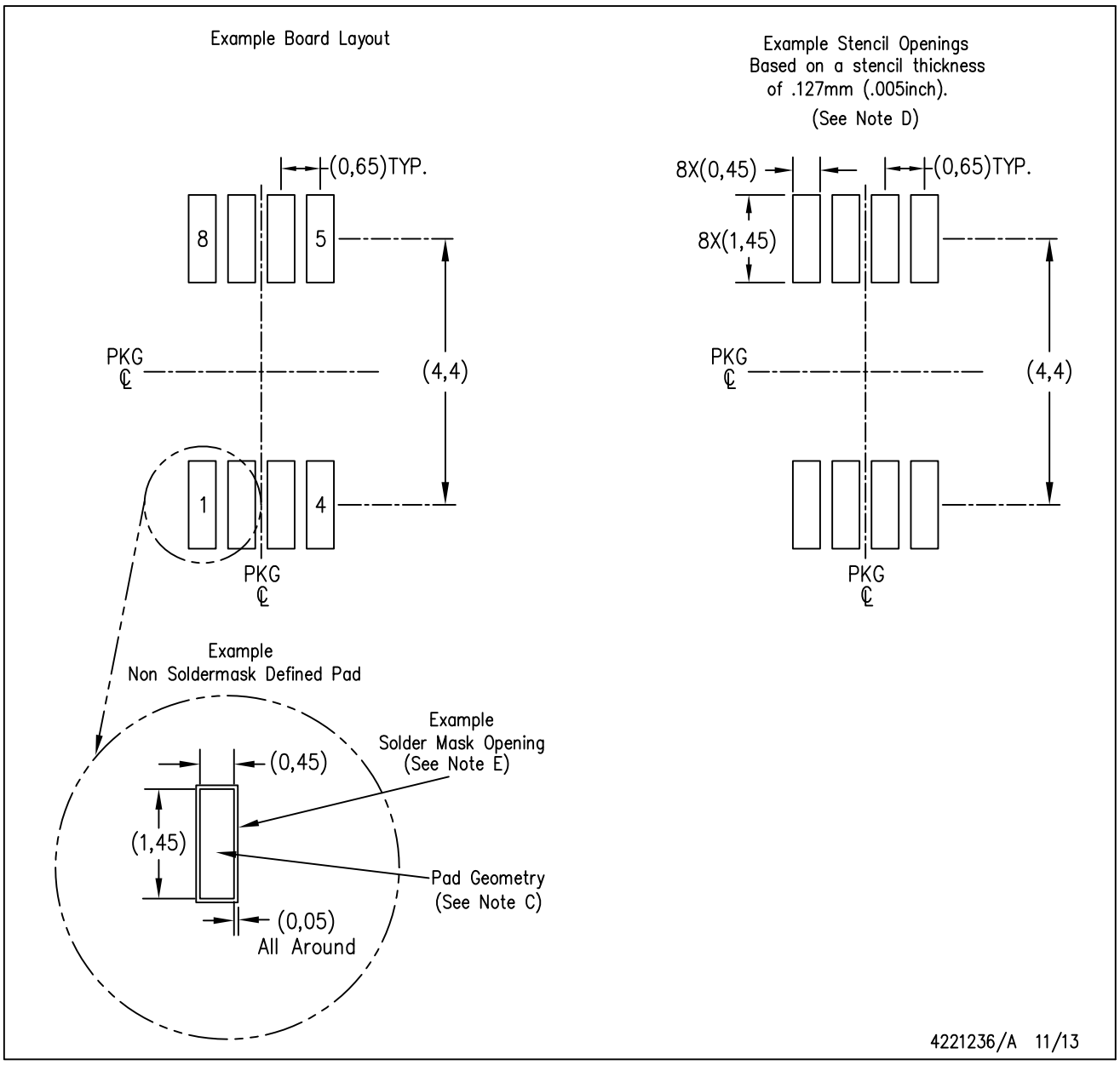
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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