TCA9416 超低电压 I2C 转换器

1 特性

- 适用于 I2C 应用中的 SDA 和 SCL 线路的 2 位双向转换器
- 在无方向引脚的情况下提供双向电压转换
- 高阻抗输出 SCL_A、SDA_A、SCL_B、SDA_B 引脚（当 OE = 0V 或 VCC = 0V 时）
- 根据相应的 VCC 电压启用所有 SDA 和 SCL 引脚上的内部 10kΩ 上拉电阻器
- A 和 B 端口上均为 1.08V 至 3.6V
- VCC 隔离特性：如果任一 VCC 输入接地 (GND)，则两个端口都处于高阻抗状态（不包括上拉电阻）
- 无需电源定序：V_{CCA} 或 V_{CCB} 均可优先斜升
- 低至 2.5μA 的 Ioff（当 VCCA 或 VCCB = 0V 时）
- OE 输入可直接连接至 V_{CCA}，也可通过 GPIO 进行控制
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2500V 人体放电模型 (A114-B)
  - 1500V 充电器件模型 (C101)

2 应用

- 可穿戴设备
- 个人电子产品
- 服务器

3 说明

TCA9416 是一款具有输出使能 (OE) 输入以及上升沿和下降沿加速器的 2 位双向 I2C 和 SMBus 电压电平转换器。该器件在 A 侧和 B 侧均能以 1.08V 至 3.6V 的电压运行。因此，该器件能够在典型的 1.2V、1.8V、2.5V 和 3.3V 电源轨之间，进行任何高低逻辑信号电平切换。

OE 输入引脚的基准为 VCCA，可以直接连接至 VCCA，但也可以承受 3.6V 的电压。用户还可以对 OE 引脚进行控制，将其设置为低电平，使所有 SCL 和 SDA 引脚均处于高阻抗状态，从而显著减少静态电流消耗。

在正常 I2C 和 SMBus 配置下，TCA9416 可以达到 SCL 频率为 100kHz（标准模式）、400kHz（快速模式）或 1MHz（快速模式升级版）的标准速度要求。

TCA9416 在 SCL_A、SDA_A、SCL_B 和 SDA_B 上具有内部 10kΩ 上拉电阻器。此外还可以向总线添加额外的上拉电阻器，从而减小总上拉电阻并加快上升沿的上升速度。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
TCA9416	X2SON (8)	1.35mm × 0.80mm
	SOT-23-T (8)	2.9mm × 1.6mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

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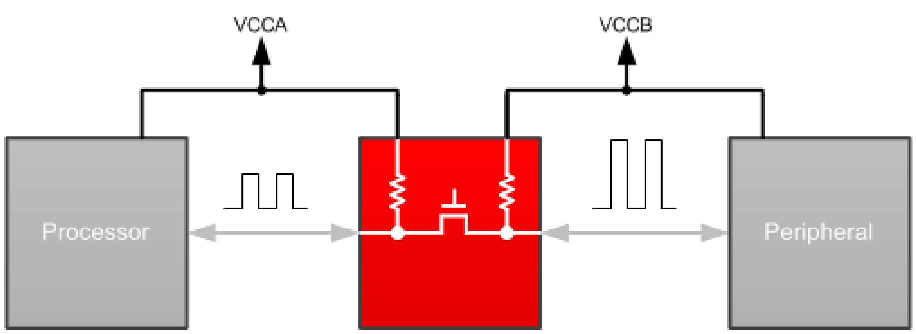

TCA9416 典型应用方框图

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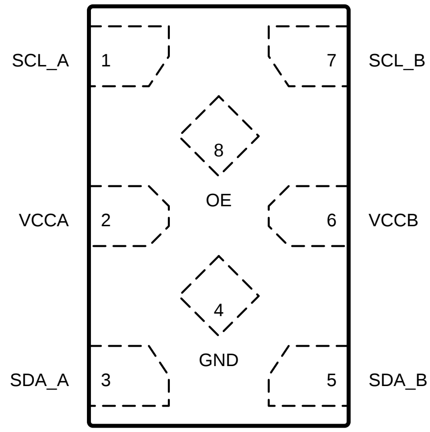
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
February 2021	*	Initial release.

5 Pin Configuration and Functions



Not to scale

图 5-1. 8-PIN DTM, (Top View)

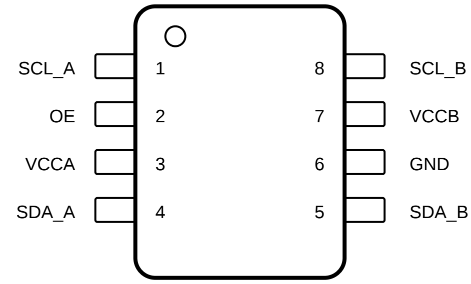


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图 5-2. 8-PIN DDF, (Top View)

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DTM	DDF		
SCL_A	1	1	I/O	Input/output A. Referenced to V_{CCA}.
VCCA	2	3	Power	A-port supply voltage. 1.08 V ≤ V_{CCA} ≤ 3.6 V
SDA_A	3	4	I/O	Input/output A. Referenced to V_{CCA}.
GND	4	6	GND	Ground
SDA_B	5	5	I/O	Input/output B. Referenced to V_{CCB}.
VCCB	6	7	Power	B-port supply voltage. 1.08 V ≤ V_{CCB} ≤ 3.6 V
SCL_B	7	8	I/O	Input/output B. Referenced to V_{CCB}.
OE	8	2	Input	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.

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6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4	V
V_{CCB}	Supply voltage range		–0.5	4	V
V_I	Input voltage range(1)	A port	–0.5	4	V
		B port	–0.5	4	
V_O	Voltage range applied to any output in the high-impedance or power-off state(1)	A port	–0.5	4	V
		B port	–0.5	4	
V_O	Voltage range applied to any output in the high or low state(1) (2)	A port	–0.5	4	V
		B port	–0.5	4	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A-Ports, B-Ports	±2500	V
			V_{CCA}, V_{CCB}, OE	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.08	3.6	V
V_{CCB}	Supply voltage				1.08	3.6	V
V_I	Input voltage	A-port I/Os, B-port I/Os, OE	0 V to 3.6 V	0 V to 3.6 V	0	3.6	V
V_{IH}	High-level input voltage	OE input	1.08 V to 3.6 V	1.08 V to 3.6 V	V_{CCA} × 0.65	3.6	V
V_{IL}	Low-level input voltage	OE input	1.08 V to 3.6 V	1.08 V to 3.6 V	0	V_{CCA} × 0.35	V
T_A	Operating free-air temperature				–40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TCA9416	TCA9416	UNIT
		DDF	DTM	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.6	212.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.7	105.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.8	124.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.2	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	97.2	23.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{UVLO_RISE}	UVLO Rising Threshold	V_{UVLO} for V_{CCA} and V_{CCB} are independent	0 V to 3.6 V	0 V to 3.6 V	0.65	0.9	1	V
V_{UVLO_FALL}	UVLO Falling Threshold	V_{UVLO} for V_{CCA} and V_{CCB} are independent	0 V to 3.6 V	0 V to 3.6 V	0.6	0.85	0.95	V
V_{RTA} (1)	RTA(2) Activation Threshold		1.08 V to 3.6 V	1.08 V to 3.6 V	V_{CCI} × 0.30	V_{CCI} × 0.45		V
V_{FTA} (1)	FTA(2) Activation Threshold		1.08 V to 3.6 V	1.08 V to 3.6 V		V_{CCI} × 0.60	V_{CCI} × 0.70	V
R_{PU}		V_I = 0.15 V	1.08V to 3.6V	1.08V to 3.6V	7.5	10	12.5	kΩ
I_I	OE	V_I = V_{CCA} or GND	1.08 V to 3.6 V	1.08 V to 3.6 V		±0.1	±1	µA
I_{OZ}	A or B port	OE less than V_{IL}	1.08 V to 3.6 V	1.08 V to 3.6 V		0	±2.5	µA
I_{off}	A port	V_I = 3.6 V, V_O = 0 V (T_A ⩽ 85 C)	0 V	0 V to 3.6 V		±0.1	±1	µA
	B port	V_I = 3.6 V, V_O = 0 V (T_A ⩽ 85 C)	0 to 3.6 V	0 V		±0.1	±1	
	A port	V_I = 3.6 V, V_O = 0 V (T_A ⩽ 125 C)	0 V	0 V to 3.6 V		±0.1	±2.5	
	B port	V_I = 3.6 V, V_O = 0 V (T_A ⩽ 125 C)	0 to 3.6 V	0 V		±0.1	±2.5	
I_{CC_OFF}	VCCA	V_I = V_O = open, I_O = 0, OE = 0 V	1.08 V to 3.6 V	1.08 V to 3.6 V		4	13	µA
	VCCB	V_I = V_O = open, I_O = 0, OE = 0 V				3	13	
I_{CCA}		V_I = V_O = open, I_O = 0, OE = VCCA	1.32 V	1.32 V to 3.6 V		3	6	µA
			1.98 V	1.32 V to 3.6 V		4	10	
			3.6 V	1.32 V to 3.6 V		6	14	
			0 V	1.32 V to 3.6 V		0	0.5	
			1.32 V to 3.6 V	0 V		3	12	
I_{CCB}		V_I = V_O = open, I_O = 0, OE = VCCA	1.32 V to 3.6 V	1.32 V		1.5	6	µA
			1.32 V to 3.6 V	1.98 V		2	8	
			1.32 V to 3.6 V	3.6 V		5	12	
			1.32 V to 3.6 V	0 V		0	0.5	
			0 V	1.32 V to 3.6 V		1	7	
I_{CCA} + I_{CCB}		V_I = V_O = open, I_O = 0, OE = VCCA	1.32 V	1.32 V		4	12	µA
			1.98 V	1.98 V		6	15	
			3.6 V	3.6 V		11	23	

6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
R_{on}		V_I = 0.2 V, I_O = 2 mA	1.08 V	1.08 V		28	50	Ω
		V_I = 0.2 V, I_O = 2 mA	1.08 V, 1.8 V	1.8 V, 1.08 V		28	50	
		V_I = 0.2 V, I_O = 3 mA	1.65 V	1.65 V		15	25	
		V_I = 0.2 V, I_O = 2 mA	1.08 V, 3.0 V	3.0 V, 1.08 V		30	55	
		V_I = 0.2 V, I_O = 3 mA	1.65 V, 3.0 V	3.0 V, 1.65 V		15	25	
		V_I = 0.2 V, I_O = 6 mA	3.0 V	3.0 V		10	15	
C_I	OE		3.3 V	3.3 V		2.5	4	pF
C_{io}	A or B port		0 V, 1.08 V, 3.6 V	0 V, 1.08 V, 3.6 V		7	10	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) RTA is "rise time accelerator" and FTA is "fall time accelerator"

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted). Typical specifications are at T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RTA}	Time from V_{RTA} to RTA disabling	SDA,SCL = Hi-Z EN = V_{CC}		80	210	ns

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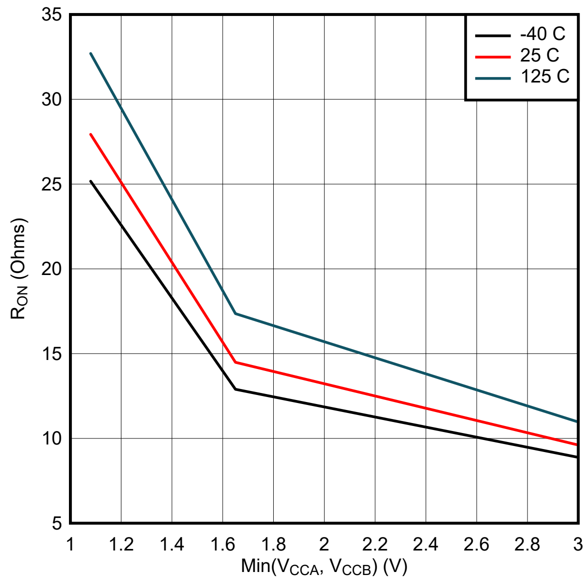
6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	A	B	V_{CCA} = 1.08 V		30	ns
			V_{CCA} = 1.8 V		20	
			V_{CCA} = 2.5 V		25	
			V_{CCA} = 3.6 V		23	
t_{PLH}	A	B	V_{CCA} = 1.08 V		25	ns
			V_{CCA} = 1.8 V		20	
			V_{CCA} = 2.5 V		20	
			V_{CCA} = 3.6 V		20	
t_{PHL}	B	A	V_{CCB} = 1.08 V		30	ns
			V_{CCB} = 1.8 V		20	
			V_{CCB} = 2.5 V		25	
			V_{CCB} = 3.6 V		23	
t_{PLH}	B	A	V_{CCB} = 1.08 V		25	ns
			V_{CCB} = 1.8 V		20	
			V_{CCB} = 2.5 V		20	
			V_{CCB} = 3.6 V		20	
$t_{SK(O)-RISE}$	Rising Channel-to-channel skew (Propagation)				5	ns
$t_{SK(O)-FALL}$	Falling Channel-to-channel skew (Propagation)				5	ns
t_{en}	OE	A or B			350	ns
t_{dis}	OE	A or B			250	ns
t_{rA}	B-port	A-port	V_{CCA} = 1.08 V		30	ns
			V_{CCA} = 1.8 V		25	
			V_{CCA} = 2.5 V		25	
			V_{CCA} = 3.6 V		25	
t_{rB}	A-port	B-port	V_{CCB} = 1.08 V		30	ns
			V_{CCB} = 1.8 V		25	
			V_{CCB} = 2.5 V		25	
			V_{CCB} = 3.6 V		25	
t_{fA}	B-port	A-port	V_{CCA} = 1.08 V		30	ns
			V_{CCA} = 1.8 V		30	
			V_{CCA} = 2.5 V		35	
			V_{CCA} = 3.6 V		40	
t_{fB}	A-port	B-port	V_{CCB} = 1.08 V		30	ns
			V_{CCB} = 1.8 V		30	
			V_{CCB} = 2.5 V		35	
			V_{CCB} = 3.6 V		40	

6.8 Typical Characteristics



The Min(V_{CCA}, V_{CCB}) signifies that the lower voltage of V_{CCA} or V_{CCB} is used. As an example, if V_{CCA} = 1.8 V and V_{CCB} = 3.3 V, then the Min(V_{CCA}, V_{CCB}) is 1.8 V.

图 6-1. R_{ON} (Ω) vs Min(V_{CCA}, V_{CCB}) (V)

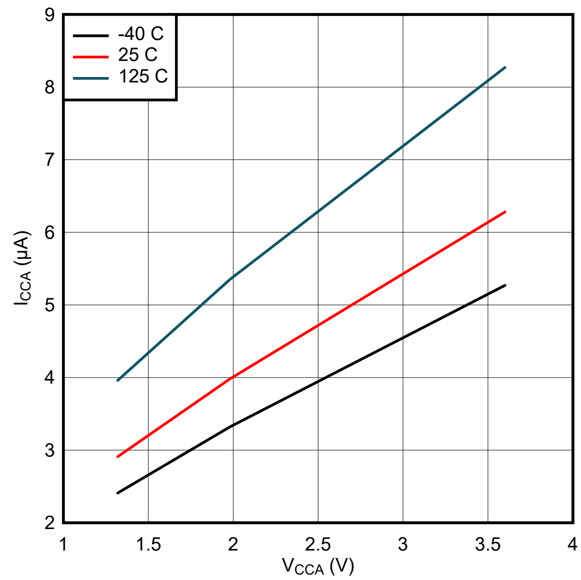


图 6-2. I_{CCA} (μA) vs V_{CCA} (V)

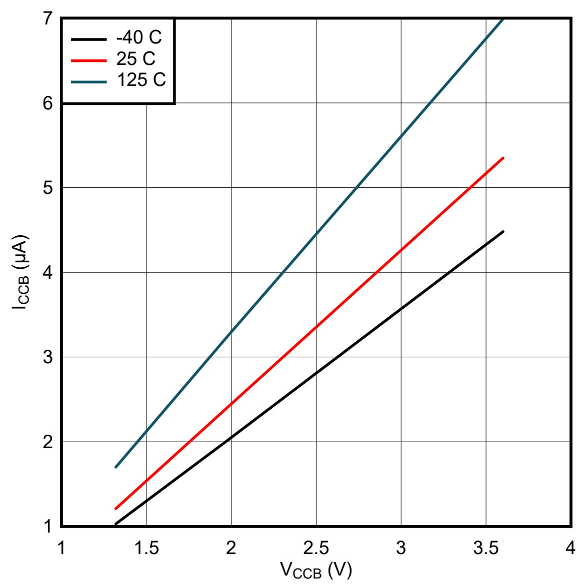


图 6-3. I_{CCB} (μA) vs V_{CCB} (V)

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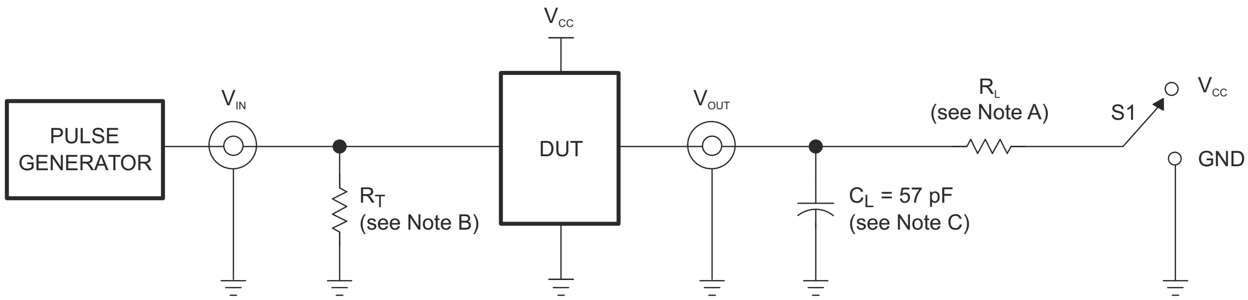
7 Parameter Measurement Information



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

图 7-1. Load Circuit for Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement

1. R_L = 1.35 kΩ
2. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
3. C_L includes probe and jig capacitance. C_L = 50 pF when on the B-side.
4. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, slew rate ⩾ 1 V/ns.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. V_{CCI} is the V_{CC} associated with the input port.
8. V_{CCO} is the V_{CC} associated with the output port.

7.1 Voltage Waveforms

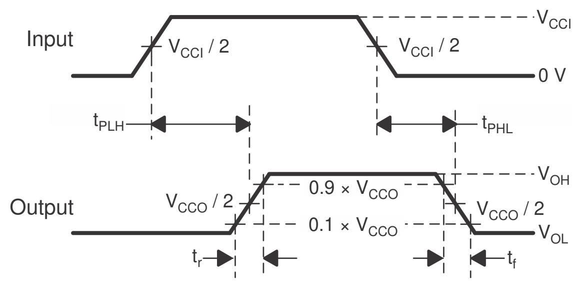
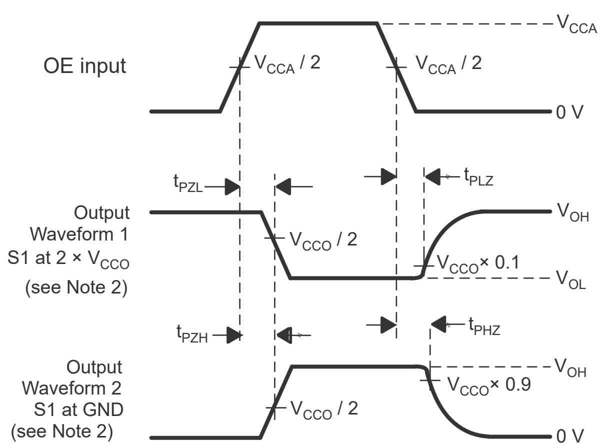


图 7-2. Propagation Delay Times



1. C_L includes probe and jig capacitance.
2. Waveform 1 in 图 7-3 is for an output with internal such that the output is high, except when OE is high (see 图 7-1). Waveform 2 in 图 7-3 is for an output with conditions such that the output is low, except when OE is high.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

图 7-3. Enable and Disable Times

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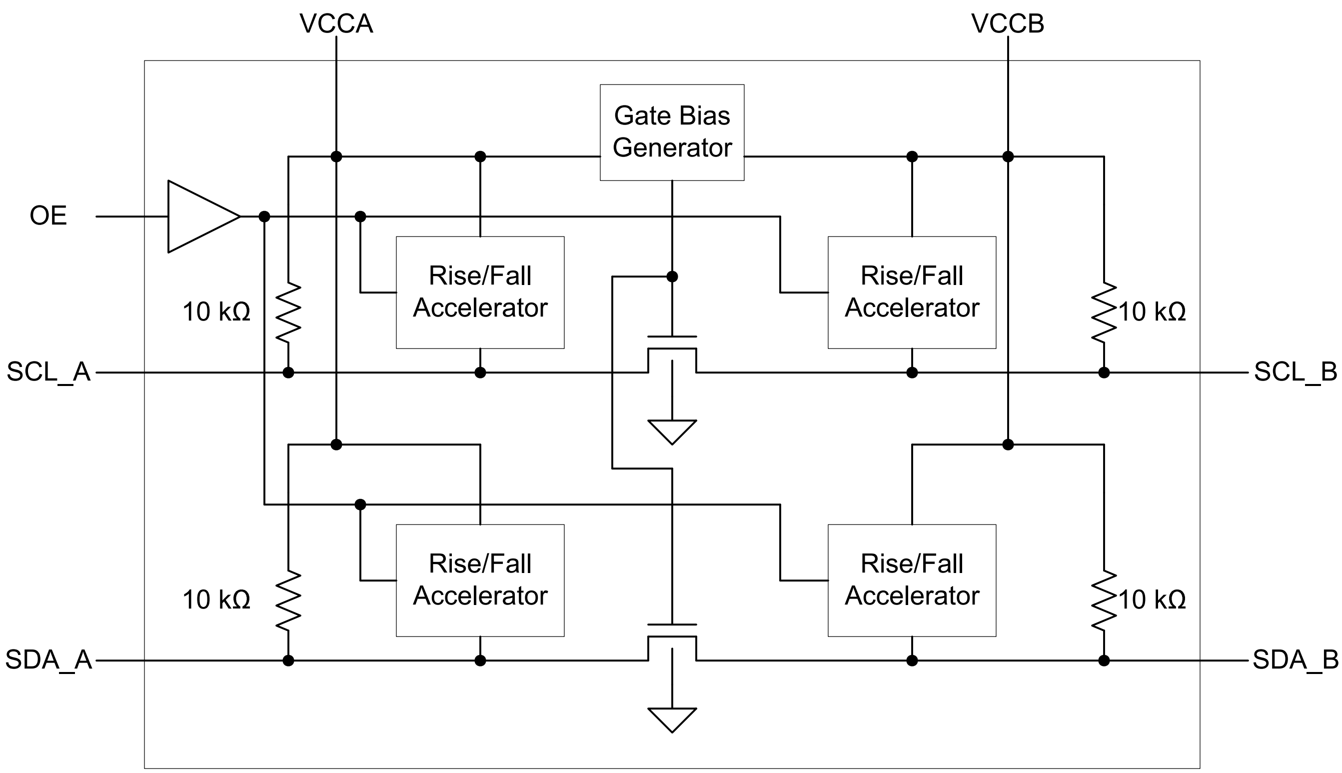
8 Detailed Description

8.1 Overview

The TCA9416 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A and B ports are able to accept I/O voltages ranging from 1.08 V to 3.6 V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10-kΩ pull up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. When TCA9416 is disabled the one shots are also disabled, but the internal pull ups are still enabled. Pull up resistors are gated on the supply voltage. When supply is above UVLO, the pull up resistor for that specific side (A vs B) is enabled.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TCA9416 architecture (see 图 8-1) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

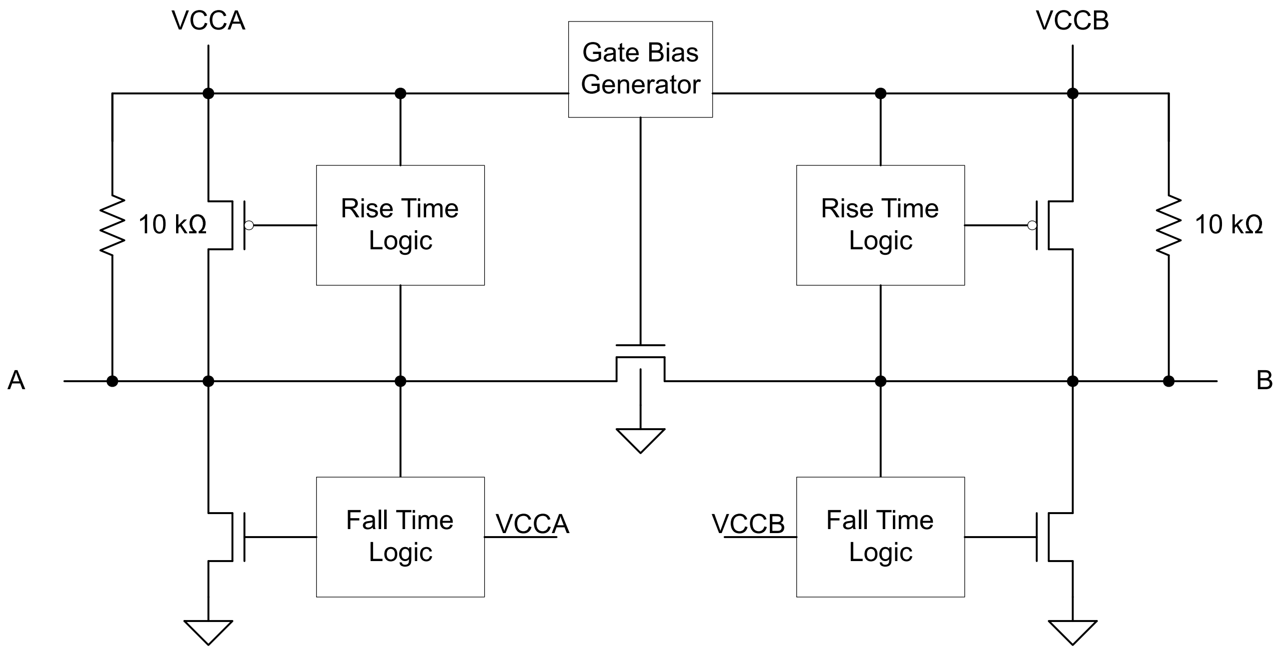


图 8-1. Architecture of a TCA9416 Cell

These two bidirectional channels support both directions of data flow without a direction-control signal. By properly biasing the gate of the pass-FET, the FET can turn on (low R_{DSON}), when either side input voltage drops to ~ 1 voltage threshold below the lowest of the two supplies.

The TCA9416 is part of the TI "Switch" type voltage translator family and employs key circuits to enable this voltage translation:

1. An N-channel pass-gate transistor topology that ties the A-port to the B-port.
2. Output rise time accelerator circuitry to detect and accelerate rising edges on the A or B ports
3. Output fall time accelerator circuitry to detect and accelerate falling edges on the A or B ports

For bidirectional voltage translation, pull up resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set to the lower supply voltage and can be represented with MIN(V_{CCA}, V_{CCB}).

The rise and fall time accelerator (RTA and FTA, respectively) circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the rise time accelerator (RTA) circuit turns on to increase the current drive capability of the driver. This edge-rate acceleration provides high ac drive by bypassing the internal 10-kΩ pull up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 150 Ω during this acceleration phase. During a high-to-low signal falling edge, the fall time accelerator (FTA) turns on to increase the current drive capability of the driver, similar to the rise time accelerator. This helps reduce the fall time for large capacitive loads. For light capacitive loads, the fall time accelerator will not enable.

Both the rise and fall time accelerators have logic to control the rate at which they turn on and off, in order to reduce ringing and over/undershoots.

8.3.2 Enable and Disable

The TCA9416 has an OE input that is used to disable the device by setting OE low, which prevents any signals from propagating across the device. This pin is referenced to the V_{CCA} supply. The rise and fall time accelerators are also disabled. Note that the internal pull up resistors will still be enabled if the supply is above V_{UVLO}. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

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8.3.3 Pull up resistors on I/O Lines

Each A-port I/O has an internal 10-kΩ pull up resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pull up resistor to V_{CCB}. If a smaller value of pull up resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors). However, adding lower value pull up resistors effects V_{OL} levels. It is recommended not to go below 1.5-kΩ. The internal pull ups of the TCA9416 are controlled by their respective supplies. The resistors have back-baising protection, so that if a supply is off, the current cannot flow through the resistors back into the supply. If a supply is above V_{UVLO_RISE}, the pull up resistor for its side is enabled.

8.4 Device Functional Modes

The TCA9416 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which disables the rise time and fall time accelerators, and prevents signals from propagating across the channels. The internal pull up resistors are not affected by the OE input. Setting the OE input high enables the device.

9 Application Information Disclaimer

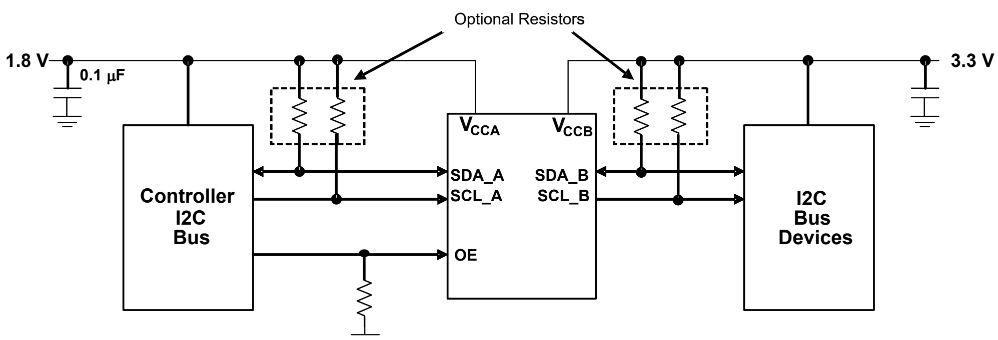
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TCA9416 can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. The primary target application use is for interfacing with open-drain drivers on the data I/Os such as I^2C or SMBus, where the data is bidirectional and no control signal is available.

9.2 Typical Application



OE is referenced to V_{CCA}

图 9-1. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.08 to 3.6 V
Output voltage range	1.08 to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TCA9416 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TCA9416 device is driving to determine the output voltage range
  - The TCA9416 device has 10-kΩ internal pull up resistors. External pull up resistors can be added to reduce the total RC of a signal trace if necessary.

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9.2.2.1 Startup Considerations with Large Capacitive Load Mismatches

Due to the FET based architecture of this translator, there are some considerations a system designer must be aware of during powering up with large differences in capacitance between the sides. If one supply with smaller capacitance is already powered up, and the other is ramping (with OE pin high), the side with the heavier load can ramp slower than the power supply ramp, due to only having an internal 10k pull up resistor. In this situation, once the rising POR threshold is met, the device enables all circuitry. If the heavy capacitance side has not yet risen above about 70% of supply, the device determins this as low, and briefly turns on the fall time accelerators to propagate a low. Once the fall time accelerator has timed out, the signals rise and sit idle high.

This phenomenom can be eliminated by holding the OE pin low (disabled) until all supplies and busses have ramped up, since this explicitly disables the bus acceleration circuitry until the bus has completed power up. Slower supply ramps also help reduce this since the bus voltage follows the supply closer if the ramp is slow.

9.2.3 Application Curve

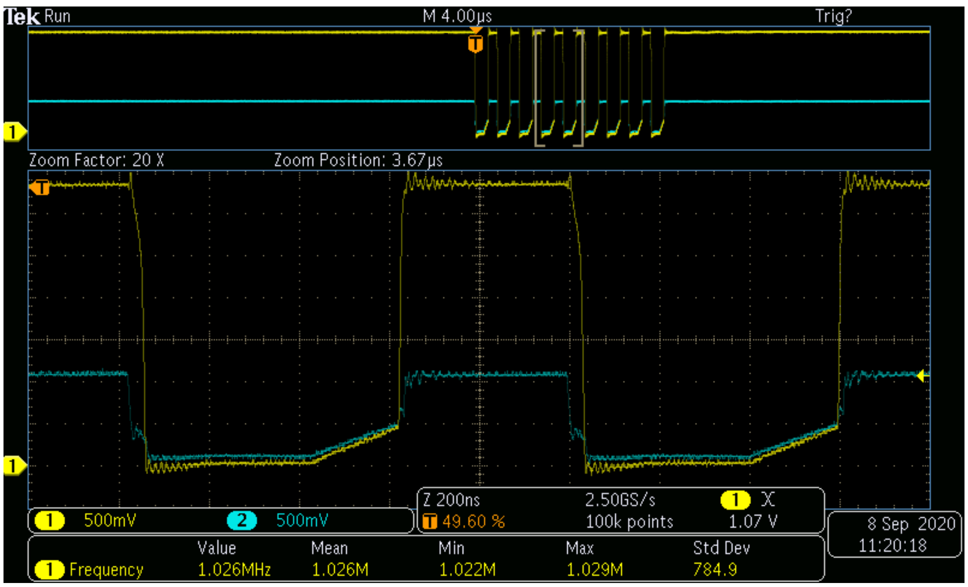

图 9-2. Level-Translation of a 1-MHz Signal

10 Power Supply Recommendations

The TCA9416 has no supply restrictions outside of the 1.08 V to 3.6 V range. V_{CCA} can be higher than or lower than V_{CCB}. The internal circuitry will select the appropriate supply automatically to correctly support translation. V_{CCA} can also be the same as V_{CCB}, and the device can be used as a buffer.

The sequencing of each power supply does not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that when the (OE) input is low, the outputs are disabled. No signals may propagate, and the rise time and fall time accelerators are disabled, but the internal pull up resistors will remain unaffected. To ensure that signals do not pass through during power up or power down, the OE input pin must be tied to GND through a pull down resistor and should not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. If OE is tied to V_{CCA}, this is OK, but might result in a glitch on the bus during power up depending on the capacitive load and ramp rates. The minimum value of the pull down resistor to ground is determined by the current-sourcing capability of the driver.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

1. Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA}, V_{CCB} pin, and G_{ND} pin.
2. Short trace lengths should be used to avoid excessive loading.
3. Keep SCL and SDA lengths close to prevent skewing the signals.
4. PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example

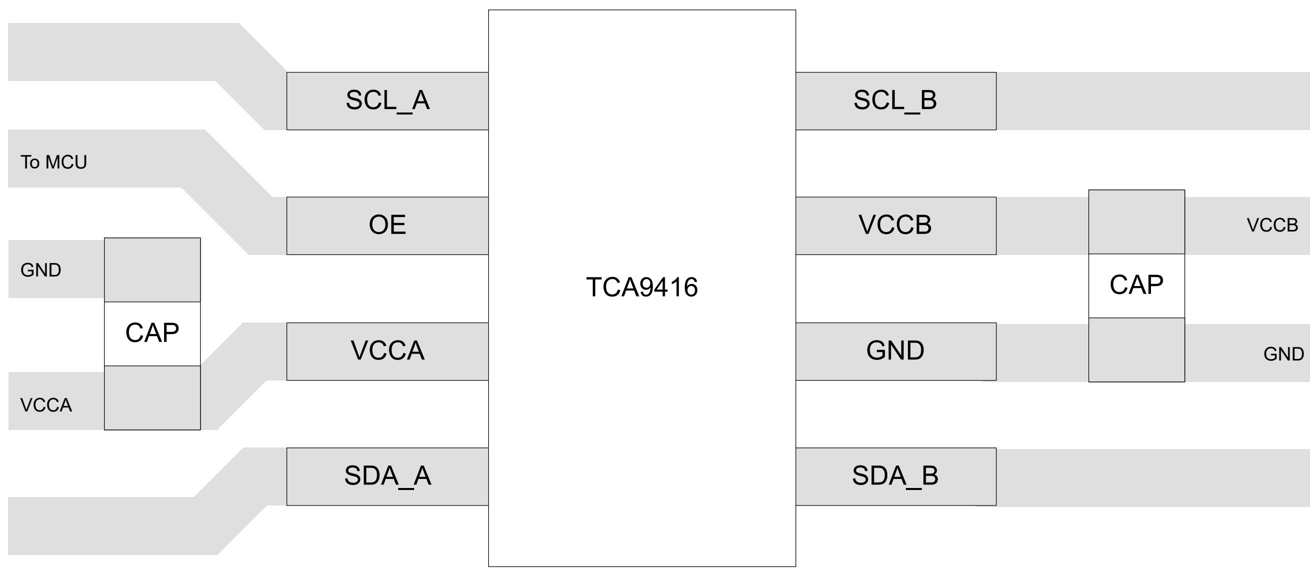

图 11-1. TCA9416 Layout Example (DDF)

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTCA9416DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples
PTCA9416DTMR	ACTIVE	X2SON	DTM	8	5000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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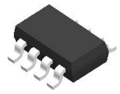
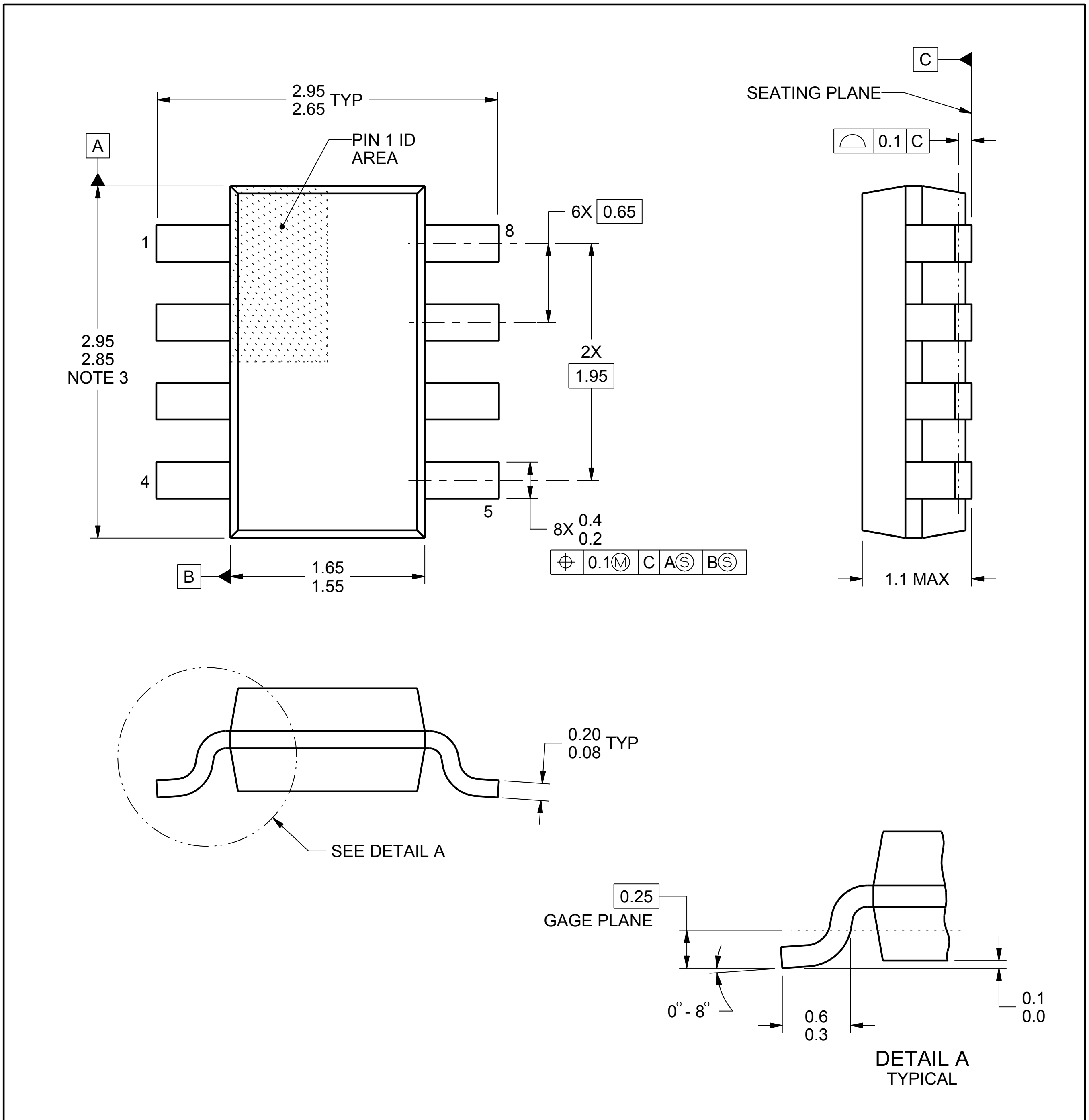
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



DDF0008A

SOT-23 - 1.1 mm max height

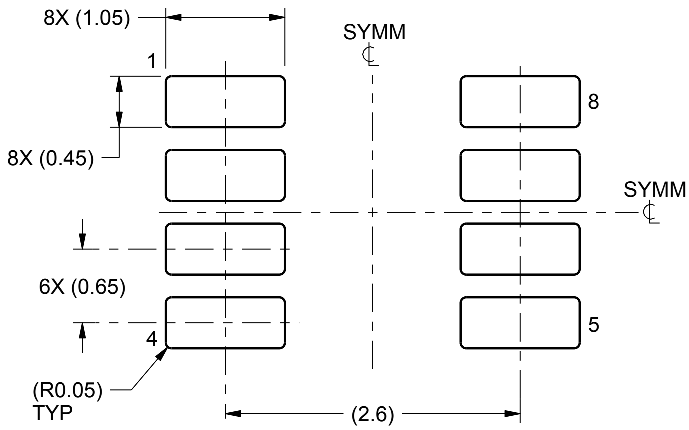
PLASTIC SMALL OUTLINE



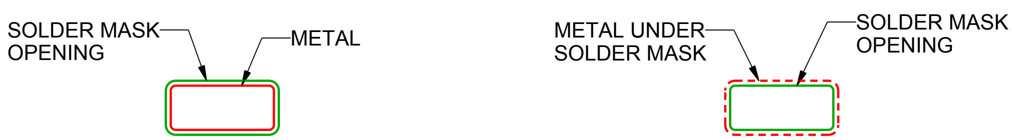
4222047/B 11/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

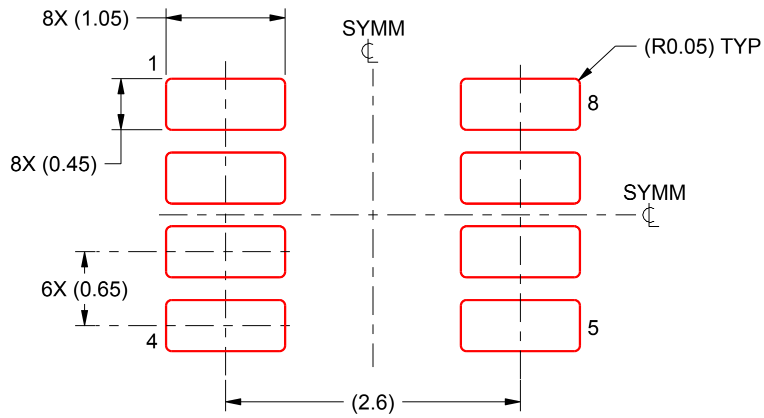
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

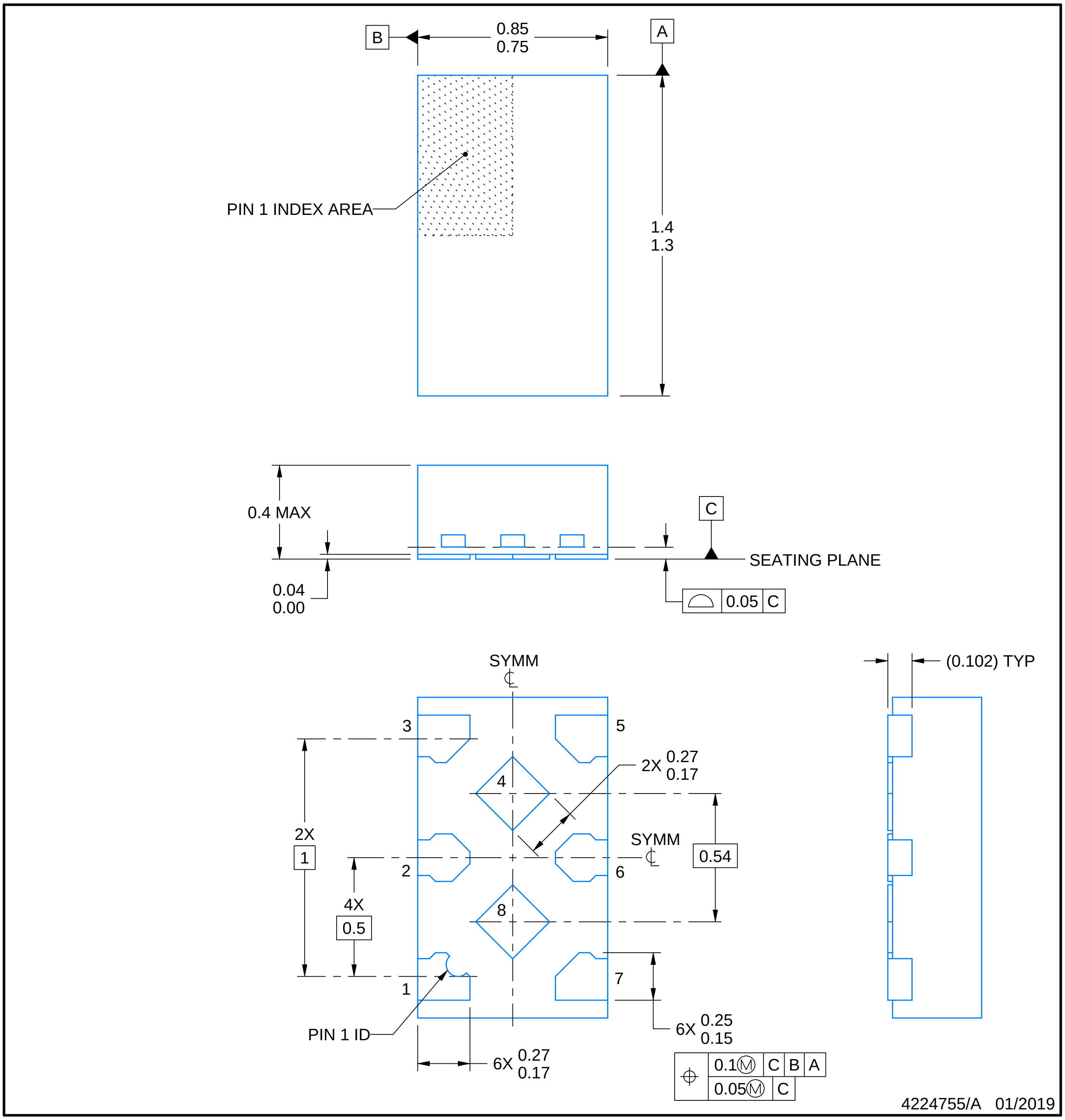
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

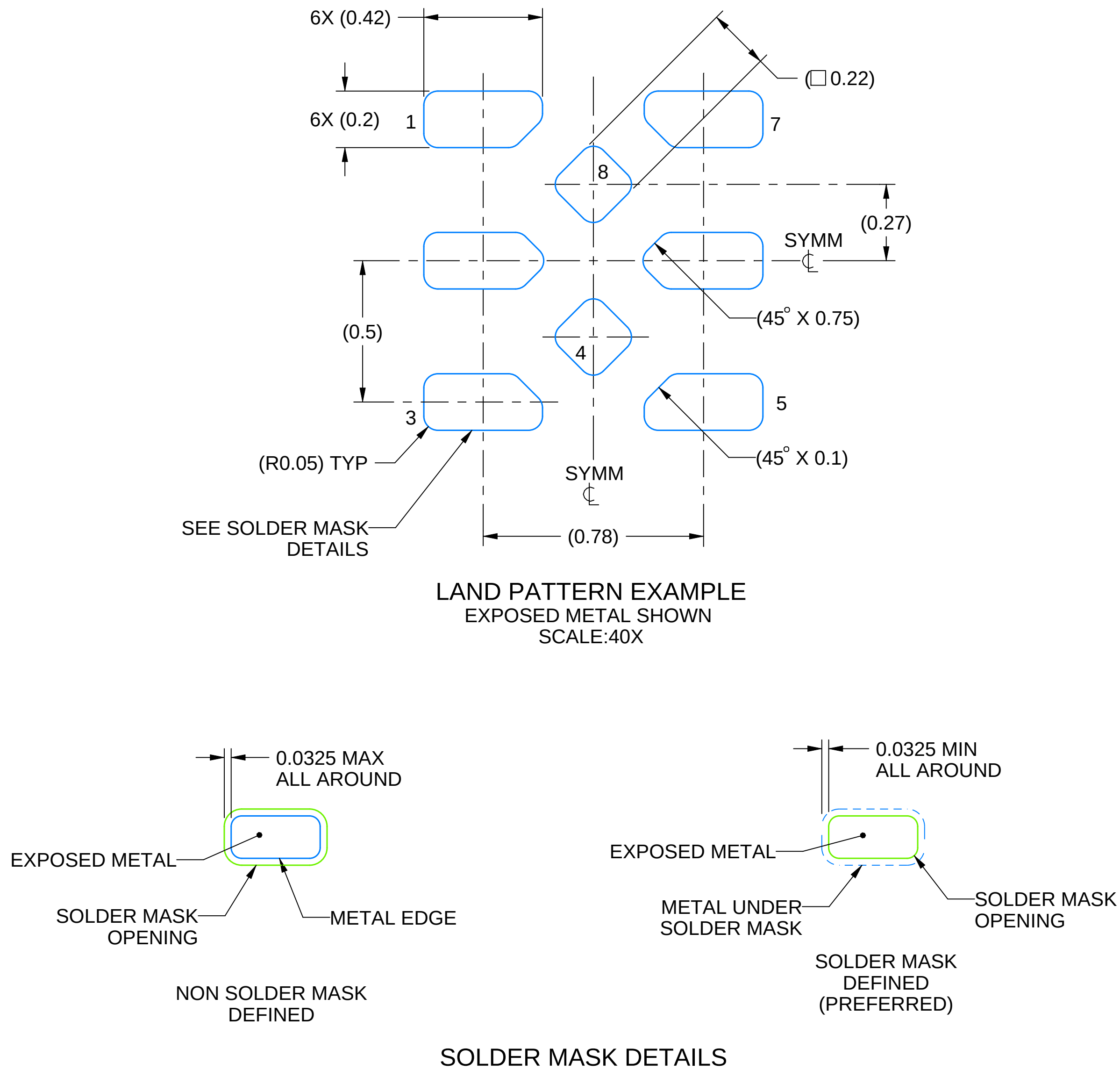
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

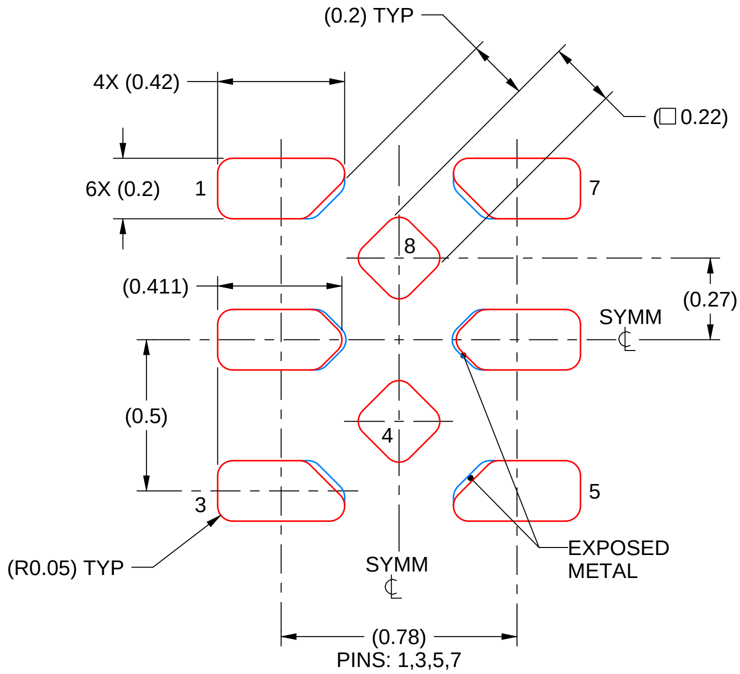
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad(s) must be soldered to the printed circuit board for thermal and mechanical performance.



4224755/A 01/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4224755/A 01/2019

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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