SN65LVDTxx 多通道 LVDS 收发器
SN65LVDT14 - 一个 LVDS 驱动器外加四个 LVDS 接收器
SN65LVDT41 - 四个 LVDS 驱动器外加一个 LVDS 接收器

1 特性

- 集成式标称 110Ω 接收器线路终端电阻
- 单个 3.3V 电源（3V 至 3.6V 的范围）
- 支持最低 250Mbps 的信号传输速率
- 直通引脚排列可简化 PCB 布局
- LVTTL 兼容型逻辑 I/O
- 超过 16KV 的总线引脚上的静电放电 (ESD) 保护
- LVDS 符合或超过 ANSI/TIA/EIA-644A 标准要求
- 20 针电源薄型缩小外形封装，26 密耳终端间距

2 应用

- LVDS Serial Peripheral Interface™(SPI) 允许主从设备间的长距离互联
- 板对板通信
- 测试和测量
- 电机驱动器
- LED 视频墙
- 无线基础设施
- 电信基础设施
- 机架式服务器

3 说明

SN65LVDTxx 器件属于多通道 LVDS 收发器，采用 LVDS 线路驱动器及接收器。SN65LVDTxx 器件支持最低 250Mbps 的信号传输速率，且该器件由单电源供电（典型值为 3.3V），采用 20 引脚 TSSOP 封装，可轻松进行 PCB 布局。

SN65LVDT14 及 SN65LVDT41 提供通用型、非对称性、双向通信功能，具有高抗扰度和低电磁干扰 (EMI) 等额外优点，并通过 LVDS 线路的使用增加了线缆长度。SN65LVDT14 及 SN65LVDT41 主要用于 LVDS 串行外设接口 应用。

SN65LVDT14 在一个封装内整合了一个 LVDS 线路驱动器和四个端接 LVDS 线路接收器。SN65LVDT14 可用于扩展长距离 SPI 等非对称型、双向接口，且应位于 SPI 从设备上。

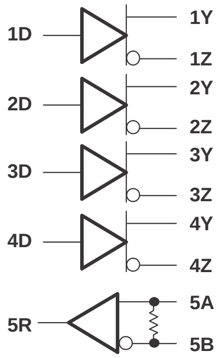
SN65LVDT41 在一个封装内整合了四个 LVDS 线路驱动器和一个端接 LVDS 线路接收器。SN65LVDT41 可用于扩展长距离 SPI 等非对称型、双向接口，且应位于 SPI 主设备上。

器件信息[1]

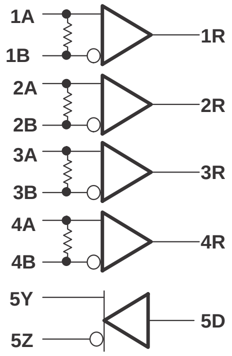
器件型号	封装	封装尺寸（标称值）
SN65LVDT14 SN65LVDT41	TSSOP (20)	6.50mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

SN65LVDT41 功能框图



SN65LVDT14 功能框图



English Data Sheet: SLLS530

目录

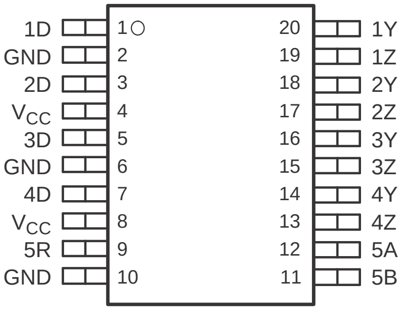
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (Feburary 2006) to Revision C	**Page**
• 添加了*器件信息* 表、*ESD 额定值* 表、*特性* *说明*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。	1
• 在数据表页面顶部添加了导航链接，并删除了 NRND 图标	1
• Moved power dissipation parameter to the *Absolute Maximum Ratings* table.	5

5 Pin Configuration and Functions

SN65LVDT41 PW Package
20-Pin TSSOP
Top View



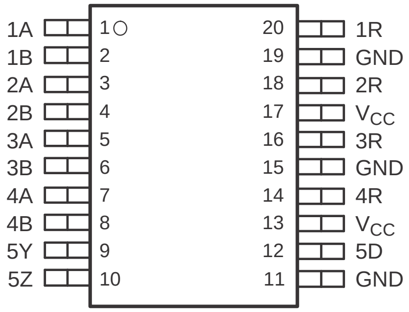
*marked as LVDT41

SN65LVDT41 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1D(1)	1	I	LVTTL Driver Input Pin
2D(1)	3		
3D(1)	5		
4D(1)	7		
1Y(1)	20	O	Noninverting LVDS Driver Output Pin
2Y(1)	18		
3Y(1)	16		
4Y(1)	14		
1Z(1)	19	O	Inverting LVDS Driver Output Pin
2Z(1)	17		
3Z(1)	15		
4Z(1)	13		
5R	9	O	LVTTL Receiver Output Pin
5A	12	I	Noninverting LVDS Receiver Input Pin
5B	11	I	Inverting LVDS Receiver Input Pin
V_{CC}	4, 8	I	Power Supply Pin, +3.3 V ± 0.3 V
GND	2, 6, 10	I	Ground Pin

(1) x = 1, 2, 3, 4 indicating channel number of SN65LVDT41

SN65LVDT14 PW Package
20-Pin TSSOP
Top View



*marked as LVDT14

SN65LVDT14 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A[(1)]	1	I	Noninverting LVDS Receiver Input Pin
2A[(1)]	3		
3A[(1)]	5		
4A[(1)]	7		
1B[(1)]	2	I	Inverting LVDS Receiver Input Pin
2B[(1)]	4		
3B[(1)]	6		
4B[(1)]	8		
1R[(1)]	20	O	LVTTL Receiver Output Pin
2R[(1)]	18		
3R[(1)]	16		
4R[(1)]	14		
5Y	9	I	Noninverting LVDS Driver Output Pin
5Z	10	I	Inverting LVDS Driver Output Pin
5D	12	O	LVTTL Driver Input Pin
GND	11, 15, 19	I	Ground Pin
V_{CC}	13, 17	I	Power Supply Pin, +3.3 V ± 0.3 V

(1) x = 1, 2, 3, 4 indicating channel number of SN65LVDT41

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage(2)	V_{CC}	–0.5	4	V
Input voltage	D or R	–0.5	6	V
	A, B, Y, or Z	–0.5	4	V
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
Continuous total power dissipation	T_A < 25°C power rating		774	mW
	T_A = 85°C power rating		402	
	Operating factor above T_A = 25°C		6.2	mW/°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except A, B, Y, Z, and GND(2)	±8000	V
			Pins A, B, Y, Z, and GND(3)	±16000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(4)(5)		±500	

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±8000 V may actually have higher performance.

(3) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±16000 V may actually have higher performance.

(4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

(5) Tested in accordance with JEDEC Standard 22, Test Method C101.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
$\lvert V_{ID} \rvert$	Magnitude of differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage, See Figure 1	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
				$V_{CC} - 0.8$	V
T_A	Operating free-air temperature	–40		85	°C

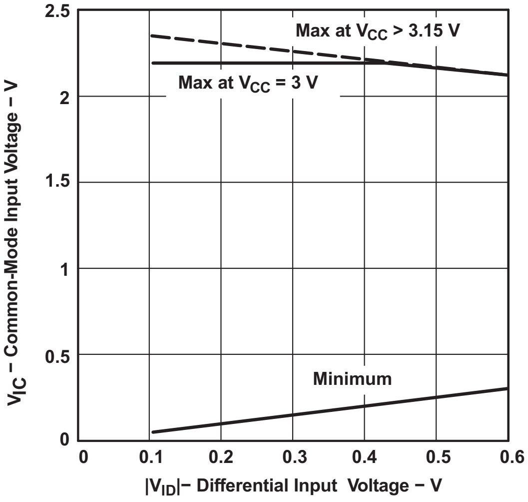


Figure 1. V_{IC} vs V_{ID} and V_{CC}

6.4 Thermal Information

THERMAL METRIC[1]		SN65LVDTxx	UNIT	
		PW (TSSOP)		
		20 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.9	°C/W	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.4	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	38.2	°C/W	
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W	
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Receiver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 8 and Table 1			100	mV
V_{ITH-}	Negative-going differential input voltage threshold		–100			
V_{OH}	High-level output voltage	I_{OH} = -8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B inputs)	V_I = 0 V and V_I = 2.4 V, other input open			±40	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0 V, V_I = 2.4 V			±40	µA
C_i	Input capacitance, A or B input to GND	$V_I = A \sin 2\pi ft + CV$		5		pF
Z_t	Termination impedance	V_{ID} = 0.4 sin2.5E09 t V	88		132	Ω

(1) All typical values are at 25°C and with a 3.3-V supply.

6.6 Driver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 9 and Figure 12	247	340	454	mV
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 13	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{IH}	High-level input current	V_{IH} = 2 V			20	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			10	μA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±24	mA
		V_{OD} = 0 V			±12	
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V			±1	μA

(1) All typical values are at 25°C and with a 3.3-V supply.

6.7 Device Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	SN65LVDT14	Driver R_L = 100 Ω, Driver V_I = 0.8 V or 2 V, Receiver V_I = ±0.4 V			25	mA
		SN65LVDT41				35	

(1) All typical values are at 25°C and with a 3.3-V supply.

6.8 Receiver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 11	1	2.6	3.8	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	2.6	3.8	ns
t_r	Output signal rise time		0.15		1.2	ns
t_f	Output signal fall time		0.15		1.2	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL}$ - $t_{PLH}\rvert$)			150	600	ps
$t_{sk(o)}$	Output skew(1)			100	400	ps
$t_{sk(pp)}$	Part-to-part skew(2)				1	ns

(1) $t_{sk(o)}$ is the magnitude of the time difference between the t_{pLH} or t_{pHL} of all the receivers of a single device with all of their inputs connected together.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.9 Driver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 14	0.9	1.7	2.9	ns
t_{PHL}	Propagation delay time, high-to-low-level output		0.9	1.6	2.9	
t_r	Differential output signal rise time		0.26		1	
t_f	Differential output signal fall time		0.26		1	

Driver Switching Characteristics (continued)

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{sk(p)}$	Pulse skew ($\|t_{PHL}$ - $t_{PLH}\|$)	R_L = 100 Ω, C_L = 10 pF, See Figure 14		150	500	ps
$t_{sk(o)}$	Output skew(1)			80	150	ps
$t_{sk(pp)}$	Part-to-part skew(2)				1.5	ns

(1) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.10 Typical Characteristics

6.10.1 Receiver

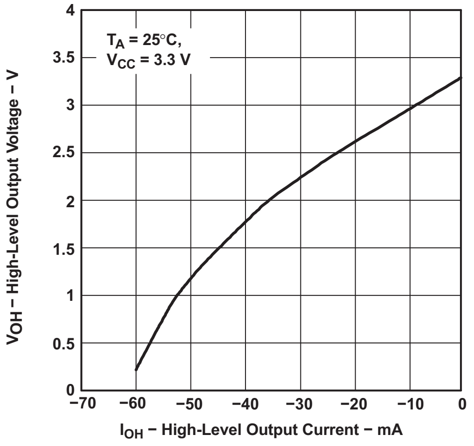


Figure 2. High-Level Output Voltage vs High-Level Output Current

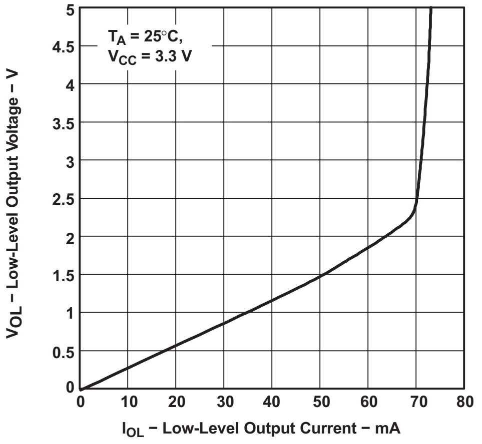


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

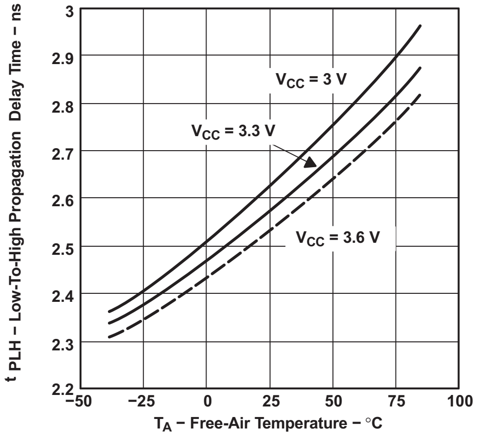


Figure 4. Low-to-High Propagation Delay Time Vs Free-Air Temperature

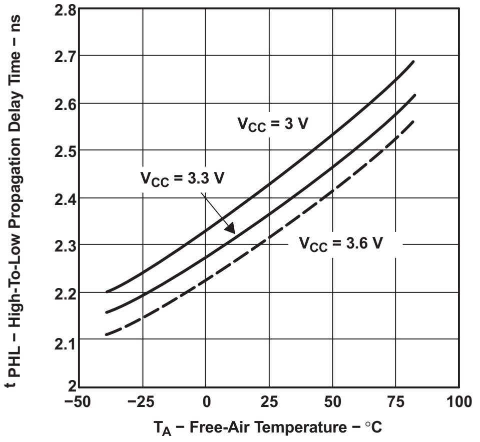


Figure 5. High-to-Low Propagation Delay Time vs Free-Air Temperature

6.10.2 Driver

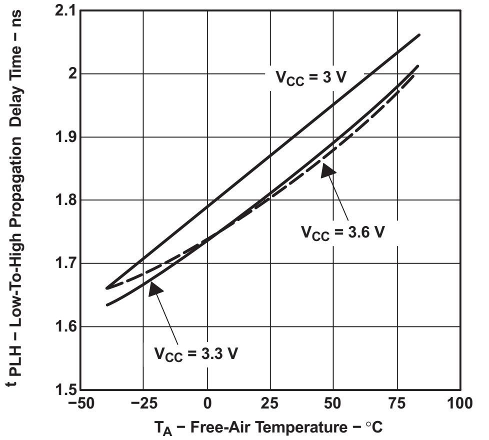


Figure 6. Low-to-High Propagation Delay Time vs Free-Air Temperature

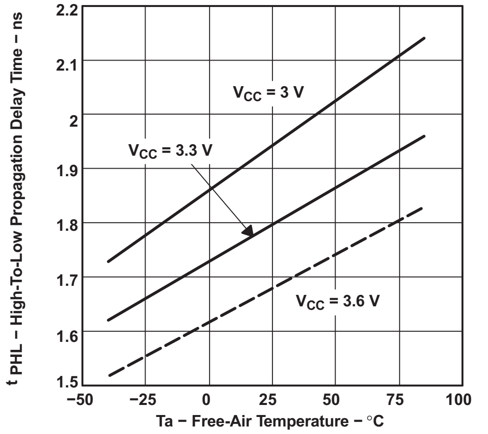


Figure 7. High-to-Low Propagation Delay Time vs Free-Air Temperature

7 Parameter Measurement Information

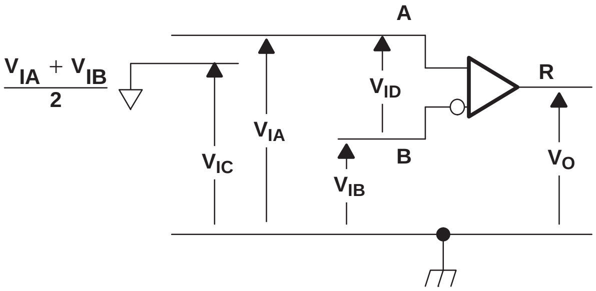


Figure 8. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0.0 V	100 mV	0.05 V
0.0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0.0 V	600 mV	0.3 V
0.0 V	0.6 V	–600 mV	0.3 V

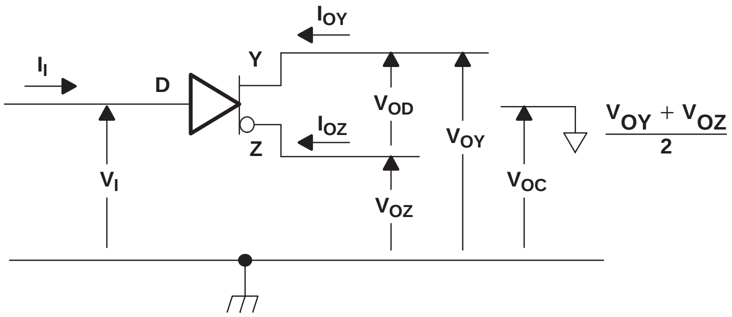


Figure 9. Driver Voltage and Current Definitions

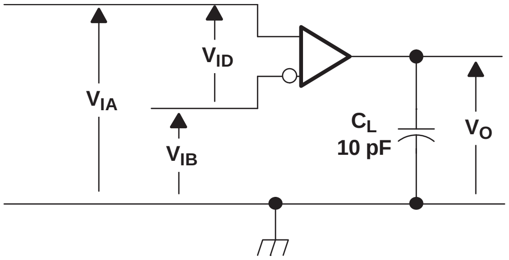
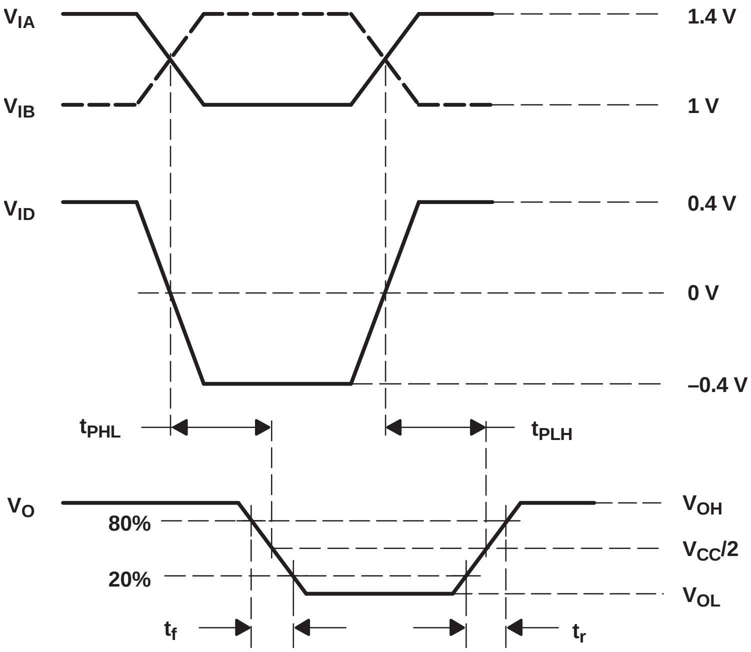


Figure 10. Receiver Timing Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ± 0.05 µs. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 11. Receiver Timing Test Circuit Waveforms

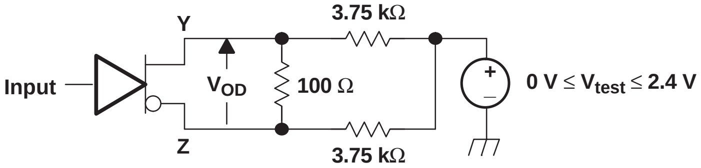
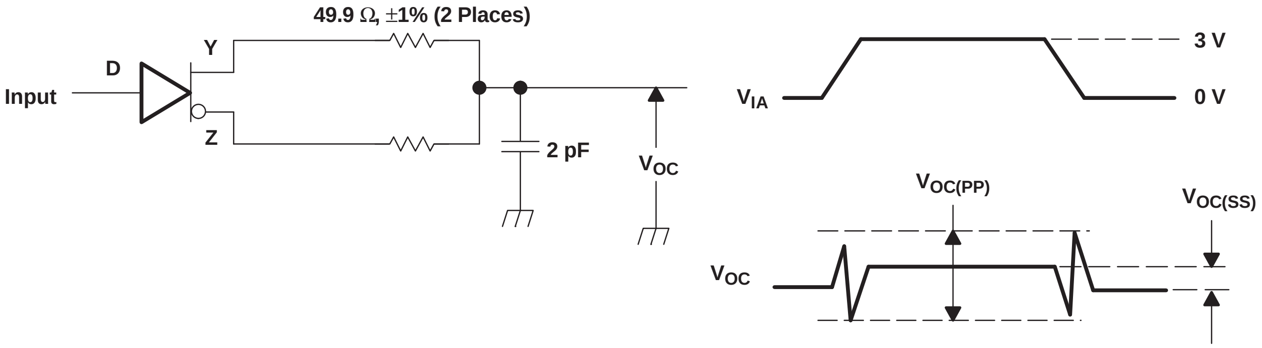
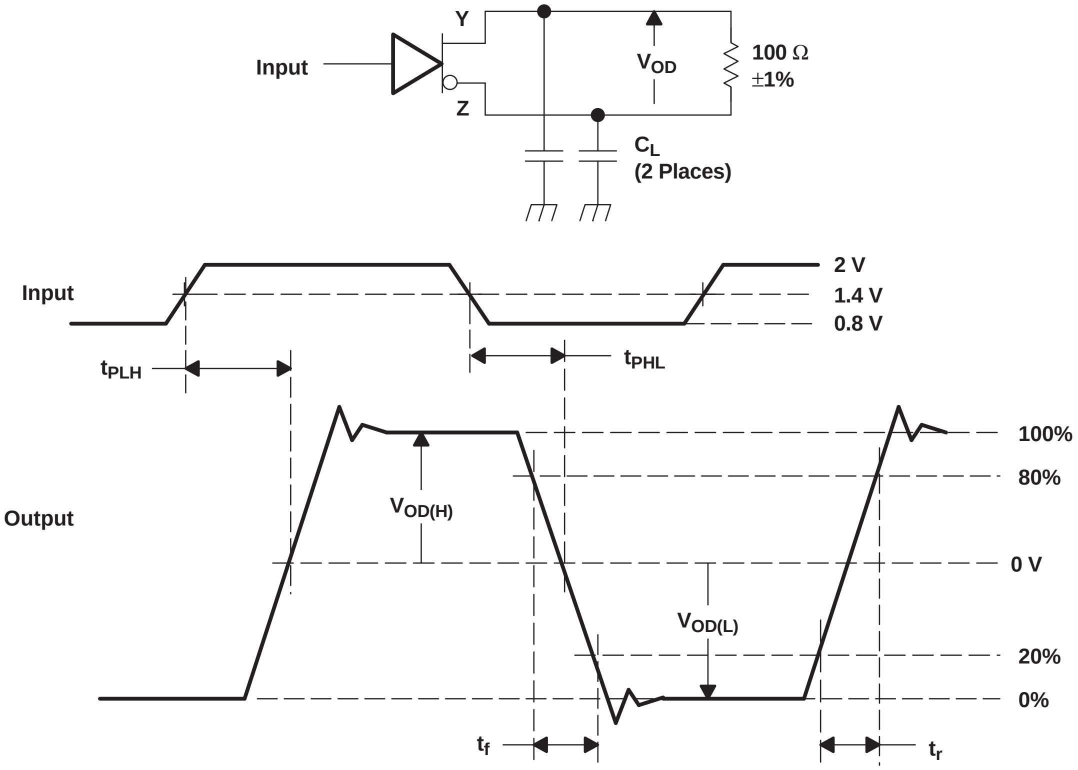


Figure 12. Driver VDO Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 1 GHz.

Figure 13. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ± 0.05 µs. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

Figure 14. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

8 Detailed Description

8.1 Overview

The SN65LVDTxx integrates both low-voltage differential signaling (LVDS) line drivers, with a balanced current source design, and LVDS line receivers into a single package. This device operates from a single supply that is nominally 3.3 V, but the supply can be as low as 3 V and as high as 3.6 V. The input to the SN65LVDTxx LVDS drivers is a LVCMOS/LVTTL signal, and the output is a differential signal complying with the LVDS standard (TIA/EIA-644). The input to the SN65LVDTxx LVDS receivers is a differential signal complying with the LVDS Standard (TIA/EIA-644), and the output is a 3.3-V LVCMOS/LVTTL signal. The differential output signal of the SN65LVDTxx LVDS line drivers operates with a signal level of 350 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in low electromagnetic interference (EMI). The differential input signal of the SN65LVDTxx LVDS line receivers operates with a signal level of 350 mV, nominally, at a common-mode voltage of 1.2 V. The differential nature of the LVDS outputs and inputs can provide immunity to common-mode coupled signals (noise) that the driven/received signal may experience, along with a low EMI solution.

The SN65LVDTxx can be used to extend asymmetric bidirectional interface buses. The SN65LVDT41 combines four LVDS line drivers with a single terminated LVDS line receiver in one package, and the SN65LVDT14 combines one LVDS line driver with four terminated LVDS line receivers in one package. The SN65LVDTxx can be used to extend asymmetric bidirectional interface buses, such as Serial peripheral interface (SPI) over LVDS, to achieve long-distance and low-cost SPI communication.

The SN65LVDTxx is primarily used in point-to-point configurations, as seen in Figure 19. This configuration provides a clean signaling environment for the fast edge rates of the SN65LVDTxx and other LVDS components. The SN65LVDTxx should be connected through a balanced media, which could be a standard twisted pair cable, a parallel pair cable, or simply PCB traces to a LVDS receiver. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. The SN65LVDTxx device is intended to drive a 100-Ω transmission line. The 100-Ω termination resistor is selected to match the media and is located as close to the LVDS receiver input pins as possible.

8.2 Functional Block Diagram

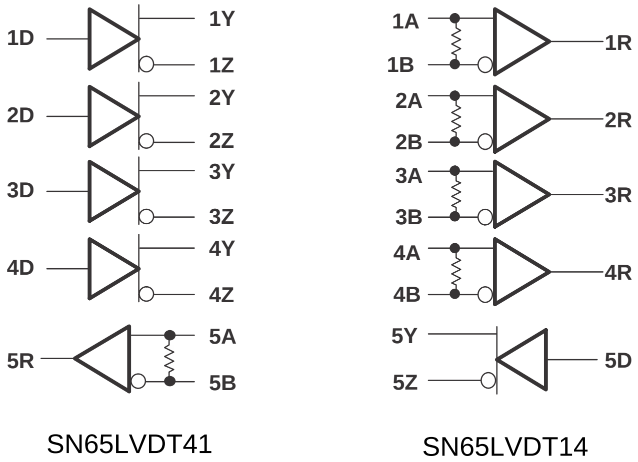


Figure 15. SN65LVDT41 (left) and SN65LVDT14 (Right) Functional Diagram

8.3 Feature Description

8.3.1 SN65LVDTxx Driver and Receiver Functionality

Table 2 shows how the LVDS receiver differential input to single-ended output relationship is defined for SN65LVDTxx. The SN65LVDTxx receiver is capable of detecting signals as low as 100 mV over a ±1-V common-mode range centered around 1.2 V.

Feature Description (continued)

Table 2. SN65LVDTxx Receiver Functionalty

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

Table 3 shows how the LVDS driver single-ended input to differential output relationship is defined for SN65LVDTxx.

Table 3. SN65LVDTxx Receiver Functionality

INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

8.3.2 Integrated Termination

SN65LVDTxx integrates termination resistors for the LVDS receiver internal to the device. The resistor value will be between 88 Ω and 132 Ω. Additional termination resistors are not required on the receiver inputs of SN65LVDTxx.

8.3.3 SN65LVDTxx Equivalent Circuits

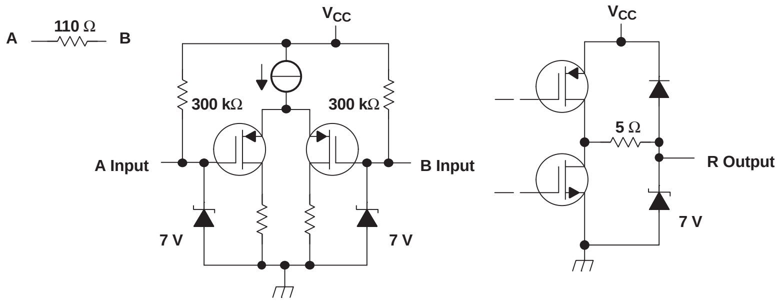


Figure 16. Receiver Equivalent Input and Output Schematic Diagrams

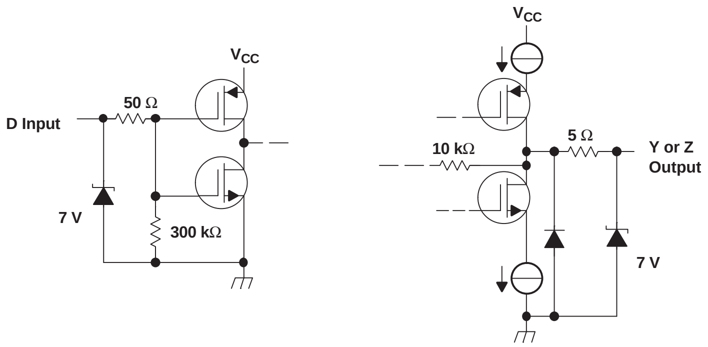


Figure 17. Driver Equivalent Input and Output Schematic Diagrams

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65LVDTxx devices are multi-channel LVDS driver and receiver pairs. The functionality of this device is simple yet extremely flexible, leading to its use in designs ranging from test and measurement to LED video wall. The varied class of potential applications share features and applications discussed in the paragraphs below.

9.1.1 Extending a Serial Peripheral Interface Using LVDS Signaling Over Differential Transmission Cables

Serial Peripheral Interface (SPI) is found in numerous applications as the communication method between processor and peripheral devices using single-ended signals over short distances. However, there is increasing demand for longer range SPI communication on the same PCB or from board to board. As distance increases, external noise, and electromagnetic interference (EMI) with single-ended SPI signals becomes an issue. Furthermore, increased distance limits the data rate due to propagation delay, and affects the signal quality due to potential ground shift between boards. A long distance SPI communication is achievable with the help of LVDS. LVDS, as specified by the TIA/EIA-644-A standard, provides several benefits when compared to alternative long-distance signaling technologies: low EMI, high noise immunity, low power consumption, and inexpensive interconnect cables.

SPI operates in a master-slave architecture, with four unidirectional signal lines. The master supplies data named Master-Out-Slave-In (MOSI), a clock (SCK), and a optional Chip Select (CS) signal to control the operation of the system with multiple slave devices. The MOSI,SCLK, and $\overline{\text{CS}}$ signals are unidirectional from the master device to slave devices. The serial data from slave to master device is a unidirectional signal named Master-In-Slave-Out (MISO). The flow of data can be seen in Figure 18.

SN65LVDT14 and SN65LVDT41 provide the necessary LVDS drivers and receivers specifically targeted at implementing a long distance SPI application. It uses the unidrectional links for the MOSI, MISO, SCK, and CS signals and converts the single-ended data into a unidirectional LVDS links.SN65LVDT41 combines four LVDS line drivers with a single terminated LVDS line receiver in one package should be located at the SPI master device. SN65LVDT14 combines one LVDS line driver with four terminated LVDS line receivers in one package and should be located at the SPI device.

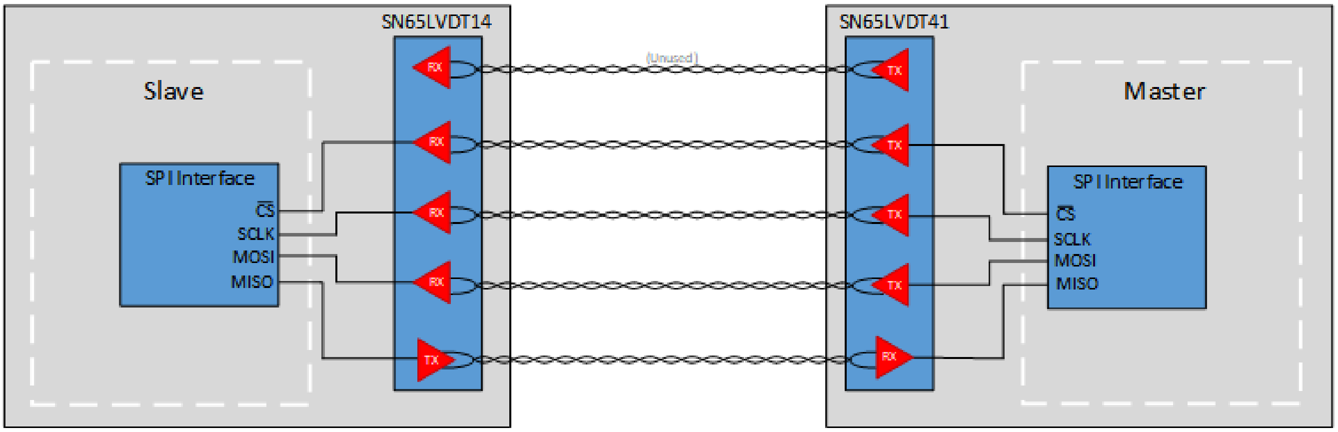


Figure 18. Typical SPI Application With LVDS

Table 4. SPI Design Parameters

Design Parameter	Example Value
Supply Voltage (V_{DD})	3 to 3.6 V
Single-ended Input Voltage	0 to V_{DD}
SPI Data Rate	0 to 10 Mbps
Interconnect Characteristic Impedance	100 Ω
Number of LVDS Channel	4
Number of Transmitter Nodes	3
Number of Receiver Nodes	1
Ground shift between driver and receiver	±1 V

9.2 Typical Application

Point-to-Point applications provide a clean signaling environment for the fast edge rates of the SN65LVDTxx and other LVDS components. The SN65LVDTxx is connected through a balanced media which may be a standard twisted-pair cable, a parallel pair cable, or simply PCB traces to a LVDS receiver. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. The SN65LVDTxx device is intended to drive a 100-Ω transmission line. The 100-Ω termination resistor is selected to match the media and is located as close to the LVDS receiver input pins as possible.

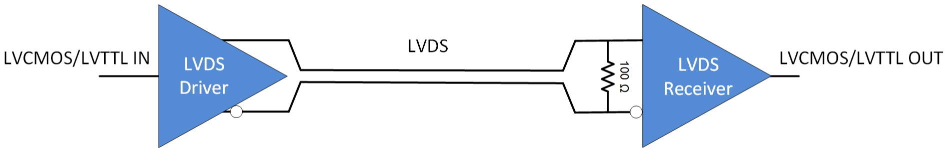


Figure 19. Typical LVDS Point-to-Point Application

9.2.1 Design Requirements

Table 5 lists the design parameters for typical point-to-point applications.

Table 5. Typical Design Parameters

Design Parameter	Example Value
Supply Voltage (V_{DD})	3 to 3.6 V
Single-ended Input Voltage	0 to V_{DD}
Data Rate	0 to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Number of LVDS Channel	5
Number of Receiver/Transmitter Nodes	5
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 SPI Propagation Delay Limitations

In typical SPI communication, the SPI master decides the sampling rate and data transfer rate, sends data at the rising edge of one clock cycle, and receives data on the falling edge within the same clock cycle. In a low latency system, the data in peripheral device should be made available to the host system with minimum delay. However in systems with high latency, the total round trip propagation delay of the SPI system must be less than half the SCLK period to avoid missing bits. There are three major delay contributors in a typical system—the SPI peripheral, data link device, and transmission media. Both the SPI peripheral and the data link device have fixed delay. The delay in transmission media, however, increases as communication distance increases. The relationship between cable length and SPI clock frequency can be seen in Figure 22. Figure 22 refers to a system where both MISO and MOSI are used, accounting for the case of slave-to-mater data transmission, including roundtrip delay. The specific setup is described in *Extending SPI and McBSP with differential interface products* (SLLA142)

9.2.2.2 Interconnecting Media

The physical communication channel between the LVDS driver and the LVDS receiver may be any balanced and paired metal conductors meeting the requirements of the LVDS standard, the key points of which are included here. This media may be shielded twisted-pair cables, twinax cables, flat ribbon cables, or PCB traces. The nominal characteristic impedance of the interconnect media should be between 100 Ω and 120 Ω with a variation of no more than 10% (90 Ω to 132 Ω). Balanced cables (for example, twisted-pair) are usually better than unbalanced cables (like ribbon and simple coax cables) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field-canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver. There should not introduce major impedance discontinuities in the system.

9.2.2.3 Input Fail-Safe Biasing

External pullup and pulldown resistors may be used to provide enough of an offset to enable an input fail-safe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD through a pullup resistor and the negative LVDS input pin is tied to GND by a pulldown resistor. The pullup and pulldown resistors should be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry. Refer to application note *AN-1194 Fail-safe biasing of LVDS interfaces* (SNLA051) for more information.

9.2.2.4 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high-frequency, ceramic (surface mount is recommended), 0.1-μF and 0.001-μF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin.

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to μF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by Equation 1 and Equation 2 according to Johnson(1) equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV. However, this figure varies depending on the noise budget available in the design. (1)

$$C_{\text{chip}} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \tag{1}$$

$$C_{\text{LVDS}} = \left(\frac{1\text{A}}{0.2\text{V}} \right) \times 200\ \text{ps} = 0.001\ \mu\text{F} \tag{2}$$

Figure 20 lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 μF) and the value of capacitance found above (0.001 μF). TI recommends that the user place the smallest value of capacitance as close to the chip as possible.

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(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

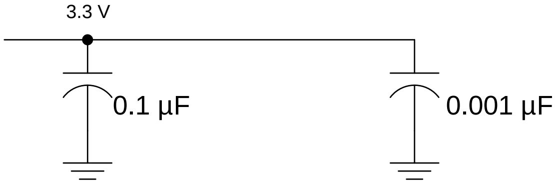

Figure 20. Recommended LVDS Bypass Capacitor Layout

9.2.2.5 *PCB Transmission Lines*

As per the *LVDS owner's manual design guide, 4th edition* (SNLA187), Figure 21 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and return path with a uniform cross section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 21 shows examples of edge-coupled microstrip lines, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent (like if S is less than 2 W, for example), the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

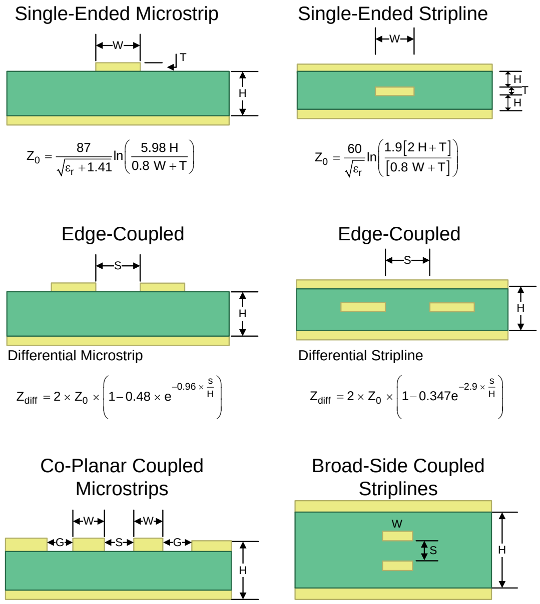

Figure 21. Controlled-Impedance Transmission Lines

9.2.2.6 *Probing LVDS Transmission Lines on PCB*

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will skew results.

9.2.3 Application Curve

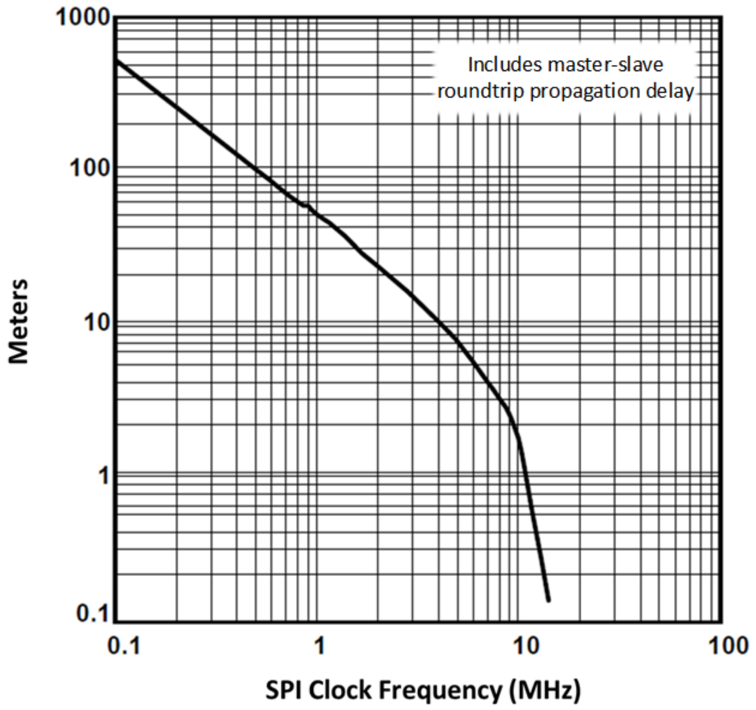

Figure 22. SN65LVDTxx SPI Performance: Cable Length vs SPI Clock

10 Power Supply Recommendations

The SN65LVDTxx devices are designed to operate from a single power supply with a supply voltage range of 3 V to 3.6 V. In a typical point-to-point application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the driver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per the *LVDS application and data handbook* (SLLD009), printed-circuit boards usually offer designers two transmission line options: microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 23.

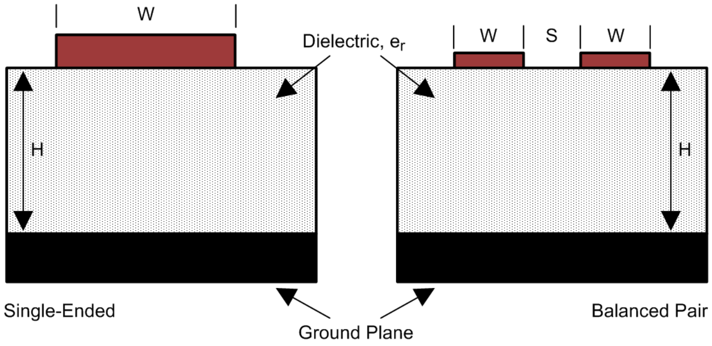

Figure 23. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines when possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1(2), 2(3), and 3(4) provide formulas for Z_O and t_{PD} for differential and single-ended traces. (2) (3) (4)

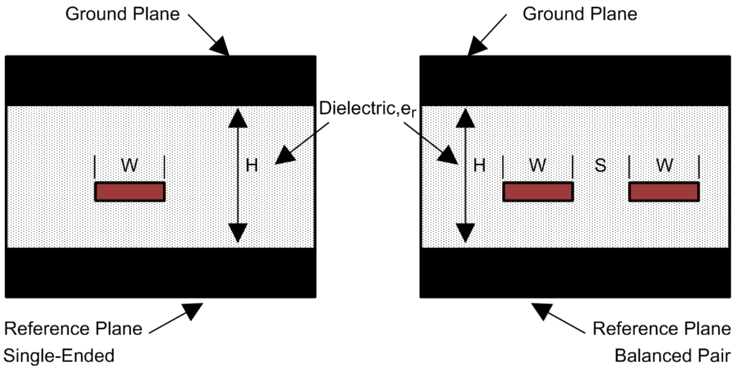

Figure 24. Stripline Topology

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(2) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(3) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(4) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or an equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of LVCMOS/LVTTL signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13, may be desired. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the designer must decide how many levels to use in the stack. To reduce the LVCMOS/LVTTL to LVDS crosstalk, it is good practice to have at least two separate signal planes as shown in Figure 25.

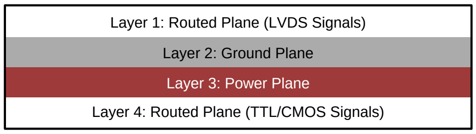


Figure 25. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 26.

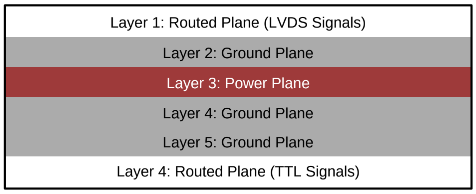


Figure 26. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity, but fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors, but the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

Layout Guidelines (continued)

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

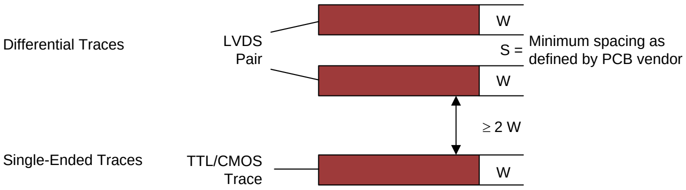


Figure 27. 3-W Rule for Single-Ended and Differential Traces (Top View)

Exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close to its originating trace as possible. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. TI recommends that the user place a via immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

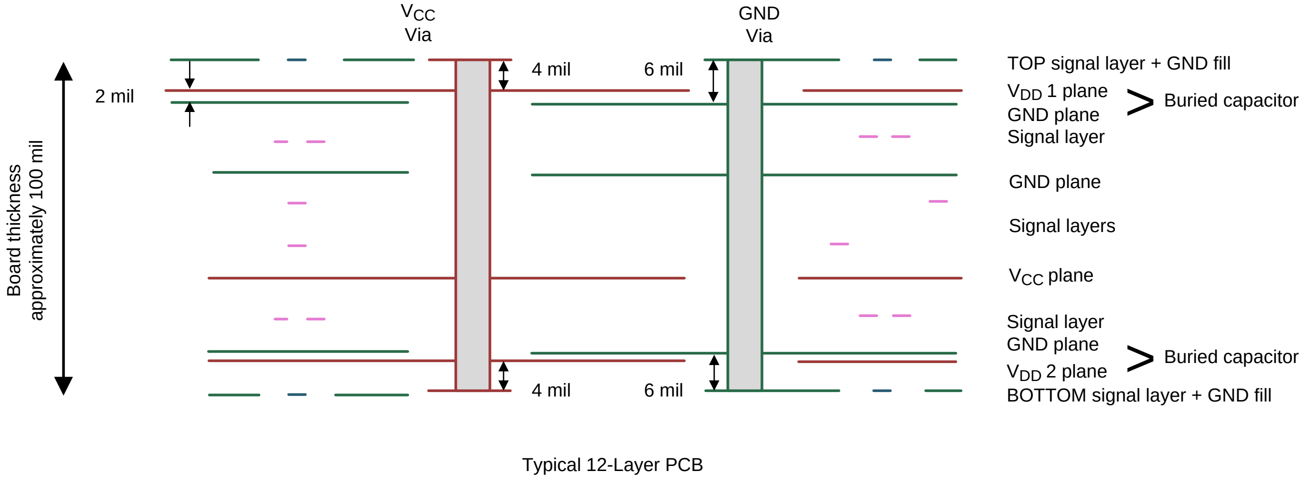


Figure 28. Low Inductance, High-Capacitance Power Connection

Layout Guidelines (continued)

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 29(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μF, and 0.1 μF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 21 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 21) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in Figure 29(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

(a) (b)

Figure 29. Typical Decoupling Capacitor Layouts

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 30.

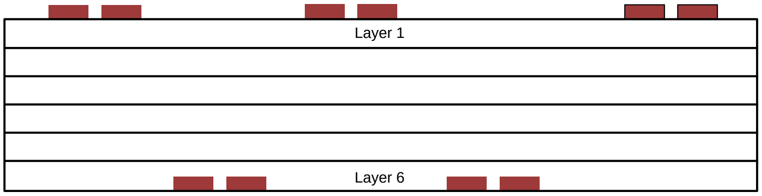


Figure 30. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers. Thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 31. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

Layout Guidelines (continued)

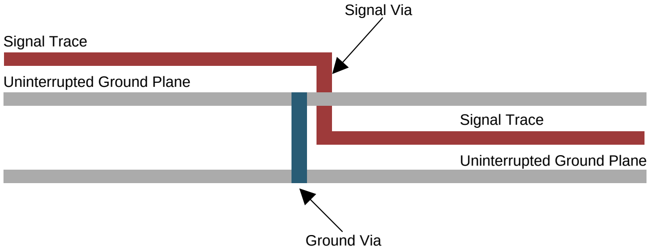


Figure 31. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

11.2 Layout Examples

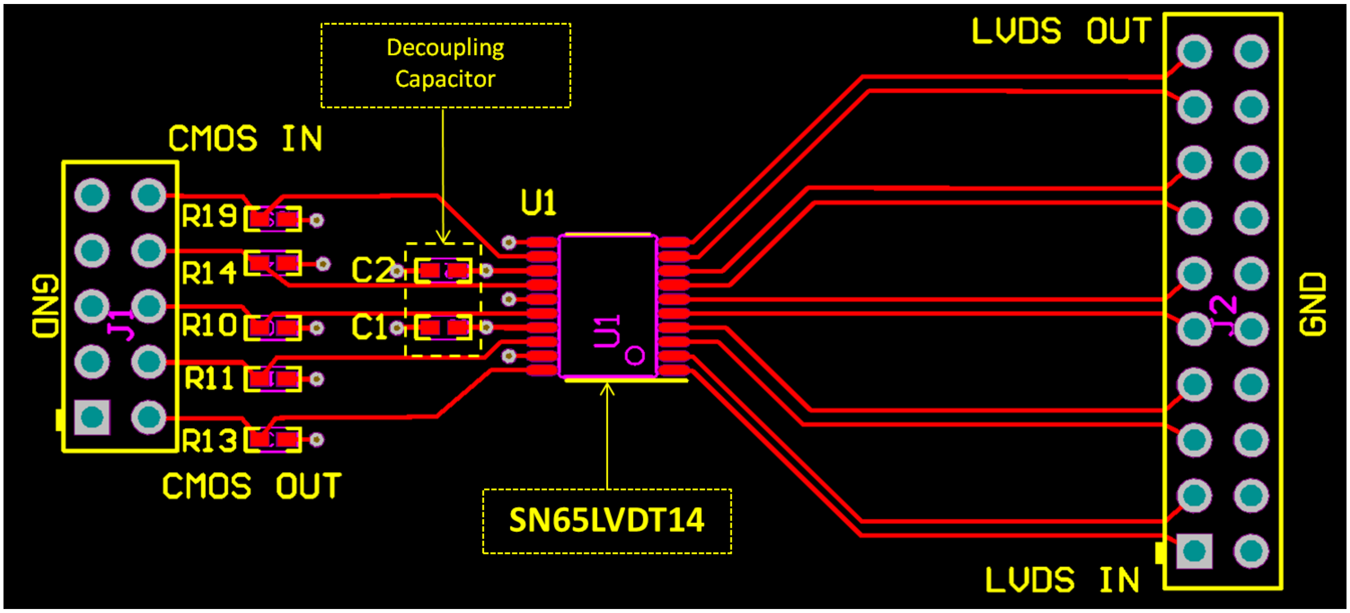


Figure 32. Example SN65LVDT14 Layout

Layout Examples (接下页)

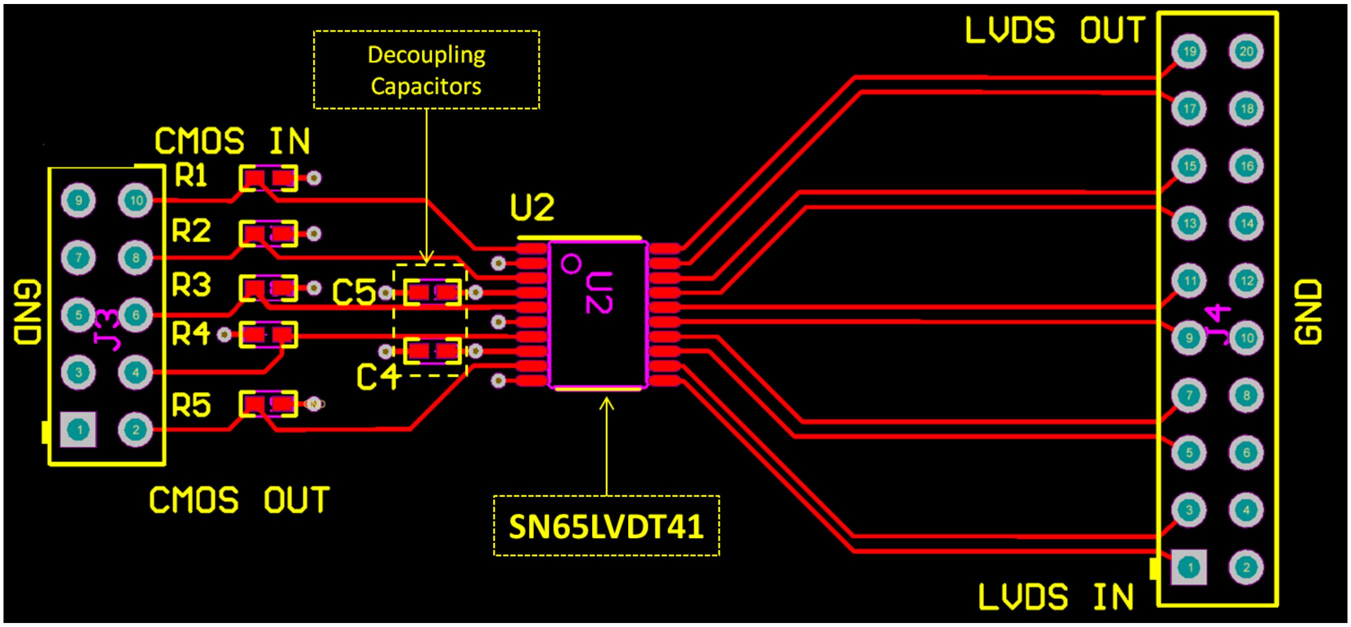


Figure 33. Example SN65LVDT41

12 器件和文档支持

12.1 相关文档

请参阅如下相关文档：

- *《LVDS 用户手册》*(SNLA187)
- *《AN-808 长距离传输与数据信号质量》*(SNLA028)
- *《AN-977 LVDS 信号质量：使用眼图测量抖动测试报告 #1》*(SNLA166)
- *《AN-971 LVDS 技术概览》*(SNLA165)
- *《AN-916 线缆选择实用指南》*(SNLA219)
- *《AN-805 差分线路驱动器的功耗计算》*(SNOA233)
- *《AN-903 差分终端技术比较》*(SNLA034)
- *《AN-1194 LVDS 接口的失效防护偏置》*(SNLA051)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **6.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
SN65LVDT14	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
SN65LVDT41	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.
LVDS Serial Peripheral Interface is a trademark of Motorola.
Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDT14PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT14	Samples
SN65LVDT14PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT14	Samples
SN65LVDT14PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT14	Samples
SN65LVDT14PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT14	Samples
SN65LVDT41PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT41	Samples
SN65LVDT41PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT41	Samples
SN65LVDT41PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT41	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

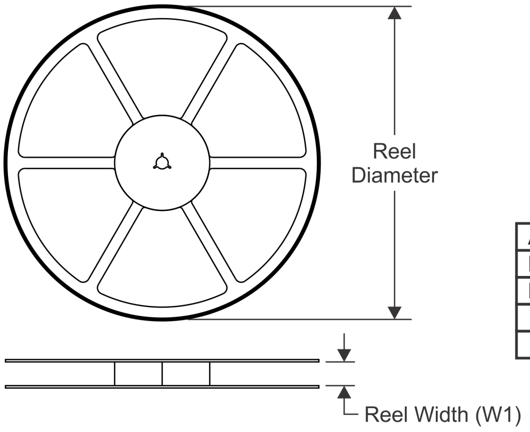
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

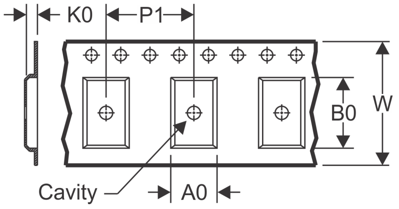
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

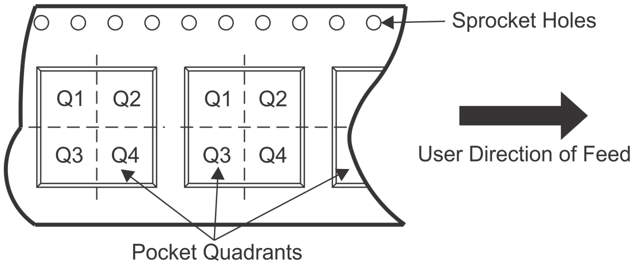


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

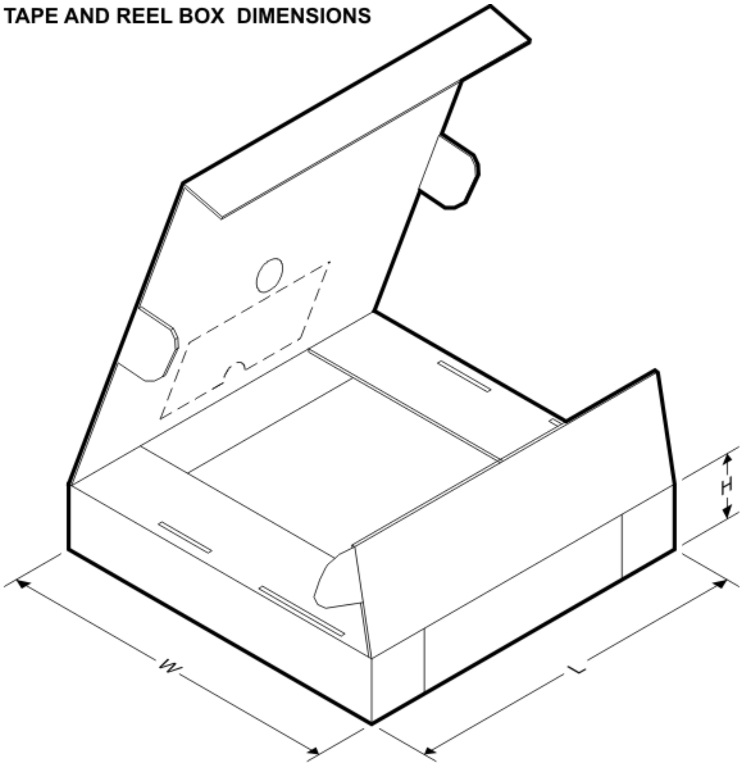


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDT14PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN65LVDT41PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

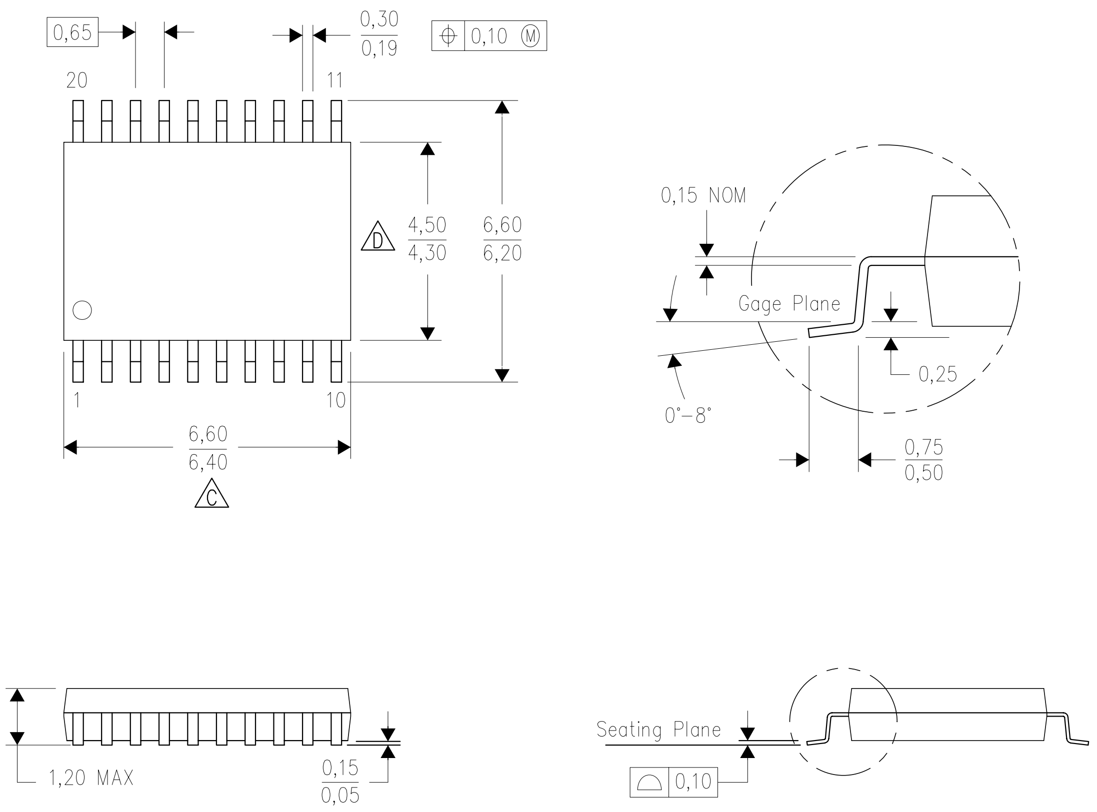
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDT14PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN65LVDT41PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



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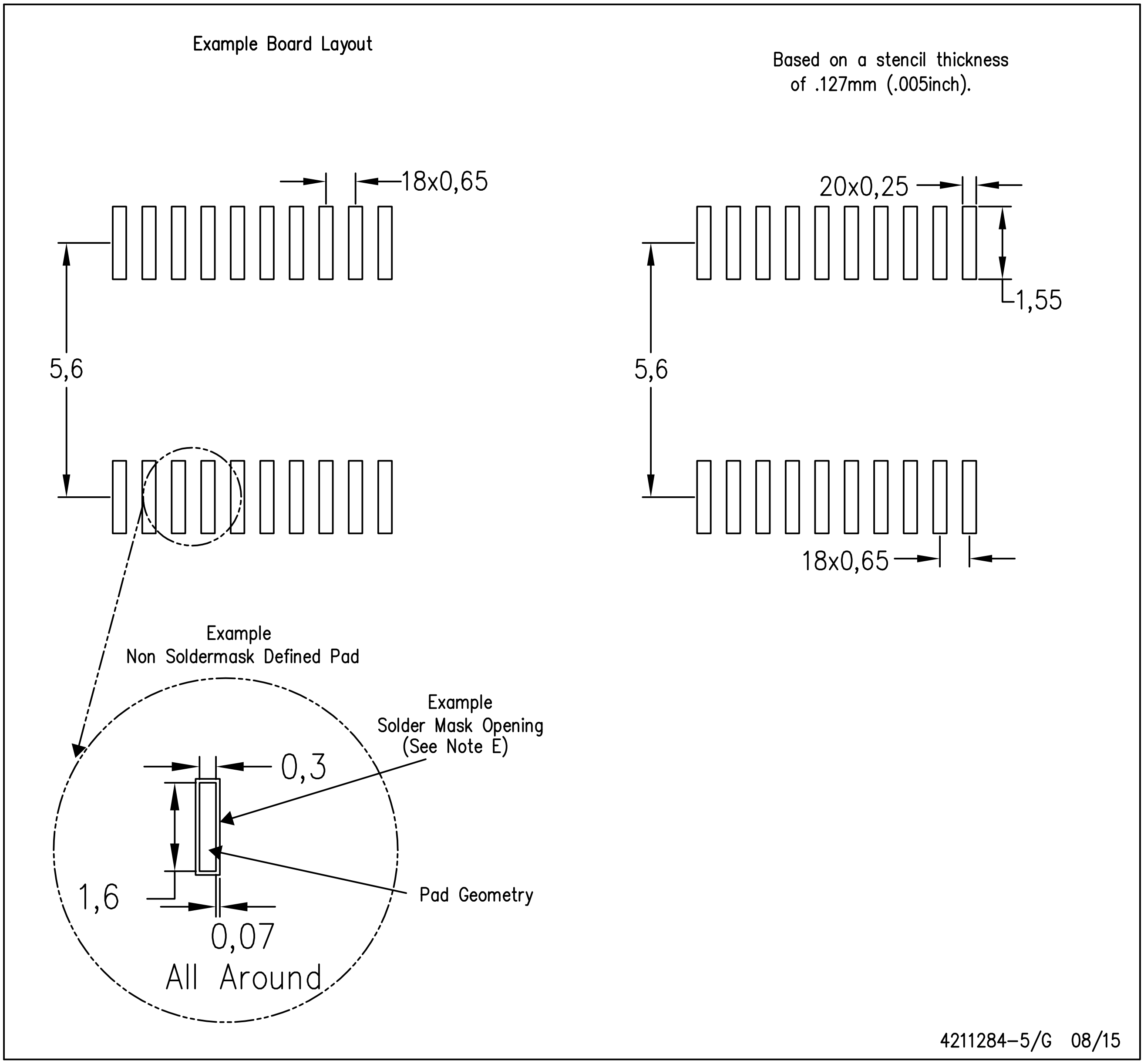
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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