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ZHCSA21C - FEBRUARY 2013 - REVISED DECEMBER 2014

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2.2

#### ADS1293 用于生理信号测量的低功耗、 24 位模拟前端 3通道、

Technical

Documents

# 1 特性

- 三个具有同步起搏输出的高分辨率数字心电图 (ECG) 通道
- 抗电磁干扰 (EMI) 输入
- 低功耗:每通道 0.3mW
- 输入引入噪声: 7µVpp(40Hz 带宽)
- 输入偏置电流: 175pA
- 数据速率: 高达 25.6ksps
- 差分输入电压范围: ±400mV
- 模拟电源电压: 2.7V 至 5.5V
- 数字输入输出 (I/O) 电源电压: 1.65V 至 3.6V
- 右腿驱动放大器
- 交流和直流导联断线检测
- Wilson 和 Goldberger 终端
- 针对中断驱动诊断的 ALARMB 引脚
- 电池电压监控 ٠
- 内置振荡器与基准
- 灵活的断电和待机模式

# 2 应用

- 便携式 1/2/3/5/6/7/8/12 导联 ECG
- 病人生命体征监控:动态心电图、事件、压力和远 程医疗
- 自动体外除颤器
- 体育运动和健身(心率和 ECG)

# 3 说明

Tools &

Software

ADS1293 包含便携式、低功耗医疗、体育运动和健身 用心电图 (ECG) 应用中通常所需要的全部特性。凭借 高度集成以及出色的性能, ADS1293 能够以大幅缩小 的尺寸、降低的功耗和整体成本创建可扩展的医疗仪器 系统。

ADS1293 特有 3 个能够以高达 25.6ksps 的速率工作 的高分辨率通道。 该器件可单独针对每个通道编程特 定的采样率和带宽,从而使用户能够针对性能和功耗来 优化配置。 所有输入引脚均包含一个 EMI 滤波器,并 且可通过一个灵活的选路开关路由至任一通道。 另 外,凭借这一灵活的选路功能,无需从外部重新连接导 联即可实现独立的导联断线检测、右腿驱动、以及生成 Wilson/Goldberger 基准电端。 对于未使用数字起搏检 测的应用,可通过第四个通道进行外部模拟起搏检测。

ADS1293 包含一个自我诊断警报系统,来检测系统何 时处于运行条件之外。这样的事件被报告给错误标 志。 错误标志的整体状态可由一个专用 ALARMB 引 脚上的信号显示。

此器件采用 5mm x 5mm x 0.8mm, 28 引脚 LLP 封 装。 -20℃ to 85℃ 的运行温度范围。

器件信息(1)

器件型号	封装	封装尺寸(标称值)
ADS1293	WQFN (28)	5.00mm x 5.00mm

(1) 要了解所有可用封装,请见数据表末尾的可订购产品附录。

应用图 4





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# 5 修订历史记录

ADS1293

# Changes from Revision B (March 2013) to Revision C

 已添加引脚配置和功能部分, ESD 额定值表,特性描述部分,器件功能模式,应用和实施部分,电源相关建议部分, 布局部分,器件和文档支持部分以及机械、封装和可订购信息部分......1

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# 6 Pin Configuration and Functions



### **Pin Functions**

PIN		TYPE	EUNCTION	
NAME	NO.	1175	FUNCTION	
IN1 - IN6	1 - 6	Analog Input	Electrode input signals	
WCT	7	Analog Output	Wilson reference output or analog pace channel output	
CMOUT	8	Output	Common-mode detector output	
RLDOUT	9	Analog Output	Right-leg drive amplifier output	
RLDINV	10	Analog Input	Right-leg drive amplifier negative input	
RLDIN	11	Analog I/O	Right-leg drive amplifier positive input or analog pace channel output	
RLDREF	12	Analog Output	Internal right-leg drive reference	
SYNCB	13	Digital I/O	Sync bar; multiple-chip synchronization signal input or output	
VSSIO	14	Digital Supply	Digital input/output supply ground	
ALARMB	15	Digital Output	Alarm bar	
CSB	16	Digital Input	Chip-select bar	
SCLK	17	Digital Input	Serial clock	
SDI	18	Digital Input	Serial data input	
SDO	19	Digital Output	Serial data output	
DRDYB	20	Digital Output	Data ready bar	
CLK	21	Digital I/O	Internal clock output or external clock input	
VDDIO	22	Digital Supply	Digital input/output supply	
XTAL1	23	Digital Input	External crystal for clock oscillator	
XTAL2	24	Digital Input	External crystal for clock oscillator	
RSTB	25	Digital Input	Reset bar	
CVREF	26	Analog I/O	External cap for internal reference voltage	
VSS	27	Analog Supply	Power supply ground	
VDD	28	Analog Supply	Positive power supply	
DAP	_	—	No connect	

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# 7 Specifications

# 7.1 Absolute Maximum Ratings

See (1)(2).

	MIN	MAX	UNIT
Analog Supply Voltage, VDD	-0.3	6.0	V
Digital Supply Voltage, VDDIO	-0.3	6.0	V
Voltage on any Input Pin	-0.3 to (V	′DD + 0.3)	V
Input Current at Any Pin		±10	mA
Max Junction Temperature <sup>(3)</sup>		150	°C
T <sub>stg</sub> Storage temperature	-60	150	°C

 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are measured with respect to the ground pin, unless otherwise specified.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation P<sub>DMAX</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>)/ θ<sub>JA</sub> or the number given in *Absolute Maximum Ratings*, whichever is lower.

# 7.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all $pins^{(2)}$	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

# 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Analog Supply Voltage, VDD		2.7	5.5	V
Digital I/O Supply	VDD > 3.6 V	1.65	3.6	V
Voltage	VDD ≤ 3.6 V	1.65	VDD	V
Supply Ground		VSS = VS	SSIO	
Full Scale Differential I	nput Voltage Range, DIVR		±400	mV
Temperature Range <sup>(1)</sup>		-20	85	°C

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation P<sub>DMAX</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>)/R<sub>θJA</sub> or the number given in *Absolute Maximum Ratings*, whichever is lower.

# 7.4 Thermal Information

		ADS1293	
	THERMAL METRIC <sup>(1)</sup>	LLP	UNIT
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	29	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation P<sub>DMAX</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>)/R<sub>θJA</sub> or the number given in *Absolute Maximum Ratings*, whichever is lower.



# 7.5 Electrical Characteristics<sup>(1)</sup>

Unless otherwise noted, all limits are specified at  $T_A = 25^{\circ}$ C, 2.7 V  $\leq$  VDD  $\leq$  5.5 V, 1.65 V  $\leq$  VDDIO  $\leq$  MIN(3.6 V, VDD), VREF = 2.4 V,  $f_{OSC} = 409.6$  kHz, 1- $\mu$ F low-ESR capacitor between CVREF and GND, 0.1- $\mu$ F capacitor between RLDREF and GND.

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
POWER S	SUPPLY (VDD, VDDIO)					
VDD	Analog Supply Voltage	$T_{MIN} \le T_A \le T_{MAX}$	2.7		5.5	V
		Power-down mode		80		
		$T_{MIN} \le T_A \le T_{MAX}$			125	μΑ
		Standby mode		120		
		$T_{MIN} \le T_A \le T_{MAX}$			175	μΑ
		1 chan, WILSON OFF, RLD OFF, CMDET OFF, LOD OFF, low-power		205		
		$T_{MIN} \le T_A \le T_{MAX}$			290	
		1 chan, WILSON OFF, RLD OFF, CMDET OFF, LOD OFF, high-res		335		
IVDD		$T_{MIN} \leq T_{A} \leq T_{MAX}$			490	
	Analog Supply Current	3 chan, WILSON OFF, RLD OFF, CMDET OFF, LOD OFF, low-power		350		
		$T_{MIN} \le T_A \le T_{MAX}$			520	
		3 chan, WILSON ON, RLD ON, CMDET ON, LOD ON, low-power, low cap-drive		440		μΑ
		$T_{MIN} \le T_A \le T_{MAX}$			595	
		3 chan, WILSON ON, RLD ON, CMDET ON, LOD ON, high-res, low cap-drive		835		
		$T_{MIN} \le T_A \le T_{MAX}$			1120	
		3 chan, WILSON ON, RLD ON, CMDET ON, LOD ON, high-res, high cap-drive		960		
		$T_{MIN} \le T_A \le T_{MAX}$			1300	
		$\label{eq:VDD} \begin{array}{l} VDD > 3.6 \ V \\ T_{MIN} \leq T_{A} \leq T_{MAX} \end{array}$	1.65		3.6	V
VDDIO	IO Supply Voltage	$\label{eq:VD} \begin{array}{l} VDD \leq 3.6 \ V \\ T_{MIN} \leq T_{A} \leq T_{MAX} \end{array}$	1.65		VDD	V
IVDDIO	Quiescent Current IO Supply			0.6		μA
ANALOG	INPUTS (IN1-IN6)					
		T <sub>A</sub> = 25°C, LOD OFF	-175		175	pА
I <sub>B</sub>	Input Bias Current	$T_A = 85^{\circ}C$ , LOD OFF $T_{MIN} \le T_A \le T_{MAX}$	-13		13	nA
RIN	Differential Input Resistance			500		MΩ
		f = 400 MHz		92		dB
	Electromagnetic Interference Rejection	f = 900 MHz		107		dB
	Ratio, IN+, IN-, and VDD	f = 1.8 GHz		98		dB
		f = 2.4 GHz		86		dB

(1)

Typical specifications are estimations only and are not ensured. Datasheet min/max specification limits are specified by test, unless otherwise noted.

(2) (3) Typical values represent the most likely parameter norms at  $T_A = 25^{\circ}C$  and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.

# **Electrical Characteristics**<sup>(1)</sup> (continued)

Unless otherwise noted, all limits are specified at  $T_A = 25^{\circ}$ C, 2.7 V  $\leq$  VDD  $\leq$  5.5 V, 1.65 V  $\leq$  VDDIO  $\leq$  MIN(3.6 V, VDD), VREF = 2.4 V,  $f_{OSC} = 409.6$  kHz, 1-µF low-ESR capacitor between CVREF and GND, 0.1-µF capacitor between RLDREF and GND.

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
ANALOG F	RONT END	<u> </u>				
DIVR	Differential Input Voltage Range	$T_{MIN} \le T_A \le T_{MAX}$	-400		400	mV
CMVR	Common-Mode Voltage Range for full DIVR	$T_{MIN} \le T_A \le T_{MAX}$	0.95		VDD – 0.95	V
V	Input Referred Offect Voltage			±16		
VOS	Input-Referred Offset voltage	$T_{MIN} \le T_A \le T_{MAX}$	-87		87	μv
CMRR	Common-Mode Rejection Ratio	50 / 60 Hz, $VCM_{DC}$ = RLDREF, $VCM_{AC}$ = 1.2V <sub>PP</sub>		100		dB
		0.1 - 215 Hz, low-power mode		23		
		$T_{MIN} \le T_A \le T_{MAX}$			30.5	
V <sub>e</sub> -ECG		0.1 - 215 Hz, high-resolution mode		15		
	Input-Referred Voltage Noise for	$T_{MIN} \le T_A \le T_{MAX}$			23.95	.,
	ECG <sup>(4)</sup>	0.1 - 40 Hz, low-power mode		10		μv <sub>pp</sub>
		$T_{MIN} \le T_A \le T_{MAX}$			23.1	
		0.1 - 40 Hz, high-resolution mode		7		
		$T_{MIN} \le T_A \le T_{MAX}$			10.3	
V <sub>e</sub> -PACE	Input-Referred Voltage Noise for Pace	1 - 1280 Hz, high-resolution mode, double pace data rate		0.4		mV <sub>PP</sub>
	Input-Referred Noise Density	0.1 - 215 Hz, low-power mode		240		nV/√Hz
N <sub>e</sub>		$T_{MIN} \le T_A \le T_{MAX}$			315	
		0.1 - 215 Hz, high-resolution mode		155		
		$T_{MIN} \le T_A \le T_{MAX}$			250	
PSRR	Power Supply Rejection Ratio	50 / 60 Hz		94		dB
XTLK	Crosstalk between channels	Crosstalk from driven channel to zero input channel		-105		dB
		215-Hz bandwidth, low-power mode		17.8		bits bits
ENOB-		$T_{MIN} \le T_A \le T_{MAX}$	17.4			
ECG	Effective Number of Bits for ECG	215 Hz bandwidth, high-resolution mode		18.4		
		$T_{MIN} \le T_A \le T_{MAX}$	17.8			
ENOB- PACE	Effective Number of Bits for Pace	1280-Hz bandwidth, high-resolution mode, double pace data rate		13.7		bits
RS-ECG	Sample Rate ECG Channel	See Table 8, Table 9, Table 10 and Table 11 $T_{MIN} \le T_A \le T_{MAX}$	25		6400	sps
RS-PACE	Sample Rate PACE Channel	$T_{MIN} \le T_A \le T_{MAX}$	3.2		25.6	ksps
TSKEW	Sample Time Skew Between Channels	Multichip simultaneous sampling architecture		0		μs
INTERNAL	REFERENCE (REF)					
	Internal Reference Voltage			2.4		V
.,	Internal Reference Accuracy			±0.5%		
VREF	Internal Reference Drift			±11		ppm/°C
	Internal Reference Start-up Time			5		ms
BATTERY I	MONITOR	L				
Division	(VDD-V <sub>REF</sub> )/factor			3.246		V/V
	Division Accuracy			±0.25%		
TEST REFE	ERENCE	· · ·				
	(V <sub>REF</sub> -VSS)/factor			12		V/V
	Division Accuracy			±0.1%		
	Current Consumption			3.5		μA

(4) At least 1000 consecutive readings are used to calculate the peak-to-peak noise in production.



# **Electrical Characteristics**<sup>(1)</sup> (continued)

Unless otherwise noted, all limits are specified at  $T_A = 25^{\circ}$ C, 2.7 V  $\leq$  VDD  $\leq$  5.5 V, 1.65 V  $\leq$  VDDIO  $\leq$  MIN(3.6 V, VDD), VREF = 2.4 V,  $f_{OSC} = 409.6$  kHz, 1-µF low-ESR capacitor between CVREF and GND, 0.1-µF capacitor between RLDREF and GND.

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup> TYP <sup>(3)</sup>	<sup>)</sup> MAX <sup>(2)</sup>	UNIT
RIGHT-LEO	G DRIVE AMPLIFIER (RLD Amp)	· ·			
V <sub>OS</sub>	Input-Referred Offset Voltage		±	5	mV
CMVR	Common-Mode Voltage Range	$T_{MIN} \le T_A \le T_{MAX}$	0.5	VDD - 0.5	V
	Dragrammable Cain Bandwidth	Low-bandwidth mode	5	)	kHz
GBW	Programmable Gain Bandwidth	High-bandwidth mode	20	)	kHz
<b>CD</b>	Slow Poto	Low-bandwidth mode	2	5	mV/μs
51		High-bandwidth mode	90	)	mV/µs
Churr	Programmable Capacitive Load Driving	High-bandwidth, Low cap-drive mode (see Table 5)	40	)	pF
UIMAX	Capability	Low-bandwidth, High cap-drive mode (see Table 5)		3	nF
		Low-bandwidth, Low cap-drive mode	20	)	uА
חחעו	Quiescent Power Consumption	$T_{MIN} \le T_A \le T_{MAX}$		36	ų,
1100		High-bandwidth, High cap-drive mode	6	)	uА
		$T_{MIN} \le T_A \le T_{MAX}$		91	μ.,
RIGHT-LEG DRIVE REFERENCE					
RLD <sub>REF</sub>	Output Voltage	Unloaded	(VDD - VSS)/2	-	V
COMMON-	MODE DETECTOR AMPLIEIER (CMDET	Amn)	V00//2.	<u> </u>	
CMVR	Common-Mode Voltage Range	$T_{A(B)} \leq T_A \leq T_{A(A)}$	0.5	VDD - 0.5	V
0		Low-bandwidth mode	50	)	kHz
BW	Programmable Bandwidth	High-bandwidth mode	15	)	kHz
		Low-bandwidth mode	2	5	mV/us
SR	Slew Rate	High-bandwidth mode	9	)	mV/µs
		High-bandwidth mode, Low capdrive mode (see	10		-
Char	Programmable Capacitive Load Driving Capability	Table 4)	40	)	р⊢
		Low-bandwidth mode, High cap- drive mode (see Table 4)		3	nF
חחעו	Power Consumption (Selected Leads)	N leads, low-bandwidth mode, low cap-drive mode	21 + 3 × N	1	μA
NDD		N leads, high-bandwidth mode, high cap-drive mode	61 + 3 × N	1	μA
WILSON R	EFERENCE CIRCUIT	FT			
IVR	Input Voltage Range	$T_{MIN} \le T_A \le T_{MAX}$	0.5	VDD - 0.5	V
BW	Bandwidth	3 buffers ON	5	)	kHz
SR	Slew Rate	3 buffers ON	4	5	mV/μs
N <sub>e</sub>	Noise Density	At 10 Hz	6	)	nV/√Hz
Ve	Input-Referred Noise for Wilson Reference Amp	0.1 - 200 Hz, 3 buffers ON	5.	5	$\mu V_{PP}$
IVDD	Power Consumption (Selected Leads)	N leads, low-power mode	7 × 1	١	μA
LEAD-OFF	DETECTION	r1			
IEXC	Excitation Current	Programmable: Min. code 0x01 (See Lead-Off Detection (LOD))	-	3	nA
ILXC		Programmable: Max. code 0xFF (See Lead-Off Detection (LOD))	204	)	nA
IEXC <sub>TOL</sub>	Excitation Current Accuracy		25%	, 0	
FEVO		AC LOD mode, programmable, minimum (see Analog AC Lead-Off Detect )	6.	1	Hz
FEAU		AC LOD mode, programmable, maximum (see Analog AC Lead-Off Detect)	12.	5	kHz
VTH <sub>DC</sub>	DC Lead-Off Comparator Threshold		VDD – 0.	5	V
V <sub>HYST</sub>	Comparator Hysteresis	DC lead-off mode	5	5	mV
IVDD	Current Consumption	Programmed excl. excitation current	2	5	μA



# Electrical Characteristics<sup>(1)</sup> (continued)

Unless otherwise noted, all limits are specified at  $T_A = 25^{\circ}$ C, 2.7 V  $\leq$  VDD  $\leq$  5.5 V, 1.65 V  $\leq$  VDDIO  $\leq$  MIN(3.6 V, VDD), VREF = 2.4 V,  $f_{OSC} = 409.6$  kHz, 1-µF low-ESR capacitor between CVREF and GND, 0.1-µF capacitor between RLDREF and GND.

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
ANALOG P	PACE CHANNEL					
	Gain			3.5		V/V
BW	–3dB Bandwidth			50		kHz
	Output Reference			RLDREF		V
V <sub>OS</sub>	Input-Referred Offset Voltage			±1.3		mV
	Differential Input Voltage Penge	$\begin{array}{l} 2.7 \text{ V} \leq \text{VDD} < 3.3 \text{ V} \\ T_{\text{MIN}} \leq T_{\text{A}} \leq T_{\text{MAX}} \end{array}$	-330		330	mV
DIVIC	Differential input voltage Kange	$\begin{array}{l} 3.3 \ V \leq V DD \\ T_{MIN} \leq T_A \leq T_{MAX} \end{array}$	-400		400	mV
CMVR	Common-Mode Voltage Range for full DIVR	$T_{MIN} \le T_A \le T_{MAX}$	0.95		VDD – 1.1	V
CMRR	Common-Mode Rejection Ratio	$0.5 \text{ V} \leq \text{VCM} \leq \text{VDD-1.5 V}$		85		dB
PSRR	Power Supply Rejection Ratio	$3 \text{ V} \leq \text{VDD} \leq 5 \text{ V}, \text{ VCM=RLDREF}$		80		dB
SR	Slew Rate			35		mV/μs
	Overload Recovery			100		μs
V <sub>e</sub> -APACE	Input-Referred Noise for Analog Pace	VCM = RLDREF, 0.1 kHz - 20 kHz		105		$\mu V_{PP}$
IVDD	Current Consumption			29		μA
CLOCK						
f <sub>OSC</sub>	Internal Clock Frequency	f <sub>CRYSTAL</sub> = 4.096 MHz		409.6		kHz
	Internal Clock Duty Cycle			50%		
TSTART	Internal Clock Start-up Time	f <sub>CRYSTAL</sub> = 4.096 MHz		15		ms
IVDD	Internal Clock Power Consumption			83		μA
f <sub>EXT</sub>	External Clock Frequency <sup>(5)</sup>	$T_{MIN} \le T_A \le T_{MAX}$	370	409.6	450	kHz
	External Clock Duty Cycle <sup>(5)</sup>	$T_{MIN} \le T_A \le T_{MAX}$	40%	50%	60%	
DIGITAL IN	IPUT / OUTPUT CHARACTERISTICS					
V <sub>IH</sub>	Logical "1" Input Voltage	$T_{MIN} \le T_A \le T_{MAX}$	0.8 × VDDIO			V
VIL	Logical "0" Input Voltage	$T_{MIN} \le T_A \le T_{MAX}$			0.2 × VDDIO	V
Varia	Logical "1" Output Voltage	$I_{SOURCE}$ = 400 $\mu A,$ Digital output high-drive mode $T_{MIN} \leq T_A \leq T_{MAX}$	VDDIO – 0.075			V
VОН		$I_{SOURCE}$ = 400 $\mu A,$ Digital output low-drive mode $T_{MIN} \leq T_A \leq T_{MAX}$	VDDIO – 0.15			v
V	Logical "0" Output Valtage	$I_{SINK}$ = 400 µA, Digital output high-drive mode $T_{MIN} \leq T_A \leq T_{MAX}$			VSSIO + 0.075	V
VOL	Logical o Oulput voltage	$I_{SINK}$ = 400 µA, Digital output low-drive mode $T_{MIN} \leq T_A \leq T_{MAX}$			VSSIO + 0.15	V
Laur	Digital IO Leakage Current	SYNCB and RESETB pins, with 1-M $\Omega$ internal pullup resistor		±1		μA
IOHL	Digital IO Leakage Guilent	Other digital I/O pins T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub>	-500		500	nA

(5) Specified by design; not production tested.



# 7.6 Write Timing Requirements

Unless otherwise noted, all limits specified at  $T_A = 25^{\circ}C$ , 2.7 V  $\leq$  VDD  $\leq$  5.5 V, 1.65  $\leq$  VDDIO  $\leq$  MIN (3.6 V, VDD), VREF = 2.4 V,  $f_{OSC} = 409.6$ -kHz and a 10-pF capacitive load in parallel with a 10-k $\Omega$  load on SDO.

			MIN	MAX	UNIT
F <sub>SCLK</sub>	Serial Clock Frequency			20	MHz
t <sub>PH</sub>	SCLK Pulse Width - High	F <sub>SCLK</sub> = 20 MHz	0.4/F <sub>SCLK</sub>		s
t <sub>PL</sub>	SCLK Pulse Width - Low	F <sub>SCLK</sub> = 20 MHz	0.4/F <sub>SCLK</sub>		s
t <sub>SU</sub>	SDI Set-up Time		5		ns
t <sub>H</sub>	SDI Hold Time		5		ns



Figure 1. Write Timing Diagram

# 7.7 Read Timing Requirements

Unless otherwise noted, all limits specified at  $T_A = 25^{\circ}$ C, 2.7 V  $\leq$  VDD  $\leq$  5.5 V, 1.65  $\leq$  VDDIO  $\leq$  MIN(3.6 V, VDD), VREF = 2.4 V, f<sub>OSC</sub> = 409.6-kHz and a 10-pF capacitive load in parallel with a 10-k $\Omega$  load on SDO.

			MIN	NOM	MAX	UNIT
t <sub>ODZ</sub>	SDO Driven-to-Tristate Time	Measured at 10% / 90% point			15	ns
t <sub>OZD</sub>	SDO Tristate-to-Driven Time	Measured at 10% / 90% point			15	ns
t <sub>OD</sub>	SDO Output Delay Time			10	ns	
t <sub>CSS</sub>	CSB Set-up Time		5			ns
t <sub>CSH</sub>	CSB Hold Time		5			ns
t <sub>IAG</sub>	Inter-Access Gap		10			ns
t <sub>DRDYB</sub>	Data Ready Bar at every 1/ODR second,	see Figure 25		4/f <sub>OSC</sub>		S



Figure 2. Read Timing Diagram



# 7.8 Typical Characteristics

All plots at  $T_A = 25^{\circ}$ C, VDD = 3.3 V, VDDIO = 1.8 V, VSS = VSSIO = 0 V, internal VREF = 2.4 V, VCM = RLDREF, internal  $f_{OSC} = 409.6$  kHz, data rate = 1067 sps, and High-Resolution mode, unless otherwise noted.





# **Typical Characteristics (continued)**

All plots at  $T_A = 25^{\circ}$ C, VDD = 3.3 V, VDDIO = 1.8 V, VSS = VSSIO = 0 V, internal VREF = 2.4 V, VCM = RLDREF, internal  $f_{OSC} = 409.6$  kHz, data rate = 1067 sps, and High-Resolution mode, unless otherwise noted.





# **Typical Characteristics (continued)**

All plots at  $T_A = 25^{\circ}$ C, VDD = 3.3 V, VDDIO = 1.8 V, VSS = VSSIO = 0 V, internal VREF = 2.4 V, VCM = RLDREF, internal  $f_{OSC} = 409.6$  kHz, data rate = 1067 sps, and High-Resolution mode, unless otherwise noted.





# 8 Detailed Description

# 8.1 Overview

The ADS1293 is a fully-integrated signal chain for ECG applications. It features three low-power, 24-bit resolution channels for ECG and pace monitoring and an auxiliary fourth channel for analog pace detection. In addition, the ADS1293 features AC and DC lead-off detection, right-leg drive capability, and Wilson and Goldberger terminals.

Each of the three channels is synchronized and provides digital filtering with a cut-off frequency that is programmable from 5 Hz to 1280 Hz. Each channel filter can be set independently while maintaining synchronization. In addition, a lower-resolution output is provided for each signal channel with a cut-off frequency programmable between 650 Hz to 2.6 kHz. These output signals are ideal for sensing a pace-maker signal. Each channel provides enough dynamic range to handle electrode offset and motion artifacts without sacrificing resolution. Each input has built-in EMI rejection that eliminates noise from RF transmitters.

# 8.2 Functional Block Diagram



TEXAS INSTRUMENTS

# 8.3 Feature Description

# 8.3.1 Flexible Routing Switch

The flexible routing switch can connect the inputs of the three analog front-end channels as well as the inputs of the analog pace channel to any of the 6 input pins. This allows system flexibility and even on-the-fly reconfiguration of the ECG monitoring system. For test purposes, the flexible routing switch can short the differential input pins of a channel or connect a differential reference signal to the input of a channel. This reference voltage can be applied with both positive and negative polarity. This feature allows to measure relative mismatches between channels, such as offset and gain mismatches. Additionally, there is an option to route a fraction of the battery voltage (the voltage source connected to the VDD pin) to an input channel. This allows the ADS1293 to monitor the state of charge of the battery.

The switch path inside the flexible routing switch is illustrated in Figure 17. The figure shows the switch path for a single channel. All channels are completely identical. The switches are controlled by the registers FLEX\_CH1\_CN, FLEX\_CH2\_CN, FLEX\_CH3\_CN, and FLEX\_VBAT\_CN, which are described in the *Input Channel Selection Registers*.



Figure 17. Flexible Routing Switch for Channel 1

It should be noted that the switches that control the input selection for the analog front-end channels have a certain priority. If the battery voltage monitoring mode is enabled by programming the VBAT\_MONI\_CHx bit in the FLEX\_VBAT\_CN register, then the POSx and NEGx bits programmed in the FLEX\_CHx\_CN register no longer have any effect. The battery voltage monitoring mode thus takes priority; this is shown in the first row of Table 1. Furthermore, the test features take second priority over the input pin selection. If the TSTx bit of the FLEX\_CHx\_CN register are not zero, then the POSx and NEGx bits are essentially ignored, and the test features will take priority as seen in Table 1. The TSTx, POSx, and NEGx bits are described in the *Input Channel Selection Registers*.

VBAT_MONI_CHx	CALx	POSx	NEGx	MODE
1	Х	Х	Х	CHx is in battery voltage monitoring mode
0	11	Х	Х	CHx input shorted
0	01	Х	Х	CHx input connected to positive reference
0	10	Х	Х	CHx input connected to negative reference
0	00	INx	INy	CHx positive input connected to pin INx and negative input connected to pin INy

Table 1. Channel 1 Switch Configuration



# Feature Description (continued)

### 8.3.2 Battery Monitoring

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The battery voltage monitoring mode is enabled by setting bit VBAT\_MONI\_CHx = 1 in the FLEX\_VBAT\_CN register. Also, the instrumentation amplifier of the selected channel must be shut down by setting SHDN\_INA\_CHx = 1 in the AFE\_SHDN\_CN register. In this mode, the positive input, POSx, of the sigma-delta modulator will sample the voltage supplied on the VDD pin. At the same time, the negative input, NEGx, of the sigma-delta modulator will sample the reference voltage,  $V_{REF}$ , generated on or provided to the CVREF pin. As a result, the output signal of the sigma-delta modulator is a measure for ( $V_{BAT}$ - $V_{REF}$ ). In this operation, the sigma-delta modulator works with a modified gain factor, and the battery voltage,  $V_{BAT}$ , can be calculated as follows:

$$V_{BAT} = V_{REF} \left[ 1 + 3.246 \left( \frac{ADC_{OUT}}{ADC_{MAX}} - \frac{1}{2} \right) \right]$$
(1)

In this equation,  $V_{REF}$  equals 2.4 V if the internal reference voltage generator is used, and ADC<sub>MAX</sub> represents the maximum output code of the ADC, which would correspond to a theoretical 2.4-V signal at the input of the sigma-delta modulator. The value of ADC<sub>MAX</sub> is dependent on the configuration of the digital filters, and the corresponding ADC<sub>MAX</sub> values are listed in Table 8 through Table 11.

The battery monitoring mode is targeted for battery operated systems within a voltage range of 2.4 V to 4.8 V. The battery monitoring mode cannot be used when the ADS1293 is powered from a regulated 5-V supply because it risks saturating the sigma-delta modulator. There is a also a low battery alarm that is implemented independently from the battery monitoring mode, which will trigger a battery alarm when the supply voltage is below 2.7 V (see the BATLOW description in *Alarm Functions*).

# 8.3.3 Test Mode

If the battery voltage monitoring function is not enabled, and if bit TSTx = 01 (see the *Input Channel Selection Registers* section), then a positive DC test signal is provided to the input of the instrumentation amplifier. If TSTx = 10, then that same test signal is provided but with negative polarity. The expected ADC output code can be calculated as follows:

$$ADC_{OUT} = \left[ \pm \frac{3.5 V_{TEST}}{2 V_{REF}} + \frac{1}{2} \right] ADC_{MAX}$$
(2)

In Equation 2, the positive or negative DC test signal  $V_{\text{TEST}} = V_{\text{REF}}/12$ . Note that this test mode is not a gain calibration since  $V_{\text{TEST}}$  and  $V_{\text{REF}}$  are generated by the same reference; however, it can be used as a self-test or to measure gain mismatches between channels.

When TSTx = 11, the inputs of the instrumentation amplifier in the channel can be shorted to provide a zero test signal. The expected ADC output code equation can be simplified to:

$$ADC_{OUT} = \frac{1}{2} ADC_{MAX}$$
(3)

For both equations, the value of  $ADC_{MAX}$  corresponding to a given decimation configuration can be obtained from Table 8 through Table 11.

# 8.3.4 Analog Front-End

The ADS1293 contains three analog front ends that convert a differential analog voltage into a digital signal. Each analog front end consists of an instrumentation amplifier (INA), a sigma-delta modulator (SDM), and a digital filter.

# 8.3.5 Instrumentation Amplifier (INA)

The instrumentation amplifier provides a high input impedance to interface with signal sources that may have relatively high output impedance, such as ECG electrodes. The maximum differential input voltage range of the Sigma-Delta Modulator (SDM) behind the INA is  $\pm 1.4$  V, and the gain of the INA is 3.5x. Therefore, the maximum differential input voltage of the INA is  $\pm 400$  mV.



# Feature Description (continued)

The input common-mode voltage range (CMVR) of the INA is 0.95 V to VDD-0.95 V. If the input differential voltage range is limited to smaller values, then the CMVR can be somewhat extended. If the differential input signal is limited to  $VIN_{MAX}$ , the CMVR range can be defined as:

$$(1.75 * VIN_{MAX} + 0.25) \le CMVR \le (VDD - 0.25 - 1.75 * VIN_{MAX})$$
<sup>(4)</sup>

The INA can be configured to operate in a low-power mode or in a high-resolution mode. The low-power mode consumes about 3 times less power than the high-resolution mode. However, the high-resolution mode has less noise than the low-power mode. Switching between these two modes is controlled by the EN\_HIRES\_CHx bits in the AFE\_RES register.

When a channel is not in use, its INA can be shut down by programming the SHDN\_INA\_CHx bit in the AFE\_SHDN\_CN register, and its SDM can also be shut down by programming the SHDN\_SDM\_CHx bit in the AFE\_SHDN\_CN register.

# 8.3.5.1 Instrumentation Amplifier Fault Detection

The output signal of the instrumentation amplifier can be monitored to ensure its output signal is within an appropriate range. The out-of-range error flags for the INAs can be observed in the ERROR\_RANGE1, ERROR\_RANGE2 and ERROR\_RANGE3 registers.

The output signal is present at two points: OUTP and OUTN. If the input common-mode voltage or differential voltage is such that the instrumentation amplifier would have to drive the voltages at these points above the positive or below the negative supply rail, then the signal accuracy would be lost. These two points are monitored and a warning flag is raised if the voltage on these pins approaches the supply rails. If the OUTP\_HIGH flag is raised, then the voltage at OUTP is close to the positive rail. This indicates the differential input signal is too large or the input common-mode voltage is too high. If the OUTP\_LOW flag is raised, then the voltage at OUTP is close to the negative rail. This happens at low input common-mode voltages and large negative differential input voltages. Similar reasoning holds for the OUTN\_HIGH and OUTN\_LOW flags.

The differential output voltage of the INA is monitored and reported to the DIF\_HIGH bit. This error flag indicates that the differential signal is out-of-range and is no longer an accurate representation of the input signal. The DIF\_HIGH error flag is raised if the differential output voltage of the INA exceeds  $\pm 1.4$  V, which is the input range of the Delta-Sigma Modulator. When this happens, the SDM will no longer sample the output of the INA, but instead will sample 0 V. The sign of the input signal can still be observed in the SIGN bit of the *ERROR\_RANGEx* registers.

The fault detection circuitry for OUTP\_HIGH, OUTP\_LOW, OUTN\_HIGH and OUTN\_LOW can be shut down by programming the SHDN\_FAULTDET\_CHx bits in the AFE\_FAULT\_CN register. These shutdown bits do not affect the operation of DIF\_HIGH and SIGN because the instrumentation amplifier should always provide these signals to the sigma-delta modulator. The circuitry that generates DIF\_HIGH and SIGN only gets shut down when the corresponding INA is shut down.

# 8.3.6 Sigma-Delta Modulator (SDM)

The Sigma-Delta Modulator (SDM) takes the output signal of the INA and converts this signal into a high resolution bit stream that is further processed by the digital filters.

The SDM can operate at clock frequencies of 102.4 kHz or 204.8 kHz; these frequencies are generated internally. Running the SDM at 204.8 kHz results in a larger oversampling ratio, which improves the resolution of the signal recovered by the digital filters behind the SDM. However, running the SDM at a higher clock frequency will increase its power consumption, resulting in a tradeoff between resolution and power consumption.

The 102.4-kHz or 204.8-kHz clock frequency can be selected for each channel individually by programming the FS\_HIGH\_CHx bits in the AFE\_RES register.

The SDM also features dithering to reduce tones in the system, a known by-product of Sigma-Delta converters. The dithering circuit is active by default and is automatically turned OFF when the input signal is larger than 40 mV.



### Feature Description (continued)

### 8.3.6.1 Sigma-Delta Modulator Fault Detection

The state of the integrators in the Sigma-Delta Modulator (SDM) are monitored to detect over-range signals that cause the SDM to become unstable. When an over-range event is detected in the SDM, the state of its integrators is reset, and the over-range error is reported to the SDM\_OR\_CHx bits of the ERROR\_RANGE1, ERROR\_RANGE2, and ERROR\_RANGE3 registers.

### 8.3.7 Programmable Digital Filters

A programmable digital filter behind the Sigma-Delta Modulator (SDM) reconstructs the signal from the SDM output bit stream. The filter consist of three programmable SINC filters as shown in Figure 18. Each stage is a fifth order SINC filter.



Figure 18. Sinc Filters

The decimation rates (R1, R2, and R3) of the SINC filters are programmable as described in Table 2. Each of the three stages further filters and decimates the bit stream so that the output data rate (ODR) and bandwidth (BW) of the signal is reduced, and at the same time, the resolution is enhanced. A 16-bit digital signal with relatively high ODR and BW, but with somewhat limited resolution, is available after the second stage; this signal can be used for PACE pulse detection. That signal is further decimated by the third stage and results in a very high-resolution filtered 24-bit digital signal that is an accurate representation of the ECG signal.

### Table 2. Programmable Digital Filter Coefficients

Stage 1 (R1)	Stage 2 (R2)	Stage 3 (R3)
4 (Standard PACE Data Rate), 2 (Double PACE Data Rate)	4, 5, 6, 8	4, 6, 8, 12, 16, 32, 64, 128

The first stage sets the Standard PACE Data Rate (where the decimation rate R1 = 4) or the Double PACE Data Rate (where R1 = 2). Operating the device in the Double PACE Data Rate will double the ODR for the first stage (and therefore also for the subsequent stages). However, the BW of the first stage does not change in this mode; only the ODR is affected. By operating the device in the Double PACE Data Rate, the ODR of the PACE data is doubled, and thus, more accurate PACE pulse detection is possible. However, operating the device in the Double PACE Data Rate will increase its power consumption. The R1 decimation rate can be programmed for each of the three channels separately by using the R1\_RATE register.

Programming the second stage (R2) to a low decimation rate sets a relatively high ODR and BW, but doing so will also increase the noise level. For digital PACE pulse detection, smaller values for R2 are recommended. The R2 decimation rate can be programmed using the R2\_RATE register.

As the third stage decimation (R3) increases, the ODR and BW of the ECG decreases. When detecting an ECG signal, higher values of R3 are recommended. The R3 decimation rate for each channel can be individually programmed using the R3\_RATE\_CH1, R3\_RATE\_CH2, and R3\_RATE\_CH3 registers.

Table 8, Table 9, Table 10, and Table 11 illustrate how these decimation rates R1, R2, and R3 affect the ODR, BW, and RMS Noise of the PACE and ECG signals. In addition, the ODR and BW also depend on whether the SDM is running at a low (102.4kHz) or high (204.8 kHz) clock frequency (set by the FS\_HIGH\_CHx bits in the AFE\_RES register). The RMS Noise of the PACE and ECG channels also depend on whether the instrumentation amplifier is running in low-power or high-resolution mode (set by the EN\_HIRES bits in the AFE\_RES register).

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In summary, the output data rate of an ECG channel can be calculated as follows:

$$ODR_{ECG} = \frac{f_S}{R1 R2 R3}$$
(5)

And the output data rate of a PACE channel can be calculated as follows:

$$ODR_{PACE} = \frac{f_S}{R1R2}$$
(6)

Where f<sub>S</sub> is the clock frequency of the modulator: 102.4 kHz, or 204.8 kHz.

### 8.3.8 Filter Settling Time

The low-pass filter frequency responses of the ECG and PACE SINC filters result in a settling time associated with their outputs as a response to a step input signal. This settling time is determined by the order of the filter, N, its differential delay, M, and the channel output data rate, ODR:

$$t_s = N \times M / ODR$$
<sup>(7)</sup>

The ODR of the filter is a function of the sigma-delta's sampling frequency,  $f_S$ , and the filter decimation rates. The value of the ODR can be calculated using Equation 5 and Equation 6. For an ECG channel, the value of NxM = 5. For a pace channel NxM = 5 when operated in the Standard Pace Data Rate (R1 = 4), and NxM = 10 when operated in the Double Pace Data Rate (R1 = 2).

As a result, an unclamped pace signal applied to the filter input results in an ECG channel minimum settling time of:

$t_{s-ECG} = 5 \times R1 \times R2 \times R3 / f_s$	(8)
A Standard Pace Data Rate operated pace channel will go through a minimum settling time of:	
$t_{s-PACE} = 5 \times R1 \times R2 / f_s$	(9)
And a Double Pace Data Rate operated pace channel will go through a minimum settling time of:	
$t_{s-PACE} = 10 \times R1 \times R2 / f_s$	(10)

# 8.3.9 Analog Pace Channel

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The ADS1293 features an additional analog pace channel to process pulses from a pacemaker. The analog pace channel is suitable for low-power applications where the device can be configured for low data rates in ECG mode only, while an analog channel detects PACE pulses. This channel consists of a traditional three opamp instrumentation amplifier and is designed to amplify an ECG signal in a typical bandwidth, as specified in the *Electrical Characteristics* table, allowing for external circuitry to detect the PACE pulses. The analog pace implementation inside the ADS1293 is depicted in Figure 19. The analog pace channel is not limited to PACE detection; it is a full-analog channel that could be used to pre-amplify signals, for instance, from a respiration sensor.

The output voltage of the analog pace channel is:

Vpaceout =  $3.5 \times (Vinp - Vinm) + RLDREF$ 

(11)

Where Vinp and Vinm are the positive and negative inputs of the analog pace channel. The input pins of this channel can be selected in the FLEX\_PACE\_CN register and can connect to any of the IN1 through IN6 pins. Note there is no battery monitoring option available through this channel. There is, however, the reference voltage test mode available as described in *Test Mode*.





Figure 19. Analog Pace Channel Instrumentation Amplifier

The output of the analog pace channel can be multiplexed to the WCT or RLDIN pin using the AFE\_PACE\_CN register. When PACE2RLDIN = 1, the output is routed to the RLDIN terminal, while internally the positive input of the Right-Leg Drive amplifier is connected to the RLDREF pin. When PACE2WCT = 1, the output is routed to the WCT terminal, and the WCT terminal is disconnected from the Wilson output. In this case, the Wilson output can still be connected internally to the IN6 pin using the WILSON\_CN register. The analog pace channel is disabled when SHDN\_PACE = 1 to save power when it is not used.

The analog pace channel is designed to drive a high pass filter and can directly drive a capacitive load of 100 pF.

For analog pace detection, TI recommends having a band pass filter at the output of the analog pace channel, amplify the resulting signal with a relatively high bandwidth amplifier, and compare the amplified pulses with a relatively high speed window comparator. The bandwidth of the band pass filter, gain of the amplification, and the thresholds of the window comparator should be tuned so the comparators trigger on pacemaker pulses, but not to other signals present in the ECG environment.

# 8.3.10 Wilson Reference

The ADS1293 features a Wilson reference block consisting of three buffer amplifiers and resistors that can generate the voltages for the Wilson Central Terminal or Goldberger terminals. Each of the three buffer amplifiers can be connected to any input pin, IN1 through IN6, by programming the WILSON\_EN1, WILSON\_EN2, and WILSON\_EN3 registers. A buffer that is not connected to an input pin is automatically disabled. When disabled, the buffers have a high-output impedance.





Figure 20. Wilson Reference Generator Circuit

The output of the Wilson Reference can be routed internally to IN6, and the outputs of the Goldberger reference can be routed internally to IN4, IN5 and IN6. This is configured in the WILSON\_CN register. If routed externally, TI strongly recommends shielding these connections, which due to their high-output impedance, are prone to pick up external interference.

# 8.3.10.1 Wilson Central Terminal

There are three main ECG leads that are measured differentially:

- Lead I: I = LA RA
- Lead II: II = LL RA
- Lead III: III = LL LA

Where LA is the left-arm electrode, LL is the left-leg electrode, and RA is the right-arm electrode.

In a standard 5-lead or 12-lead ECG, the Wilson Central Terminal is used as the reference voltage for the chest electrodes, which are measured differentially against this reference. The Wilson Central Terminal is defined as the average of the three limb electrodes, RA, LA, and LL:

Wilson Central Terminal = (RA + LA + LL)/3

The output of Wilson Central Terminal generated by the ADS1293, as seen in Figure 20, is defined as:

 $WCT_{OUT} = (BUF_1 + BUF_2 + BUF_3)/3$ 

The user could program the WILSON\_EN1 register to connect the RA electrode to  $BUF_1$ , program the WILSON\_EN2 register to connect the LA electrode to  $BUF_2$ , and program the WILSON\_EN3 register to connect the LL electrode to  $BUF_3$ .



When the Wilson reference is enabled, its output is present at the WCT pin, except when the analog pace channel is routed to the WCT pin (see *Analog Pace Channel*). In such a configuration, the Wilson terminal can still be made available at an external pin by programming the WILSONINT bit to 1. Setting this bit connects the output of the Wilson reference internally to the IN6 pin.

# 8.3.10.2 Goldberger Terminals

Augmented leads in 3-lead, 5-lead or 12-lead ECG are typically calculated digitally based on the measurement results of Lead I and Lead II. The augmented leads are defined as:

- aVR = -(I + II)/2 = RA (LA + LL)/2 = RA G1
- aVL = I II/2 = LA (RA + LL)/2 = LA G2
- aVF = II I/2 = LL (RA + LA)/2 = LL G3

Augmented leads can also be measured directly with the Goldberger terminals to give the best SNR. The Goldberger terminals generated by the ADS1293, as seen in Figure 20, are defined as:

- $G1 = (BUF_2 + BUF_3)/2$
- $G2 = (BUF_1 + BUF_3)/2$
- $G3 = (BUF_1 + BUF_2)/2$

In this case, the user must program the WILSON\_EN1 register to connect the RA electrode to  $BUF_1$ , program the WILSON\_EN2 register to connect the LA electrode to  $BUF_2$ , and program the WILSON\_EN3 register to connect the LL electrode to  $BUF_3$ .

The Goldberger output terminals, G1, G2 and G3 can be made available on external pins programming the GOLDINT bit to 1. Setting this bit connects the Goldberger terminals internally to the IN4, IN5 and IN6 pins.

- IN4 = G1
- IN5 = G2
- IN6 = G3

Note that multiple ADS1293 chips are required if both the augmented leads and the three basic leads need to be converted directly.

The WILSONINT and GOLDINT bits must not be programmed to 1 simultaneously because it will short-circuit the Wilson output terminal and the third Goldberger output terminal. The options described in these sections are summarized in Table 3.

		DACEOWCT	TERMINAL OUTPUTS						
GOLDINI	WILSONINT	PACEZWCI	WCT PIN	IN4 PIN	IN5 PIN	IN6 PIN			
0	0	0	WCT <sub>OUT</sub>	General input	General input	General input			
0	1	0	WCT <sub>OUT</sub>	General input	General input	WCT <sub>OUT</sub>			
1	0	0	WCT <sub>OUT</sub>	$(BUF_2 + BUF_3)/2$ $(BUF_1 + BUF_3)/2$		$(BUF_1 + BUF_2)/2$			
1	1	Х	Illegal	Illegal	Illegal	Illegal			
0	0	1	Vpaceout	General input	General input	General input			
0	1	1	Vpaceout	baceout General input General input		WCT <sub>OUT</sub>			
1	0	1	Vpaceout	(BU <sub>F2</sub> + BUF <sub>3</sub> )/2	(BUF <sub>1</sub> + BUF <sub>3</sub> )/2	(BUF <sub>1</sub> + BUF <sub>2</sub> )/2			

### **Table 3. Wilson and Goldberger Reference Control**

# 8.3.11 Common-Mode (CM) Detector

The Common-Mode Detector averages the voltage of up to six input pins. Its output can be used in a right-leg drive feedback circuit. The selection of the input pins that contribute to the average is configured in the CMDET\_EN register. The Common-Mode Detector is automatically disabled when no input pin is selected.







### 8.3.11.1 Cable Shield Driving

The Common-Mode Detector also has a programmable capacitive load driving capability of up to 8 nF that allows it to drive a cable shield to reduce the common-mode signal current through a cable. This effectively increases the bandwidth of the filter formed by the electrode impedance and the cable capacitance, reducing the amount of common-mode to differential mode crosstalk. As a result, the CMRR of the overall ECG system is improved.

The bandwidth and capacitive load driving capability of the Common-Mode Detector can be configured in the CMDET\_CN register to achieve an optimal tradeoff with power consumption. Table 4 lists the power consumption corresponding to different configuration scenarios given that all inputs are enabled by setting the CMDET\_EN register = 0x3F.

The lowest current consumption setting can be used when the Common-Mode Detector is only used to drive the Right-Leg Driver, and no cable shield is driven. If a cable shield needs to be driven, the power can be increased to drive the cable capacitance depending on the number and type of the driven cable shields. Note that the capacitive driving capability is reduced in the higher bandwidth mode.

CMDET_BW	CMDET_CAPDRIVE	BW (kHz)	C <sub>LOAD</sub> (nF)	CMDET I <sub>SUPPLY</sub> (µA)
0: Low BW mode	00: Low Cap Drive	50	2	39
0: Low BW mode	01: Medium Low Cap Drive	50	3.3	45
0: Low BW mode	10: Medium High Cap Drive	50	4.5	56
0: Low BW mode	11: High Cap Drive	50	8	75
1: High BW mode	00: Low Cap Drive	150	0.4	43
1: High BW mode	01: Medium Low Cap Drive	150	0.65	49
1: High BW mode	10: Medium High Cap Drive	150	1	60
1: High BW mode	11: High Cap Drive	150	1.6	79

### Table 4. Typical Common-Mode Detector Bandwidth, Capacitive Drive and Power Consumption

# 8.3.11.2 Common-Mode Output Range (CMOR)

The Common-Mode Detector incorporates an out-of-range alarm to sense if the common-mode voltage is outside of the common-mode voltage range of the ADS1293. A Common-Mode Out-of-Range Alarm is created in the CMOR bit of the ERROR\_STATUS register when the common-mode drops below 0.75 V or exceeds VDD-0.75 V. System alarms are filtered by the digital circuitry (see *Error Filtering*), and for this reason, the master clock must be active in order to capture an alarm.

# 8.3.12 Right-Leg Drive (RLD)

The RLD is a programmable operational amplifier that is intended to control the common-mode level of the patient connected through electrodes to the ADS1293 and thereby improving the AC CMRR of the overall ECG system. In a typical ADS1293 application, the common-mode level of the patient's body is measured by the Common-Mode Detector described in the previous section. The CMOUT is compared by the RLD to the reference voltage present on the RLDREF pin. When used in an inverting amplifier topology, the right-leg electrode is driven by the RLD to counter any differences between the reference voltage and the detected common-mode level. This reduces the amount of power-line common-mode interference.

The negative input terminal of the RLD op-amp is always connected to the RLDINV pin. By default, the positive input terminal of the RLD op-amp is routed to the RLDIN pin. However, when bit PACE2RLDIN = 1 in the AFE\_PACE\_CN register, the positive input terminal is routed to the internally to the RLD reference. This will allow connecting the output of the analog pace instrumentation amplifier to the RLDIN pin. The output of the RLD op-amp is always connected to the RLDOUT pin, and in addition, can be connected to one of the IN1-IN6 terminals by programming the SELRLD bit in the RLD\_CN register. The RLD circuit can be shut down in the same register by setting bit SHDN\_RLD = 1.





Figure 22. Right-Leg Drive Circuit

# 8.3.13 Capacitive Load Driving

The bandwidth and capacitive load driving capability of the RLD can be configured in the RLD\_CN register to achieve an optimal tradeoff of power consumption. Table 5 lists the power consumption corresponding to different configuration scenarios.

RLD_BW	RLD_CAPDRIVE	GBW (kHz)	C <sub>LOAD</sub> (nF)	RLD I <sub>SUPPLY</sub> (µA)
0: Low BW mode	00: Low Cap Drive	50	2	20
0: Low BW mode	01: Medium Low Cap Drive	50	3.3	25
0: Low BW mode	10: Medium High Cap Drive	50	4.5	36
0: Low BW mode	11: High Cap Drive	50	8	55
1: High BW mode	00: Low Cap Drive	200	0.4	23
1: High BW mode	01: Medium Low Cap Drive	200	0.65	29
1: High BW mode	10: Medium High Cap Drive	200	1	39
1: High BW mode	11: High Cap Drive	200	1.6	60

Table 5. Typical Right-Leg Drive Bandwidth, Capacitive Drive, and Power Consumption

# 8.3.14 Error Status: RLD Rail

The RLD amplifier incorporates a near to rail alarm function that is triggered when the output of the op-amp is below 0.2 V or above VDD-0.2 V. The alarm is reported to the RLDRAIL bit in the ERROR\_STATUS register and indicates that the RLD's feedback loop has difficulty maintaining a constant voltage on the patient's body. In this case, the common-mode on the patient's body may drift away from its target value, but it may still be within the proper input common-mode voltage range of the ADS1293, and the ECG signal data acquisition can continue. When the common-mode on the patient's body is outside the operation range of the ADS1293, the CMOR error will be raised, as described in the previous section. System alarms are filtered by the digital circuitry (see *Error Filtering*), and for this reason, the master clock must be active in order to capture an alarm.

# 8.3.15 Lead-Off Detection (LOD)

The lead-off detect (LOD) block of the ADS1293 can be used to monitor the connectivity of the 6 input pins to electrodes. The LOD block injects a programmable DC or AC excitation current into selected input pins and detects the voltages that appear on the input pins in response to that current. If a lead is not making a proper contact, then the electrode impedance will be high, and as a result, the voltage in response to a small test current will be relatively large, while the voltage for a well-connected lead will be small.



The LOD block can work in one of the three following modes: 1) DC lead-off detect, 2) analog AC lead-off detect or 3) digital AC lead-off detect. All three LOD modes use a common DAC that provides a programmable reference current. This reference current is used to set the magnitude of the test current for lead-off detection. The amplitude of the excitation current used for lead-off detection can be programmed in the LOD\_CURRENT register, where codes 0 to 255 result in currents ranging from 0 to 2.040  $\mu$ A in steps of 8 nA.

The complete LOD block can be shut down by programming the SHDN\_LOD bit to 1 in the LOD\_CN register.

# 8.3.16 DC Lead-Off Detect

The LOD block can be configured for DC LOD mode by programming a 0 in the SELAC\_LOD bit of the LOD\_CN register. In the DC LOD mode, a DC test current can be injected into any of the six input pins by setting the corresponding bit EN\_LOD[x] of the LOD\_EN register. Programming a bit to 1 in this register enables a switch that allows a copy of the current programmed into the DAC to be injected into the desired input pins, as shown in the simplified block diagram of Figure 23.



Figure 23. Simplified DC Lead-Off Detect Block Diagram

For the selected input pins, a Schmitt-trigger comparator then compares the voltage that appears on the pin to (VDD-0.5 V). The result of this comparison can be accessed through the corresponding OUT\_LOD[x] bit of the ERROR\_LOD register. If a lead is off, then the injected current has no return path-to-ground, and as a result, the voltage on the associated input pin will rise towards VDD. This is detected by the comparator and is used as a signal to indicates the lead is not properly connected.

It is important to note that the lead-off detection circuit requires a low impedance return path from the right-leg electrode-to-ground, such as a voltage reference or the RLD amplifier output. Without a proper low impedance return path for the LOD currents, all enabled LOD pins will report a lead disconnected.

# 8.3.17 Analog AC Lead-Off Detect

DC lead-off detection cannot be used when using capacitively coupled electrodes, such as dry electrodes, because they have a high-DC impedance that will block DC test currents. In this case, the analog AC LOD block can be used. Contrary to the DC LOD, the AC LOD injects AC excitation currents with programmable amplitudes and frequencies into the desired lead.

To operate the LOD in analog AC LOD mode, the SELAC\_LOD and the ACAD\_LOD bits of the LOD\_CN register must be set to 1.

A simplified block diagram of the analog AC LOD block is shown in Figure 25. The AC excitation frequency can be programmed by a 7-bit number, ACDIV\_LOD, and a division factor, ACDIV\_FACTOR, in the LOD\_AC\_CN register. The register sets the output frequency of the divider to a rate of:

 $\Phi = 50/(4 \times K \times (ACDIV\_LOD + 1)) \text{ kHz}$ 

(12)

Where K is 1 if the ACDIV\_FACTOR bit equals 0, and K is 16 if the ACDIV\_FACTOR bit equals 1. For instance,  $ACDIV\_LOD = 0$  and  $ACDIV\_FACTOR = 0$  result in an excitation frequency of 12.5 kHz, which is the maximum excitation frequency.



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Complimentary driven switches, enabled by the EN\_LOD[x] bits of the LOD\_EN register, sink and source the AC excitation currents into the desired input pins. The resulting AC current has a frequency  $\Phi$  and a peak-to-peak amplitude equal to the current programmed into the DAC. An AC coupled synchronous detector detects the amplitude of the AC voltage appearing on the lead. The detected amplitude is compared to a reference voltage by means of a Schmitt-trigger comparator. The comparator's reference voltage level, as shown in Figure 24, is determined by a 2-bit reference DAC configured in the ACLVL\_LOD bits of the LOD\_CN register.



Figure 24. Analog AC Lead-Off Reference Levels

The comparator outputs can be accessed at the OUT\_LOD[x] bit of the ERROR\_LOD register. A high comparator output signal indicates that the AC voltage at the excitation frequency is larger than the programmed threshold, which indicates that the lead is not well connected.

The lead-off detection circuit requires a low-impedance return path from the right-leg electrode-to-ground, such as a voltage reference or the RLD amplifier output. Without a proper low-impedance return path for the LOD currents, all enabled LOD pins will report a lead disconnected.



Figure 25. Simplified Analog AC Lead-Off Detect Block Diagram

# 8.3.18 Digital AC Lead-Off Detect

The digital AC lead-off detect (LOD) allows for measurement of the impedance of the two electrodes connected to an AFE channel by measuring a signal through the AFE. In this mode, the lead-off detect current is injected in a balanced manner at the inputs of the AFE behind the flex routing switch. The AC test current is injected into the positive input of the AFE behind the flex routing switch; while at the same time, a similar test current with opposite sign is injected into the negative input of the AFE. Since the AFE has a very high input impedance, the current injected into the positive input pin cannot flow into the AFE. Instead, it will flow through the flex routing switch, via the positive input electrode into the patient, and then back through the negative input electrode and via another path in the flex routing switch towards the negative input of the AFE, where it is cancelled by the



current injected at that point. As a result of this test current, an additional AC voltage input will occur at the input of the AFE with a frequency equal to the frequency of the AC LOD test signal frequency. The magnitude of this voltage equals the magnitude of the AC LOD test current (programmed into the CUR\_LOD bit in the LOD\_CURRENT register) multiplied by the impedances of the two electrodes routed to the AFE input in series. This AC voltage will be digitized by the AFE, and the result is available in the digital AFE output signals. The lead connectivity can be determined in the digital domain by applying an FFT to the digital data and by measuring the amplitude of the tone at the AC LOD excitation frequency. It should be noted that the digital AC LOD can only determine the series connectivity of the two leads attached to the inputs of a differential channel, and hence the connectivity of the individual input pins can only be determined by the DC or the analog AC LOD.



Figure 26. Simplified Digital Analog AC Lead-Off Detect Block Diagram

Figure 26 shows a simplified block diagram of the digital AC LOD. Follow the procedures below to activate the Digital AC LOD:

- 1. Select the Digital AC lead-off mode by setting bit SELAC\_LOD = 1 and ACAD\_LOD = 0 in the LOD\_CN register.
- 2. Program the excitation frequency Φ by using the ACDIV\_LOD and ACDIV\_FACTOR bits in the LOD\_AC\_CN register. See the equation in *Analog AC Lead-Off Detect.*
- 3. Enable which channel the digital AC LOD will be applied to by selecting the EN\_LOD[2:0] bits in the LOD\_EN register. These bits correspond to the AFE channels CH3 to CH1 from MSB to LSB, respectively.
- 4. Determine the phase of the injected current to the AFE channels by programming the EN\_LOD[5:3] bits in the LOD\_EN register.

The EN\_LOD[5:3] bits determine the phase of the injected current to the AFE channels CH3 to CH1 from MSB to LSB, respectively. A bit set to 1 means that the corresponding channel will receive an anti-phase excitation current in respect to the frequency divider's phase. In some applications, it may be necessary to invert the sign of the digital AC lead-off test current on a channel. Consider an example where the first AFE is configured through the flexible routing switch to measure the voltage between IN1 and IN2, and the second AFE is configured through the flexible routing switch to measure the voltage between IN2 and IN3.

In this configuration, if digital AC LOD test currents are applied to the inputs of both AFEs, the test current that is applied to the negative input of the first AFE and the test current that is applied to the positive input of the second AFE are both flowing through IN2. Depending on the sign of the test current in the second AFE, these currents can add up or cancel each other. If the currents add up, the system will correctly measure the differential input impedance on both AFE channels. If the currents on IN2 cancel, the test current will only flow through IN1 and IN3, and the impedance of the electrode connected to IN2 cannot be measured. To apply the digital AC LOD to CH3 and CH2, set  $EN_LOD[2] = 1$  and  $EN_LOD[1] = 1$ . Then, by programming  $EN_LOD[5] = 0$  and  $EN_LOD[4] = 1$ , CH3 and CH2 will receive excitation currents in-phase and anti-phase, respectively.

# 8.3.19 Clock Oscillator

The ADS1293 is designed to operate from a 409.6-kHz clock. This clock can be generated by an on-chip crystal oscillator or provided externally on the bi-directional CLK. The high-accuracy low-power on-chip crystal oscillator will work with an external 4.096 MHz crystal connected between the XTAL1 and XTAL2 pins, each of which must be loaded with a 20-pF capacitor to get an accurate oscillation frequency. The output frequency of the on-chip crystal oscillator is divided by 10 to generate the required 409.6-kHz clock frequency as shown in Figure 27.



Figure 27. Block Diagram of the Clock

Even though the required oscillation frequency of the external crystal is rated at 4.096 MHz, both the oscillator and the chip can tolerate a wider crystal oscillation frequency (3.7 MHz to 4.5 MHz). Note though that the output data rate and bandwidth of the SINC filters given in Table 8 through Table 11 will scale according to the crystal oscillation frequency.

When the internal clock is used, the generated clock can be brought off chip through the CLK pin. Its output driver is enabled by configuring bit  $EN_CLKOUT = 1$  in the OSC\_CN register, allowing a multichip system to operate synchronously from a single crystal oscillator. Setting bit STRTCLK = 1 allows the internal 409.6-kHz clock to propagate to the digital circuitry and to the output driver of the CLK pin.

The internal crystal oscillator can be shut down to save power or when the clock of the device is provided externally. Configuring bit SHDN\_OSC = 1 powers down the internal crystal oscillator and enables the input driver of the CLK pin. The external clock should have a frequency of 409.6kHz with a duty cycle of 50% to get the SINC filter bandwidth given in Table 8 through Table 11. The chip can tolerate a wider frequency range and clock duty cycle on this pin (see the External Clock Frequency and the External Clock Duty Cycle parameters in the Clock section of the *Electrical Characteristics* table) in exchange of scaling up or down the bandwidth of the SINC filters. Setting bit STRTCLK = 1 allows the external 409.6 kHz clock to propagate to the digital circuitry.

The STRTCLK bit is designed to ensure all critical blocks of the chip get a clean clock start. The clock source should first be configured and allowed to start up using the SHDN\_OSC and EN\_CLKOUT bits, and subsequently, the STRTCLK bit can be set high.

The oscillator control register bits are summarized in Table 6. In a multichip system, the CLK pins of the master and slaves should be connected together. The master should be configured to generate a clock on the CLK pin while the slaves should use the CLK pin as a clock input source.



			5
STRTCLK	SHDN_OSC	EN_CLKOUT	CLOCK PROPAGATION
0	Х	Х	No clock
1	0	0	Internal clock to digital circuitry
1	0	1	Internal clock to digital circuitry and CLK pin
1	1	Х	External clock to digital circuitry

Table 6. Clock Oscillator Configuration Bits

### 8.3.20 Synchronization

There are three filter timing generators implemented to support independent filter settings. Under normal conditions, the filters always start synchronized when the START\_CON bit in the CONFIG register is set to 1, and will remain synchronized. Synchronization can also be continually enforced for the eventuality of a channel losing synchronization, and it can be used in single-chip and multiple-chip systems.

# 8.3.21 Single-Chip Multi-Channel Synchronization

The filter channels are synchronized when DRDYB assertion is at a fixed frequency and new data from each source is available at some integer multiple of DRDYB. This synchronization mode requires that the fastest output data source is selected to drive DRDYB in the DRDYB\_SRC register.

The filter channels will start synchronized if the output data rates in all channels are the same or integer multiples of each other. Synchronization between channels will be continuously enforced as long as the slowest output source is selected as the synchronization source in the SYNCB\_CN register. The SYNCB pin output driver can be disabled in a single-chip system, regardless of the synchronization source selected, and synchronization will continue to be enforced between channels. The SYNCB output driver is disabled programming bit DIS\_SYNCBOUT=1 in the SYNCB\_CN register.

# 8.3.22 Multichip Synchronization

Synchronization in a multiple ADS1293 system is achieved when all the devices share a common clock and synchronization source. The common clock source,  $f_{OSC}$ , can be driven from the CLK pin of an ADS1293 when its CLK pin output driver is enabled in the OSC\_CN register. The common synchronization source can be driven from the SYNCB pin of the device with the slowest data rate in the system. An ADS1293 is configured as a synchronization source by enabling its SYNCB output driver and selecting the slowest data rate channel to drive the line in the SYNCB\_CN register. The SYNCB\_CN register of the other devices should be programmed to 0x40 to configure their SYNCB pins as inputs. When configured as an output, SYNCB is driven on the falling edge of  $f_{OSC}$  and when configured as an input, SYNCB is sampled on the rising edge of  $f_{OSC}$ .

# 8.3.23 Synchronization Errors

Detected synchronization events are reported to the ERROR\_SYNC register. A phase error is generated when the phase of divided clocks of the timing generator has been adjusted to comply with the SYNCB input signal. A timing error is generated when the timing of the indicated channel has been updated to comply with the timing of the synchronization source, internal or external. By default, a synchronization error will propagate to the ALARMB output pin. Reporting of a synchronization error can be disabled in the MASK\_ERR register.

# 8.3.24 Alarm Functions

The ADS1293 has multiple warning flags to diagnose possible fault conditions in the ECG-monitoring application. The warning flags can be read in the *Error Status Registers*. The system errors are filtered by the digital circuitry (see *Error Filtering*), and for this reason, the master clock must be active for the alarms to be reflected in the error registers.

- 1. **ERROR\_LOD:** Indicates which input has a lead-off error. The lead-off detection was described in *Lead-Off Detection (LOD)*.
- 2. **ERROR\_STATUS:** Contains the following error flags:
  - **SYNCEDGEERR:** This flag is raised when a synchronization error occurs, as described in *Synchronization Errors*.
  - CH3ERR: This flag is raised when one of the 5 LSBs or bit 6 of the ERROR\_RANGE3 register is a logic
     1. It indicates an out-of-range condition at the AFE in channel 3. These error conditions are described in *Instrumental Amplifier Fault Detection* and in *Sigma-Delta Modulator Fault Detection*.



- CH2ERR: See above, but for channel 2.
- CH1ERR: See above, but for channel 1.
- LEADOFF: This error flag is raised when one of the OUT\_LOD bits in the ERROR\_LOD register is a logic 1.
- BATLOW: This error flag is raised when the supply voltage of the ADS1293 drops below 2.7 V. This can be used as a warning sign to the microcontroller that the state of charge of a supply battery is almost below levels of operation. The ADS1293 is designed to function within specification for supplies larger than 2.7 V but communication the digital communication interface will work down to 2.4 V so that this alarm condition can still be communicated to the microcontroller. A low battery error propagates to the ALARMB pin unless the MASK\_BATLOW bit in the MASK\_ERR register is set to 1. System alarms are filtered by the digital circuitry (see *Error Filtering*), and for this reason, the master clock must be active in order to capture an alarm. There is also a battery voltage monitoring feature that can be used to monitor the state of charge of the battery during normal operation described in *Battery Monitoring*.
- RLDRAIL: This error flag is raised when the output voltage of the right-leg drive amplifier is approaching the supply rails. The flag goes high when the output voltage of the common-mode detector is 200 mV away from either supply rail. This condition would occur if the common-mode on the patient's body is far away from the target value and as a result the right-leg drive amplifier needs to deliver a lot of charge to the patient's body to restore the common-mode voltage. In this scenario, the common-mode may still be inside the range of the instrumentation amplifier and the ECG signal may still be accurately acquired.
- CMOR: The CMOR error flag is raised when the output voltage of the common-mode detector is 750 mV away from either supply rail. In this case, the common-mode voltage detected on the patient's body is outside of the input CMVR where the instrumentation amplifier can process the full differential input signal (see *Instrumentation Amplifier (INA)*). When this flag is raised, the ECG signal accuracy may be lost.
- 3. ERROR\_RANGE1, ERROR\_RANGE2, ERROR\_RANGE3: These registers contain the out-of-range error signals of the AFEs in the three channels. The flags in these registers are described in *Instrumentation Amplifier Fault Detection* and in *Sigma-Delta Modulator Fault Detection*.
- 4. **ERROR\_SYNC:** This register contains flags that indicate certain synchronization errors have been detected. These errors have been described in *Synchronization Errors*.
- 5. **ERROR\_MISC:** This register contains status flags for common-mode out-of-range, right-leg drive near rail and low battery errors.

# 8.3.25 Error Filtering

The alarms that are generated by the analog circuitry inside the ADS1293 are filtered by digital logic. Alarms will only be accepted if they are active for a number of consecutive digital clock cycles, which toggle on the falling edge of the 409.6-kHz oscillator clock. The number of digital clock cycles that an alarm will have to be active before it is accepted is programmable between 1 and 16 counts using the ALARM\_FILTER register. This register contains two separate filter parameters. The 4 LSBs in this register program the filtering of the lead-off detect error bits. The 4 MSBs program the filtering of the instrumentation amplifier signal out-of-range errors, the sigma-delta input over range errors, and the CMOR, RLDRAIL and BATLOW errors.

# 8.3.26 ALARMB Pin and Error Masking

The ADS1293 has an ALARMB output pin. This open-drain output will go low when a new alarm condition occurs in the ERROR\_STATUS register. The ALARMB pin can be used as an interrupt signal to a microcontroller to warn about error conditions that can potentially corrupt the data that is being collected so that the microcontroller can take appropriate preventive action. The functionality of the ALARMB pin is flexible and programmable using the MASK\_ERR register. This register allows masking some of the errors in the *ERROR\_STATUS* register so that certain alarm events will not trigger a high to low transition on the ALARMB pin.

# 8.3.27 Error Register Automatic Clearing Description

All error bits in the registers 0x18 through 0x1E are latched in a high state when an error occurs and will only return to zero after being read. The error bits will remember an error until the user reads the error. The sign bits in the CH1ERR, CH2ERR and CHR3ERR registers are latched on low to high transition of the DIF\_HIGH transitions in the corresponding registers. In this way, when the differential signal goes out-of-range, the sign of the signal can also be detected when the alarm register is read. Upon read, the error bits will be cleared. If the



error condition has disappeared before the error is read, the error bits will remain low after being read. For all error registers, except *ERROR\_STATUS*, the error bits will return to their high state within a few internal clock cycles if the error condition is still present after a register read. The bits in the *ERROR\_STATUS* register only respond to new errors. If an error persists after the *ERROR\_STATUS* register is read, the error condition will not be reflected in the error status register and the ALARMB pin will not pulse low again.

# 8.3.28 Alarm Propagation

Figure 28 shows how the alarms propagate through the digital circuitry inside the ADS1293. The errors propagate from left to right. Synchronization errors are not filtered because they are generated synchronously inside the digital circuitry, and if they occur, they are latched in the *ERROR\_SYNC* register. Lead-off detect errors are filtered by a counter programmed in the 4 LSBs of the ALARM\_FILTER register and are latched in the *ERROR\_LOD* register. The instrumentation amplifier out-of-range, sigma-delta over range, right-leg drive amplifier out-of-range, common-mode amplifier out-of-range and low battery signals are also filtered by a counter programmed in the *ALARM\_FILTER* register. The out-of-range signals for the 3 channels are latched in the *ERROR\_RANGE1, ERROR\_RANGE2* and *ERROR\_RANGE3* registers. The first 6 registers on the right-hand side of the circuit latch errors until the error is being read. After being read, the error bit will be reset, but it will return to a logic 1 if the internal alarm condition persists. After being filtered the alarms are all routed to a digital logic block that detects whether a new alarm has occurred. If this happens, the appropriate bit in the *ERROR\_STATUS* register will be reset and the *ALARMB* pin will be pulled down. The bits in the *ERROR\_STATUS* register will be reset and the ALARMB pin will released when the *ERROR\_STATUS* register is read.



Figure 28. Graphical Illustration of Alarm Propagation

# 8.3.29 Reference Voltage Generators

The common-mode and right-leg drive reference generates VDD/2.2 volts, which are present on the RLDREF pin. This reference is used as an internal common-mode reference, as the reference for the analog pace channel, and should be powered on at all times when a sigma-delta modulator is running. It can be powered down by programming bit SHDN\_CMREF=1 in the REF\_CN register. The RLDREF pin should have a  $0.1-\mu$ F bypass capacitor-to-ground.

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The internal reference,  $V_{REF}$ , generates 2.4 V, which are present on the CVREF pin. The CVREF pin must have a 1  $\mu$ F bypass capacitor-to-ground with low ESR and is not designed to be loaded with other circuitry. This reference should also be powered on at all times when a sigma-delta modulator is running. It can be powered down programming bit SHDN\_REF=1 in the REF\_CN register. It is possible to provide the reference voltage externally on this pin when the internal reference generator is shut down.

All three voltage generators require a somewhat larger start up time compared to the other circuit blocks inside the ADS1293, which is why they are treated differently in the global power-down or standby states, as will be described in the next section.

### 8.3.30 Power Management

The ADS1293 has many features that allow the optimization of power consumption. The common-mode detector and right-leg drive amplifier can be configured to achieve the optimum AC performance to power consumption ratio in a given application environment. Almost all internal circuit blocks can be powered down to reduce power consumption. Table 7 lists the typical power consumption budget for all of the circuit blocks that can be individually powered down.

There are two master control bits, PWR\_DOWN and STANDBY, in addition to the power-down control bits that are used to power-down an individual circuit block, and they are located in the CONFIG register. In the power-down mode, all circuits that can be powered down are powered down, irrespective of the state of their individual shutdown bits. With the PWR\_DOWN bit, the entire ADS1293 can be quickly placed in its minimal current consumption state without needing to do many individual configuration register writes. The STANDBY bit operates in a similar manner, but it does not affect the state of the three voltage generators and the crystal oscillator inside the ADS1293, which require a somewhat longer time to start up. When placing the ADS1293 can return to operation quicker. The difference between the current consumption in power-down and in standby depends on the logic state of the shutdown bits of the two reference voltage generators and the crystal oscillator, as described in Table 7.

Table 7 specifies the current consumption of the blocks that are always ON in the first row. The second group in the table specifies the current consumption of the two reference voltage generators and the crystal oscillator that are OFF in power-down mode but that remain active during standby mode. The last group of circuit blocks in the table specifies the current consumption of the other circuit blocks. The ADS1293 will need about 100 ms to return to operation after being powered down. The time to recover from standby is limited by the time latency of the programmable logic filters in the AFE channels, as described in the *Filter Settling Time* section.

GLOBAL POWER CONTROL	BLOCK NAME	CONDITIONS / NOTES	CURRENT µA
Always on	Supporting circuitry		80
	Reference voltage generator		17
Off in power-down	Right-leg drive reference		9
	Crystal oscillator		7
	Instrumentation amplifier	low-power, per channel	38
		high-resolution, per channel	121
	Analog front end fault detect	Per channel	2
	Sigma dalta modulator	102.4kHz, per channel	22
		204.8kHz, per channel	41
Off in standby	Analog output channel		29
	Lead-off detect	Excluding excitation currents	25
	Wilson reference	per channel	7
	Common mode detector	low-speed, cap drive 1, 6 active leads	39
		high-speed, cap drive 4, 6 active leads	79
	Pight log drive emplifier	low-speed, cap drive 1	20
		high-speed, cap drive 4	60

# Table 7. Typical Current Consumption Per Block



# 8.4 Device Functional Modes

A channel can be configured in different modes of operation that allow optimizing for performance and power consumption as required for an application. Further more, the on-chip programmable digital filters provide a range of bandwidth and output data rate configurations that result in different levels of performance.

### 8.4.1 Low Sampling Rate

The following tables summarize the output data rate, digital filter bandwidth and typical RMS noise of a channel for every decimation ratio combination possible when the sigma-delta modulator is configured for a sampling rate of 102.4 kHz. Table 8 shows the channel parameters when the standard pace data rate is selected, and Table 9 shows the channel parameters when the double pace data rate is selected. The sampling rate of the sigma-delta modulator is selected in the AFE\_RES register and the pace data rate is selected in the R1\_RATE register.

		PACE CHANNEL			ECG CHANNEL					
					540				RMS	NOISE
R2	R3	ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	NOISE [mV]	ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	LOW POWER [µV]	HIGH RES [µV]
	4					0x800000	1600	325	4.47	4.16
	6					0xF30000	1067	215	3.42	3.05
	8		0.400			0x800000	800	160	2.92	2.57
4	12	0,000		1200	1 610	0xF30000	533	105	2.37	2.07
	16	00000	6400	1300	1.012	0x800000	400	80	2.06	1.81
	32					0x800000	200	40	1.50	1.29
	64					0x800000	100	20	1.12	0.94
	128					0x800000	50	10	0.85	0.70
	4					0xC35000	1280	260	3.82	3.42
	6	-		1040	0.572	0xB964F0	853	175	3.02	2.67
	8		5120			0xC35000	640	130	2.60	2.29
F	12	0xC350				0xB964F0	427	85	2.13	1.86
Э	16					0xC35000	320	65	1.86	1.62
	32					0xC35000	160	32	1.36	1.16
	64					0xC35000	80	16	1.02	0.85
	128					0xC35000	40	8	0.79	0.64
	4			870	0.238	0xF30000	1067	215	3.41	3.04
	6					0xE6A900	711	145	2.74	2.42
	8					0xF30000	533	110	2.38	2.07
C	12	0, 5200	4067			0xE6A900	356	70	1.96	1.70
0	16	0XF300	4267			0xF30000	267	55	1.71	1.48
	32					0xF30000	133	27	1.25	1.07
	64					0xF30000	67	13	0.94	0.79
	128					0xF30000	33	7	0.74	0.60
	4					0x800000	800	160	2.91	2.58
	6					0xF30000	533	110	2.37	2.08
	8					0x800000	400	80	2.08	1.79
0	12	0x8000	2200	650	0.060	0xF30000	267	55	1.71	1.48
8	16		3200	050	0.060	0x800000	200	40	1.50	1.29
	32	]				0x800000	100	20	1.12	0.94
	64	]				0x800000	50	10	0.85	0.70
	128					0x800000	25	5	0.68	0.54

### Table 8. Channel Parameters With SDM Running at 102.4 kHz and at Standard Pace Data Rate (R1 = 4)<sup>(1)</sup>

(1) 10000 consecutive readings were used to calculate the RMS noise values in this table.

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# Table 9. Channel Parameters With SDM Running at 102.4 kHz and at Double Pace Data Rate (R1 = 2)<sup>(1)</sup>

		PACE CHANNEL			ECG CHANNEL					
					DMC				RMS	NOISE
R2	R3	ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	NOISE [mV]	ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	LOW POWER [µV]	HIGH RES [µV]
	4					0x800000	3200	640	38.17	37.92
	6					0xF30000	2133	430	7.04	6.72
	8		40000			0x800000	1600	320	4.35	3.93
4	12	0,0000		1000	1 470	0xF30000	1067	215	3.40	3.02
	16	000000	12600	1260	1.479	0x800000	800	160	2.92	2.57
	32					0x800000	400	80	2.08	1.79
	64					0x800000	200	40	1.49	1.29
	128					0x800000	100	20	1.11	0.93
5	4			1030		0xC35000	2560	510	12.64	12.38
	6		10240		0.540	0xB964F0	1707	340	4.53	4.12
	8					0xC35000	1280	255	3.74	3.35
	12	0xC350				0xB964F0	853	170	3.01	2.65
	16					0xC35000	640	130	2.59	2.28
	32					0xC35000	320	65	1.86	1.62
	64					0xC35000	160	32	1.36	1.16
	128					0xC35000	80	16	1.02	0.85
	4					0xF30000	2133	420	6.20	5.88
	6					0xE6A900	1422	285	3.94	3.57
	8					0xF30000	1067	210	3.38	3.02
e	12	075200	0500	960	0.000	0xE6A900	711	140	2.74	2.42
0	16	UXF300	0000	860	0.228	0xF30000	533	105	2.37	2.07
	32					0xF30000	267	55	1.70	1.47
	64					0xF30000	133	26	1.26	1.07
	128					0xF30000	67	13	0.95	0.78
	4					0x800000	1600	320	4.14	3.73
	6					0xF30000	1067	215	3.35	2.96
	8					0x800000	800	160	2.89	2.54
0	12	0x8000	6400	CE0	0.059	0xF30000	533	110	2.37	2.07
0	16		6400	650	0.056	0x800000	400	80	2.06	1.79
	32					0x800000	200	40	1.50	1.29
	64					0x800000	100	20	1.11	0.94
	128					0x800000	50	10	0.85	0.70

(1) 10000 consecutive readings were used to calculate the RMS noise values in this table.



### 8.4.2 High Sampling Rate

The following tables summarize the output data rate, digital filter bandwidth and typical RMS noise of a channel for every decimation ratio combination possible when the sigma-delta modulator is configured for a sampling rate of 204.8 kHz. Table 10 shows the channel parameters when the standard pace data rate is selected, and Table 11 shows the channel parameters when the double pace data rate is selected. The sampling rate of the sigma-delta modulator is selected in the AFE\_RES register and the pace data rate is selected in the R1\_RATE register.

Table 10. Channel	<b>Parameters With S</b>	DM Running at 20	04.8 kHz and at 3	Standard Pace Data	a Rate (R1 =
		<b>4</b> ) <sup>(1)</sup>			•
		•,			

		PACE CHANNEL			ECG CHANNEL					
					RMS NOISE					
R2	R3	ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	RMS NOISE [mV]	ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	LOW POWER [µV]	HIGH RES [µV]
4	4	0x8000	12800	2600	1.738	0x800000	3200	640	5.20	4.59
	6					0xF30000	2133	430	3.92	3.38
	8					0x800000	1600	325	3.32	2.86
	12					0xF30000	1067	215	2.69	2.31
	16					0x800000	800	160	2.34	1.99
	32					0x800000	400	80	1.68	1.43
	64					0x800000	200	40	1.25	1.04
	128					0x800000	100	20	0.95	0.78
	4		10240	2080	0.613	0xC35000	2560	520	4.36	3.81
	6					0xB964F0	1707	350	3.44	2.96
	8	0xC350				0xC35000	1280	260	2.95	2.54
F	12					0xB964F0	853	170	2.41	2.06
Э	16					0xC35000	640	130	2.10	1.79
	32					0xC35000	320	65	1.53	1.29
	64					0xC35000	160	32	1.14	0.95
	128					0xC35000	80	15	0.88	0.72
	4	0xF300	8533	1740	0.256	0xF30000	2133	430	3.91	3.38
	6					0xE6A900	1422	290	3.12	2.68
	8					0xF30000	1067	215	2.68	2.30
6	12					0xE6A900	711	140	2.21	1.88
0	16					0xF30000	533	110	1.93	1.64
	32					0xF30000	267	55	1.41	1.18
	64					0xF30000	133	27	1.06	0.88
	128					0xF30000	67	13	0.83	0.68
	4	0x8000	6400	1300		0x800000	1600	325	3.32	2.86
	6				0.064	0xF30000	1067	215	2.69	2.31
8	8					0x800000	800	160	2.34	2.00
	12					0xF30000	533	105	1.93	1.64
	16					0x800000	400	80	1.69	1.44
	32					0x800000	200	40	1.25	1.04
	64					0x800000	100	20	0.96	0.78
	128					0x800000	50	10	0.76	0.61

(1) 10000 consecutive readings were used to calculate the RMS noise values in this table.

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# Table 11. Channel Parameters With SDM Running at 204.8 kHz and at Double Pace Data Rate (R1 = 2)<sup>(1)</sup>

R2	R3	PACE CHANNEL			ECG CHANNEL					
					RMS NOISE					
		ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	NOISE [mV]	ADC <sub>MAX</sub>	ODR [Hz]	BW [Hz]	LOW POWER [µV]	HIGH RES [µV]
4	4		25600	2550	1.592	0x800000	6400	1280	41.27	40.81
	6					0xF30000	4267	850	7.79	7.32
	8					0x800000	3200	640	4.97	4.35
	12					0xF30000	2133	430	3.88	3.36
	16					0x800000	1600	325	3.32	2.85
	32					0x800000	800	160	2.34	1.98
	64					0x800000	400	80	1.69	1.43
	128					0x800000	200	40	1.25	1.04
	4		20480	2050	0.580	0xC35000	5120	1020	13.57	13.38
	6					0xB964F0	3413	680	5.18	4.56
	8					0xC35000	2560	510	4.30	3.73
5	12	0,0250				0xB964F0	1707	340	3.41	2.94
	16					0xC35000	1280	260	2.94	2.53
	32					0xC35000	640	130	2.10	1.79
	64					0xC35000	320	65	1.53	1.29
	128					0xC35000	160	32	1.14	0.95
	4	0xF300	17067	1720	0.245	0xF30000	4267	850	6.99	6.43
	6					0xE6A900	2844	570	4.53	3.94
	8					0xF30000	2133	420	3.86	3.33
6	12					0xE6A900	1422	285	3.11	2.67
0	16					0xF30000	1067	215	2.69	2.29
	32					0xF30000	533	110	1.93	1.64
	64					0xF30000	267	55	1.41	1.18
	128					0xF30000	133	26	1.06	0.88
	4	0x8000	12800	1300	0.062	0x800000	3200	640	4.74	4.15
8	6					0xF30000	2133	425	3.82	3.28
	8					0x800000	1600	320	3.29	2.83
	12					0xF30000	1067	215	2.68	2.30
	16					0x800000	800	160	2.34	2.00
	32					0x800000	400	80	1.69	1.42
	64					0x800000	200	40	1.25	1.05
	128					0x800000	100	20	0.95	0.79

(1) 10000 consecutive readings were used to calculate the RMS noise values in this table.

# 8.4.3 Ouput Code (ADC<sub>OUT</sub>)

The ADC<sub>OUT</sub> of the ADS1293 is due to a differential voltage applied between the positive and negative input terminals of the instrumentation amplifier and can be calculated with Equation 13:

$$ADC_{OUT} = \left[\frac{3.5 \left(V_{INP} - V_{INM}\right)}{2 V_{REF}} + \frac{1}{2}\right] ADC_{MAX}$$
(13)

(13)

The reference voltage  $V_{REF}$ , equals to 2.4 V if the on-chip voltage reference is used. ADC<sub>MAX</sub> represents the maximum output code of the ADC, which corresponds to a theoretical 2.4-V signal at the input of the SDM. The value of ADC<sub>MAX</sub> changes with the configuration of the digital filters, and the corresponding value can be found in Table 8, Table 9, Table 10, and Table 11. Note that ADC<sub>OUT</sub> equals ADC<sub>MAX</sub>/2 for a OV differential input.


#### 8.5 Programming

#### 8.5.1 Serial Digital Interface

A serial peripheral interface (SPI) allows access to the control registers of the ADS1293. The serial interface is a generic 4-wire synchronous interface compatible with SPI type interfaces used on many microcontrollers and DSP controllers.

#### 8.5.2 Digital Output Drive Strength

The strength of the transistors driving the serial data out pin (SDO) can be programmed to four levels in the DIGO\_STRENGTH register. The drive strength will affect the slope of the digital output signal edges, and the optimal drive strength will depend on the capacitive loading on the SDO pin, where larger capacitive loads require larger drive strength. The output drive strength configurability may help reduce interference from the SPI communication into the AFE signal path. In this sense, it is advised to use the lowest drive strength that works for a particular system.

#### 8.5.3 SPI Protocol

A typical serial interface access cycle is exactly 16 bits long, which includes an 8-bit command field (R/WB + 7bit address) to provide for a maximum of 128 direct access addresses, and an 8-bit data field. Figure 29 shows the access protocol used by this interface. Extended access cycles are possible and they are described in the *Auto-Incrementing Address* and *Streaming* sections.



Figure 29. Serial Interface Protocol



## **Programming (continued)**

Each assertion of chip select bar (CSB) starts a new register access. The R/Wb bit in the command field configures the direction of the access operation; a value of 0 indicates a write operation and a value of 1 indicates a read operation. All output data is driven on the falling edge of the serial clock (SCLK), and for the 16-bit protocol, SDO read data is driven on the falling edge of clocks 8 through 15. All input data on the serial data in (SDI) pin is sampled on the rising edge of SCLK and is written into the register on the rising edge of the 16th clock. The user is required to deassert CSB after the 16th clock; if CSB is deasserted before the 16th clock, no data write will occur.

#### 8.5.4 Random Register Access Protocol

The 16-bit protocol is useful for random address access. CSB must be asserted during 16 clock cycles of SCLK.

#### 8.5.5 Auto-Incrementing Address

An access cycle may be extended to multiple registers by simply keeping the CSB asserted beyond the stated 16 clocks of the standard 16-bit protocol. In this mode, CSB must be asserted during 8\*(1+N) clock cycles of SCLK, where N is the amount of bytes to write or read during the access cycle. The auto-incrementing address mode is useful to access a block of registers of incrementing addresses.

For example, to read the pace and ECG data registers located from address 0x30 to address 0x3F and worth 16 bytes of data, follow the next steps:

- 1. Execute a read command to address 0x30.
- 2. Extend the CSB assertion during 136 clock cycles (8+8\*16).

During an auto-incrementing read access, SDO outputs the register contents every 8 clock cycles after the initial 8 clocks of the command field. During an auto-incrementing write access, the data is written to the registers every 8 clock cycles after the initial 8 clocks of the command field.

Automatic address increment stops at address 0x4F for both write and read operations.

#### 8.5.6 Streaming

A read access cycle can operate in streaming mode, also referred to as loop read-back mode, by performing a read operation from the DATA\_LOOP register and extending the CSB assertion beyond the standard 16 clocks. The streaming mode is supported for the DATA\_STATUS, DATA\_CH1\_PACE, DATA\_CH2\_PACE, DATA\_CH3\_PACE, DATA\_CH1\_ECG, DATA\_CH2\_ECG and DATA\_CH3\_ECG registers described in Pace and ECG Data Read Back Registers. The streaming mode is useful to access the block of pace and ECG data registers when not all data needs to be read. The channels to read in this mode are selected in the CH\_CNFG register. In this mode, CSB must be asserted during 8\*(1+N) clock cycles, where N is the number source bytes enabled in CH\_CNFG. The source for pace data is 2 bytes long; the source for ECG data is 3 bytes long, and the source for data status is 1 byte long.

For example, to read the *DATA\_STATUS*, *DATA\_CH3\_PACE* and *DATA\_CH3\_ECG* registers located at address 0x30, 0x35 and 0x3D and worth 6 bytes of data, follow the next steps:

- 1. Write a value of 0x49 to the CH\_CNFG register (address 0x2F).
- 2. Read from the DATA\_LOOP register (address 0x50).
- 3. Extend the CSB assertion for 56 clock cycles (8+8\*6).

#### 8.5.7 Data Ready Bar

Data ready bar (DRDYB) is an active low-output signal and is asserted when new data is ready to be read. After DRDYB is asserted and an SPI read of ECG or PACE data occurs, DRDYB will be deasserted at the 14th rising edge of SCLK.



## Programming (continued)



Figure 30. DRDYB Behavior for a Complete Read Operation

New data is available regardless of the serial interface being ready to read the data or not, and therefore, the data is lost if it is not read before the next DRDYB assertion. If DRDYB is asserted and the data is not read, DRDYB is automatically deasserted at least t<sub>DRDYB</sub> seconds before the next DRDYB assertion. The value for t<sub>DRDYB</sub> can be found in Figure 1 and Figure 2.



The source channel driving the assertion of the DRDYB signal can be configured in the DRDYB\_SRC register. In order to see the DRDYB output pin asserted, one bit of this register must be set to 1 to select the digital channel to drive it. Multiple channels should not be selected to drive the DRDYB output pin, otherwise, it will result in unexpected behavior. The selected channel should not be shut down in the AFE\_SHDN\_CN register, and if the source is an ECG channel, its filter should not be disabled in the DIS\_EFILTER register. TI strongly recommends selecting the channel with the fastest data rate as the source for the DRDYB signal to avoid loss of data.

By default, the DRDYB signal is masked during the first few data samples after the start of a conversion or when a synchronization error is detected. If any ECG channel is enabled, DRDYB is masked during the first six data samples of the slowest enabled ECG channel. If all ECG channels are disabled, DRDYB is masked for the first six data samples of the slowest enabled pace channel when the data rate is 1xODR, and for the first eleven data samples of the slowest enabled pace channel when the data rate is 2xODR. Masking can be disabled in the MASK DRDYB register.

#### 8.5.8 Simultaneous ECG and Pace Data Read

Each of the three digital channels of the ADS1293 provides a high-performance path for ECG monitoring and a lower-resolution path for monitoring of pace-maker signals. The digitized signals from these two paths can be read simultaneously from the Pace and ECG Data Read Back Registers.

The ECG signal path achieves higher resolution than the PACE signal path by having one extra filtering stage (as shown in Sinc Filters). Due to the difference in filtering stages of the two paths, the PACE data is available for reading at a much higher rate than the ECG data. In this sense, the PACE channel must be selected as the driving source of the DRDYB signal.

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## **Programming (continued)**

In the *Streaming* mode, the data from the DATA\_LOOP register should be read after the DRDYB line is asserted; this means that new data is available. In order to read both ECG and PACE data from the DATA\_LOOP register, the channels of interest must be enabled in the CH\_CNFG register.

As an example, the <u>3-Lead ECG Application</u> can be reconfigured to perform simultaneous ECG and PACE data reads from channel 1:

- 1. Set address 0x00 = 0x00: Stops data conversion (if any).
- 2. Set address 0x2F = 0x32: Enables channel 1 PACE, channel 1 ECG, and channel 2 ECG for loop. read-back mode
- 3. Set address 0x27 = 0x01: Reconfigures the DRDYB source to channel 1 PACE .
- 4. Set address 0x00 = 0x01: Starts data conversion.

In this case, new PACE data from channel 1 is available on every DRDYB assertion; ECG data from channel 1 and channel 2, on the other hand, is available every six DRDYB assertions (R3\_RATE\_CH1 = R3\_RATE\_CH2 = 6).

There are different approaches for handling simultaneous ECG and PACE data read. One approach is to read ECG data every time that PACE data is ready, over-sampling the ECG channel. This is possible because old conversion values are retained in the data registers until new data overwrites them.

A second approach is to also read the DATA\_STATUS register. Continuing from the steps above:

- 5. Set address 0x00 = 0x00: Stops data conversion.
- 6. **Set address 0x2F = 0x33:** Enables data ready status, channel 1 PACE, channel 1 ECG, and channel 2. ECG for loop read-back mode
- 7. Set address 0x00 = 0x01: Starts data conversion.

The DATA\_STATUS register indicates the channel(s) that are updated at a given DRDYB assertion; this information can potentially be used to discard irrelevant data.

A third and more complex approach is to continuously reprogram the CH\_CNFG register based on the contents of DATA\_STATUS register. The CH\_CNFG register should be reprogrammed to read PACE+ECG data only when the DATA\_STATUS register indicates ECG data is available. After reading the PACE+ECG data, the CH\_CNFG register should be reprogrammed back to reading only the DATA\_STATUS register and the PACE data. In this case, the ECG data is not oversampled and the SPI communication can be significantly reduced for cases where a decimation rate, R3\_RATE\_CHx, is large. The reconfiguration of the CH\_CNFG register should be done before the next DRDYB assertion to avoid losing data.



## 8.6 Register Maps

- 1. If written to, RESERVED bits must be written to 0 unless otherwise indicated.
- 2. Read back value of RESERVED bits and registers is unspecified and should be discarded.
- 3. Recommended values must be programmed and forbidden values must not be programmed where they are indicated in order to avoid unexpected results.
- 4. If written to, registers indicated as Reserved must have the indicated default value as shown in the register map. Any other value can cause unexpected results.

REGISTER NAME	DESCRIPTION	ADDRESS	ACCESS	DEFAULT
Operation Mode Registers	1			
CONFIG	Main Configuration	0x00	R/W	0x02
Input Channel Selection Reg	isters	ų.		ł
FLEX_CH1_CN	Flex Routing Switch Control for Channel 1	0x01	R/W	0x00
FLEX_CH2_CN	Flex Routing Switch Control for Channel 2	0x02	R/W	0x00
FLEX_CH3_CN	Flex Routing Switch Control for Channel 3	0x03	R/W	0x00
FLEX_PACE_CN	Flex Routing Switch Control for Pace Channel	0x04	R/W	0x00
FLEX_VBAT_CN	Flex Routing Switch for Battery Monitoring	0x05	R/W	0x00
Lead-off Detect Control Regi	isters	i.		
LOD_CN	Lead-Off Detect Control	0x06	R/W	0x08
LOD_EN	Lead-Off Detect Enable	0x07	R/W	0x00
LOD_CURRENT	Lead-Off Detect Current	0x08	R/W	0x00
LOD_AC_CN	AC Lead-Off Detect Control	0x09	R/W	0x00
Common-Mode Detection an	d Right-Leg Drive Feedback Control Registers	i.		
CMDET_EN	Common-Mode Detect Enable	0x0A	R/W	0x00
CMDET_CN	Common-Mode Detect Control	0x0B	R/W	0x00
RLD_CN	Right-Leg Drive Control	0x0C	R/W	0x00
Wilson Control Registers	•			•
WILSON_EN1	Wilson Reference Input one Selection	0x0D	R/W	0x00
WILSON_EN2	Wilson Reference Input two Selection	0x0E	R/W	0x00
WILSON_EN3	Wilson Reference Input three Selection	0x0F	R/W	0x00
WILSON_CN	Wilson Reference Control	0x10	R/W	0x00
Reference Registers				
REF_CN	Internal Reference Voltage Control	0x11	R/W	0x00
<b>OSC Control Registers</b>				
OSC_CN	Clock Source and Output Clock Control	0x12	R/W	0x00
AFE Control Registers				
AFE_RES	Analog Front End Frequency and Resolution	0x13	R/W	0x00
AFE_SHDN_CN	Analog Front End Shutdown Control	0x14	R/W	0x00
AFE_FAULT_CN	Analog Front End Fault Detection Control	0x15	R/W	0x00
RESERVED	—	0x16	R/W	0x00
AFE_PACE_CN	Analog Pace Channel Output Routing Control	0x17	R/W	0x01
Error Status Registers				
ERROR_LOD	Lead-Off Detect Error Status	0x18	RO	
ERROR_STATUS	Other Error Status	0x19	RO	
ERROR_RANGE1	Channel 1 AFE Out-of-Range Status	0x1A	RO	
ERROR_RANGE2	Channel 2 AFE Out-of-Range Status	0x1B	RO	—
ERROR_RANGE3	Channel 3 AFE Out-of-Range Status	0x1C	RO	_
ERROR_SYNC	Synchronization Error	0x1D	RO	
ERROR_MISC	Miscellaneous Errors	0x1E	RO	0x00

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# **Register Maps (continued)**

REGISTER NAME	DESCRIPTION	ADDRESS	ACCESS	DEFAULT
Digital Registers				
DIGO_STRENGTH	Digital Output Drive Strength	0x1F	R/W	0x03
R2_RATE	R2 Decimation Rate	0x21	R/W	0x08
R3_RATE_CH1	R3 Decimation Rate for Channel 1	0x22	R/W	0x80
R3_RATE_CH2	R3 Decimation Rate for Channel 2	0x23	R/W	0x80
R3_RATE_CH3	R3 Decimation Rate for Channel 3	0x24	R/W	0x80
R1_RATE	R1 Decimation Rate	0x25	R/W	0x00
DIS_EFILTER	ECG Filter Disable	0x26	R/W	0x00
DRDYB_SRC	Data Ready Pin Source	0x27	R/W	0x00
SYNCB_CN	SYNCB In/Out Pin Control	0x28	R/W	0x40
MASK_DRDYB	Optional Mask Control for DRDYB Output	0x29	R/W	0x00
MASK_ERR	Mask Error on ALARMB Pin	0x2A	R/W	0x00
Reserved	—	0x2B	_	0x00
Reserved	-	0x2C		0x00
Reserved	—	0x2D	_	0x09
ALARM_FILTER	Digital Filter for Analog Alarm Signals	0x2E	R/W	0x33
CH_CNFG	Configure Channel for Loop Read Back Mode	0x2F	R/W	0x00
Pace and ECG Data Read	Back Registers			<u>.</u>
DATA_STATUS	ECG and Pace Data Ready Status	0x30	RO	
DATA_CH1_PACE	Channel 1 Pace Data	0x31 0x32	RO	—
DATA_CH2_PACE	Channel 2 Pace Data	0x33 0x34	RO	_
DATA_CH3_PACE	Channel 3 Pace Data	0x35 0x36	RO	—
DATA_CH1_ECG	Channel 1 ECG Data	0x37 0x38 0x39	RO	_
DATA_CH2_ECG	Channel 2 ECG Data	0x3A 0x3B 0x3C	RO	_
DATA_CH3_ECG	Channel 3 ECG Data	0x3D 0x3E 0x3F	RO	_
REVID	Revision ID	0x40	RO	0x01
DATA_LOOP	Loop Read-Back Address	0x50	RO	

# 8.6.1 Operation Mode Registers

# Figure 32. CONFIG: Main Configuration

Addr		7	6	5	4	3	2	1	0
0x00							PWR_DOWN	STANDBY	START_CON
[7:3]	RE	SERVED	—						
[2]	P٧	VR_DOWN	Power-	down mode					
			0: Disab	oled (default)					
			1: Circu	it powered dowr	n				
[1]	ST	ANDBY	Standb	y mode					
			0: Disab	oled					



1: Most circuits powered down (default)

[0]	START_CON	Start conversion
		0: Disabled (default)
		1: Conversion active
		Note: Programming START_CON = 1 locks write access to registers 0x11, 0x12, 0x13 and 0x21–0x29.

#### 8.6.2 Input Channel Selection Registers

# Figure 33. FLEX\_CH1\_CN: Flex Routing Switch Control For Channel 1

Addr		7	6	5	4	3	2	1	0			
0x01		TS	T1	POS1 NEG1								
[7:6]	TSI	Г1	Test sig	Test signal selector								
			00: Test 01: Con 10: Con 11: Con	t signal disconne nect channel on nect channel on nect channel on	ected and CH1 i le to positive tes le to negative te le to zero test si	nputs determine t signal st signal gnal	d by POS1 and	l NEG1 (default)				
[5:3]	PO	S1	Positive	e terminal of ch	annel 1							
			000: Po 001: Po 010: Po 011: Po 100: Po 101: Po 110: Po	000: Positive terminal is disconnected (default) 001: Positive terminal connected to input IN1 010: Positive terminal connected to input IN2 011: Positive terminal connected to input IN3 100: Positive terminal connected to input IN4 101: Positive terminal connected to input IN5 110: Positive terminal connected to input IN6								
[2:0]	NE	G1	Negativ	e terminal of c	hannel 1							
			000: Ne 001: Ne 010: Ne 011: Ne 100: Ne 101: Ne 110: Ne	gative terminal i gative terminal o gative terminal o gative terminal o gative terminal o gative terminal o gative terminal o	s disconnected connected to inp connected to inp connected to inp connected to inp connected to inp connected to inp	(default) out IN1 out IN2 out IN3 out IN3 out IN4 out IN5 out IN6						

# Figure 34. FLEX\_CH2\_CN: Flex Routing Switch Control for Channel 2

Addr	7	6	5	4	3	2	1	0
0x02		TST2		POS2			NEG2	
[7:6]	TST2	<b>Test sig</b> 00: Test 01: Con 10: Con 11: Con	gnal selector t signal disconne nect channel tw nect channel tw nect channel tw	ected and CH2 i to to positive tes to to negative tes to to zero test sit	nputs determine t signal st signal gnal	ed by POS2 and	NEG2 (default)	
[5:3]	POS2	Positive 000: Po 001: Po 010: Po 011: Po 100: Po 101: Po 110: Po	e terminal of ch sitive terminal is sitive terminal c sitive terminal c sitive terminal c sitive terminal c sitive terminal c	annel 2 disconnected ( onnected to inpu onnected to inpu onnected to inpu onnected to inpu onnected to inpu	default) it IN1 it IN2 it IN3 it IN4 it IN5 it IN6			
[2:0]	NEG2	Negativ	e terminal of c	hannel 2				

000: Negative terminal is disconnected (default) 001: Negative terminal connected to input IN1 010: Negative terminal connected to input IN2 011: Negative terminal connected to input IN3 100: Negative terminal connected to input IN4 101: Negative terminal connected to input IN5 110: Negative terminal connected to input IN5

#### Figure 35. FLEX\_CH3\_CN: Flex Routing Switch Control for Channel 3

Addr		7	6	5	4	3	2	1	0	
0x03		TS	Т3		POS3			NEG3		
[7:6]	TS.	ГЗ	<b>Test sig</b> 00: Test 01: Con 10: Con 11: Con	gnal selector t signal disconne nect channel thi nect channel thi nect channel thi	ected and CH3 i ree to positive to ree to negative t ree to zero test	nputs determine est signal est signal signal	d by POS3 and	NEG3 (default)		
[5:3]	PO	S3	Positive 000: Po 001: Po 010: Po 011: Po 100: Po 101: Po 110: Po	Positive terminal of channel 3000: Positive terminal is disconnected (default)001: Positive terminal connected to input IN1010: Positive terminal connected to input IN2011: Positive terminal connected to input IN3100: Positive terminal connected to input IN4101: Positive terminal connected to input IN4101: Positive terminal connected to input IN5110: Positive terminal connected to input IN5						
[2:0]	NE	G3	Negativ 000: Ne 001: Ne 010: Ne 100: Ne 100: Ne 110: Ne	e terminal of c gative terminal i gative terminal o gative terminal o gative terminal o gative terminal o gative terminal o	hannel 3 s disconnected connected to inp connected to inp connected to inp connected to inp connected to inp connected to inp	(default) out IN1 out IN2 out IN3 out IN4 out IN5 out IN6				

#### Figure 36. FLEX\_PACE\_CN: Flex Routing Switch Control for Pace Channel

Addr		7	6	5	4	3	2	1	0
0x04		TS	ST4		POS4			NEG4	
[7:6]	TS	Г4	Test sig	gnal selector t signal disconne	ected and PACE	inputs determin	ned by POS4 an	nd NEG4 (defau	lt)
			10: Cor 11: Cor	inect pace chan inect pace chan inect pace chan	nel to negative te nel to negative t nel to zero test s	est signal signal			
[5:3]	PO	S4	Positiv	e terminal of pa	ace channel				
			000: Po	sitive terminal is	s disconnected (	default)			
			001: Po	sitive terminal c	onnected to inpu	it IN1			
			010: Po	sitive terminal c	onnected to inpu	it IN2			
			011: Po	sitive terminal c	onnected to inpl	it IN3			
			100: Po	sitive terminal c	onnected to inpl	it IN4			
			101: Po	sitive terminal c	onnected to inpl	It IN5			
			110: Po	sitive terminal c	onnected to inpl				
[2:0]	NE	G4	Negativ	ve terminal of p	ace channel				



000: Negative terminal is disconnected (default) 001: Negative terminal connected to input IN1 010: Negative terminal connected to input IN2 011: Negative terminal connected to input IN3 100: Negative terminal connected to input IN4 101: Negative terminal connected to input IN5 110: Negative terminal connected to input IN5

#### Figure 37. FLEX\_VBAT\_CN: Flex Routing Switch for Battery Monitoring

Addr	7	7	6	5	4	3	2	1	0
0x05							VBAT_ MONI_CH3	VBAT_ MONI_CH2	VBAT_ MONI_CH1
[7:3]	RESERVE	ED	—						
[2]	VBAT_MO	DNI_CH	3 Battery	monitor config	guration for cha	annel 3			
			0: Batte 1: Batte	ry voltage monit ry voltage monit	tor disabled (def tor enabled and	ault) overrides FLEX	_CH3_CN regis	ter	
[1]	VBAT_MO	DNI_CH	2 Battery	monitor config	guration for cha	annel 2			
			0: Batte 1: Batte	ry voltage monit ry voltage monit	tor disabled (def tor enabled and	ault) overrides FLEX	_CH2_CN regis	ter	
[0]	VBAT_MC	ONI_CH	1 Battery 0: Batte 1: Batte	monitor config ry voltage monit ry voltage monit	guration for cha tor disabled (def tor enabled and	a <b>nnel 1</b> ault) overrides FLEX	_CH1_CN regis	ter	

Note: The INA of the corresponding monitoring channel must be shut down in 0x14.

#### 8.6.3 Lead-Off Detect Control Registers

#### Figure 38. LOD\_CN: Lead-Off Detect Control

Addr	7	6	5	4	3	2	1	0		
0x06				ACAD_LOD	SHDN_LOD	SELAC_LOD	ACLVI	_LOD		
[7:5]	RESERVED	—								
[4]	ACAD_LOD	AC ana	log/digital lead	-off mode seled	rt 🛛					
		0: Digita	0: Digital AC lead-off detect (default)							
		T: Analo	1: Analog AC lead-off detect							
[3]	SHDN_LOD	Shut do	wn lead-off de	tection						
		0: Lead-	off detection cir	cuitry is active						
		1: Lead-	off detection cir	cuitry is shut do	wn (default)					
[2]	SELAC_LOD	Lead-of	f detect operat	ion mode						
		0: DC le	ad-off mode (de	efault)						
[4.0]		T. AC IE		rotor trigger los	al for AC load	off detection				
[1:0]	ACLVL_LOD	00 <sup>°</sup> Leve	el 1 (default)	rator trigger ie	ver for AC lead	-on detection				
		01: Leve	el 2							
		10: Leve	el 3							
		11: Leve	914							

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# Figure 39. LOD\_EN: Lead-Off Detect Enable

Addr	7	6	5	4	3	2	1	0
0x07					EN_	LOD		
[7:6]	RESERVED	_						
[5]	EN_LOD_6	DC or A These b 0: Lead 1: Lead Digital These b 0: In-ph 1: Anti-p	Analog AC Lead bits enable the lead off detection dis- off detection er AC Lead-off-De bits configure the ase (default) ohase	d-off-Detection ead-off-detection sabled (default) nabled etection: e phase of the c	: n for input IN6. surrent injected in	nto channel CH3	3.	
[4]	EN_LOD_5	DC or A These b 0: Lead 1: Lead	Analog AC Lead bits enable the lead off detection dis off detection er	d-off-Detection ead-off-detection sabled (default) nabled	: n for input IN5.			
		<b>Digital</b> These b 0: In-ph 1: Anti-p	AC Lead-off-De bits configure the ase (default) bhase	etection: e phase of the c	current injected in	nto channel CH2	2.	
[3]	EN_LOD_4	DC or A These b 0: Lead 1: Lead	Analog AC Lead oits enable the lead off detection dia off detection er	d-off-Detection ead-off-detection sabled (default) nabled	: n for input IN4.			
		<b>Digital</b> These b 0: In-ph 1: Anti-p	AC Lead-off-De bits configure the ase (default) bhase	etection: e phase of the c	current injected in	nto channel CH1	Ι.	
[2]	EN_LOD_3	<b>DC or A</b> These b 0: Lead 1: Lead	Analog AC Lead bits enable the lead off detection dis off detection er	d-off-Detection ead-off-detection sabled (default) nabled	: n for input IN3.			
		<b>Digital</b> These b 0: Lead 1: Lead	AC Lead-off-De bits enable the le -off detection dis -off detection er	etection: ead-off-detection sabled (default) nabled	n for channel CH	13.		
[1]	EN_LOD_2	<b>DC or A</b> These b 0: Lead 1: Lead	Analog AC Lead bits enable the lead off detection dis off detection er	d-off-Detection ead-off-detection sabled (default) nable	: n for input IN2.			
		<b>Digital</b> These b 0: Lead 1: Lead	AC Lead-off-De bits enable the le -off detection dis -off detection er	etection: ead-off-detection sabled (default) nabled	n for channel CH	12.		
[0]	EN_LOD_1	<b>DC or A</b> These b 0: Lead 1: Lead	Analog AC Lead bits enable the lead off detection dis off detection er	d-off-Detection ead-off-detection sabled (default) nable	: n for input IN1.			
		<b>Digital</b> These b 0: Lead 1: Lead	AC Lead-off-De bits enable the le -off detection dis -off detection er	etection: ead-off-detection sabled (default) nabled	n for channel CH	11.		



#### Figure 40. LOD\_CURRENT: Lead-Off Detect Current

Addr	7	6	5	4	3	2	1	0
0x08				CUR_	LOD			
[7:0] (	CUR_LOD	Lead-of The lea 0000000   111111 111111	ff detect curren d-off detect curre 00: 0.000 μΑ (de 01: 0.008 μΑ 10: 2.032 μΑ 11: 2.040 μΑ	<b>t select</b> ent is programm efault)	able in a range	of 2.04µA with s	steps of 8nA.	

## Figure 41. LOD\_AC\_CN: AC Lead-Off Detect Control

Addr	7	6	5	4	3	2	1	0
0x09	ACDIV_ FACTOR				ACDIV_LOD			

[7]	ACDIV_FACTOR	AC lead off test frequency division factor 0: Clock divider factor K = 1 (default) 1: Clock divider factor K = 16
[6:0]	ACDIV_LOD	<b>Clock divider ratiio for AC lead off</b> There are 7 bits available to program the clock divider that generates the AC lead off test frequency.

#### 8.6.4 Common-Mode Detection and Right-Leg Drive Common-Mode Feedback Control Registers

#### Figure 42. CMDET\_EN: Common-Mode Detect Enable

Addr	7	6	5	4	3	2	1	0
0x0A			CMDET_ EN IN6	CMDET_ EN IN5	CMDET_ EN IN4	CMDET_ EN IN3	CMDET_ EN IN2	CMDET_ EN IN1

#### [7:6] RESERVED

[5:0] CMDET\_EN\_INx

#### Common-mode detect input enable

There is one bit available per input pin, where the MSB corresponds to input pin IN6 and the LSB corresponds to input pin IN1.

0: Disable (default)

1: Enable the corresponding pin's voltage to contribute to the average voltage of the common-mode detect block.

Figure 43.	CMDET_	CN:	Common-Mode	Detect	Control
------------	--------	-----	-------------	--------	---------

Addr	7	6	5	4	3	2	1	0
0x0B						CMDET_BW	CMDET_C	APDRIVE

[7:6]	RESERVED	_
[2]	CMDET_BW	Common-mode detect bandwidth mode
		0: Low-bandwidth mode (default) 1: High-bandwidth mode
[1:0]	CMDET_CAPDRIVE	Common-mode detect capacitive load drive capability
[1:0]	CMDET_CAPDRIVE	Common-mode detect capacitive load drive capability 00: Low cap-drive mode (default)
[1:0]	CMDET_CAPDRIVE	Common-mode detect capacitive load drive capability 00: Low cap-drive mode (default) 01: Medium low cap-drive mode
[1:0]	CMDET_CAPDRIVE	Common-mode detect capacitive load drive capability 00: Low cap-drive mode (default) 01: Medium low cap-drive mode 10: Medium high cap-drive mode

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Addr	7	6	5	4	3	2	1	0	
0x0C		RLD_BW	RLD_CA	APDRIVE	SHDN_RLD		SELRLD		
[7]	RESERVED	_	_						
[6]	RLD_BW	Right-le	Right-leg drive bandwidth mode						
		0: Low-l 1: High-	0: Low-bandwidth mode (default) 1: High-bandwidth mode						
[5:4]	RLD_CAPDRIVE	Right-le	Right-leg drive capacitive load drive capability						
		00: Low	00: Low cap-drive mode (default)						
		01: Med	01: Medium low cap-drive mode						
		11: High	n cap-drive mod	e					
[3]	SHDN_RLD	Shut do	Shut down right-leg drive amplifier						
		0: RLD	amplifier powere	ed up (default)					
		1: RLD	amplifier powere	ed down					
[2:0]	SELRLD	Right-le	eg drive multip	lexer					
		000: Right-leg drive output disconnected (default)							
		001: Right-leg drive output connected to IN1							
		010: Right-leg drive output connected to IN2							
		011: Right-leg drive output connected to IN3							
		100. Rig	nt-leg drive out	put connected to	5 IN4 5 IN5				
		110: Ric	101: Right-leg drive output connected to IN5 110: Right-leg drive output connected to IN6						

#### Figure 44. RLD\_CN: Right-Leg Drive Control

# 8.6.5 Wilson Control Registers

#### Figure 45. WILSON\_EN1: Wilson Reference Input One Selection

Addr	7	6	5	4	3	2	1	0
0x0D							SELWILSON1	
[7] R [2:0] S	ESERVED ELWILSON1		reference routi connection to the st buffer amplifies to buffer amplifies to buffer amplifies to buffer amplifies to buffer amplifies	ing for the first he first buffer an er connected to er connected to er connected to er connected to er connected to er connected to	buffer amplifie nplifier (default) input IN1 input IN2 input IN3 input IN4 input IN5 input IN6	ır		

# Figure 46. WILSON\_EN2: Wilson Reference Input Two Selection

Addr	7	6	5	4	3	2	1	0
0x0E							SELWILSON2	
[7:3]	RESERVED	_						
[2:0] SELWILSON2 Wilson reference routing for the second buffer amplifier								
		000: No connection to the second buffer amplifier (default)						
		001: Second buffer amplifier connected to input IN1						
		010: Se	cond buffer amp	olifier connected	to input IN2			
		011: Second buffer amplifier connected to input IN3						
		100: Second buffer amplifier connected to input IN4						
		101: Second buffer amplifier connected to input IN5						
		110: Second buffer amplifier connected to input IN6						



#### Figure 47. WILSON\_EN3: Wilson Reference Input Three Selection

Addr		7	6	5	4	3	2	1	0			
0x0F								SELWILSON3				
[7:3] RESERVED —												
[2:0]	SE	ELWILSON3 Wilson reference routing for the third buffer amplifier										
			000: No connection to the third buffer amplifier (default)									
			001: Third buffer amplifier connected to input IN1									
			010: Third buffer amplifier connected to input IN2									
011: Third buffer amplifier connected to input IN3												
			100: Thi	ird buffer amplifi	er connected to	input IN4						
			101 <sup>.</sup> Thi	101. Third buffer amplifier connected to input IN5								

110: Third buffer amplifier connected to input IN6

#### Figure 48. WILSON\_CN: Wilson Reference Control

Addr	7	6	5	4	3	2	1	0
0x10							GOLDINT	WILSONINT

[7:2]	RESERVED	_
[1]	GOLDINT	Goldberger reference routing
		0: Goldberger reference disabled (default)
		1: Goldberger reference outputs internally connected to IN4, IN5 and IN6 Note: GOLDINT bit can not be 1 when WILSONINT is 1.
[0]	WILSONINT	Wilson reference routing
		0: Wilson reference output internally disconnected from IN6 (default)
		1: Wilson reference output internally connected to IN6
		Note: WILSONINT bit can not be 1 when GOLDINT is 1.

#### 8.6.6 Reference Registers

#### Figure 49. REF\_CN: Internal Reference Voltage Control

Addr	7	6	5	4	3	2	1	0	
0x11							SHDN_ CMREF	SHDN_REF	
[7:2]	RESERVED	_							
[1]	SHDN_CMREF	Shut d	own the comm	on-mode and r	ight-leg drive	reference volt	age circuitry		
		0: CM a 1: Shut Note: E Power-	0: CM and RLD reference voltage is on (default) 1: Shut down CM and RLD reference voltage Note: Enable this bit to save power when the analog block is shut down (SHDN_REF = 1). Power-down mode automatically shuts down the common-mode and right-leg drive reference.						
[0]	SHDN_REF	Shut d	own internal 2.	4-V reference	voltage				
		0: Inter 1: Shut	nal reference vo down internal r	oltage is on (def eference voltage	ault) e				
		Note: E Power-	nabling this bit a down mode aut	allows driving th omatically shuts	ne IC with an e s down the inte	xternal referenc rnal 2.4-V refere	e voltage on the C ence.	VREF pin.	

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# 8.6.7 OSC Control Registers

Figure 50.	OSC_CN:	<b>Clock Source</b>	and Output	<b>Clock Control</b>
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Addr	7		6	5	4	3	2	1	0			
0x12							STRTCLK	SHDN_OSC	EN_CLKOUT			
[7:3]	RESERVE	D	_									
[2]	STRTCLK		Start th	Start the clock								
			0: Clock 1: Enab Note: S the exte	0: Clock to digital disabled (default) 1: Enable clock to digital Note: Set this bit high only after the oscillator has started up or after the oscillator has shut down and the external clock has started up.								
[1]	SHDN_OS	С	Select	clock source								
			0: Use i 1: Shut Note: S	0: Use internal clock with external crystal on XTAL1 and XTAL2 pins (default) 1: Shut down internal oscillator and use external clock from CLK pin Note: STRTCLK bit should be low at the time this bit is reconfigured.								
[0]	EN_CLKOU	UT	Enable	CLK pin outpu	ut driver							
			0: Clock 1: Clock	c output driver c c output driver e	lisabled (defaul enabled	:)						

## 8.6.8 AFE Control Registers

# Figure 51. AFE\_RES: Analog Front-End Frequency and Resolution

Addr	7	6	5	4	3	2	1	0	
0x13			FS_HIGH_ CH3	FS_HIGH_ CH2	FS_HIGH_ CH1	EN_HIRES_ CH3	EN_HIRES_ CH2	EN_HIRES_ CH1	
[7:6]	RESERVED	_							
[5]	FS_HIGH_CH3	<b>Clock f</b> 0: 1024 1: 2048	<b>requency for c</b> 00 Hz (default) 00 Hz	hannel 3					
[4 ]	FS_HIGH_CH2	<b>Clock f</b> 0: 1024 1: 2048	Clock frequency for Channel 2 0: 102400 Hz (default) 1: 204800 Hz						
[3]	FS_HIGH_CH1	<b>Clock f</b> 0: 1024 1: 2048	<b>requency for C</b> 00 Hz (default) 00 Hz	Channel 1					
[2]	EN_HIRES_CH3	<b>High-re</b> 0: Disal 1: Enab	esolution mode bled (default) bled	for Channel 3	instrumentat	ion amplifier			
[1]	EN_HIRES_CH2	<b>High-re</b> 0: Disal 1: Enab	esolution mode bled (default) bled	e for Channel 2	instrumentat	ion amplifier			
[0]	EN_HIRES_CH1	<b>High-re</b> 0: Disal 1: Enab	esolution mode bled (default) led	for Channel 1	instrumentat	ion amplifier			



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# Figure 52. AFE\_SHDN\_CN: Analog Front-End Shutdown Control

Addr		7	6	5	4	3	2	1	0		
0x14				SHDN_	SHDN_	SHDN_	SHDN_	SHDN_	SHDN_		
				SDM_CH3	SDM_CH2	SDM_CH1	INA_CH3	INA_CH2	INA_CH1		
[7:6]	RE	SERVED	_								
[5]	SH	IDN_SDM_CH:	3 Shut do 0: Active 1: Shut	Shut down the sigma-delta modulator for Channel 3 0: Active (default) 1: Shut down							
[4 ]	SH	IDN_SDM_CH2	2 Shut do 0: Active 1: Shut	Shut down the sigma-delta modulator for Channel 2 0: Active (default) 1: Shut down							
[3]	SH	IDN_SDM_CH <sup>^</sup>	I Shut do 0: Active 1: Shut	<b>own the sigma</b> - e (default) down	-delta modulato	or for Channe	11				
[2]	SH	IDN_INA_CH3	Shut do 0: Active 1: Shut	<b>own the instrur</b> e (default) down	nentation amp	lifier for Chan	nel 3				
[1]	SH	IDN_INA_CH2	Shut do 0: Active 1: Shut	<b>own the instrur</b> e (default) down	nentation amp	lifier for Chan	nel 2				
[0]	SH	IDN_INA_CH1	Shut do 0: Active 1: Shut	<b>own the instrur</b> e (default) down	nentation amp	lifier for Chan	nel 1				

## Figure 53. AFE\_FAULT\_CN: Analog Front-End Fault Detection Control

Addr	7	6	5	4	3	2	1	0
0x15						SHDN_	SHDN_	SHDN_
						CH3	CH2	CH1

[7:3]	RESERVED	—
[2]	SHDN_ FAULTDET_CH3	Disable the instrumentation amplifier fault detection for Channel 3
		0: Fault detection active (default) 1: Disable the fault detection
[1 ]	SHDN_ FAULTDET_CH2	Disable the instrumentation amplifier fault detection for Channel 2
		0: Active (default)
		1: Disable the fault detection
[0]	SHDN_ FAULTDET_CH1	Disable the instrumentation amplifier fault detection for Channel 1
		0: Active (default)
		1: Disable the fault detection



#### Figure 54. AFE\_PACE\_CN: Analog Pace Channel Output Routing Control

Addr	7	6	5	4	3	2	1	0	
0x17						PACE2RLDI N	PACE2WCT	SHDN_PACE	
[7:3]	RESERVED	_							
[2]	PACE2RLDIN	Connec	t the analog p	ace channel ou	utput to RLDI	N pin			
		0: Analo 1: Conr Note: T RLDRE	<ul> <li>0: Analog pace channel output is disconnected from the RLDIN pin (default)</li> <li>1: Connect the analog pace channel output to the RLDIN pin.</li> <li>Note: The right-leg drive amplifier is disconnected from the RLDIN pin and connected internally to the RLDREF pin when this bit is 1.</li> </ul>						
[1]	PACE2WCT	Connec	ct the analog p	ace channel ou	utput to WCT	pin			
		0: Analo 1: Conr Note: T output o	<ul> <li>0: Analog pace channel output is disconnected from the WCT pin (default)</li> <li>1: Connect the analog pace channel output to the WCT pin.</li> <li>Note: The Wilson reference output is disconnected from the WCT pin when this bit is 1. The Wilson output can be connected internally to IN6 pin with the <i>WILSON_CN</i> register.</li> </ul>						
[0]	SHDN_PACE	Shut de	own analog pa	ce channel					
		0: Analo 1: Analo	og pace channe og pace channe	l is powered up I is shut down (	default)				

#### 8.6.9 Error Status Registers

## Figure 55. ERROR\_LOD: Lead-Off Detect Error Status

Addr	7	6	5	4	3	2	1	0		
0x18				OUT_LOD						

[7:6]	RESERVED	_
[5:0]	OUT_LOD	Lead-Off Detect Status
		There is one bit available per input pin, where the MSB corresponds to input pin IN6 and the LSB corresponds to input pin IN1.

1: Indicates a lead off error detected on the corresponding input pin.

Note: The clock-to-digital (internal or external) must be enabled in 0x12[2] for this error register to update.



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#### Figure 56. ERROR\_STATUS: Other Error Status

Addr	7	6	5	4	3	2	1	0			
0x19	SYNC EDGEERR	CH3ERR	CH2ERR	CH1ERR	LEADOFF	BATLOW	RLDRAIL	CMOR			
[7]	SYNCEDGEERR	Digital 1: Indica	Digital synchronization error 1: Indicates a digital synchronization error occurred								
[6]	<b>CH3ERR</b>	Channe	el 3 out-of-rang	e error							
		1: Indica	ates an out-of-ra	ange error deteo	cted on Channe	el 3					
[5]	CH2ERR	Channe	el 2 out-of-rang	e error							
		1: Indica	1: Indicates an out-of-range error detected on Channel 2								
[4]	CH1ERR	Channe	el 1 out-of-rang	e error							
		1: Indica	ates an out-of-ra	ange error deteo	cted on Channe	el 1					
[3]	LEADOFF	Lead of	f detected								
		1: Indica	ates a lead off v	vas detected on	at least one ir	nput pin					
[2]	BATLOW	Low ba	ttery								
		1: Indica	ates the battery	voltage has dro	pped below 2.	7 V					
[1]	RLDRAIL	Right le	eg drive near ra	ail							
		1: Indicates the right leg drive amplifier output is approaching the supply rails									
[0]	CMOR	Common-mode level out-of-range									
		1: Indica mode ra	ates the level de ange of the amp	etected by the c olifiers in the ana	ommon-mode alog front-end	detect block is	outside of the input	common-			

Note: The clock to digital (internal or external) must be enabled in 0x12[2] for this error register to update.

#### Figure 57. ERROR\_RANGE1: Channel 1 AFE Out-Of-Range Status

		•				Ŭ					
Addr	7	6	5	4	3	2	1	0			
0x1A		SDM_OR_CH1	SIGN_CH1	OUTN_ LOW_CH1	OUTN_ HIGH_CH1	OUTP_ LOW_CH1	OUTP_ HIGH_CH1	DIF_HIGH_ CH1			
[7]	RESERVED	_									
[6]	SDM_OR_CH	1 Channe 1: Indic	el 1 sigma-delta ates an over rar	a modulator ov	<b>ver range</b> Channel 1 SE	DM					
[5]	SIGN_CH1	<b>Channe</b> This bit 0: Posit 1: Posit	<ul> <li>Channel 1 instrumentation amplifier output sign</li> <li>This bit specifies the sign of the output signal of the instrumentation amplifier for Channel 1.</li> <li>0: Positive output of INA larger than negative output</li> <li>1: Positive output of INA smaller than negative output</li> </ul>								
[4 ]	OUTN_LOW_	CH1 Channe 1: Indic	el 1 instrument ates the negativ	ation amplifier	negative out	<b>out near negati</b> the negative ra	i <b>ve rail</b> il for Channel 1				
[3]	OUTN_HIGH_	CH1 Channe 1: Indic	el 1 instrument ates the negativ	ation amplifier	negative outp INA is close to	out near positive the positive rail	<b>ve rail</b> I for Channel 1				
[2]	OUTP_LOW_0	CH1 Channe 1: Indic	Channel 1 instrumentation amplifier positive output near negative rail 1: Indicates the positive output of the INA is close to the negative rail for Channel 1								
[1]	OUTP_HIGH_	CH1 Channe 1: Indic	Channel 1 instrumentation amplifier positive output near positive rail 1: Indicates the positive output of the INA is close to the positive rail for Channel 1								
[0]	DIF_HIGH_CH	I1 Channe 1: Indic	Channel 1 instrumentation amplifier output out-of-range 1: Indicates the differential output voltage of the INA is out-of-range for Channel 1								
	Note: The cloc	k-to-digital (interna	I or external) m	ust be enabled	in 0x12[2] for t	his error registe	r to update.				

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Figure 58.	ERROR	RANGE2: Channel 2 AFE Out-Of-Range Status
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Addr	7	6	5	4	3	2	1	0
0x1B		SDM_OR_CH2	SIGN_CH2	OUTN_ LOW_CH2	OUTN_ HIGH_CH2	OUTP_ LOW_CH2	OUTP_ HIGH_CH2	DIF_HIGH_ CH2
[7]	DESERVED							
[/]	RESERVED							
[6]	SDM_OR_CH2         Channel 2 sigma-delta modulator over range           1: Indicates an over range detected for channel 2 SDM							
[5]	SIGN_CH2	<b>Channe</b> This bit 0: Positi 1: Positi	Channel 2 instrumentation amplifier output sign This bit specifies the sign of the output signal of the instrumentation amplifier for Channel 2. 0: Positive output of INA larger than negative output 1: Positive output of INA smaller than negative output					
[4 ]	OUTN_LOW_C	CH2 Channe 1: Indica	Channel 2 instrumentation amplifier negative output near negative rail 1: Indicates the negative output of the INA is close to the negative rail for Channel 2					
[3]	OUTN_HIGH_(	CH2 Channe 1: Indica	Channel 2 instrumentation amplifier negative output near positive rail 1: Indicates the negative output of the INA is close to the positive rail for Channel 2					
[2]	OUTP_LOW_C	CH2 Channe 1: Indica	Channel 2 instrumentation amplifier positive output near negative rail 1: Indicates the positive output of the INA is close to the negative rail for Channel 2					
[1]	OUTP_HIGH_(	CH2 Channe 1: Indica	Channel 2 instrumentation amplifier positive output near positive rail 1: Indicates the positive output of the INA is close to the positive rail for Channel 2					
[0]	DIF_HIGH_CH	2 Channe 1: Indica	el 2 instrumen ates the differe	tation amplifier of the test of test o	output out-of- ge of the INA is	range s out-of-range fo	r Channel 2	

Note: The clock-to-digital (internal or external) must be enabled in 0x12[2] for this error register to update.

## Figure 59. ERROR\_RANGE3: Channel 3 AFE Out-Of-Range Status

Addr	7	6	5	4	3	2	1	0
0x1C		SDM_OR_CH3	SIGN_CH3	OUTN_ LOW_CH3	OUTN_ HIGH_CH3	OUTP_ LOW_CH3	OUTP_ HIGH_CH3	DIF_HIGH_ CH3
[7]	RESERVED	—						
[6]	[6] SDM_OR_CH3 Channel 3 sigma-delta modulator over range							
[5]	SIGN_CH3	<b>Channe</b> This bit 0: Positi 1: Positi	<ul> <li>Channel 3 instrumentation amplifier output sign</li> <li>This bit specifies the sign of the output signal of the instrumentation amplifier for Channel 3.</li> <li>0: Positive output of INA larger than negative output</li> <li>1: Positive output of INA smaller than negative output</li> </ul>					
[4 ]	OUTN_LOW_C	CH3 Channe 1: Indica	Channel 3 instrumentation amplifier negative output near negative rail 1: Indicates the negative output of the INA is close to the negative rail for Channel 3					
[3]	OUTN_HIGH_(	CH3 Channe 1: Indica	Channel 3 instrumentation amplifier negative output near positive rail 1: Indicates the negative output of the INA is close to the positive rail for Channel 3					
[2]	OUTP_LOW_C	Channe 1: Indica	Channel 3 instrumentation amplifier positive output near negative rail 1: Indicates the positive output of the INA is close to the negative rail for Channel 3					
[1]	OUTP_HIGH_(	CH3 Channe 1: Indica	Channel 3 instrumentation amplifier positive output near positive rail 1: Indicates the positive output of the INA is close to the positive rail for Channel 3					
[0]	DIF_HIGH_CH	F_HIGH_CH3       Channel 3 instrumentation amplifier output out-of-range         1: Indicates the differential output voltage of the INA is out-of-range for Channel 3						

Note: The clock-to-digital (internal or external) must be enabled in 0x12[2] for this error register to update.



#### Figure 60. ERROR\_SYNC: Synchronization Error

Addr	7	6	5	4	3	2	1	0	
0x1D					SYNC_PHASEE RR	SYNC_ CH3ERR	SYNC_ CH2ERR	SYNC_ CH1ERR	
[7:4]	RESERVED	_							
[3]	SYNC_PHASE	ERR Close 1: T	Clock timing generator phase error 1: Timing generator phase adjusted to comply with SYNCB signal						
[2]	SYNC_CH3ER	<b>R Cha</b> 1: C	Channel 3 synchronization error 1: Channel's filter timing updated to comply with synchronization source						
[1]	SYNC_CH2ER	<b>R Cha</b> 1: C	Channel 2 synchronization error 1: Channel's filter timing updated to comply with synchronization source						
[0]	SYNC_CH1ER	<b>R Cha</b> 1: C	Channel 1 synchronization error 1: Channel's filter timing updated to comply with synchronization source						

Figure 61.	ERROR	_MISC:	Miscellaneous	Error
------------	-------	--------	---------------	-------

Addr	7	6	5	4	3	2	1	0
0x1E						BATLOW_ STATUS	RLDRAIL_ STATUS	CMOR_ STATUS

[7:3]	RESERVED	_
[2]	BATLOW_STATUS	Low-battery error status 1: Indicates the battery voltage has dropped below 2.7 V
[1]	RLDRAIL_STATUS	Right-leg drive near rail error status 1: Indicates the right leg drive amplifier output is approaching the supply rails
[0]	CMOR_STATUS	<b>Common-mode level out-of-range error status</b> 1: Indicates the level detected by the common-mode detect block is outside of the input common- mode range of the amplifiers in the analog front end

Note: The clock-to-digital (internal or external) must be enabled in 0x12[2] for this error register to update.

## 8.6.10 Digital Registers

## Figure 62. DIGO\_STRENGTH: Digital Output Drive Strength

Addr	7	6	5	4	3	2	1	0
0x1F							DIGO_ST	RENGTH

[7:2]	RESERVED	_	
[1:0]	DIGO_STRENGTH	Digital Output Drive Strength	
		00: Low drive mode 01: Mid-low drive mode	

10: Mid-high drive mode

11: High drive mode (Default)

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Addr	7	6	5	4	3	2	1	0
0x21					R2_RATE			
[7:4]	RESERVED	—						
[3:0]	R2_RATE	R2 deci	mation rate					
		0001: 4						
		0010: 5						
		0100: 6						
		1000: 8	(default)					
		Note: Th	ne register sets	to its default val	ue if none or mo	ore than one bit	are enabled.	

#### Figure 63. R2\_RATE: R2 Decimation Rate

#### Figure 64. R3\_RATE\_CH1: R3 Decimation Rate for Channel 1

Addr	7	6	5	4	3	2	1	0
0x22				R3_RA1	FE_CH1			

[7:0]	R3_RATE	CH1
F 1		

## R3 decimation rate for channel 1

0000001: 4 0000010: 6 0000100: 8 00001000: 12 00010000: 16 00100000: 32 01000000: 64 10000000: 128 (default) Note: The register sets to its default value if none or more than one bit are enabled.

#### Figure 65. R3\_RATE\_CH2: R3 Decimation Rate for Channel 2

Addr	7	6	5	4	3	2	1	0	
0x23				R3_RA	FE_CH2				
[7:0] F	R3_RATE_CH2	R3 deci	mation rate for	r channel 2					
		000000	01: 4						
		000000	10: 6						
		000001	00: 8						
		000010	00: 12						
		000100	00: 16						
		001000	00100000: 32						
		010000	01000000: 64						
		100000	00: 128 (default)	)					
		Note: Th	ne register sets	to its default val	ue if none or m	ore than one bit	are enabled.		

## Figure 66. R3\_RATE\_CH3: R3 Decimation Rate for Channel 3

Addr	7	6	5	4	3	2	1	0	
0x24		R3_RATE_CH3							
[7:0] R	3_RATE_CH3	R3 deci	imation rate for	channel 3					
		000000	01: 4						
		000000	10: 6						
		000001	00: 8						
		000010	00: 12						
		000100	00: 16						
		001000	00100000: 32						
		010000	01000000: 64						
		100000	00: 128 (default)	)					
		Note: TI	he register sets	to its default val	ue if none or mo	ore than one bit	are enabled.		



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#### Figure 67. R1\_RATE: R1 Decimation Rate

Addr	7	6	5	4	3	2	1	0
0x25						R1_RATE_ CH3	R1_RATE_ CH2	R1_RATE_ CH1
[7:3]	RESERVED	_						

[2]	R1_RATE_CH3	Pace data rate for channel 3 0: R1 = 4: Standard PACE Data Rate (default) 1: R1 = 2: Double PACE Data Rate
[1]	R1_RATE_CH2	Pace data rate for channel 2 0: R1 = 4: Standard PACE Data Rate (default) 1: R1 = 2: Double PACE Data Rate
[0]	R1_RATE_CH1	Pace data rate for channel 1 0: R1 = 4: Standard PACE Data Rate (default)

1: R1 = 2: Double PACE Data Rate

#### Figure 68. DIS\_EFILTER: ECG Filter Disable

Addr	7	6	5	4	3	2	1	0
0x26						DIS_E3	DIS_E2	DIS_E1

[7:3]	RESERVED	—
[2]	DIS_E3	Disable the ECG filter for channel 3
		0: ECG filter enabled (default)
		1: ECG filter disabled
[1]	DIS_E2	Disable the ECG filter for channel 2
		0: ECG filter enabled (default)
		1: ECG filter disabled
[0]	DIS_E1	Disable the ECG filter for channel 1
		0: ECG filter enabled (default)
		1: ECG filter disabled

#### Figure 69. DRDYB\_SRC: Data Ready Pin Source

Addr	7	6	5	4	3	2	1	0
0x27					DF	RDYB_SRC		

[7.0]	RESERVED	—
[6:0]	DRDYB_SRC	Select channel to drive the DRDYB pin
		000000: DRDYB pin not asserted (default)
		000001: Driven by Channel 1 pace
		000010: Driven by Channel 2 pace
		000100: Driven by Channel 3 pace
		001000: Driven by Channel 1 ECG
		010000: Driven by Channel 2 ECG
		100000: Driven by Channel 3 ECG

# Figure 70. SYNCB\_CN: Syncb In/Out Pin Control

Addr	7	6	5	4	3	2	1	0
0x28		DIS_SYNCB	SYNCB_SRC					
		OUT						

#### [7] RESERVED

DECEDVED

[7.6]



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[6]	DIS_SYNCBOUT	<b>Disable the SYNCB pin output driver</b> 0: Driver enabled and pin configured as output 1: Driver disabled and pin configured as input (default) Note: Bit should be set to 1 for slave devices.
[5:0]	SYNCB_SRC	Select channel to drive the SYNCB pin 000000: No source selected (default) 000001: Driven by Channel 1 pace 000010: Driven by Channel 2 pace 000100: Driven by Channel 3 pace 001000: Driven by Channel 1 ECG 010000: Driven by Channel 2 ECG 100000: Driven by Channel 3 ECG Note: Choose the slowest pace or ECG channel as source. Bits[5:0] must be cleared to 0 for slave devices.

#### Figure 71. MASK\_DRDYB: Optional Mask Control for DRDYB Output

Addr	7	6	5	4	3	2	1	0
0x29							DRDYB MASK_CTL1	DRDYB MASK_CTL0

[7:2]	RESERVED	_
[1]	DRDYBMASK_CTL1	START_CON mask control for DRDYB output 0: DRDYB signal is masked when START_CON is set (default)
		1: Disable initial DRDYB masking when START_CON is set
[0]	DRDYBMASK_CTL0	Optional mask control for DRDYB output 0: DRDYB signal is masked after out of sync is detected (default) 1: Disable DRDYB masking after out of sync is detected
[1] [0]	DRDYBMASK_CTL1 DRDYBMASK_CTL0	<ul> <li>START_CON mask control for DRDYB output</li> <li>0: DRDYB signal is masked when START_CON is set (default)</li> <li>1: Disable initial DRDYB masking when START_CON is set</li> <li>Optional mask control for DRDYB output</li> <li>0: DRDYB signal is masked after out of sync is detected (default)</li> <li>1: Disable DRDYB masking after out of sync is detected</li> </ul>

Note: If an ECG channel is enabled, DRDYB is masked during 6 ECG output data periods.

If all ECG channels are disabled, DRDYB is masked during 6 or 11 pace output data periods, for 1x pace or 2x pace mode respectively.

#### Figure 72. MASK\_ERR: Mask Error on ALARMB Pin

Addr	7	6	5	4	3	2	1	0			
0x2A	MASK_SYNC EDGEERR	MASK_ CH3ERR	MASK_ CH2ERR	MASK_ CH1ERR	MASK_ OUTLOD	MASK_ BATLOW	MASK_ RLDRAIL	MASK_ CMOR			
[7]	MASK_SYNCEDO R	GEER Mask a	ER Mask alarm condition when SYNCEDGEERR=1								
		0: Alarm 1: Alarm	n condition is a n condition is m	ctive (default) nasked							
[6]	MASK_CH3ERR	<b>Mask a</b> l 0: Alarm 1: Alarm	l <b>ask alarm condition for CH3ERR=1</b> : Alarm condition active (default) : Alarm condition is masked								
[5]	MASK_CH2ERR	<b>Mask a</b> l 0: Alarm 1: Alarm	larm condition n condition acti n condition is m	n for CH2ERR=1 ve (default) nasked							
[4 ]	MASK_CH1ERR	<b>Mask a</b> 0: Alarm 1: Alarm	larm condition n condition acti n condition is m	n for CH1ERR=1 ve (default) nasked							
[3]	MASK_LEADOFF	• Mask a 0: Alarm 1: Alarm	Mask alarm condition for LEADOFF=1 0: Alarm condition active (default) 1: Alarm condition is masked								
[2]	MASK_BATLOW	<b>Mask a</b> 0: Alarm 1: Alarm	larm condition n condition acti n condition is m	n for BATLOW=1 ve (default) nasked							

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[1]	MASK_RLDRAIL	Mask alarm condition for RLDRAIL=1
		0: Alarm condition active (default) 1: Alarm condition is masked
[0]	MASK_CMOR	Mask alarm condition for CMOR=1
		0: Alarm condition active (default) 1: Alarm condition is masked

## Figure 73. ALARM\_FILTER: Digital Filter for Analog Alarm Signals

Addr	7	6	5	4	3	2	1	0
0x2E	AFILTER_OTHER					AFILTER	R_LOD	

[7:4]	AFILTER_OTHER	Filter for all other alarms count
		Number of consecutive analog alarm signal counts +1 before ALARMB is asserted. 0011: (default)
[3:0]	AFILTER_LOD	Filter for OUT_LOD[5:0] alarm count
		Number of consecutive lead off alarm signal counts +1 before ALARMB is asserted. 0011: (default)

#### Figure 74. CH\_CNFG: Configure Channel for Loop Read Back Mode

Addr	7	6	5	4	3	2	1	0
0x2F		E3_EN	E2_EN	E1_EN	P3_EN	P2_EN	P1_EN	STS_EN
[7]	RESERVED	_						
[6]	E3_EN	<b>Enable</b> 0: Disab 1: Enab	DATA_CH3_E ble data read b le data read ba	CG read back ack for this chanr ack for this chann	nel (default) el			
[5]	E2_EN	<b>Enable</b> 0: Disab 1: Enab	DATA_CH2_E ble data read b le data read ba	CG read back ack for this chanr ack for this chann	nel (default) el			
[4 ]	E1_EN	<b>Enable</b> 0: Disat 1: Enab	DATA_CH1_E ble data read b le data read ba	CG read back ack for this chanr ack for this chann	nel (default) el			
[3]	P3_EN	<b>Enable</b> 0: Disab 1: Enab	DATA_CH3_F ole data read b le data read ba	PACE read back ack for this chanr ack for this chann	nel (default) el			
[2]	P2_EN	<b>Enable</b> 0: Disab 1: Enab	DATA_CH2_F ole data read b le data read ba	PACE read back ack for this chanr ack for this chann	nel (default) el			
[1]	P1_EN	<b>Enable</b> 0: Disab 1: Enab	DATA_CH1_F ble data read b le data read ba	PACE read back ack for this chanr ack for this chann	nel (default) el			
[0]	STS_EN	<b>Enable</b> 0: Disab 1: Enab	DATA_STATU ble data status le data status	<b>JS read back</b> read back (defau read back	lt)			

#### 8.6.11 Pace and ECG Data Read Back Registers

## Figure 75. DATA\_STATUS: ECG and Pace Data Ready Status

Addr	7	6	5	4	3	2	1	0
0x30	E3_DRDY	E2_DRDY	E1_DRDY	P3_DRDY	P2_DRDY	P1_DRDY	ALARMB	0

[7]	E3_DRDY	Channel 3 ECG data ready



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		1: Channel 3 ECG data ready
[6]	E2_DRDY	Channel 2 ECG data ready 1: Channel 2 ECG data ready
[5]	E1_DRDY	Channel 1 ECG data ready 1: Channel 1 ECG data ready
[4 ]	P3_DRDY	Channel 3 pace data ready 1: Channel 3 pace data ready
[3]	P2_DRDY	Channel 2 pace data ready 1: Channel 2 pace data ready
[2]	P1_DRDY	Channel 1 pace data ready 1: Channel 1 pace data ready
[1]	ALARMB	ALARMB status 1: Alarm active (ALARMB output pin driven low)
[0]	Reserved	<u> </u>

## Figure 76. DATA\_CH1\_PACE: Channel 1 Pace Data

Addr	15	14	13	12	11	10	9	8		
0x31		DATA_CH1_PACE								
	7	6	5	4	3	2	1	0		
0x32		DATA_CH1_PACE								

[15:8]	DATA_CH1_PACE	Channel 1 pace data
		Address 0x31 contains the upper byte
[7:0]	DATA_CH1_PACE	Channel 1 pace data
		Address 0x32 contains the lower byte

## Figure 77. DATA\_CH2\_PACE: Channel 2 Pace Data

Addr	15	14	13	12	11	10	9	8		
0x33		DATA_CH2_PACE								
	7	7 6 5 4 3 2 1 0								
0x34				DATA	_CH2_PACE					

[15:8] DATA\_CH2\_PACE Channel 2 pace data

DATA\_CH2\_PACE

Address 0x33 contains the upper byte

[7:0]

Channel 2 pace data

Address 0x34 contains the lower byte

#### Figure 78. DATA\_CH3\_PACE: Channel 3 Pace Data

Addr	15	14	13	12	11	10	9	8	
0x35	DATA_CH3_PACE								
	7	6	5	4	3	2	1	0	
0x36	DATA_CH3_PACE								

[15:8]	DATA_CH3_PACE	Channel 3 pace data Address 0x35 contains the upper byte
[7:0]	DATA_CH3_PACE	Channel 3 pace data
		Address 0x36 contains the lower byte



## Figure 79. DATA\_CH1\_ECG: Channel 1 ECG Data

Addr	23	22	21	20	19	18	7	6
0x37	DATA_CH1_ECG							
	15	14	13	12	11	10	9	8
0x38		DATA_CH1_ECG						
	7	6	5	4	3	2	1	0
0x39	DATA_CH1_ECG							

[23:16]	DATA_CH1_ECG	Channel 1 ECG data
		Address 0x37 contains the upper byte
[15:8]	DATA_CH1_ECG	Channel 1 ECG data Address 0x38 contains the middle byte
[7:0]	DATA_CH1_ECG	Channel 1 ECG data
		Address 0x39 contains the lower byte

# Figure 80. DATA\_CH2\_ECG: Channel 2 ECG Data

Addr	23	22	21	20	19	18	7	6
0x3A	DATA_CH2_ECG							
	15	14	13	12	11	10	9	8
0x3B	DATA_CH2_ECG							
	7	6	5	4	3	2	1	0
0x3C	DATA_CH2_ECG							

[23:16]	DATA_CH2_ECG	Channel 2 ECG data
		Address 0x3A contains the upper byte
[15:8]	DATA_CH2_ECG	Channel 2 ECG data
		Address 0x3B contains the middle byte
[7:0]	DATA_CH2_ECG	Channel 2 ECG data
		Address 0x3C contains the lower byte

## Figure 81. DATA\_CH3\_ECG: Channel 3 ECG Data

Addr	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT7	BIT6
0x3D	DATA_CH3_ECG							
	15	14	13	12	11	10	9	8
0x3E		DATA_CH3_ECG						
	7	6	5	4	3	2	1	0
0x3F	DATA CH3 ECG							

[23:16]	DATA_CH3_ECG	Channel 3 ECG data Address 0x3D contains the upper byte
[15:8]	DATA_CH3_ECG	Channel 3 ECG data Address 0x3E contains the middle byte
[7:0]	DATA_CH3_ECG	Channel 3 ECG data Address 0x3F contains the lower byte

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Figure 82. REVID: REVISION ID								
Addr	7	6	5	4	3	2	1	0
0x40					REVID			
[7:0]	REVID Revision ID 00000001 (Default) Figure 83, DATA LOOP: Loop Read Back Address							
		i iyu	C 05. DAIP		Jop Read L			
Addr	7	6	5	4		2	1	0

#### . .: . : ....

[7:0] PE\_LPRD

#### Loop read back address

Special address to read back the contents of registers 0x30 - 0x3F if they are enabled in CH\_CNFG.



## 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 9.1 Application Information

The ADS1293 is an AFE for biopotential measurements. The device is typically used in portable, low-power medical, sports, and fitness ECG applications. The device's flexibility and synchronization features allows it to be used it in configurations that range from single-chip/single-channel applications to multi-chip/multi-channel applications. The following sections will explore the use model in some of these configurations.

#### 9.2 Typical Applications

#### 9.2.1 3-Lead ECG Application

In the 3-Lead ECG example shown in Figure 84, the right-arm (RA), left-arm (LA), left-leg (LL) and right-leg (RL) electrodes are connected to the IN1, IN2, IN3 and IN4 pins. The ADS1293 uses the Common-Mode Detector to measure the common-mode of the system by averaging the voltage of input pins IN1, IN2 and IN3, and uses this signal in the right-leg drive feedback circuit <sup>(1)</sup>. The output of the RLD amplifier is connected to RL through IN4 to drive the common-mode of the system. The chip uses an external 4.096-MHz crystal oscillator connected between the XTAL1 and XTAL2 pins to create the clock source for the device.



Figure 84. 3-Lead ECG Application

(1) The ideal values of R<sub>1</sub>, R<sub>2</sub> and C<sub>1</sub> will vary per system / application; typical values for these components are: R<sub>1</sub> = 100 k $\Omega$ , R<sub>2</sub> = 1 M $\Omega$  and C<sub>1</sub> = 1.5 nF.

## **Typical Applications (continued)**

### 9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 12 as the set-up parameters.

	-
DESIGN PARAMETER	EXAMPLE VALUE
Number of electrodes	4
Lead I definition	LA – RA
Lead II definition	LL –RA
Bandwidth	175 Hz
Output data rate	853 sps
Analog supply voltage	5.0 V
Digital I/O supply voltage	3.3 V

#### Table 12. Design Parameters

#### 9.2.1.2 Detailed Design Procedure

Follow the next steps to configure the device for this example, starting from default registers values.

- 1. Set address 0x01 = 0x11: Connect channel 1's INP to IN2 and INN to IN1.
- 2. Set address 0x02 = 0x19: Connect channel 2's INP to IN3 and INN to IN1.
- 3. Set address 0x0A = 0x07: Enable the common-mode detector on input pins IN1, IN2 and IN3.
- 4. Set address 0x0C = 0x04: Connect the output of the RLD amplifier internally to pin IN4.
- 5. Set address 0x12 = 0x04: Use external crystal and feed the internal oscillator's output to the digital.
- 6. Set address 0x14 = 0x24: Shuts down unused channel 3's signal path.
- 7. Set address 0x21 = 0x02: Configures the R2 decimation rate as 5 for all channels.
- 8. Set address 0x22 = 0x02: Configures the R3 decimation rate as 6 for channel 1.
- 9. Set address 0x23 = 0x02: Configures the R3 decimation rate as 6 for channel 2.
- 10. Set address 0x27 = 0x08: Configures the DRDYB source to channel 1 ECG (or fastest channel).
- 11. Set address 0x2F = 0x30: Enables channel 1 ECG and channel 2 ECG for loop read-back mode.
- 12. Set address 0x00 = 0x01: Starts data conversion.

Follow the description in the Streaming section to read the data. The ADS1293 will measure lead I and lead II. Lead III can be calculated as follows: Lead III = Lead II – Lead I

Optionally, the third channel could be used to measure Lead III.

#### 9.2.1.3 Application Curves

Figure 85 show measurement data collected by a single ADS1293 device connected to an ECG simulator configured to produce an ECG signals at a rate of 60 per minute and with an amplitude of 2 mV. The data was collected simultaneously by channels 1 and 2 of the device during a period of 10 seconds.



Figure 85. Single ADS1293 Device With an ECG Simulator, CH1 and CH2: ECG Signals



#### 9.2.2 5-Lead ECG Application

In the 5-Lead ECG example shown in Figure 86, the ADS1293 uses the Common-Mode Detector to measure the common-mode of the system by averaging the voltage of input pins IN1, IN2 and IN3, and uses this signal in the right-leg drive feedback circuit <sup>(1)</sup>. The output of the RLD amplifier is connected to RL through IN4 to drive the common-mode of the system. The Wilson Central Terminal is generated by the ADS1293 and is used as a reference to measure the chest electrode, V1. The chip uses an external 4.096 MHz crystal oscillator connected between the XTAL1 and XTAL2 pins to create the clock source for the device.



Figure 86. 5-Lead ECG Application

#### 9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 13 as the setup parameters.

Table 13. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE			
Number of electrodes	5			
Lead I definition	LA – RA			
Lead II definition	LL –RA			
Lead V definition	V1 – WCT			
Bandwidth	175 Hz			
Output data rate	853 sps			
Analog supply voltage	5.0 V			
Digital I/O supply voltage	3.3 V			

(1) The ideal values of R<sub>1</sub>, R<sub>2</sub> and C<sub>1</sub> will vary per system / application; typical values for these components are: R<sub>1</sub> = 100 k $\Omega$ , R<sub>2</sub> = 1 M $\Omega$  and C<sub>1</sub> = 1.5 nF.

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## 9.2.2.2 Detailed Design Procedure

The following steps configure the ADS1293 for a 5-lead application with an ECG bandwidth of 175 Hz and an output data rate of 853 Hz; it is assumed that the device registers contain their default power-up values.

- 1. Set address 0x01 = 0x11: Connects channel 1's INP to IN2 and INN to IN1.
- 2. Set address 0x02 = 0x19: Connect channel 2's INP to IN3 and INN to IN1.
- 3. Set address 0x03 = 0x2E: Connects channel 3's INP to IN5 and INN to IN6.
- 4. Set address 0x0A = 0x07: Enables the common-mode detector on input pins IN1, IN2 and IN3.
- 5. Set address 0x0C = 0x04: Connects the output of the RLD amplifier internally to pin IN4.
- 6. Set addresses 0x0D = 0x01, 0x0E = 0x02, 0x0F = 0x03: Connects the first buffer of the Wilson reference to the IN1 pin, the second buffer to the IN2 pin, and the third buffer to the IN3 pin.
- 7. Set address 0x10 = 0x01: Connects the output of the Wilson reference internally to IN6.
- 8. Set address 0x12 = 0x04: Uses external crystal and feeds the output of the internal oscillator module to the digital.
- 9. Set address 0x21 = 0x02: Configures the R2 decimation rate as 5 for all channels.
- 10. Set address 0x22 = 0x02: Configures the R3 decimation rate as 6 for channel 1.
- 11. Set address 0x23 = 0x02: Configures the R3 decimation rate as 6 for channel 2.
- 12. Set address 0x24 = 0x02: Configures the R3 decimation rate as 6 for channel 3.
- 13. Set address 0x27 = 0x08: Configures the DRDYB source to ECG channel 1 (or fastest channel).
- 14. Set address 0x2F = 0x70: Enables ECG channel 1, ECG channel 2, and ECG channel 3 for loop read-back mode.
- 15. Set address 0x00 = 0x01: Starts data conversion.

Follow the description in the *Streaming* section to read the data.

## 9.2.2.3 Application Curves

Figure 87 show measurement data collected by a single ADS1293 device connected to an ECG simulator configured to produce an ECG signals at a rate of 60 per minute and with an amplitude of 2 mV. The data was collected simultaneously by channels 1, 2 and 3 of the device during a period of 10 seconds.



Figure 87. Single ADS1293 Device With an ECG Simulator, CH1, CH2, and CH3: ECG Signals



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# 9.2.3 8- or 12-Lead ECG Application





Figure 88 shows the ADS1293 master/slave setup for an 8-Lead to 12-Lead ECG system. The ADS1293 uses the Common-Mode Detector to measure the common-mode of the system by averaging the voltage of input pins IN1, IN2 and IN3, and uses this signal in the right-leg drive feedback circuit <sup>(1)</sup>. The output of the RLD amplifier is connected to the right-leg electrode to drive the common-mode of the system. The Wilson Central Terminal is generated by the ADS1293 and is used as a reference to measure the chest electrodes, V1-V6; TI strongly recommends shielding the external Wilson connections, which due to the high output impedance of the Wilson reference, is prone to pick up external interference. The master ADS1293 generates a synchronization pulse on the SYNCB pin (configured as an output). This drives the SYNCB pins (configured as inputs) of the two slave ADS1293. The master chip uses an external 4.096 MHz crystal oscillator connected between the XTAL1 and XTAL2 pins to create the clock source for the device and outputs this clock on the CLK pin.

#### 9.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 14 as the setup parameters.

DESIGN PARAMETER	EXAMPLE VALUE
Number of electrodes	10
Lead I definition	LA – RA
Lead II definition	LL –RA
Lead V1 definition	V1 – WCT
Lead V2 definition	V2 – WCT
Lead V3 definition	V3 – WCT
Lead V4 definition	V4 – WCT
Lead V5 definition	V5 – WCT
Lead V6 definition	V6 – WCT
Bandwidth	175 Hz
Output data rate	853 sps
Analog supply voltage	5.0 V
Digital I/O supply voltage	3.3 V

#### **Table 14. Design Parameters**

(1) The ideal values of R<sub>1</sub>, R<sub>2</sub> and C<sub>1</sub> will vary per system / application; typical values for these components are: R<sub>1</sub> = 100 k $\Omega$ , R<sub>2</sub> = 1 M $\Omega$  and C<sub>1</sub> = 1.5 nF.

## 9.2.3.2 Detailed Design Procedure

The next steps will configure the master device; it is assumed that the device registers contain their default power-up values.

- 1. Set address 0x01 = 0x11: Connects channel 1's INP to IN2 and INN to IN1.
- 2. Set address 0x02 = 0x19: Connect channel 2's INP to IN3 and INN to IN1.
- 3. Set address 0x0A = 0x07: Enables the common-mode detector on input pins IN1, IN2 and IN3.
- 4. Set address 0x0C = 0x04: Connects the output of the RLD amplifier internally to pin IN4.
- 5. Set addresses 0x0D = 0x01, 0x0E = 0x02, 0x0F = 0x03: Connects the first buffer of the Wilson reference to the IN1 pin, the second buffer to the IN2 pin, and the third buffer to the IN3 pin.
- 6. Set address 0x12 = 0x05: Uses external crystal, feeds the output of the internal oscillator module to the digital, and enables the CLK pin output driver
- 7. Set address 0x14 = 0x24: Shuts down unused channel 3's signal path.
- 8. **Set address 0x21 = 0x02:** Configures the R2 decimation rate as 5 for all channels.
- 9. Set address 0x22 = 0x02: Configures the R3 decimation rate as 6 for channel 1.
- 10. Set address 0x23 = 0x02: Configures the R3 decimation rate as 6 for channel 2.
- 11. Set address 0x27 = 0x08: Configures the data-ready source to channel 1 ECG (or fastest channel).
- 12. Set address 0x28 = 0x08: Configures the synchronization source to channel 1 ECG (or slowest channel).
- 13. Set address 0x2F = 0x30: Enables ECG channel 1 and ECG channel 2 for loop read-back mode.



Next, configure the slave devices; it is assumed that the device registers contain their default power-up values. In this example, both devices will have the same configuration; therefore, they can potentially be configured in parallel by asserting the CSB signal of both chips.

- 14. Set address 0x01 = 0x0C: Connects channel 1's INP to IN1 and INN to IN4.
- 15. Set address 0x02 = 0x14: Connects channel 2's INP to IN2 and INN to IN4.
- 16. Set address 0x03 = 0x1C: Connects channel 3's INP to IN3 and INN to IN4.
- 17. Set address 0x12 = 0x06: Uses external clock signal on the CLK pin and feeds it to the digital.
- 18. Set address 0x21 = 0x02: Configures the R2 decimation rate as 5 for all channels.
- 19. Set address 0x22 = 0x02: Configures the R3 decimation rate as 6 for channel 1.
- 20. Set address 0x23 = 0x02: Configures the R3 decimation rate as 6 for channel 2.
- 21. Set address 0x24 = 0x02: Configures the R3 decimation rate as 6 for channel 3.
- 22. Set address 0x27 = 0x00: DRDYB pin not asserted by slave devices.
- 23. Set address 0x28 = 0x40: Disables SYNCB driver and configures pin as input.
- 24. Set address 0x2F = 0x70: Enables ECG channel 1, ECG channel 2, and ECG channel 3 for loop read-back mode.

Finally, start the conversion. This should be written to all three chips.

25. Set address 0x00 = 0x01: Starts data conversion (repeat this step for every device).

The three devices will run synchronously using the SYNCB signal. Follow the description in the *Streaming* section to read the data. The ADS1293 measures lead I, lead II and leads V1-V6. For a 12-lead application, the remaining 4 leads can be calculated as follows:

- Lead III = Lead II Lead I
- aVR = (I + II) / 2
- aVL = I II / 2
- aVF = II I / 2



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## 9.2.3.3 Application Curves

Figure 89 show measurement data collected by 3 synchronized ADS1293 devices connected to an ECG simulator configured to produce an ECG signals at a rate of 60 per minute with an amplitude of 2 mV. The data was collected simultaneously by multiple channels from all 3 devices during a period of 10 seconds.





## **10** Power Supply Recommendations

TI recommends placing a  $0.1-\mu$ F ceramic bypass capacitor from VDD to ground as close as possible to the pin. An electrolytic or tantalum capacitor of value larger than 1  $\mu$ F is recommeded as a bulk capacitor. The bulk capacitor does not need to be in close proximity to the device and could be close to the voltage source terminals or at the output of the voltage regulator. The same recommendations apply for the VDDIO pin.

The CVREF pin requires a 1- $\mu$ F bypass capacitor-to-ground; this capacitor should have a low ESR and should be placed as close as possible to the pin. The RLDREF pin requires a 0.1- $\mu$ F ceramic bypass capacitor-to-ground; this capacitor should be placed as close as possible to the pin.

# 11 Layout

## 11.1 Layout Guidelines

- Bypass capacitors should be placed in close proximity to the VDD and VDDIO pins.
- A low-ESR bypass capacitor should be placed in close proximity to the CVREF pin.
- A bypass capacitor should be placed in close proximity to the RLDREF pin.
- The SPI signal traces should be routed close together.
- Series resistors should be placed at the source of SDO and DRDYB (close to the DUT). Series resistors should be placed at the sources of SDI, SCLK and CSB (close to the SPI master).

## 11.2 Layout Example



Figure 90. PCB Layout Example



# 12 器件和文档支持

## 12.1 商标

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## 12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。存储或装卸时,应将导线一起截短或将装置放置于导电泡棉中,以防止 MOS 门极遭受静电损 伤。

## 12.3 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

## 13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对 本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本,请查阅左侧的导航栏。
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10-Dec-2020

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
ADS1293CISQ/NOPB	ACTIVE	WQFN	RSG	28	1000	RoHS & Green	SN	Level-3-260C-168 HR	-20 to 85	ADS1293	Samples
ADS1293CISQE/NOPB	ACTIVE	WQFN	RSG	28	250	RoHS & Green	SN	Level-3-260C-168 HR	-20 to 85	ADS1293	Samples
ADS1293CISQX/NOPB	ACTIVE	WQFN	RSG	28	4500	RoHS & Green	SN	Level-3-260C-168 HR	-20 to 85	ADS1293	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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#### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1293CISQ/NOPB	WQFN	RSG	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
ADS1293CISQE/NOPB	WQFN	RSG	28	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
ADS1293CISQX/NOPB	WQFN	RSG	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

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# PACKAGE MATERIALS INFORMATION

20-Sep-2016



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1293CISQ/NOPB	WQFN	RSG	28	1000	210.0	185.0	35.0
ADS1293CISQE/NOPB	WQFN	RSG	28	250	210.0	185.0	35.0
ADS1293CISQX/NOPB	WQFN	RSG	28	4500	367.0	367.0	35.0

### **MECHANICAL DATA**



- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions. ∕∆

- Falls within JEDEC MO-220. E.



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