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LMX2491

ZHCSFL5A-OCTOBER 2016-REVISED JANUARY 2017

LMX2491 具有斜坡/线性调频生成功能的 6.4GHz 低噪声 RF PLL

特性 1

TEXAS

INSTRUMENTS

- -227dBc/Hz 标准化锁相环 (PLL) 噪声
- 500MHz 至 6.4GHz 宽带 PLL
- 3.15V 至 5.25V 电荷泵 PLL 电源
- 多用途斜坡/超宽带信号源生成功能
- 200MHz 最大相位检测器频率
- 频移键控/相移键控 (FSK/PSK) 调制引脚
- 数字锁检测
- 3.3V 单电源供电 •

应用 2

- 调频连续波 (FMCW) 雷达
- 军用雷达
- 微波回程
- 测试和测量
- 卫星通信 .
- 无线基础设施
- 适用于高速模数转换器/数模转换器 (ADC/DAC) 的 采样时钟

3 说明

LMX2491 器件是一款具有斜坡/线性调频生成功能的低 噪声 6.4GHz 宽带 Δ -Σ 分数 N PLL。它由一个相位频 率检测器、可编程电荷泵以及适用于外部 VCO 的高频 输入组成。LMX2491 广泛支持各类灵活的斜坡功能, 包括 FSK、PSK 和多达 8 段的可配置分段线性 FM 调 制配置文件。该器件具有精密 PLL 分辨率和快速斜升 功能,相位检测器速率高达 200MHz。LMX2491 允许 读回其任一寄存器。LMX2491 可由 3.3V 单电源供电 运行。此外,该器件支持电压高达 5.25V 的电荷泵, 无需使用外部放大器即可提供相位噪声性能得到改善的 简易解决方案。

器件信息

器件编号	封装	封装尺寸(标称值)			
LMX2491	WQFN (24)	4.00mm x 4.00mm			

(1) 要了解所有可用封装,请见数据表末尾的可订购产品附录。





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Changes from Original (October 2016) to Revision A

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5 Pin Configuration and Functions



Pin Functions

TERMINAL		TVDE	DESCRIPTION	
NO.	NAME	ITPE	DESCRIPTION	
0	DAP	GND	Die Attach Pad. Connect to PCB ground plane.	
1	GND	GND	Ground for charge pump.	
2, 3	GND	GND	Ground for Fin Buffer	
4, 5	Fin Fin*	Input	Complimentary high frequency input pins. Should be AC-coupled. If driving single-ended, impedance as seen from Fin and Fin* pins looking outwards from the part should be roughly the same.	
6	Vcc	Supply	Power Supply for Fin Buffer	
7	Vcc	Supply	Supply for On-chip LDOs	
8	Vcc	Supply	Supply for OSCin Buffer	
9	OSCin	Input	Reference Frequency Input	
10	GND/ OSCin*	GND/Input	Complimentary input for OSCin. If not used, it is recommended to match the termination as seen from the OSCin terminal looking outwards. However, this may also be grounded as well.	
11	GND	GND	Ground for OSCin Buffer	
12	MOD	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics	
13	CE	Input	Chip Enable	
14	CLK	GND	Serial Programming Clock.	
15	DATA	GND	Serial Programming Data	
16	LE	Input	Serial Programming Latch Enable	
17	MUXout	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics	
18	Vcc	Supply	Supply for delta sigma engine.	
19	Vcc	Supply	Supply for general circuitry.	
20	TRIG1	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics	
21	TRIG2	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics	
22	Vcp	Supply	Power Supply for the charge pump.	
23	Rset	NC	No connect.	
24	CPout	Output	Charge Pump Output	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CP}	Supply voltage for charge pump	V _{CC}	5.5	V
V _{CC}	Supply voltage	-0.3	3.6	V
V _{IN}	I/O input voltage	-0.3	V _{CC} + 0.3	V
T _{Solder}	Lead temperature (solder 4 seconds)		260	°C
T _{Junction}	Junction temperature		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T _{stg}	DMD storage temperature	-65	150	°C
T _{DP}	Storage dew point		3	°C

6.3 ESD Ratings

			VALUE	UNIT
V	Electrostatio discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
V(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	v

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3.15	3.3	3.45	V
V _{CP}	Charge pump supply voltage	V _{CC}		5.25	V
T _A	Ambient temperature	-40		85	°C
TJ	Junction temperature	-40		125	°C

6.5 Thermal Information

	THERMAL METRIC ⁽¹⁾	RTW (VQFN)	UNIT
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.4	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	7.1	°C/W
ΨJB	Junction-to-board characterization parameter	20	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



6.6 Electrical Characteristics

 $3.15 \text{ V} \leq \text{V}_{\text{CC}} \leq 3.45 \text{ V}, \text{ V}_{\text{CC}} \leq \text{V}_{\text{CP}} \leq 5.25 \text{ V}, -40 \text{ °C} \leq \text{T}_{\text{A}} \leq 85 \text{ °C}, \text{ except as specified. Typical values are at } \text{V}_{\text{CC}} = \text{V}_{\text{CP}} = 3.3 \text{ V}, \text{ V}_{\text{CC}} \leq 1.45 \text{ V}, \text{ V}_{\text{CC}} \approx 1.45 \text{ V}, \text{ V}_{\text{CC}}$ 25 °C.

	PARAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT
			f _{PD} = 10 MHz		45		
		All Vcc pins	f _{PD} = 100 MHz		50		
	Current consumption		f _{PD} = 200 MHz		55		
ICC			K _{PD} = 0.1 mA		2		mA
		Vcp pin	K _{PD} = 1.6 mA		10		
			K _{PD} = 3.1 mA		19		
I _{CC} PD	Power down current	POWERDOWN			3		
		OSC_DIFFR = 0	, doubler disabled	10		600	
	Frequency for OSCin	OSC_DIFFR = 0	, doubler enabled	10		300	N411-
TOSCin	terminal	OSC_DIFFR = 1	, doubler disabled	10		1200	IVIHZ
		OSC_DIFFR = 1	, doubler enabled	10		600	
V _{OSCin}	Voltage for OSCin pin ⁽¹⁾					$V_{CC} - 0.5$	V _{PP}
f _{Fin}	Frequency for Fin pin			500		6400	MHz
P _{Fin}	Power for Fin pin	Single-ended operation		-5		5	dBm
f _{PD}	Phase detector frequency					200	MHz
PN1Hz	PLL figure of merit ⁽²⁾				-227		dBc/Hz
PN10kHz	Normalized PLL 1/f noise ⁽²⁾	Normalized to 10-kHz offset for a 1- GHz carrier.			-120		dBc/Hz
I _{CPout} TRI	Charge pump leakage tri- state leakage					10	nA
I _{CPout} MM	Charge pump mismatch ⁽³⁾	$V_{CPout} = V_{CP} / 2$			5%		
			CPG = 1X		0.1		
I _{CPout}	Charge pump current	$V_{CPout} = V_{CP} / 2$					mA
			CPG = 31X		3.1		
LOGIC OUT	PUT TERMINALS (MUXout,	TRIG1, TRIG2, MO	OD)				
V _{OH}	Output high voltage			0.8 × V _{CC}	V _{CC}		V
V _{OL}	Output low voltage				0	$0.2 \times V_{CC}$	V
LOGIC INPL	JT TERMINALS (CE, CLK, DA	ATA, LE, MUXout	, TRIG1, TRIG2, MC	D)			
V _{IH}	Input high voltage			1.4		V _{CC}	V
V _{IL}	Input low voltage			0		0.6	V
IIH	Input leakage current			-5	1	5	μA
t _{CE} LOW	Chip enable low time			5			μs
t _{CE} HIGH	Chip enable high time			5			μs

(1) For optimal phase noise performance, higher input voltage and a slew rate of at least 3 V/ns is recommended

(2) PLL Noise Metrics are measured with a clean OSCin signal with a high slew rate using a wide loop bandwidth. The noise metrics model (2) PLL Noise Metrics are measured with a clear OSCIN signal with a high siew rate using a wide loop bandwidth. The holse metrics mode the PLL noise for an infinite loop bandwidth as: PLL_Total = 10 × log(10^{PLL_Flat / 10} + 10^{PLL_Flicker(Offset) / 10}) PLL_Flat = PN1Hz + 20 × log(N) + 10 × log(f_{PD} / 1 Hz) PLL_Flicker = PN10kHz - 10 × log(Offset / 10 kHz) + 20 × log(f_{VCO} / 1 GHz)
 (3) Charge pump mismatch varies as a function of charge pump voltage. Consult typical performance characteristics to see this variation.

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NSTRUMENTS

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6.7 Timing Requirements, Programming Interface (CLK, DATA, LE)

		MIN	TYP	MAX	UNIT
t _{CE}	Clock to LE low time	10			ns
t _{CS}	Data to clock setup time	4			ns
t _{CH}	Data to clock hold time	4			ns
t _{CWH}	Clock pulse width high	10			ns
t _{CWL}	Clock pulse width low	10			ns
t _{CES}	Enable to clock setup time	10			ns
t _{EWH}	Enable pulse width high	10			ns



Figure 1. Serial Data Input Timing

There are several other considerations for programming:

- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift register to an actual counter.
- If no LE signal is given after the last data bit and the clock is kept toggling, then these bits are read into the next lower register. This eliminates the need to send the address each time.
- A slew rate of at least 30 V/µs is recommended for the CLK, DATA, and LE signals
- Timing specs also apply to readback. Readback can be done through the MUXout, TRIG1, TRIG2, or MOD terminals.



6.8 Typical Characteristics



Typical Characteristics (continued)





Typical Characteristics (continued)





7 Detailed Description

7.1 Overview

The LMX2491 is a microwave PLL, consisting of a reference input and divider, high frequency input and divider, charge pump, ramp generator, and other digital logic. The Vcc power supply pins run at a nominal 3.3 volts, while the charge pump supply pin, Vcp, operates anywhere from V_{CC} to 5 volts. The device is designed to operate with an external loop filter and VCO. Modulation is achieved by manipulating the MASH engine.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 OSCin Input

The reference can be applied in several ways. If using a differential input, this must be terminated differentially with a 100- Ω resistance and AC-coupled to the OSCin and GND/OSCin* terminals. If driving this single-ended, then the GND/OSCin* terminal may be grounded, although better performance is attained by connecting the GND/OSCin* terminal through a series resistance and capacitance to ground to match the OSCin terminal impedance.

7.3.2 OSCin Doubler

The OSCin doubler allows the input signal to the OSCin to be doubled to have higher phase detector frequencies. This works by clocking on both the rising and falling edges of the input signal, so it therefore requires a 50% input duty cycle.

7.3.3 R Divider

The R counter is 16 bits divides the OSCin signal from 1 to 65535. If DIFF_R = 0, then any value can be chosen in this range. If DIFF_R = 1, then the divide is restricted to 2, 4, 8, and 16, but allows for higher OSCin frequencies.

7.3.4 PLL N Divider

The 16-bit N divider divides the signal at the Fin terminal down to the phase detector frequency. It contains a 4/5 prescaler that creates minimum divide restrictions, but allows the N value to increment in values of one.

MODULATOR ORDER	MINIMUM N DIVIDE			
Integer Mode, 1st-Order Modulator	16			
2nd-Order Modulator	17			
3rd-Order Modulator	19			
4th-Order Modulator	25			

Table 1. Allowable Minimum N Divider Values

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7.3.5 Fractional Circuitry

The fractional circuitry controls the N divider with delta sigma modulation that supports a programmable first, second, third, and fourth-order modulator. The fractional denominator is a fully programmable 24-bit denominator that can support any value from 1, 2, ..., 2^{24} , with the exception when the device is running one of the ramps, and in this case it is a fixed size of 2^{24} .

7.3.6 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the R and N dividers and generates a correction voltage corresponding to the phase error. This voltage is converted to a correction current by the charge pump. The phase detector frequency, f_{PD} , can be calculated as follows: $f_{PD} = f_{OSCin} \times OSC_2X / R$.

The charge pump supply voltage on this device, V_{CP} , can be either run at the V_{CC} voltage, or up to 5.25 volts to get higher tuning voltages to present to the VCO.

7.3.7 External Loop Filter

The loop filter is external to the device and is application specific. Texas Instruments website has details on this at www.ti.com.

7.3.8 Fastlock and Cycle Slip Reduction

This PLL has a Fastlock and a cycle slipping reduction feature. The user can enable these two features by programming FL_TOC to a non-zero value. Every time PLL_N (the feedback divider, register R17 and R16) is written, the Fastlock feature engages for the prescribed time set in FL_TOC. There are 3 actions that can be enabled while the counter is running:

- 1. Change the charge pump current to the desired higher value FL_CPG. Typically this value would be set to the maximum at 31x. This increases the loop bandwidth and hence reduces lock time.
- 2. Change the phase detector frequency with FL_CSR to reduce cycle slipping. The phase detector frequency can be reduced by a factor 2 or 4 to reduce cycle slipping.
- 3. The loop filter can be configured to have a switchable R2 resistor to increase loop bandwidth and hence reduce lock time. A resistor R2pLF is added in parallel to R2_LF and connected to the a terminal on the PLL to use the internal switch. Any of the terminal MUXout, MOD, TRIG1,or TRIG2 can be configured for the function. The terminal configuration is set as *Output TOC Running*. Also set the terminal as *output inverted OD* (OD for open-drain) so the output will be high impedance in normal operation and act as ground in Fastlock. The suggested schematic for that feature is shown in Figure 12.



Figure 12. Suggested Schematic to Enable the Variable Loop Bandwidth Filter In Fastlock Mode

PARAMETER	NORMAL OPERATION	FASTLOCK OPERATION		
Charge Pump Gain	CPG	FL_CPG		
Device Pin (TRIG1, TRIG2, MOD, or MUXout)	High Impedance	Grounded		

Table 2. Fastlock Settings: Charge Pump Gain and Fastlock Pin Status



The resistor and the charge pump current are changed simultaneously so that the phase margin remains the same while the loop bandwidth is by a factor of K as shown in the following table:

	PARAMETER	CALCULATION
FL_CPG	Charge Pump Gain in Fastlock	Typically use the highest value.
К	Loop Bandwidth Multiplier	K = sqrt(FL_CPG / CPG)
R2pLF	External Resistor	R2 / (K - 1)

Table 3. Suggested Equations to Calculate R2pLF

Cycle slip reduction is another method that can also be used to speed up lock time by reducing cycle slipping. Cycle slipping typically occurs when the phase detector frequency exceeds about 100x the loop bandwidth of the PLL. Cycle slip reduction works in a different way than fastlock. To use this, the phase detector frequency is decreased while the charge pump current is simultaneously increased by the same factor. Although the loop bandwidth is unchanged, the ratio of the phase detector frequency to the loop bandwidth is, and this is helpful for cases when the phase detector frequency is high. Because cycle slip reduction changes the phase detector rate, it also impacts other things that are based on the phase detector rate, such as the fastlock timeout-counter and ramping controls.

7.3.9 Lock Detect and Charge Pump Voltage Monitor

The LMX2491 offers two methods to determine if the PLL is in lock: charge pump voltage monitoring and digital lock detect. These features can be used individually or in conjunction to give a reliable indication of when the PLL is in lock. The output of this detection can be routed to the TRIG1, TRIG2, MOD, or MUXout terminals.

7.3.9.1 Charge Pump Voltage Monitor

The charge pump voltage monitor allows the user to set low (CMP_THR_LOW) and high (CMP_THR_HIGH) thresholds for a comparator that monitors the charge pump output voltage.

V _{CP}	THRESHOLD	SUGGESTED LEVEL
3.3 V	CPM_THR_LOW = (Vthresh + 0.08) / 0.085	6 for 0.5-V limit
	CPM_THR_HIGH = (Vthresh - 0.96) / 0.044	42 for 2.8-V limit
5.0.1/	CPM_THR_LOW = (Vthresh + 0.056) / 0.137	4 for 0.5-V limit
5.0 V	CPM_THR_HIGH = (Vthresh -1.23) / 0.071	46 for 4.5-V limit

Table 4. Desired Comparator Threshold Register Settings for Two Charge Pump Supplies

7.3.9.2 Digital Lock Detect

Digital lock detect works by comparing the phase error as presented to the phase detector. If the phase error plus the delay as specified by the PFD_DLY bit is outside the tolerance as specified by DLD_TOL, then this comparison would be considered to be an error, otherwise passing. The DLD_ERR_CNT specifies how may errors are necessary to cause the circuit to consider the PLL to be unlocked. The DLD_PASS_CNT specifies how many passing comparisons are necessary to cause the PLL to be considered to be locked and also resets the count for the errors. The DLD_TOL value should be set to no more than half of a phase detector period plus the PFD_DLY value. The DLD_ERR_CNT and DLD_PASS_CNT values can be decreased to make the circuit more sensitive. If the circuit is too sensitive, then chattering can occur and the DLD_ERR_CNT, DLD_PASS_CNT, or DLD_TOL values should be increased.

NOTE

If the OSCin signal goes away and there is no noise or self-oscillation at the OSCin pin, then it is possible for the digital lock detect to indicate a locked state when the PLL really is not in lock. If this is a concern, then digital lock detect can be combined with charge pump voltage monitor to detect this situation.

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7.3.10 FSK/PSK Modulation

Two-level FSK or PSK modulation can be created whenever a trigger event, as defined by the FSK_TRIG field is detected. This trigger can be defined as a transition on a terminal (TRIG1, TRIG2, MOD, or MUXout) or done purely in software. The RAMP_PM_EN bit defines the modulation to be either FSK or PSK and the FSK_DEV register determines the amount of the deviation. Remember that the FSK_DEV[32:0] field is programmed as the 2's complement of the actual desired FSK_DEV value. This modulation can be added to the modulation created from the ramping functions as well.

Table 5. How to Obtain Deviation for Two Types of Modulation

RAMP_PM_EN	MODULATION TYPE	DEVIATION
0	2 Level FSK	f _{PD} × FSK_DEV / 2 ²⁴
1	2 Level PSK	360° × FSK_DEV / 2 ²⁴

7.3.11 Ramping Functions

The LMX2491 supports a broad and flexible class of FMCW modulation formed by up to 8 linear ramps. When the ramping function is running, the denominator is fixed to a forced value of $2^{24} = 16777216$. The waveform always starts at RAMP0 when the LSB of the PLL_N (R16) is written to. After it is set up, it starts at the initial frequency and have piecewise linear frequency modulation that deviates from this initial frequency as specified by the modulation. Each of the eight ramps can be individually programmed. Various settings are as follows:

RAMP CHARACTERISTIC	PROGRAMMING FIELD NAME	DESCRIPTION
Ramp Length	RAMPx_LEN RAMPx_DLY	The user programs the length of the ramp in phase detector cycles. If RAMPx_DLY = 1, then each count of RAMPx_LEN is actually two phase detector cycles.
Ramp Slope	RAMPx_LEN RAMPx_DLY RAMPx_INC	The user does not directly program slope of the line, but rather this is done by defining how long the ramp is and how much the fractional numerator is increased per phase detector cycle. The value for RAMPx_INC is calculated by taking the total expected increase in the frequency, expressed in terms of how much the fractional numerator increases, and dividing it by RAMPx_LEN. The value programmed into RAMPx_INC is actually the two's complement of the desired mathematical value.
Trigger for Next Ramp	RAMPx_NEXT_TRIG	The event that triggers the next ramp can be defined to be the ramp finishing or can wait for a trigger as defined by Trigger A, Trigger B, or Trigger C.
Next Ramp	RAMPx_NEXT	This sets the ramp that follows. Waveforms are constructed by defining a chain ramp segments. To make the waveform repeat, make RAMPx_NEXT point to the first ramp in the pattern.
Ramp Fastlock	RAMPx_FL	This allows the ramp to use a different charge pump current or use Fastlock
Ramp Flags	RAMPx_FLAG	This allows the ramp to set a flag that can be routed to external terminals to trigger other devices.

Table 6. Register Descriptions of the Ramping Function

7.3.11.1 Ramp Count

If it is desired that the ramping waveform keep repeating, then all that is needed is to make the RAMPx_NEXT of the final ramp equal to the first ramp. This runs until the RAMP_EN bit is set to zero. If this is not desired, then one can use the RAMP_COUNT to specify how may times the specified pattern is to repeat.

7.3.11.2 Ramp Comparators and Ramp Limits

The ramp comparators and ramp limits use programable thresholds to allow the device to detect whenever the modulated waveform frequency crosses a limit as set by the user. The difference between these is that comparators set a flag to alert the user while a ramp limits prevent the frequency from going beyond the prescribed threshold. In either case, these thresholds are expressed by programming the Extended_Fractional_Numerator. CMP0 and CMP1 are two separated comparators but they work in the same fashion.

Extended_Fractional_Numerator = Fractional_Numerator + (N - N^{*}) × 2^{24}

(1)



In Equation 1, N* is the PLL feedback value without ramping. Fractional_Numerator and N are the new values as defined by the threshold frequency. The actual value programmed is the 2's complement of Extended_Fractional_Numerator.

TYPE	PROGRAMMING BIT	THRESHOLD
Domn Limita	RAMP_LIMIT_LOW	Lower Limit
Ramp Limits	RAMP_LIMIT_HIGH	Upper Limit
Ramp Comparators	RAMP_CMP0 RAMP_CMP1	For the ramp comparators, if the ramp is increasing and exceeds the value as specified by RAMP_CMPx, then the flag goes high, otherwise it is low. If the ramp is decreasing and goes below the value as specified by RAMP_CMPx, then the flag goes high, otherwise it is low.

Table 7. Regis	ster Descriptions	of Ramp Com	parators and Limits

7.3.12 Power-on-reset (POR)

The power-on-reset circuitry sets all the registers to a default state when the device is powered up. This same reset can be done by programming SWRST = 1. In the programming section, the power on reset state is given for all the programmable fields.

7.3.13 Register Readback

The LMX2491 allows any of its registers to be read back. MOD, MUXout, TRIG1 or TRIG2 pin can be programmed to support register-readback serial-data output. To read back a certain register value, follow the following steps:

- 1. Set the R/W bit to 1; the data field contents are ignored.
- 2. Send the register to the device; readback serial data will be output starting at the 17th clock cycle.



Figure 13. Register Readback Timing Diagram

7.4 Device Functional Modes

The two primary ways to use the LMX2491 are to run it to generate a set of frequencies

7.4.1 Continuous Frequency Generator

In this mode, the LMX2491 generates a single frequency that only changes when the N divider is programmed to a new value. In this mode, the RAMP_EN bit is set to 0 and the ramping controls are not used. The fractional denominator can be programmed to any value from 1 to 16777216. In this kind of application, the PLL is tuned to different channels, but at each channel, the goal is to generate a stable fixed frequency.

7.4.1.1 Integer Mode Operation

In integer mode operation, the VCO frequency needs to be an integer multiple of the phase detector frequency. This can be the case when the output frequency or frequencies are nicely related to the input frequency. As a rule of thumb, if this an be done with a phase detector of as high as the lesser of 10 MHz or the OSCin frequency, then this makes sense. To operate the device in integer mode, disable the fractional circuitry by programming the fractional order (FRAC_ORDER), dithering (FRAC_DITH), and numerator (FRAC_NUM) to zero.

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Device Functional Modes (continued)

7.4.1.2 Fractional Mode Operation

In fractional mode, the output frequency does not need to be an integer multiple of the phase detector frequency. This makes sense when the channel spacing is more narrow or the input and output frequencies are not nicely related. There are several programmable controls for this such as the modulator order, fractional dithering, fractional numerator, and fractional denominator. There are many trade-offs with choosing these, but here are some guidelines

PARAMETER	FIELD NAME	HOW TO CHOOSE
Fractional Numerator and Denominator	FRAC_NUM FRAC_DEN	The first step is to find the fractional denominator. To do this, find the frequency that divides the phase detector frequency by the channel spacing. For instance, if the output ranges from 5000 to 5050 in 5-MHz steps and the phase detector is 100 MHz, then the fractional denominator is 100 MHz / 5 = 20. So for a an output of 5015 MHz, the N divider would be 50 + 3/20. In this case, the fractional numerator is 3 and the fractional denominator is 20. Sometimes when dithering is used, it makes sense to express this as a larger equivalent fraction. Note that if ramping is active, the fractional denominator is forced to 2^{24} .
Fractional Order	FRAC_ORDER	There are many trade-offs, but in general try either the 2nd or 3rd-order modulator as starting points. The 3rd-order modulator may give lower main spurs, but may generate others. Also if dithering is involved, it can generate phase noise.
Dithering	FRAC_DITH	Dithering can reduce some fractional spurs, but add noise. Consult application note AN-1879 Fractional N Frequency Synthesis for more details on this.

7.4.2 Modulated Waveform Generator

In this mode, the device can generate a broad class of frequency sweeping waveforms. The user can specify up to 8 linear segments to generate these waveforms. When the ramping function is running, the denominator is fixed to a forced value of $2^{24} = 16777216$

In addition to the ramping functions, there is also the capability to use a terminal to add phase or frequency modulation that can be done by itself or added on top of the waveforms created by the ramp generation functions.

7.5 Programming

7.5.1 Loading Registers

The device is programmed using several 24-bit registers. Each register consists of a data field, an address field, and a R/W bit. The MSB is the R/W bit. 0 means register write while 1 means register read. The following 15 bits of the register are the address, followed by the next 8 bits of data. The user has the option to pull the LE terminal high after this data, or keep sending data and it applies this data to the next lower register. So instead of sending three registers of 24 bits each, one could send a single 40-bit register with the 16 bits of address and 24 bits of data. For that matter, the entire device could be programmed as a single register if desired.

7.6 Register Maps

Registers are programmed in REVERSE order from highest to lowest. Registers NOT shown in this table or marked as reserved can be written as all 0s unless otherwise stated. The POR value is the power on reset value that is assigned when the device is powered up or the SWRST bit is asserted.

REGI	STER	D7 D6 D5 D4 D3 D2 D1 D0						POR		
0	0	0	0	0	1	1	0	0	0	0x18
1	0x1	Reserved							0x00	
2	0x2	0 0 0 0 0 0 SWRST POWERDOWN[1:0]					0x00			
3 - 15	0x3 - 0xF	Reserved							-	
16	0x10	PLL_N[7:0]						0x64		

i able 9. Register Map	Fable	9.	Reg	ister	Map
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Register Maps (continued)

REGISTER D7 D6 D5 D4 D3 D2 D0 POR D1 0x00 PLL_N[15:8] 17 0x11 0 0x00 18 0x12 FRAC_ORDER[2:0] FRAC_DITHER[1:0] PLL_N[17:16] 0x13 FRAC_NUM[7:0] 0x00 19 FRAC_NUM[15:8] 0x00 20 0x14 21 FRAC_NUM[23:16] 0x00 0x15 22 0x16 FRAC_DEN[7:0] 0x00 23 0x17 FRAC_DEN[15:8] 0x00 24 0x18 FRAC_DEN[23:16] 0x00 25 0x04 0x19 PLL_R[7:0] 26 0x1A PLL_R[15:8] 0x00 PLL_R_ OSC_2X 0x08 27 0x1B 0 FL_CSR[1:0] PFD_DLY[1:0] 0 DIFF CPPOL 28 0x1C 0 0 CPG[4:0] 0x00 29 0x1D FL_TOC[10:8] FL_CPG[4:0] 0x00 CPM 0 0x0A 30 0x1E CPM_THR_LOW[5:0] FLAGL CPM 31 0x1F 0 CPM_THR_HIGH[5:0] 0x32 FLAGH 0x00 32 0x20 FL_TOC[7:0] 33 0x21 DLD_PASS_CNT[7:0] 0x0F DLD_TOL[2:0] DLD_ERR_CNTR[4:0] 0x00 34 0x22 MOD **MUXout** TRIG2 TRIG1 35 0x23 1 0 0 1 0x41 MUX[5] _MUX[5] _MUX[5] _MUX[5] TRIG1_MUX[4:0] TRIG1_PIN[2:0] 0x08 36 0x24 37 0x25 TRIG2_MUX[4:0] TRIG2_PIN[2:0] 0x10 38 0x26 MOD_MUX[4:0] MOD_PIN[2:0] 0x18 MUXout_PIN[2:0] MUXout_MUX[4:0] 0x38 39 0x27 0x28 -40 - 57 Reserved _ 0x39 RAMP RAMP 58 0x3A RAMP_TRIG_A[3:0] 0 RAMP_EN 0x00 PM_EN CLK 59 0x3B RAMP_TRIG_C[3:0] RAMP_TRIG_B[3:0] 0x00 60 0x3C RAMP_CMP0[7:0] 0x00 61 0x3D RAMP_CMP0[15:8] 0x00 62 0x3E RAMP_CMP0[23:16] 0x00 63 0x3F RAMP_CMP0[31:24] 0x00 64 0x40 RAMP_CMP0_EN[7:0] 0x00 65 0x41 RAMP_CMP1[7:0] 0x00 66 0x42 RAMP_CMP1[15:8] 0x00 RAMP_CMP1[23:16] 67 0x43 0x00 68 0x44 RAMP_CMP1[31:24] 0x00 69 0x45 RAMP_CMP1_EN[7:0] 0x00 RAMP RAMP FSK_ RAMP RAMP 0 70 0x46 FSK_TRIG[1:0] 0x08 LIML[32] DEV[32] CMP1[32] CMP0[32] LIMH[32] FSK_DEV[7:0] 71 0x47 0x00 72 0x48 FSK_DEV[15:8] 0x00 73 0x00 0x49 FSK_DEV[23:16] 74 0x4A FSK_DEV[31:24] 0x00

Table 9. Register Map (continued)



Register Maps (continued)

Table 9. Register Map (continued)

REGI	STER	D7	D6	D5	D4	D3	D2	D1	D0	POR
75	0x4B		RAMP_LIMIT_LOW[7:0]						0x00	
76	0x4C	RAMP_LIMIT_LOW[15:8]						0x00		
77	0x4D	RAMP_LIMIT_LOW[23:16]							0x00	
78	0x4E	RAMP_LIMIT_LOW[31:24]							0x00	
79	0x4F	RAMP_LIMIT_HIGH[7:0]							0xFF	
80	0x50				RAMP_LIMIT	_HIGH[15:8]]			0xFF
81	0x51				RAMP_LIMIT_	_HIGH[23:16	6]			0xFF
82	0x52				RAMP_LIMIT_	_HIGH[31:24]			0xFF
83	0x53				RAMP_CC	DUNT[7:0]				0x00
84	0x54	RAMP_TR	RAMP_TRIG_INC[1:0] RAMP_ AUTO RAMP_COUNT[12:8]							0x00
85	0x55				Rese	erved				0x00
86	0x56				RAMP0_	INC[7:0]				0x00
87	0x57				RAMP0_I	NC[15:8]				0x00
88	0x58		1	1	RAMP0_II	NC[23:16]				0x00
89	0x59	RAMP0_ DLY	RAMP0_ FL			RAMP0_I	NC[29:24]			0x00
90	0x5A				RAMP0_	LEN[7:0]				0x00
91	0x5B				RAMP0_L	EN[15:8]				0x00
92	0x5C	RAMP0_NEXT[2:0]RAMP0_ NEXT_TRIG[1:0]RAMP0_ RSTRAMP0_FLAG[1:0]						0x00		
93	0x5D	RAMP1_INC[7:0]						0x00		
94	0x5E	RAMP1_INC[15:8]						0x00		
95	0x5F	RAMP1_INC[23:16]						0x00		
96	0x60	RAMP1_ DLY	RAMP1_ RAMP1_ DLY FL RAMP1_INC[29:24]						0x00	
97	0x61	RAMP1_LEN[7:0]						0x00		
98	0x62	RAMP1_LEN[15:8]						0x00		
99	0x63	RAMP1_NEXT[2:0] RAMP1_ RAMP1_ RAMP1_FLAG[1:0]					0x00			
100	0x64				RAMP2_	INC[7:0]				0x00
101	0x65				RAMP2_I	NC[15:8]				0x00
102	0x66				RAMP2_I	NC[23:16]				0x00
103	0x67	RAMP2 DLY	RAMP2_ FL			RAMP2_I	NC[29:24]			0x00
104	0x68				RAMP2_	LEN[7:0]				0x00
105	0x69				RAMP2_L	EN[15:8]				0x00
106	0x6A	RA	MP2_NEXT[2:0]	RAM NEXT_T	IP2_ RIG[1:0]	RAMP2_ RST	RAMP2_I	FLAG[1:0]	0x00
107	0x6B				RAMP3_	INC[7:0]				0x00
108	0x6C				RAMP3_I	NC[15:8]				0x00
109	0x6D				RAMP3_II	NC[23:16]				0x00
110	0x6E	RAMP3_ DLY	RAMP3_ FL			RAMP3_I	NC[29:24]			0x00
111	0x6F		,	,	RAMP3_	LEN[7:0]				0x00
112	0x70				RAMP3_L	EN[15:8]				0x00
113	0x71	RA	MP3_NEXT[2:0]	RAM NEXT_T	IP3_ RIG[1:0]	RAMP3_ RST	RAMP3_I	FLAG[1:0]	0x00



Register Maps (continued)

REGI	STER	D7	D6	D5	D4	D3	D2	D1	D0	POR	
114	0x72				RAMP4_	INC[7:0]				0x00	
115	0x73		RAMP4_INC[15:8]								
116	0x74		RAMP4_INC[23:16]								
117	0x75	RAMP4_ DLY	RAMP4_ RAMP4_ RAMP4_INC[29:24]							0x00	
118	0x76				RAMP4_	LEN[7:0]				0x00	
119	0x77				RAMP4_I	_EN[15:8]				0x00	
120	0x78	RA	.MP4_NEXT[2:0]	RAM NEXT_T	1P4_ RIG[1:0]	RAMP4_ RST	RAMP4_	FLAG[1:0]	0x00	
121	0x79				RAMP5_	INC[7:0]				0x00	
122	0x7A				RAMP5_	INC[15:8]				0x00	
123	0x7B				RAMP5_I	NC[23:16]				0x00	
124	0x7C	RAMP5_ DLY	RAMP5_ FL			RAMP5_I	NC[29:24]			0x00	
125	0x7D			•	RAMP5_	LEN[7:0]				0x00	
126	0x7E				RAMP5_I	_EN[15:8]				0x00	
127	0x7F	RA	MP5_NEXT[2:0]	RAM NEXT_T	1P5_ RIG[1:0]	RAMP5_ RST	RAMP5_	FLAG[1:0]	0x00	
128	0x80				RAMP6_	INC[7:0]				0x00	
129	0x81				RAMP6_	INC[15:8]				0x00	
130	0x82				RAMP6_I	NC[23:16]				0x00	
131	0x83	RAMP6_ DLY	RAMP6_ FL			RAMP6_I	NC[29:24]			0x00	
132	0x84				RAMP6_	LEN[7:0]				0x00	
133	0x85				RAMP6_I	_EN[15:8]				0x00	
134	0x86	RA	MP6_NEXT[2:0]	RAM NEXT_T	1P6_ RIG[1:0]	RAMP6_ RST	RAMP6_	FLAG[1:0]	0x00	
135	0x87				RAMP7_	INC[7:0]				0x00	
136	0x88				RAMP7_	INC[15:8]				0x00	
137	0x89				RAMP7_I	NC[23:16]				0x00	
138	0x8A	RAMP7_ DLY	RAMP7_ FL			RAMP7_I	NC[29:24]			0x00	
139	0x8B	RAMP7_LEN[7:0]								0x00	
140	0x8C				RAMP7_I	_EN[15:8]				0x00	
141	0x8D	RA	MP7_NEXT[2:0]	RAM NEXT_T	1P7_ RIG[1:0]	RAMP7_ RST	RAMP7_	FLAG[1:0]	0x00	
142 - 32767	0x8E - 0x7FFF		Reserved							0x00	

Table 9. Register Map (continued)

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7.6.1 Register Field Descriptions

The following sections go through all the programmable fields and their states. Additional information is also available in the applications and feature descriptions sections as well. The POR column is the power on reset state that this field assumes if not programmed.

7.6.1.1 POWERDOWN and Reset Fields

FIELD	LOCATION	POR	DESCRIPTION	N AND STATE	S
	R2[1:0]	0	POWERDOWN Control	Value	POWERDOWN State
				0	Power Down, ignore CE
POWERDOWN [1:0]				1	Power Up, ignore CE
				2	Power State Defined by CE terminal state
				3	Reserved
	R2[2]	0	Software Reset. Setting this bit sets all	Value	Reset State
SWRST				0	Normal Operation
				1	Register Reset

Table 10. POWERDOWN and Reset Fields



7.6.1.2 Dividers and Fractional Controls

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
PLL_N [17:0]	R18[1] to R16[0]	16	Feedback N counter Divide value. Minimum the register R16 begins any ramp execution	count is 16. when RAMP_	Maximum is 262132. Writing of EN = 1.
				Value	Dither
				0	Weak
FRAC_ DITHER	R18[3:2]	0	Dither used by the fractional modulator	1	Medium
[1:0]				2	Strong
				3	Disabled
				Value	Modulator Order
				0	Integer Mode
				1	1st Order Modulator
FRAC_ORDER	R18[6:4]	0	Fractional Modulator order	2	2nd Order Modulator
[2.0]				3	3rd Order Modulator
				4	4th Order Modulator
				5-7	Reserved
FRAC_NUM [23:0]	R21[7] to R19[0]	0	Fractional Numerator. This value should denominator.	be less that	an or equal to the fractional
FRAC_DEN [23:0]	R24[7] to R22[0]	0	Fractional Denominator. If RAMP_EN = 1, fixed to 2^{24} .	this field is i	gnored and the denominator is
PLL_R [15:0]	R26[7] to R25[0]	1	Reference Divider value. Selecting 1 bypass	es counter.	
	R27[0]	0		Value	Doubler
OSC_2X			Enables the Doubler before the Reference	0	Disabled
				1	Enabled
	R27[2]	0	Enables the Differential R counter.	Value	R Divider
PLL_R _DIFF			This allows for higher OSCin frequencies,	0	Single-Ended
			16.	1	Differential
				Value	Pulse Width
			Sets the charge pump minimum pulse	0	Reserved
PFD_DLY	R27[4:3]	1	width. This could potentially be a trade-off	1	860 ps
[1.0]			Setting 1 is recommended for general use.	2	1200 ps
				3	1500 ps
				Value	Charge Pump State
				0	Tri-State
CPG	Destinat			1	100 µA
[4:0]	R28[4:0]	0	Charge pump gain	2	200 µA
				31	3100 µA
			Charge pump polarity is used to	Value	Charge Pump Polarity
			accommodate VCO with either polarity so	0	Positive
CPPOL	R28[5]	0	IF reference (R) output is faster than feedback (N) output, R28[5]==0 THEN charge pump will source current R28[5]==1 THEN charge pump will sink current	1	Negative

Table 11. Dividers and Fractional Controls

7.6.1.2.1 Speed Up Controls (Cycle Slip Reduction and Fastlock)

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
			Cycle Slip Reduction (CSR) reduces the	Value	CSR Value
			phase detector frequency by multiplying both the R and N counters by the CSR	0	Disabled
			value while either the FastLock Timer is	1	x 2
FL_CSR	R27[6:5]	0	counting or the RAMPx_FL = 1 and the part is ramping. Care must be taken that	2	x 4
[1.0]			the R and N divides remain inside the range of the counters. Cycle slip reduction is generally not recommended during ramping.	3	Reserved
	R29[4:0]	0		Value	Fastlock Charge Pump Gain
				0	Tri-State
FL_ CPG			Charge pump gain only when Fast Lock Timer is counting down or a ramp is running with RAMPx_FL = 1	1	100 µA
[4:0]				2	200 µA
				31	3100 µA
			Fast Lock Timer. This counter starts	Value	Fastlock Timer Value
			counting when the user writes the PLL N(Register R16). During this time the	0	Disabled
FL TOC	R29[7:5]	_	FL_CPG gain is sent to the charge pump,	1	1 x 32 = 32
[10:0]	and R32[7:0]	0	and the FL_CSR shifts the R and N counters if enabled. When the counter		
			terminates, the normal CPG is presented and the CSR undo's the shifts to give a normal PFD frequency.	2047	2047 x 32 = 65504

Table 12. FastLock and Cycle Slip Reduction



7.6.2 Lock Detect and Charge Pump Monitoring

FIELD	LOCATION	POR	R DESCRIPTION AND STATES		
				Value	Threshold
CPM_THR _LOW	D20[5:0]	0.00	Charge pump voltage low threshold value.	0	Lowest
[5:0]	R30[5:0]	UXUA	this threshold, the LD goes low.		
				63	Highest
				Value	Flag Indication
CPM_FLAGL	R30[6]	-	This is a read only bit. Low indicates the charge pump voltage is	0	Charge pump is below CPM_THR_LOW threshold
			below the minimum threshold.	1	Charge pump is above CPM_THR_LOW threshold
				Value	Threshold
CPM_THR _HIGH	D21[5:0]	0,22	Charge pump voltage high threshold value.	0	Lowest
[5:0]	K31[5.0]	0x32	this threshold, the LD goes low.		
				63	Highest
	R31[6]		This is a second a she hit	Value	Threshold
CPM_FLAGH		-	Charge pump voltage high comparator reading High indicates the charge pump	0	Charge pump is below CPM_THR_HIGH threshold
			voltage is above the maximum threshold.	1	Charge pump is above CPM_THR_HIGH threshold
DLD_ PASS_CNT [7:0]	R33[7:0]	0xFF	Digital Lock Detect Filter amount. There mu and less than DLD_ERR edges before the D smaller speeds the detection of lock, but also	ust be at leas DLD is conside o allows a high	t DLD_PASS_CNT good edges ered in lock. Making this number her chance of DLD chatter.
DLD_ ERR_CNT [4:0]	R34[4:0]	0	Digital Lock Detect error count. This is th DLD_TOL that are allowed before DLD is recommended value is 4.	e maximum de-asserted.	number of errors greater than Although the default is 0, the
				Value	Window and f _{PD} Frequency
				0	1 ns (f _{PD} > 130 MHz)
			Digital Lock detect edge window. If both N and R edges are within this window, it is considered a "good" edge. Edges that are	1	1.7 ns (80 MHz < f _{PD} ≤ 130 MHz)
DLD _TOL	D24[7:5]	0	farther apart in time are considered "error"	2	3 ns (60 MHz < $f_{PD} \le 80$ MHz)
[2:0]	1.04[7.0]	U	edges. Window choice depends on phase	3	6 ns (45 MHz < $f_{PD} \le$ 60 MHz)
			pulse width, fractional modulator order and the users desired margin.	4	10 ns (30 MHz < f _{PD} ≤ 45 MHz)
				5	18 ns (f _{PD} ≤ 30 MHz)
				6 and 7	Reserved

Table 13. Lock Detect and Charge Pump Monitor

7.6.3 TRIG1, TRIG2, MOD, and MUXout Pins

FIELD	LOCATION	POR	DESCRIPTION	AND STATE	S
				Value	Pin Drive State
TRIG1_PIN	D26[2:0]	0	-	0	TRISTATE (default)
[2:0]	R30[2:0]			1	Open Drain Output
				2	Pullup / Pulldown Output
TRIG2 _PIN [2:0]	R37[2:0]	0	This is the terminal drive state for the	3	Reserved
MOD_ PIN [2:0]	R38[2:0]	0	TRIG1, TRIG2, MOD, and MUXout Pins	4	GND
				5	Inverted Open Drain Output
MUXout_ PIN [2:0]	R39[2:0]	0		6	Inverted Pullup / Pulldown Output
				7	Input

Table 14. TRIG1, TRIG2, MOD, and MUXout Terminal States



FIELD	LOCATION	POR	DESCRIPTION	NAND STATE	S	
				Value	MUX State	
				0	GND	
				1	Input TRIG1	
				2	Input TRIG2	
				3	Input MOD	
				4	Output TRIG1 after synchronizer	
				5	Output TRIG2 after synchronizer	
				6	Output MOD after synchronizer	
				7	Output Read back	
				8	Output CMP0	
				9	Output CMP1	
				10	Output LD (DLD good AND CPM good)	
				11	Output DLD	
				12	Output CPMON good	
			These fields control what signal is muxed to or from the TRIG1, TRIG2, MOD, and MUXout pins. Some of the abbreviations used are:	13	13	Output CPMON too High
				14	Output CPMON too low	
TRIG1_MUX [5:0]	R36[7:3], R35[3]	1		15	Output RAMP LIMIT EXCEEDED	
TRIG2_MUX	R37[7:3],	2		16	Output R Divide/2	
[5:0]	R35[4]		COMP0, COMP1: Comparators 0 and 1	17	Output R Divide/4	
	R38[7:3],	3	CPM: Charge Pump Monitor	18	Output N Divide/2	
			CPG: Charge Pump Gain	19	Output N Divide/4	
MUXout_MUX [5:0]	R39[7:3], R35[5]	7	CPUP: Charge Pump Up Pulse	20	Reserved	
[0:0]	[0]		CPDN: Charge Pump Down Pulse	21	Reserved	
				22	Output CMP0RAMP	
				23	Output CMP1RAMP	
				24	Reserved	
				25	Reserved	
				26	Reserved	
				27	Reserved	
				28	Output Faslock	
				29	Output CPG from RAMP	
				30	Output Flag0 from RAMP	
				31	Output Flag1 from RAMP	
				32	Output TRIGA	
				33	Output TRIGB	
				34	Output TRIGC	
				35	Output R Divide	
				36	Output CPUP	
				37	Output CPDN	
				38	Output RAMP_CNT Finished	
				39 to 63	Reserved	

Table 15. TRIG1, TRIG2, MOD, and MUXout Selections

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7.6.4 Ramping Functions

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
		Enables the RAMP functions. When this bi		Value	Ramp
RAMP FN	R58[0]	0	is set, the Fractional Denominator is fixed to 2 ²⁴ , RAMP execution begins at RAMP0	0	Disabled
	[0]	Ū	upon the PLL_N[7:0] write. The Ramp should be set up before RAMP_EN is set.	1	Enabled
			RAMP clock input source. The ramp can	Value	Source
RAMP_CLK	R58[1]	0	be clocked by either the phase detector clock or the MOD terminal based on this	0	Phase Detector
			selection.	1	MOD Terminal
				Value	Modulation Type
RAMP_PM_EN	R58[2]	0	Phase modulation enable.	0	Frequency Modulation
				1	Phase Modulation
				Value	Source
				0	Never Triggers (default)
				1	TRIG1 terminal rising edge
				2	TRIG2 terminal rising edge
				3	MOD terminal rising edge
				4	DLD Rising Edge
RAMP_TRIGA	R58[7·4]			5	CMP0 detected (level)
	100[7.4]			6	RAMPx_CPG Rising edge
RAMP_TRIGB [3:0]	R59[3:0]	0	Trigger A, B, and C Sources	7	RAMPx_FLAG0 Rising edge
				8	Always Triggered (level)
[3:0]	R59[7:4]			9	TRIG1 terminal falling edge
				10	TRIG2 terminal falling edge
				11	MOD terminal falling edge
				12	DLD Falling Edge
				13	CMP1 detected (level)
				14	RAMPx_CPG Falling edge
				15	RAMPx_FLAG0 Falling edge
RAMP_CMP0 [32:0]	R70[0], R63[7] to R60[0]	0	Twos compliment of Ramp Comparator 0 va R70.	lue. Be aware	e of that the MSB is in Register
RAMP_CMP0_EN [7:0]	R64[7:0]	0	Comparator 0 is active during each RAMP co is active in and 0 for ramps it should be igno corresponds to R64[7]	prresponding to pred. RAMP0	to the bit. Place a 1 for ramps it corresponds to R64[0], RAMP7
RAMP_CMP1 [32:0]	R70[1], R68[7] to R65[0]	0	Twos compliment of Ramp Comparator 1 va R70.	lue. Be aware	e of that the MSB is in Register
RAMP_CMP1_EN [7:0]	R69[7:0]	0	Comparator 1 is active during each RAMP corresponding to the bit. Place a 1 for ramps is active in and 0 for ramps it should be ignored. RAMP0 corresponds to R64[0], RAMF corresponds to R64[7].		
				Value	Trigger
	DEGLA		Deviation trigger source. When this trigger	0	Always Triggered
FSK_TRIG	R76[4] to R75[3]	0	source specified is active, the FSK_DEV	1	Trigger A
[]			value is applied.	2	Trigger B
				3	Trigger C
FSK_DEV [32:0]	R70[2], R74[7] to R71[0]	0	Twos compliment of the deviation value for f This value should be written with 0 when no R70.	frequency mo t used. Be aw	dulation and phase modulation. are that the MSB is in Register

Table 16. Ramping Functions



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Table 16. Ramping Functions (continued)

FIELD	LOCATION	POR	DESCRIPTION	N AND STATE	ES			
RAMP_LIMIT_LOW [32:0]	R70[3], R78[7] to R75[0]	0	Twos compliment of the ramp lower limit that the ramp can not go below . The ramp limit occurs before any deviation values are included. Care must be taken if the deviation is used and the ramp limit must be set appropriately. Be aware that the MSB is in Register R70.					
RAMP_LIMIT_HIGH [32:0]	R70[4], R82[7] to R79[0]	0x1FF FFFF FF	Twos compliment of the ramp higher limit that the ramp can not go above. The ramp limit occurs before any deviation values are included. Care must be taken if the deviation is used and the ramp limit must be set appropriately. Be aware that the MSB is in Register R70.					
RAMP_COUNT [12:0]	R84[4] to R83[0]	0	Number of RAMPs that is executed before a trigger or ramp enable is brought down. Load zero if this feature is not used. Counter is automatically reset when RAMP_EN goes from 0 to 1.					
	R84[5]			Value	Ramp			
RAMP AUTO		0	Automatically clear RAMP_EN when	0	RAMP_EN unaffected by ramp counter (default)			
			RAMP Count hits terminal count.	1	RAMP_EN automatically brought low when ramp counter terminal counts			
				Value	Source			
RAMP TRIG INC		_	Increment Trigger source for RAMP	0	Increments occur on each ramp transition			
[1:0]	R84[7:6]	0	Counter. To disable ramp counter, load a count value of 0	1	Increment occurs on Trigger A			
				2	Increment occurs on Trigger B			
				3	Increment occurs on Trigger C			

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7.6.5 Individual Ramp Controls

These bits apply for all eight ramp segments. For the field names, x can be 0, 1, 2, 3, 4, 5, 6, or 7.

FIELD	LOCATI ON	POR	DESCRIPTION AND STATES						
RAMPx _INC[29:0]	Varies	0	Signed ramp increment.						
				Value	CPG				
RAMPx _FL	Varies	0	This enables fastlock and cycle slip reduction for ramp x.	0	Disabled				
				1	Enabled				
				Value	Clocks				
RAMPx _DLY	Varies	0	LEN clock instead of the normal 1 f _{PD} cycle. Slows the ramp by a factor of 2	0	1 f _{PD} clock per RAMP tick.(default)				
				1	2 f _{PD} clocks per RAMP tick.				
RAMPx _LEN	Varies	0	Number of f _{PD} clocks (if DLY is 0) to continue to increme Maximum of 65536 cycles.	nt RAMP. 1 =	1 cycle, $2 = 2$ cycles, etc.				
					Value	Flag			
			General purpose FLAGs sent out of RAMP at the start of a ramp pattern.	0	Both FLAG1 and FLAG0 are zero. (default)				
RAMPx	Varies	s 0		1	FLAG0 is set, FLAG1 is clear				
				2	FLAG0 is clear, FLAG1 is set				
				3	Both FLAG0 and FLAG1 are set.				
			Forces a clear of the ramp accumulator at the start of a	Value	Reset				
RAMPx RST	Varies	0	ramp pattern. This is used to erase any accumulator creep	0	Disabled				
			that can occur depending on how the ramps are defined.	1	Enabled				
				Value	Operation				
RAMPx_			Determines what event is necessary to cause the state	0	RAMPx_LEN				
NEXT TRIG Varie	Varies	0	RAMPX LEN counter reaches zero or one of the events for	1	Trigger A				
[1:0]			Triggers A, B, or C.	2	Trigger B				
				3	Trigger C				
RAMPx _NEXT[2:0]	Varies	0	The next RAMP to execute when the length counter times out						

Table 17. Individual Ramp Controls



8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMX2491 can be used in a broad class of applications such as generating a single frequency for a high frequency clock, generating a tunable range of frequencies, or generating swept waveforms that can be used in applications such as radar.

8.2 Typical Application

Figure 14 is an example that could be used in a typical application.



Figure 14. Typical Schematic

Typical Application (continued)

8.2.1 Design Requirements

For these examples, it will be assumed that there is a 100 MHz input signal and the output frequency is between 1500 and 1520 MHz with various modulated waveforms.

PARAMETER	SYMBOL	VALUE	COMMENTS
Input frequency	f _{OSCin}	100 MHz	
Phase detector frequency	f _{PD}	50 MHz	There are many possibilities, but this choice gives good performance.
VCO frequency	f _{VCO}	1500 - 1520 MHz	In the different examples, the VCO frequency is actually changing. However, the same loop filter design can be used for all examples. Unmodulated VCO frequency or steady state VCO frequency without ramp is 1500 MHz.
VCO gain	K _{VCO}	65 MHz/V	This parameter has nothing to do with the LMX2491, but is rather set by the external VCO choice.

8.2.2 Detailed Design Procedure

The first step is to calculate the reference divider (PLL_R) and feedback divider (PLL_N) values as shown in the table that follows.

PARAMETE R	SYMBOL AND CALCULATIONS	VALUE	COMMENTS
Average VCO frequency	$f_{VCOavg} = (f_{VCOmax} + f_{VCOmin}) / 2$	1510 MHz	To design a loop filter, one designs for a fixed VCO value, although it is understood that the VCO will tune around. This typical value is usually chosen as the average VCO frequency
VCO gain	K _{vco}	65 MHz/V	This parameter has nothing to do with LMX2491, but is rather set by the external VCO choice. In this case, it was the CVC055BE-1400-1624 VCO.
VCO input capacitance	C _{VCO}	120 pF	This parameter has nothing to do with LMX2491, but is rather set by the external VCO choice.
PLL loop bandwidth	LBW	380 kHz	This bandwidth is very wide to allow the VCO frequency to be modulated.
Charge pump gain	CPG	3.1 mA	Using the larger gain allows a wider loop bandwidth and gives good phase performance.
R-divider	$PLL_R = f_{OSCin} / f_{PD}$	2	
N-divider	$PLL_N = f_{VCO} / f_{PD}$	96	
	C1_LF	68 pF	
	C2_LF	3.9 nF	
Loop filter	C3_LF	150 pF	These were calculated by TI PLLatinum Simulator Tool.
componenta	R2_LF	390 Ω	
	R3_LF	150 Ω	

Table 19. Detailed Design Procedure

Once a loop filter bandwidth is chosen, the external loop filter component values can be calculated with a tool such as PLLatinum Simulator Tool. It is also highly recommended to look at the EVM User's Guide. TICS Pro software is an excellent starting point and example to see how to program this device.

8.2.3 TICS Pro Basic Setup

In the following application examples, TICS Pro is used to program the device to implement different ramp profiles. The following procedure shows how to setup TICS Pro to put the device to lock to 1500 MHz without modulation or ramp.





Figure 15. TICS Pro

- 1. In the Menu bar, click Select Device and then select LMX2491.
- 2. In the Menu bar, click Default Configuration and then select Default Mode.
- 3. In the Page window, click PLL.
- 4. In the Main window, change R Divider value to 2 and VCO value to 1500.
- 5. In the Menu bar, click USB Communications and then click Write All Registers. The device is now locked to 1500 MHz.

Other TICS Pro fundamentals:

- When a particular content in the Main window is moused-over, the Context window will show a brief description of that content.
- An alternative method to write all registers is press the Ctrl key and L key from the keyboard.
- Whenever a value is updated in the Main window, the Message window will show which register is being updated

8.2.4 Frequency Shift Keying Example

FSK operation requires an external input trigger signal at either MOD, TRIG1 or TRIG2 pin. In this example, MOD pin is selected as the Trigger A source. A 20 kHz square-wave clock will be applied to MOD pin to toggle the RF output to switch between 1500 MHz and 1502 MHz. That is, FSK frequency deviation is 2 MHz. The following register bits are required to set in order to initiate FSK operation.

PARAMETER	REGISTER BIT	SETTING	COMMENTS
Frequency deviation	FSK_DEV	671089 = 2 MHz	Frequency deviation = ($f_{PD} \times FSK_DEV$) / 2^{24}
MOD pin characteristic	MOD_PIN	7 = Input	Set MOD pin as an input pin
FSK trigger source	FSK_DEV_TRIG	1 = Trigger A	Use Trigger A to trigger FSK
Trigger source definition	RAMP_TRIGA	3 = MOD Rising Edge	When there is a L-to-H transition at MOD pin, the set amount of frequency deviation will be added to the unmodulated carrier
Enable ramp	RAMP_EN	1 = Enabled	Activate FSK operation

Table 20. FSK Register Settings



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Figure 16. TICS Pro FSK Configuration



Figure 17. Frequency Shift Keying Example

8.2.5 Single Sawtooth Ramp Example

In this example, Trigger B is used to trigger the ramp generator of LMX2491 to general a single frequency ramp between 1500 MHz and 1520 MHz. Ramp duration is 50 μ s. The ramp will finish and return back to 1500 MHz immediately when the output frequency reaches 1520 MHz. Trigger 1 pin is assigned as Trigger B source.

Two ramp segments are setup to create this one-time single ramp. RAMP0 is used to establish a trigger for the second ramp segment - RAMP1. When a trigger signal is received, RAMP1 will execute and bring the output frequency to 1520 MHz in 50 µs.



Table 21. Single Sawtooth Ramp Register Setting

PARAMETER	REGISTER BIT	SETTING	COMMENTS
Set maximum ramp frequency threshold	RAMP_LIMIT_HIGH	16777216 = 1550 MHz	This threshold frequency can be anything above 1520 MHz. The fractional numerator is equal to 0 at 1550 MHz. The N-Divider difference between 1500 MHz and 1550 MHz is 1. From Equation 1, this threshold is equal to $0 + (1 \times 2^{24}) = 16777216$.
Set minimum ramp frequency threshold	RAMP_LIMIT_LOW	8573157376 = 1450 MHz	This threshold frequency can be anything below 1500 MHz. This threshold is equal to –16777216. This is a 33-bit long register, 2's complement is therefore equal to 8573157376.
Number of ramp in each ramp segment	RAMP0_LEN, RAMP1_LEN	2500 = for ramp duration equals 50 μs	The duration of RAMP0 is not matter, for demonstration convenience, it has the same ramp duration as RAMP1. During ramp, LMX2491 ramp generator will increment its output frequency once per phase detector cycle. For ramp duration of 50 μ s and f _{PD} = 50 MHz, there are 2500 ramps [= 50 μ s / (1 / 50 MHz)].
Frequency change per ramp in RAMP0	RAMP0_INC	0	Since the output frequency would not change in RAMP0, there is no frequency increment.
Set next ramp segment	RAMP0_NEXT	1 = RAMP1	Set RAMP1 as the next ramp segment following RAMP0.
Set next ramp segment trigger source	RAMP0_NEXT_TRIG	2 = Trigger B	Use Trigger B to trigger the execution of RAMP1.
Rest fractional numerator	RAMP0_RST	1 = Reset	RAMP0 will execute again after RAMP1 is finished but RAMP1 does not end at 1500 MHz, a reset to the fractional numerator is required before RAMP0 is executed.
Frequency change per ramp in RAMP1	RAMP1_INC	2684 = 8 kHz	Between 1500 MHz and 1520 MHz, there are 2500 ramps. For each ramp, the output frequency will increment by 20 MHz / 2500 = 8 kHz. For f _{PD} = 50 MHz and fractional denominator = 2^{24} , fractional numerator is incremented by a value of (8 kHz x 2^{24}) / 50 MHz \approx 2684.
Set next ramp segment	RAMP1_NEXT	0 = RAMP0	Set RAMP0 as the next ramp segment following RAMP1.
Set next ramp segment trigger source	RAMP1_NEXT_TRIG	0 = TOC Timeout	After RAMP1 is finished, the next ramp segment will execute immediately.
Trigger source definition	RAMP_TRIGB	1 = TRIG1 Rising Edge	When there is a L-to-H transition at TRIG1 pin, RAMP1 will execute.
TRIG1 pin characteristic	TRIG1_PIN	7 = Input	Set TRIG1 pin as an input pin.

It is recommended to use the Ramp Calculator in TICS Pro to create the ramp profile. TICS Pro will calculate the ramp-related register values automatically.

Limit	s and Com	nparato	rs													
	VCO Output Limit	:											1	Register Pro	gramming	
Hig	h 1550	MHz									1	Si High ()	gn [Decimal Valu 6777216	ue 2's 0 167	omplement 77216
Lov	1 450	MHz	0	Valid	In Ra	mp 56	7				1	Low 1		6777216	857	3157376
СМР	0 1500	MHz							on't c	are b	ecause	Sig	gn [ecimal Valu	ie 2's (Complement
СМР	1500	MHz						e	nable	d	с	MP0 0		,)	0	
Ram	ps	Ramp Enat	ole 🗸										_			
Ramp Number	Actual Start Frequency (MHz)	Desired En Frequency (MHz)	id Y	Duration (us)	Dly	Next Ramp	Stra	tart next mp after	RST	r FL	Flags		A	ctual End requency (MHz)	Length	Increment (dec)
0	1500	1500		50		1 -	Trigge	er B	• 1		Disabled	•	150	00	2500	0
1	1500	1520		50		0 -	TOC	Timeout	-		Disabled	•	151	9.9973583	22500	2684
2	-1	10500		100		0 -	TOC 1	Timeout	•		Disabled	•	-1		5000	10000
3	-1	10500		100		0 -	TOC	Timeout	•		Disabled	•	-1		5000	10000
4	-1	10500		100		0 -	TOC	Timeout	•		Disabled	•	-1		5000	10000
5	-1	10500		100		0 -	TOC T	Timeout	•		Disabled	•	-1		5000	10000
6	-1	10500		100		0 -	TOC T	Timeout	•		Disabled	•	-1		5000	10000
7	-1	10500		100		0 -	TOC	Timeout	•		Disabled	•	-1		5000	10000
	Ramp Count 0		Ra	amp Auto	RA	MP_AU	то	Ramp In S	Source	Ramp	Transition	•	0	Incr 0	ement (2s c	complement)
	Trigger Source A	Disabled			_	•		FSK 1	rigger	Disab	led	•	1	2684	1	5 0
	Trigger Source B	TRIG1 Ri	sing E	dge		•		FSK De	viation	0			2	0	6	5 0
	Trigger Source C	Disabled				•		Phase M	lod. En	RA	MP_PM_E	N	3	0	7	7 0

Figure 18. TICS Pro Ramp Calculator



Figure 19. Single Sawtooth Ramp Example

8.2.6 Continuous Sawtooth Ramp Example

This example shows how to generate a continuous sawtooth ramp. Only one ramp segment is necessary as it will loop back to itself.



Ram	ips	Ramp Enable 🛛									
Ramp Number	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	Duration (us)	N Diy Ra	ext St amp ra	art next mp after R	ST FL	Flags	Actual End Frequency (MHz)	Length	Increment (dec)
0	1500	1520	50	0	TOC .	Fimeout 🔻	/	Disabled •	1519.9973583	322500	2684
1	-1	10500	100	0	TOC T	Timeout 🔹		Disabled •	-1	5000	10000
2	-1	10500	100	0	TOC .	Timeout 🔹		Disabled •	-1	5000	10000
3	-1	10500	100	0	TOC .	Fimeout 🔹		Disabled •	-1	5000	10000
4	-1	10500	100	0	TOC .	Fimeout 🔹		Disabled 🔹	-1	5000	10000
5	-1	10500	100	0	TOC .	Fimeout 🔹		Disabled •	-1	5000	10000
6	-1	10500	100	0	TOC .	Fimeout 🔹		Disabled •	-1	5000	10000
7	-1	10500	100	0	TOC .	Fimeout 🔹		Disabled •	-1	5000	10000
							-		Inci	rement (2s co	omplement)
	Ramp Count ()	R	amp Auto	RAMP	AUTO	Ramp in Source	Ram	o Iransition •	0 2684	4	0
	Trigger Source A	Disabled			•	FSK Trigge	Disa	bled 🔻	1 0	5	0
	Trigger Source B	Disabled			•	FSK Deviation	0		2 0	6	0
	Trigger Source C	Disabled			•	Phase Mod. E	n 🗌 R/	MP_PM_EN	3 0	7	0

Figure 20. Continuous Sawtooth Ramp Configuration



Figure 21. Continuous Sawtooth Ramp Example

8.2.7 Continuous Sawtooth Ramp with FSK Example

A ramp and FSK can coexist at the same time. Since the amount of FSK is added to the instantaneous carrier, the FSK will appear at the envelope of the ramp. Furthermore, a ramp and FSK are two independent operations, their register settings can be combined in a single configuration setting. That is, when RAMP_EN is enabled, both frequency ramp and FSK will be activated together.



Ram	nps	Ramp Enable 👿	1								
Ramp Number	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	Duration (us)	Next Dly Ramp	Start next ramp after	RST	FL	Flags	Actual End Frequency (MHz)	Length	Increment (dec)
0	1500	1520	1000	0 -	TOC Timeout	▼		Disabled •	1519.9675559	\$50000	134
1	-1	10500	100	0 -	TOC Timeout	•		Disabled 🔹	Frequent ramp	cy 000	10000
2	-1	10500	100	0 -	TOC Timeout	•		Disabled •	-1	5000	10000
3	-1	10500	100	0 -	TOC Timeout	•		Disabled •	-1	5000	10000
4	-1	10500	100	0 -	TOC Timeout	•		Disabled •	-1	5000	10000
5	-1	10500	100	0 -	TOC Timeout	•		Disabled •	-1	5000	10000
6	-1	10500	100	0 -	TOC Timeout	•		Disabled •	-1	5000	10000
7	-1	10500	100	0 -	TOC Timeout	•		Disabled -	-1	5000	10000
	Ramp Count 0	R	amp Auto	RAMP_A	JTO Ramp In S	Source F	Ramp	Transition •	Incr 0 134	ement (2s c	omplement) 0
	Trigger Source A	MOD Rising Ed	ge	•	FSK 1	rigger 📑	Trigge	er A 🔹	10	5	0
	Trigger Source B	Disabled		•	FSK De	viation	33554	14	28 FSK	6	0
	Trigger Source C	Disabled		•	Phase N	lod. En 🗌	RA	MP_PM_EN	30	7	0

Figure 22. Continuous Sawtooth Ramp with FSK Configuration



Figure 23. Continuous Sawtooth Ramp with FSK Example

8.2.8 Continuous Triangular Ramp Example

Two ramp segments are used to create this ramp pattern. RAMP0 ramps from 1500 MHz to 1520 MHz. RAMP1 brings the frequency back to 1500 MHz and then RAMP0 starts over again. Since RAMP1 already brought the frequency back to 1500 MHz, which is also the start frequency of RAMP0, a reset to fractional numerator is not required.



	is and oon	purute	// 3													
	VCO Output Limit													Register Prog	Iramming	
Hig	h 1550	MH-										Si	gn	Decimal Valu	e 2's 0	Complement
riig	1000	141112										High ()		16777216	167	77216
Lov	1450	MHZ	0	Valid 1 2 3	In Ramp 4 5	5 6	7					Low 1		16777216	857	3157376
СМР	1505	MHz					- •	Ran	np C	ompa	arators	Si	gn	Decimal Value	2's	Complement
СМР	1515	MHz					- /	are	enat	bled		CMP0 0		5033164	503	3164
Ram	ps	Ramp Ena	ble 🔽					Nor	reset	here						
Ramp Number	Actual Start Frequency (MHz)	Desired Er Frequenc (MHz)	nd :y	Duration (us)	Ne Diy Ra	ext imp	Start ramp	next after	RST	FL	Flag	js		Actual End Frequency (MHz)	Length	Increment (dec)
0	1500	1520		25	1	• T(OC Tim	neout 🗖			Disable	d 🔻	15	20.00108361	1250	5369
1	1520.00108361	1500		25		• [OC Tim	neout 🔹			Disable	d 🔻	15	00	1250	-5369
2	-1	10500		100		• T	OC Tim	neout 🗖	1		Disable	d 🔻	-1		5000	10000
3	-1	10500		100		• T(OC Tim	neout 🔹	-		Disable	d 🔻	-1		5000	10000
4	-1	10500		100		• T(OC Tim	neout 🔹			Disable	d 🔻	-1		5000	10000
5	-1	10500		100		• T(OC Tim	neout 🗖	-		Disable	d 🔻	-1		5000	10000
6	-1	10500		100		• T(OC Tim	neout 🗖	•		Disable	d 🔻	-1		5000	10000
7	-1	10500		100	0	• T(OC Tim	neout 🗖	•		Disable	d 🔻	-1		5000	10000
	Ramp Count		D	mn Auto) Pa	mn in Soi	urce (Dama	Transitio			Incre	ment (2s o	complement)
			r.c					mp m oo		Ramp	Transitio	•	0) 5369	4	4 0
	Trigger Source A	Disabled	_			•		FSK Trig	ger (Disabl	ed	•	:	L 10737364	55	5 0
	Trigger Source B	Disabled				•	F	SK Devia	tion	0				2 0	(5 0
	Trigger Source C	Disabled				•	P	hase Mod	l. En [RAN	IP_PM_E	EN	1	3 0		7 0

Limits and Comparators

Figure 24. Continuous Triangular Ramp Configuration

Ramp comparators are enabled so as to output flag signals when the threshold frequencies are hit. MOD pin is assigned for CMP0 while TRIG1 pin is assigned for CMP1. RAMP_CMP0_EN is equal to 3 because ramp segment 0 and 1 are monitored.



Figure 25. Ramp Comparators Configuration





Figure 26. Continuous Triangular Ramp Example



Figure 27. Ramp Comparators Output Flags

8.2.9 Continuous Trapezoid Ramp Example

This is a long-ramp example, the ramp duration is 2 ms. Since $f_{PD} = 50$ MHz, 100000 ramps are required for each ramp segment. However, LMX2491 supports up to a maximum ramp length (RAMPx_LEN) of 65536 only. There are two solutions to resolve this problem:

- 1. Reduce phase detector frequency. For example, reduce f_{PD} to 25 MHz, then the required RAMPx_LEN becomes 50000.
- Enable RAMPx_DLY. When this register bit is set, the ramp generator will ramp every 2 phase detector cycles instead of the normal 1 f_{PD} cycle. In this example, this bit is set and as a result, RAMPx_LEN is 50000.

Four ramp segments are used to construct the ramp pattern. Again there is no need to reset the fractional numerator because the last ramp end frequency is equal to the first ramp start frequency.



Ram	ips	Ramp Enable 🗔	RAN	/Px	DLY							
Ramp Number	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	Duration (us)	Dly	Next Ramp	Start next ramp after	RST	FL	Flags	Actual End Frequency (MHz)	Length	Increment (dec)
0	1500	1500	2000	✓	1 • T	OC Timeout	-		Disabled -	1500	50000	0
1	1500	1520	2000	✓	2 • T(OC Timeout	•		Disabled -	1519.9675559	\$50000	134
2	1519.96755599	1520	2000	✓	3 • T	OC Timeout	•		Disabled -	1519.9675559	\$50000	0
3	1519.96755599	1500	2000	✓	0 • T(OC Timeout	-		Disabled -	1500	50000	-134
4	-1	10500	100		0 • T(OC Timeout	•		Disabled -	-1	5000	10000
5	-1	10500	100		0 • T(OC Timeout	•		Disabled -	-1	5000	10000
6	-1	10500	100		0 • T(OC Timeout	•		Disabled -	-1	5000	10000
7	-1	10500	100		0 • T(OC Timeout	•		Disabled -	-1	5000	10000
	Ramp Count 0	R	amp Auto	RA	MP_AUTO) Ramp In S	Source F	Ramp	Transition •	Incr	ement (2s co 4	omplement) O
	Trigger Source A	Disabled			•	FSK 1	Trigger [Disab	led 🔹	1 134	5	0
	Trigger Source B	Disabled			•	FSK De	viation (D		2 0	6	0
	Trigger Source C	Disabled			•	Phase N	lod. En	RAI	MP_PM_EN	3 10737416	90 7	0

Figure 28. Continuous Trapezoid Ramp Configuration



Figure 29. Continuous Trapezoid Ramp Example

8.2.10 Arbitrary Waveform Ramp Example

An arbitrary ramp waveform can be easily constructed with the 8 ramp segments provided in LMX2491. LMX2491 also provides flag signals output to indicate the start of a ramp. This example used the MOD pin to initiate the ramp and used TRIG1 and TRIG2 as the output flags to indicate the status of the ramp.



Ram	ps	Ramp Enable 🛛 🖌									
Ramp Number	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	Duration (us)	Next Dly Ramp	Start next ramp after	RST	FL	Flags	Actual End Frequency (MHz)	Length	Increment (dec)
0	1500	1500	50	□ 1 ▼	Trigger A	•		Disabled •	1500	2500	0
1	1500	1520	2000	✓ 2 ▼	TOC Timeout	•		Flag0 🔹	1519.9675559	£50000	134
2	1519.96755599	1510	500	3 🔻	TOC Timeout	•		Flag1 🔹	1509.9837779	£25000	-134
3	1509.98377799	1510	500	4 🔻	TOC Timeout	•		Disabled •	1509.9837779	£25000	0
4	1509.98377799	1500	500	5 🔻	TOC Timeout	•		Flag0 & Fla 🔻	1500	25000	-134
5	1500	1500	500	□ 1 ▼	TOC Timeout	•		Disabled •	1500	25000	0
6	-1	10500	100	0 -	TOC Timeout	•		Disabled •	-1	5000	10000
7	-1	10500	100	0 -	TOC Timeout	•		Disabled •	-1	5000	10000
	Ramp Count 0	R	amp Auto	RAMP_A	UTO Ramp In S	ource	Ramp	Transition •	Incr	rement (2s c 4	omplement) 1073741690
	Trigger Source A	MOD Rising Ed	ge	•	FSK T	igger [Disab	led 🔻	1 134	5	5 0
	Trigger Source B	Disabled		•	FSK Dev	iation	0		2 10737416	690 E	5 0
	Trigger Source C	Disabled		•	Phase Mo	od. En	RAI	MP_PM_EN	3 0	7	0

Figure 30. Arbitrary Waveform Ramp Configuration



Figure 31. Arbitrary Waveform Ramp Example





Figure 32. Arbitrary Waveform Ramp Timing

9 Power Supply Recommendations

For power supplies, TI recommends placing 100 nF close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree.

10 Layout

10.1 Layout Guidelines

For layout examples, the EVM instructions are the most comprehensive document. In general, the layout guidelines are similar to most other PLL devices. For the high frequency Fin pin, it is recommended to use 0402 components and match the trace width to these pad sizes. Also the same needs to be done on the Fin* pin. If layout is easier to route the signal to Fin* instead of Fin, then this is acceptable as well.



10.2 Layout Example



Figure 33. Layout Recommendation



11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

德州仪器 (TI) 提供多款开发辅助软件工具,包括 TICS Pro 编程辅助工具、PLLatinum Simulator Tool 回路滤波器 设计辅助工具以及相位噪声/毛刺仿真辅助工具。所有这些工具均可从以下网址获得:www.ti.com。

11.2 文档支持

11.2.1 相关文档

相关文档如下:

- 《AN-1879 分数 N 频率合成》(文献编号: SNAA062)
- 《PLL 性能仿真和设计》

11.3 接收文档更新通知

要接收文档更新通知,请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的通知我进行注册,即可收到任意产品信息更改每周摘要。有关更改的详细信息,请查看任意已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点;请参阅 TI 的 《使用条款》。

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设计支持 **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

E2E is a trademark of Texas Instruments.

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11.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序,可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级,大至整个器件故障。精密的集成电路可能更容易受到损坏,这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据发生变化时, 我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本,请参阅左侧的导航栏。



10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2491RTWR	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	X2491	Samples
LMX2491RTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	X2491	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2491RTWR	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMX2491RTWT	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

9-Mar-2017



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2491RTWR	WQFN	RTW	24	1000	210.0	185.0	35.0
LMX2491RTWT	WQFN	RTW	24	250	210.0	185.0	35.0

RTW0024A



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



RTW0024A

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



RTW0024A

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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Ⅱ 均以"原样"提供技术性及可靠性数据(包括数据表)、设计资源(包括参考设计)、应用或其他设计建议、网络工具、安全信息和其他资源,不保证其中不含任何瑕疵,且不做任何明示或暗示的担保,包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

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