MSP430F47x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low supply-voltage range: 1.8 V to 3.6 V
- Ultra-low power consumption
  - Active mode: 262 µA at 1 MHz, 2.2 V
  - Standby mode: 1.1 µA
  - Off mode (RAM retention): 0.1 µA
- Five power-saving modes
- Wakeup from standby mode in less than 6 µs
- 16-bit RISC architecture, extended memory, 125-ns instruction cycle time
- 16-bit sigma-delta analog-to-digital converter (ADC) with internal reference and five differential analog inputs
- One 12-bit digital-to-analog converter (DAC)
- 16-bit Timer_A with three capture/compare registers
- 16-bit Timer_B with seven capture/compare-with-shadow registers
- Two universal serial communication interfaces (USCIs)
  - USCI_A0
    - Enhanced UART supports automatic baud-rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - USCI_B0
    - I^2C
    - Synchronous SPI
- Integrated LCD driver up to 160 segments with regulated charge pump
- Brownout detector
- Basic timer with real-time clock (RTC) feature
- Supply voltage supervisor and monitor with programmable level detection
- On-Chip Comparator
- Serial onboard programming, programmable code protection by security fuse
- Bootloader
- On chip emulation module
- Device Comparison summarizes the available family members
  - MSP430F477: 32KB + 256 bytes of flash, 2KB of RAM
  - MSP430F478: 48KB + 256 bytes of flash, 2KB of RAM
  - MSP430F479: 60KB + 256 bytes of flash, 2KB of RAM
- Available in 113-ball MicroStar Junior™ BGA (ZQW), 113-ball nFBGA (ZCA), and 80-pin QFP (PN) packages (see Device Comparison)

1.2 Applications

- Analog and digital sensor systems
- Digital motor control
- Remote controls
- Thermostats
- Digital timers
- Hand-held meters

1.3 Description

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 µs.

The MSP430F47x is a microcontroller configuration with two 16-bit timers, a basic timer with a real-time clock, a high-performance 16-bit sigma-delta A/D converter, single 12-bit D/A converter, two universal serial communication interface, 48 I/O pins, and a liquid crystal display driver.

For complete module descriptions, see the *MSP430x4xx Family User's Guide*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430F479IPN	LQFP (80)	12 mm × 12 mm
MSP430F479IZCA	nFBGA (113)	7 mm × 7 mm
MSP430F479IZQW(3)	MicroStar Junior™ BGA (113)	7 mm × 7 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.
(3) All orderable part numbers in the ZQW (MicroStar Junior BGA) package have been changed to a status of Last Time Buy. Visit the Product life cycle page for details on this status.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.

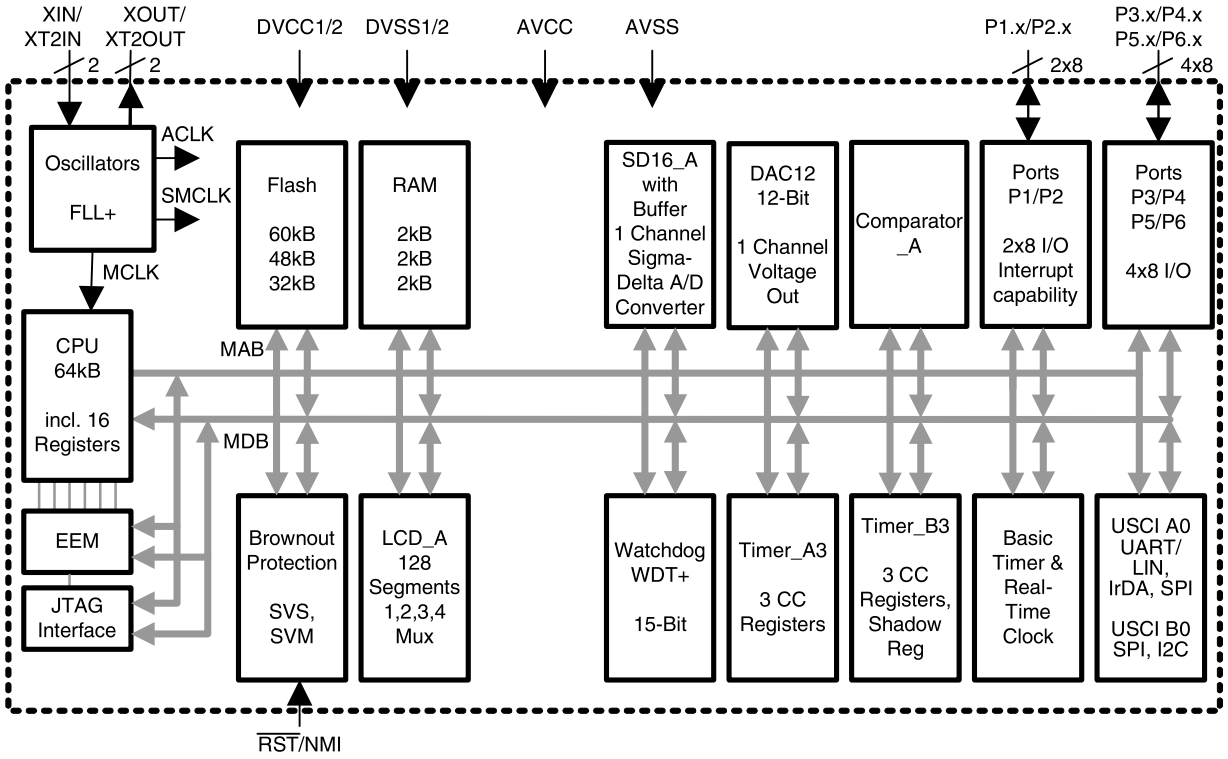

Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 25, 2009 to May 4, 2020	Page

- Changes to document format including section numbering and organization 1
- Throughout the document, added the ZCA package 1
- Added Section 1.2, *Applications* 1
- Added *Device Information* table 2
- Changed the status of all orderable part numbers in the ZQW package 2
- Removed former section *Development Tool Support* 2
- Moved functional block diagram to Section 1.4 2
- Added Section 3, *Device Comparison* 5
- Added Section 5 and moved all electrical specifications to it 12
- Added Section 5.2, *ESD Ratings* 12
- In *Recommended Operating Conditions*, added test conditions for TYP values 13
- Changed all instances of "bootstrap loader" to "bootloader" throughout document 50
- Added Section 7 and moved Trademarks and ESD Caution sections to it 81
- Added Section 8 85

3 Device Comparison

The following table summarizes the available family members.

Table 3-1. Device Comparison(1)(2)

DEVICE	FLASH (KB)	RAM (KB)	Timer_A	Timer_B	SD16_A	DAC12	USCI	I/Os	PACKAGE
MSP430F479	60	2	TA3	TB3	1	1	A0, B0	48	PN 80 ZCA 113 ZQW 113
MSP430F478	48	2	TA3	TB3	1	1	A0, B0	48	PN 80 ZCA 113 ZQW 113
MSP430F477	32	2	TA3	TB3	1	1	A0, B0	48	PN 80 ZCA 113 ZQW 113

(1) For the most current device, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Microcontrollers TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

Companion Products for MSP430F479 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs Find reference designs leveraging the best in TI technology to solve your system-level challenges

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 80-pin PN package.

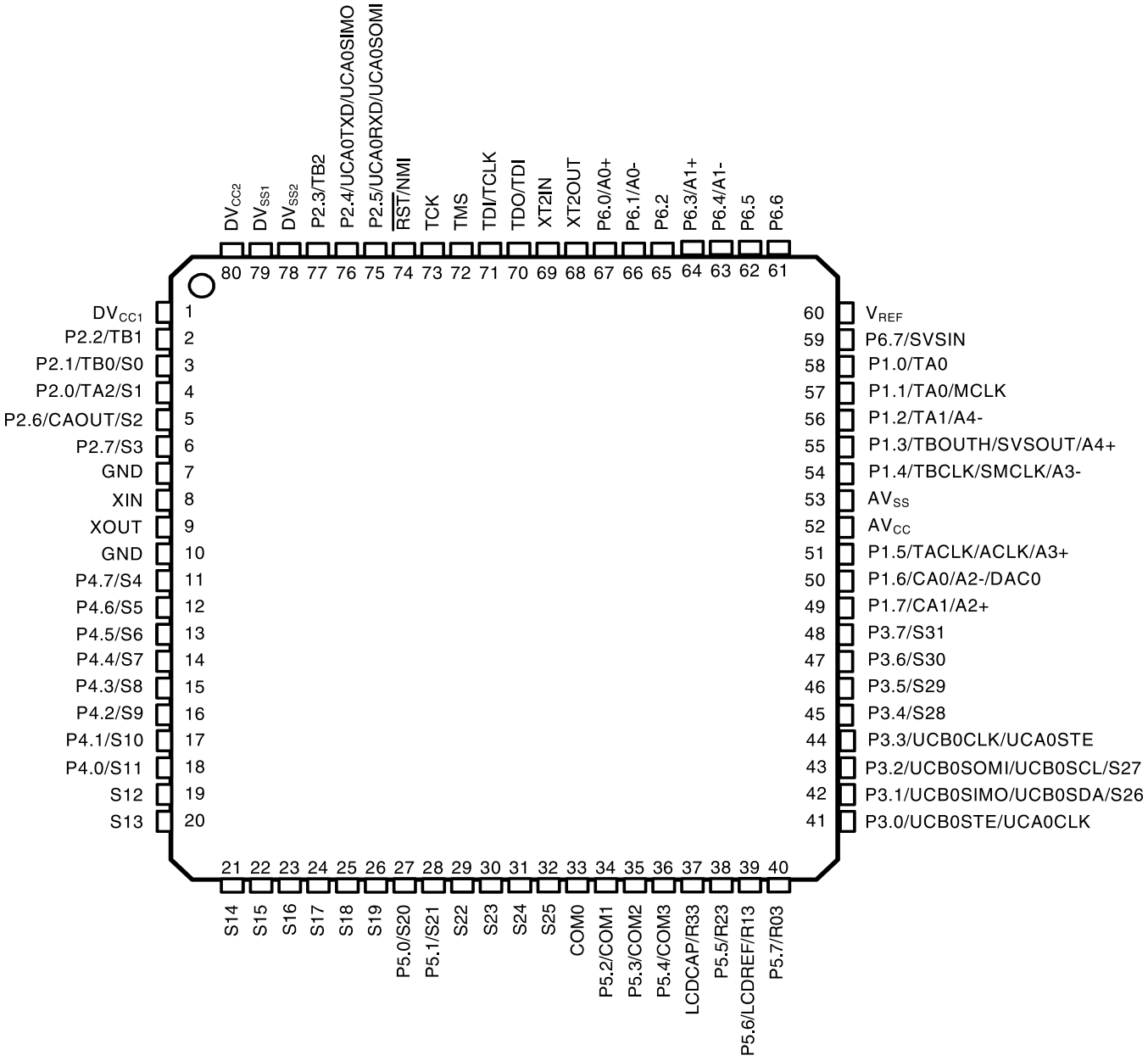
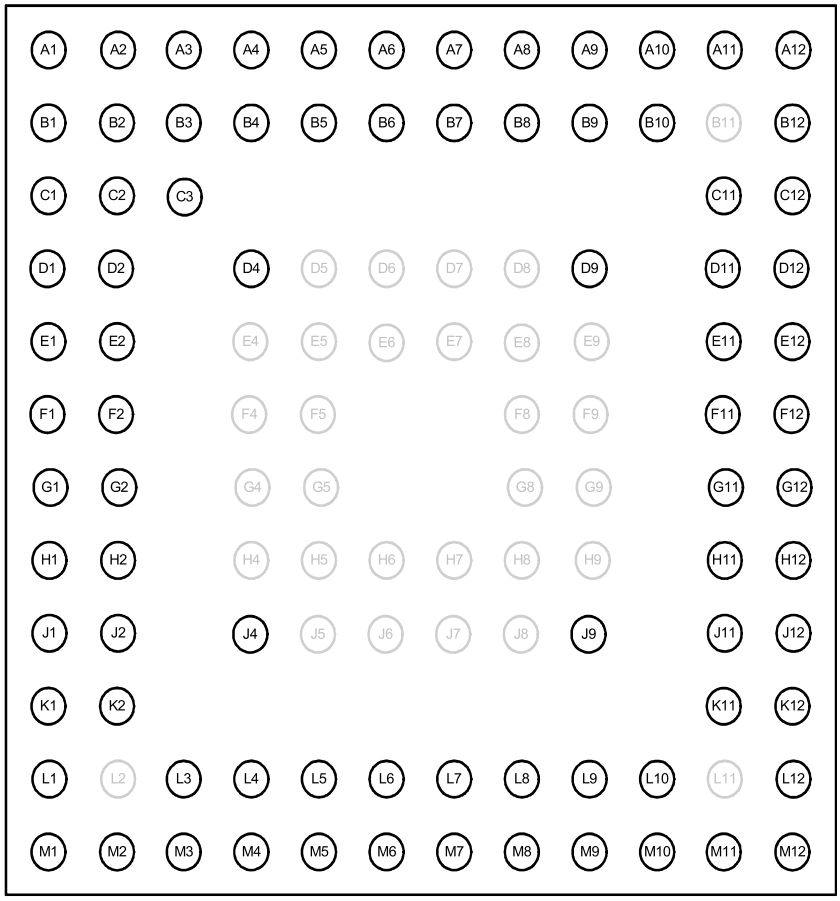


Figure 4-1. 80-Pin PN Package (Top View)

Figure 4-2 shows the pinout for the 113-pin ZCA and ZQW packages. For pin assignments, see Table 4-1.



NOTE: For the terminal assignments, see Section 4.2.

Figure 4-2. 113-Pin ZCA and ZQW Packages (Top View)

4.2 Signal Descriptions

Table 4-1 describes the device signals.

Table 4-1. Signal Descriptions

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PN	ZCA, ZQW		
AVCC	52	F12		Analog supply voltage, positive terminal.
AVSS	53	E12		Analog supply voltage, negative terminal.
DVCC1	1	A1		Digital supply voltage, positive terminal. Supplies all digital parts.
DVSS1	79	A3		Digital supply voltage, negative terminal. Supplies all digital parts.
DVCC2	80	A2		Digital supply voltage, positive terminal. Supplies all digital parts.
DVSS2	78	B2, B3		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TA0	58	C11	I/O	General-purpose digital I/O pin
				Timer_A, capture: CCI0A input, compare: Out0 output
				BSL transmit
P1.1/TA0/MCLK	57	C12	I/O	General-purpose digital I/O pin
				Timer_A, capture: CCI0B input, compare: Out0 output
				MCLK signal output
				BSL receive
P1.2/TA1/A4-	56	D11	I/O	General-purpose digital I/O pin
				Timer_A, capture: CCI1A input, compare: Out1 output
				SD16 negative analog input A4
P1.3/TBOUTH/SVSOUT/A4+	55	D12	I/O	General-purpose digital I/O pin
				Timer_A, capture: CCI2A input, compare: Out2 output
				Set all PWM digital output ports to high impedance - Timer_B TB0 to TB2
				SVS comparator output
				SD16 positive analog input A4
P1.4/TBCLK/SMCLK/A3-	54	E11	I/O	General-purpose digital I/O pin
				Timer_B, clock signal TBCLK input
				SMCLK signal output
				SD16 negative analog input A3
P1.5/TACLK/ACLK/A3+	51	F11	I/O	General-purpose digital I/O pin
				Timer_A, clock signal TACLK input
				ACLK signal output
				SD16 positive analog input A3
P1.6/CA0/A2-/DAC0	50	G12	I/O	General-purpose digital I/O pin
				Comparator_A input 0
				SD16 negative analog input A2
				DAC12.0 output
P1.7/CA1/A2+	49	G11	I/O	General-purpose digital I/O pin
				Comparator_A input 1
				SD16 positive analog input A2
P2.0/TA2/S1	4	C2, C3	I/O	General-purpose digital I/O pin
				Timer_A, capture: CCI2A/B input, compare: Out2 output
				LCD segment output 1
P2.1/TB0/S0	3	C1	I/O	General-purpose digital I/O pin
				Timer_B, capture: CCI0A/B input, compare: Out0 output
				LCD segment output 0

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PN	ZCA, ZQW		
P2.2/TB1	2	B1	I/O	General-purpose digital I/O pin
				Timer_B, capture: CCI1A/B input, compare: Out1 output
P2.3/TB2	77	B4	I/O	General-purpose digital I/O pin
				Timer_B, capture: CCI2A/B input, compare: Out2 output
P2.4/UCA0TXD/ UCA0SIMO	76	A4	I/O	General-purpose digital I/O pin
				USCIA transmit data output in UART mode, slave data in/master out in SPI mode
P2.5/UCA0RXD/ UCA0SOMI	75	D4	I/O	General-purpose digital I/O pin
				USCI A0 receive data input in UART mode, slave data out/master in in SPI mode
P2.6/CAOUT/S2	5	D1	I/O	General-purpose digital I/O pin
				Comparator_A output
				LCD segment output 2
P2.7/S3	6	D2	I/O	General-purpose digital I/O pin
				LCD segment output 3
P3.0/UCB0STE/UCA0CLK	41	M12	I/O	General-purpose digital I/O pin
				USCI B0 slave transmit enable
				USCI A0 clock input/output
P3.1/UCB0SIMO/ UCB0SDA/S26	42	L12	I/O	General-purpose digital I/O pin
				USCI B0 slave in/master out in SPI mode, SDA I2C data in I2C mode
				LCD segment output 26
P3.2/UCB0SOMI/ UCB0SCL/S27	43	K11	I/O	General-purpose digital I/O pin
				USCI B0 slave out/master in in SPI mode, SCL I2C clock in I2C mode
				LCD segment output 27
P3.3/UCB0CLK/UCA0STE	44	K12	I/O	General-purpose digital I/O
				USCI B0 clock input/output, USCI A0 slave transmit enable
P3.4/S28	45	J11	I/O	General-purpose digital I/O pin
				LCD segment output 28
P3.5/S29	46	J12	I/O	General-purpose digital I/O pin
				LCD segment output 29
P3.6/S30	47	H11	I/O	General-purpose digital I/O pin
				LCD segment output 30
P3.7/S31	48	H12	I/O	General-purpose digital I/O pin
				LCD segment output 31
P4.0/S11	18	K2	I/O	General-purpose digital I/O pin
				LCD segment output 11
P4.1/S10	17	K1	I/O	General-purpose digital I/O pin
				LCD segment output 10
P4.2/S9	16	J2	I/O	General-purpose digital I/O pin
				LCD segment output 9
P4.3/S8	15	J1	I/O	General-purpose digital I/O pin
				LCD segment output 8
P4.4/S7	14	H2	I/O	General-purpose digital I/O pin
				LCD segment output 7
P4.5/S6	13	H1	I/O	General-purpose digital I/O pin
				LCD segment output 6

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PN	ZCA, ZQW		
P4.6/S5	12	G2	I/O	General-purpose digital I/O pin
				LCD segment output 5
P4.7/S4	11	G1	I/O	General-purpose digital I/O pin
				LCD segment output 4
COM0	33	L8	O	Common output, COM0- 3 are used for LCD backplanes
P5.0/S20	27	L5	I/O	General-purpose digital I/O pin
				LCD segment output 20
P5.1/S21	28	M5	I/O	General-purpose digital I/O pin
				LCD segment output 21
P5.2/COM1	34	M8	I/O	General-purpose digital I/O pin
				common output, COM0- 3 are used for LCD backplanes
P5.3/COM2	35	L9	I/O	General-purpose digital I/O pin
				common output, COM0- 3 are used for LCD backplanes
P5.4/COM3	36	M9	I/O	General-purpose digital I/O pin
				common output, COM0- 3 are used for LCD backplanes
LCDCAP/R33	37	J9	I/O	Capacitor connection for LCD charge pump
				input port of most positive analog LCD level (V4)
P5.5/R23	38	M10	I/O	General-purpose digital I/O pin
				input port of the second most positive analog LCD level (V3)
P5.6/LCDREF/R13	39	L10	I/O	General-purpose digital I/O pin
				External LCD reference voltage input
				input port of the third most positive analog LCD level (V3 or V2)
P5.7/R03	40	M11	I/O	General-purpose digital I/O pin
				input port of the fourth most positive analog LCD level (V1)
P6.0/A0+	67	B8	I/O	General-purpose digital I/O pin
				SD16 positive analog input A0
P6.1/A0-	66	B9	I/O	General-purpose digital I/O pin
				SD16 positive negative input A0
P6.2	65	A9	I/O	General-purpose digital I/O pin
P6.3/A1+	64	D9	I/O	General-purpose digital I/O pin
				SD16 positive analog input A1
P6.4/A1-	63	A10	I/O	General-purpose digital I/O pin
				SD16 positive negative input A1
P6.5	62	B10	I/O	General-purpose digital I/O pin
P6.6	61	A11	I/O	General-purpose digital I/O pin
P6.7/SVSIN	59	B12	I/O	General-purpose digital I/O pin
				SVS input
S12	19	L1	O	LCD segment output 12
S13	20	M1	O	LCD segment output 13
S14	21	M2	O	LCD segment output 14
S15	22	M3	O	LCD segment output 15
S16	23	L3	O	LCD segment output 16
S17	24	L4	O	LCD segment output 17
S18	25	M4	O	LCD segment output 18
S19	26	J4	O	LCD segment output 19
S22	29	L6	O	LCD segment output 22

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PN	ZCA, ZQW		
S23	30	M6	O	LCD segment output 23
S24	31	L7	O	LCD segment output 24
S25	32	M7	O	LCD segment output 25
GND	7	E2		Ground. It is used to shield the oscillator. See Note 1.
XIN	8	E1	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	F1	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.
GND	10	F2		Ground. It is used to shield the oscillator.(1)
V_{REF}	60	A12	O	Input for an external reference voltage/internal reference voltage output
$\overline{RST}$/NMI	74	B5	I	Reset input, nonmaskable interrupt input port, or bootloader start (in flash devices).
TCK	73	A5	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootloader start.
TDI/TCLK	71	A6	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	70	B7	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	72	B6	I	Test mode select. TMS is used as an input port for device programming and test.
XT2OUT	68	A8	O	Output terminal of crystal oscillator XT2
XT2IN	69	A7	I	Input port for crystal oscillator XT2
Reserved	NA	B11, D6, D7, D8, E4, E5, E6, E7, E8, E9, F4, F5, F8, F9, G4, G5,G8, G9, H4, H5, H6, H7, H8, H9, J5, J6, J7, J8, L2, L11		Unused BGA balls. Connection to DVSS/AVSS recommended.

(1) It is recommended to connect GND externally to DV_{SS}.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}		–0.3	4.1	V
Voltage applied to any pin(2)		–0.3	V_{CC} + 0.3	V
Diode current at any device terminal			±2	mA
Storage temperature, T_{stg}(3)	Unprogrammed device	–55	150	°C
	Programmed device	–40	85	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to V_{SS}.The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution (AV_{CC} = DV_{CC1} = DV_{CC2} = V_{CC})		1.8		3.6	V
		During flash memory programming (AV_{CC} = DV_{CC1} = DV_{CC2} = V_{CC})		2.7		3.6	
V_{SS}	Supply ground (AV_{SS} = DV_{SS1} = DV_{SS2} = V_{SS})			0		0	V
T_A	Operating free-air temperature range			–40		85	°C
$f_{(LFXT1)}$	LFXT1 crystal frequency(1)	LF selected, XTS_FLL = 0	Watch crystal		32.768		kHz
		XT1 selected, XTS_FLL = 1	Ceramic resonator	0.45		6	MHz
		XT1 selected, XTS_FLL = 1	Crystal	1		6	
$f_{(XT2)}$	XT2 crystal frequency		Ceramic resonator	0.45		8	MHz
			Crystal	1		8	
$f_{(System)}$	Processor frequency (MCLK, SMCLK, ACLK)		V_{CC} = 1.8 V	DC		4.15	MHz
			V_{CC} = 2.5 V	DC		8	

(1) In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

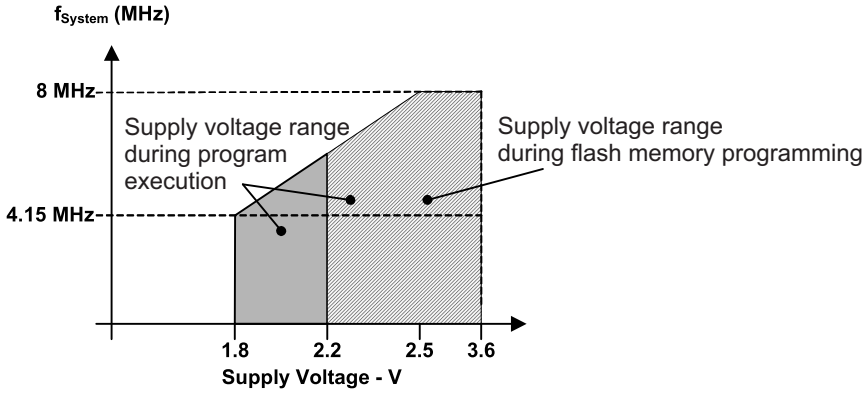


Figure 5-1. Frequency vs Supply Voltage

5.4 Supply Current Into AV_{CC} and DV_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode(1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32768 Hz, XTS = 0, SELM = 0 or 1	T_A = –40°C to 85°C	V_{CC} = 2.2 V		262	295	µA
			V_{CC} = 3 V		420	460	
$I_{(LPM0)}$	Low power mode (LPM0)(1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	62	µA
			V_{CC} = 3 V		51	77	
$I_{(LPM2)}$	Low-power mode (LPM2), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 0(2)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		5	9	µA
			V_{CC} = 3 V		7	13	
$I_{(LPM3)}$	Low-power mode (LPM3), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 1, Basic Timer1 enabled, ACLK selected, LCD_A enabled, LCDCPEN = 0, (static mode, $f_{LCD} = f_{(ACLK)}/32$)(2) (3)	T_A = –40°C	V_{CC} = 2.2 V		1.0	1.8	µA
		T_A = 25°C			1.0	1.8	
		T_A = 60°C			1.1	2.0	
		T_A = 85°C			2.3	4.0	
		T_A = –40°C	V_{CC} = 3 V		1.2	2.0	
		T_A = 25°C			1.2	2.0	
		T_A = 60°C			1.4	2.2	
		T_A = 85°C			2.7	4.5	
$I_{(LPM3)}$	Low-power mode (LPM3), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 1, Basic Timer1 enabled, ACLK selected, LCD_A enabled, LCDCPEN = 0, (4-mux mode; $f_{LCD} = f_{(ACLK)}/32$)(2) (3)	T_A = –40°C	V_{CC} = 2.2 V		1.0	3.0	µA
		T_A = 25°C			1.1	3.2	
		T_A = 85°C			3.5	6.0	
		T_A = –40°C	V_{CC} = 3 V		1.8	3.3	
		T_A = 25°C			2.0	4.0	
		T_A = 85°C			4.2	7.5	
$I_{(LPM4)}$	Low-power mode (LPM4), $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1(2)	T_A = –40°C	V_{CC} = 2.2 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 60°C			0.7	1.1	
		T_A = 85°C			1.7	3.0	
		T_A = –40°C	V_{CC} = 3 V		0.1	0.8	
		T_A = 25°C			0.1	0.8	
		T_A = 60°C			0.8	1.2	
		T_A = 85°C			1.5	3.5	

(1) Timer_A is clocked by $f_{(DCOCLK)}$= 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(3) The LPM3 currents are characterized with a Micro Crystal CC4V-T1A (9 pF) crystal and OSCCAPx = 1h.

Current consumption of active mode versus system frequency:

$I_{(AM)} = I_{(AM)\ [1\ MHz]} \times f_{(System)}$ [MHz]

Current consumption of active mode versus supply voltage:

$I_{(AM)} = I_{(AM)\ [3\ V]} + 200\ \mu A/V \times (V_{CC} - 2.2\ V)$

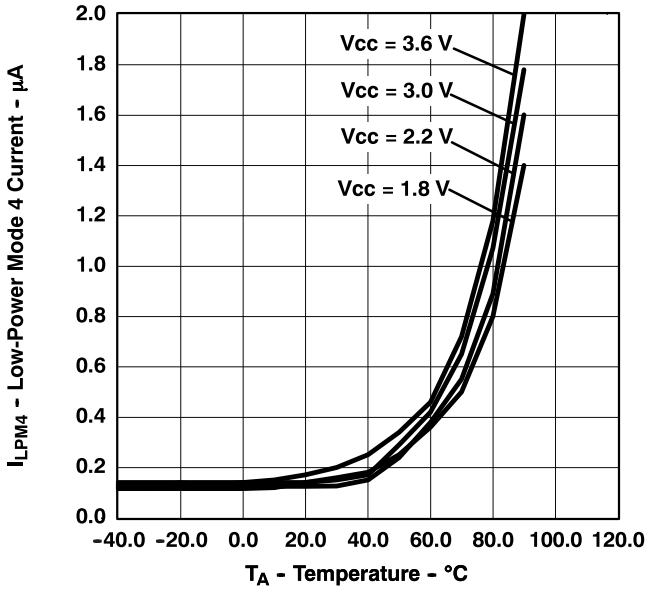


Figure 5-2. I_{LPM4} -- LPM4 Current vs Temperature

5.5 Schmitt-Trigger Inputs – Ports P1 to P6, $\overline{RST}$/NMI, JTAG (TCK, TMS, TDI/TCLK,TDO/TDI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1	1.55	V
		V_{CC} = 3 V	1.5	1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4	0.9	V
		V_{CC} = 3 V	0.9	1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3	1.1	V
		V_{CC} = 3 V	0.5	1	

5.6 Inputs Px.y, TAx

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag[1]	2.2 V	62		ns
			3 V	50		
$t_{(cap)}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V	62		ns
			3 V	50		
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
$f_{(TBext)}$			3 V		10	
$f_{(TAint)}$	Timer A clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
$f_{(TBint)}$			3 V		10	

(1) The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

5.7 Leakage Current – Ports P1 to P6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current, Port Px	$V_{(Px.y)}$[2]	V_{CC} = 2.2 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The port pin must be selected as input.

5.8 Outputs – Ports P1 to P6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA, V_{CC} = 2.2 V(1)	V_{CC} – 0.25	V_{CC}	V
		$I_{OH(max)}$ = –6 mA, V_{CC} = 2.2 V(2)	V_{CC} – 0.6	V_{CC}	
		$I_{OH(max)}$ = –1.5 mA, V_{CC} = 3 V(1)	V_{CC} – 0.25	V_{CC}	
		$I_{OH(max)}$ = –6 mA, V_{CC} = 3 V(2)	V_{CC} – 0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA, V_{CC} = 2.2 V(1)	V_{SS}	V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA, V_{CC} = 2.2 V(2)	V_{SS}	V_{SS} + 0.6	
		$I_{OL(max)}$ = 1.5 mA, V_{CC} = 3 V(1)	V_{SS}	V_{SS} + 0.25	
		$I_{OL(max)}$ = 6 mA, V_{CC} = 3 V(2)	V_{SS}	V_{SS} + 0.6	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

5.9 Output Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	1 ≤ × ≤ 6, 0 ≤ y ≤ 7	C_L = 20 F, I_L = ±1.5 mA	V_{CC} = 2.2 V, 3 V	DC		f_{System}	MHz
$f_{(MCLK)}$	P1.1/TA0/MCLK	C_L = 20 pF				f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V, 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50% – 15 ns	50%	50%+ 15 ns	

5.10 Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

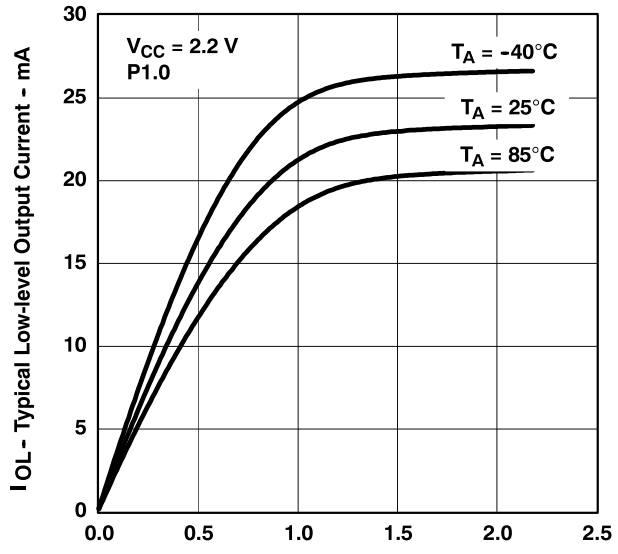


Figure 5-3. Typical Low-Level Output Current vs Typical Low-Level Output Current

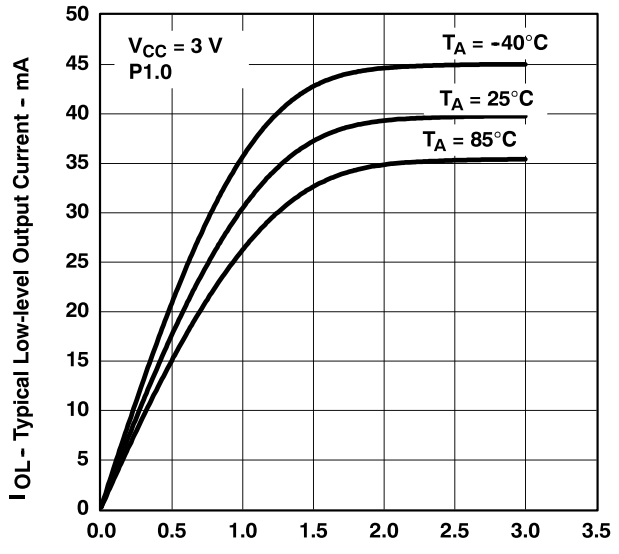


Figure 5-4. Typical Low-Level Output Current vs Typical Low-Level Output Current

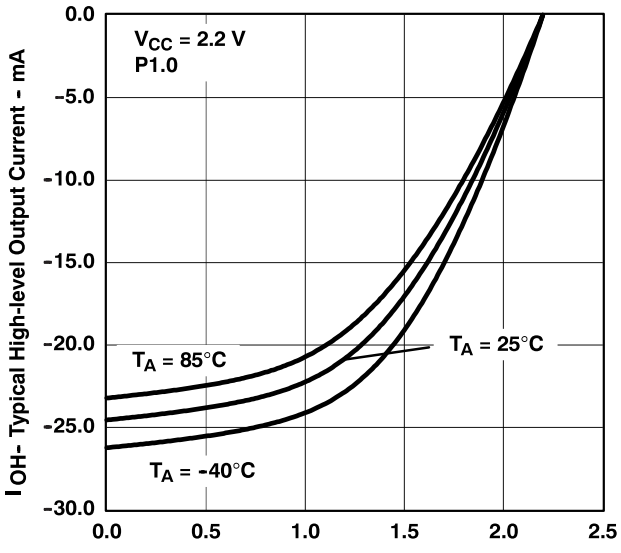


Figure 5-5. Typical High-Level Output Current vs Typical High-Level Output Current

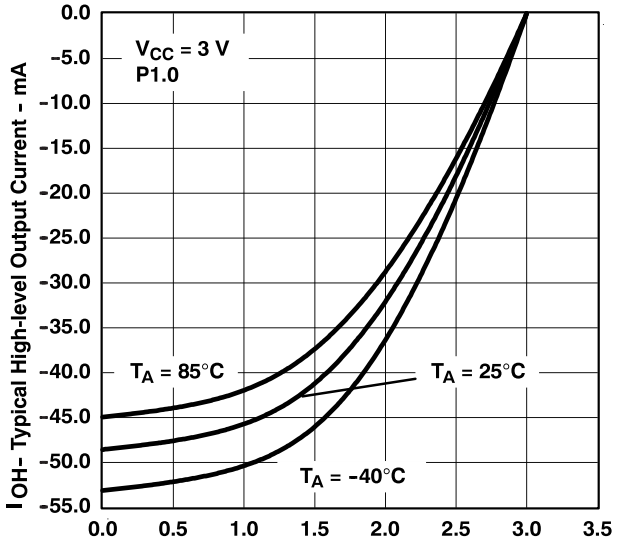


Figure 5-6. Typical High-Level Output Current vs Typical High-Level Output Current

5.11 Wake-up Timing From LPM3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V, 3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

5.12 POR – Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout(2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-7)		0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-7 through Figure 5-9)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-7)				mV
$t_{(reset)}$		Pulse duration needed at RST/NMI pin to accepted reset internally, V_{CC} = 2.2 V, 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)} \le 1.89$ V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout and SVS circuit.

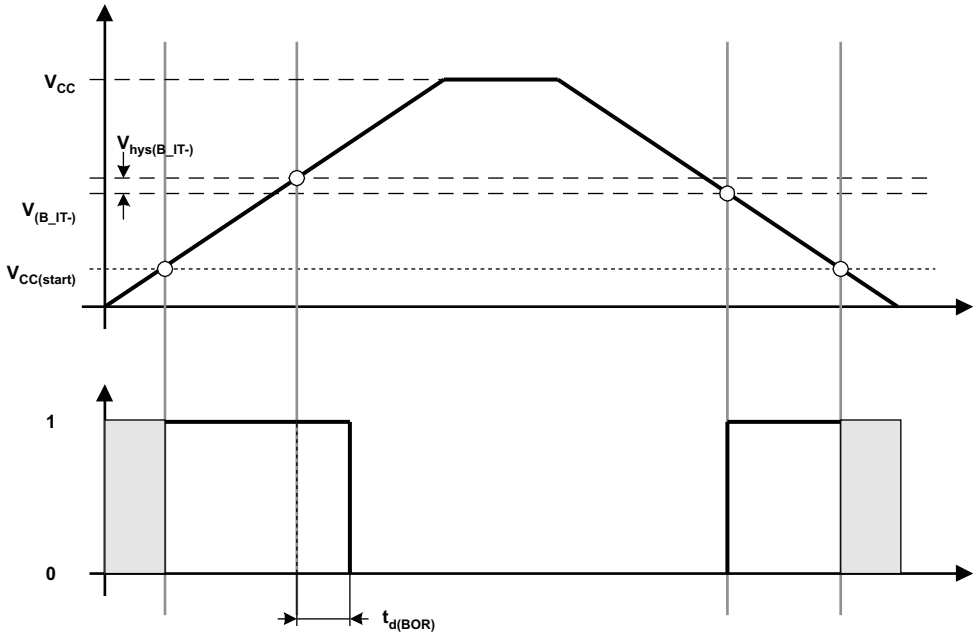


Figure 5-7. POR, BOR vs Supply Voltage

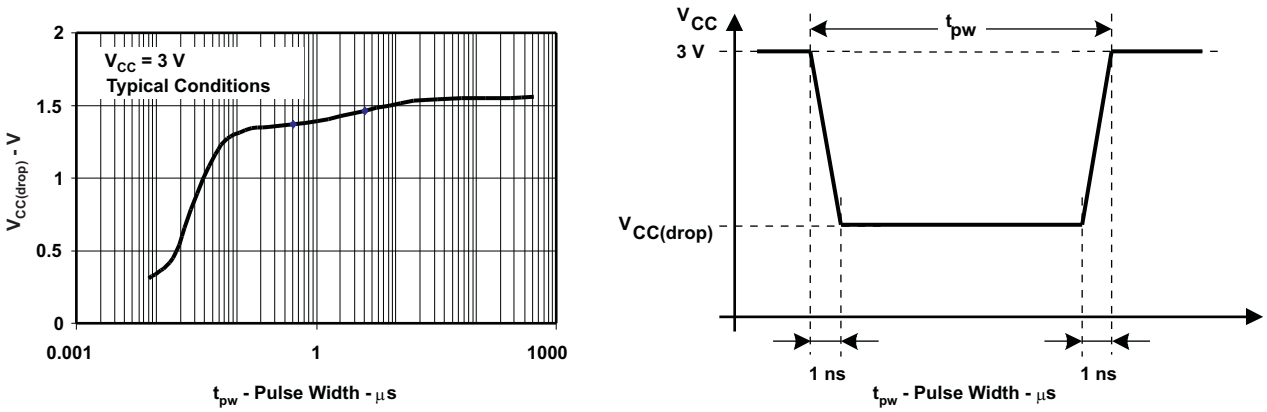


Figure 5-8. $V_{CC(drop)}$ Level with a Square Voltage Drop to Generate a POR or BOR Signal

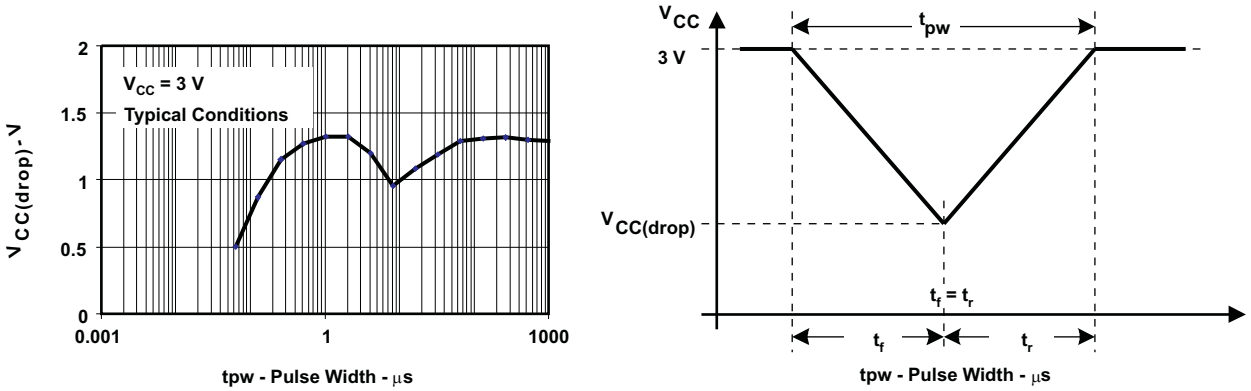


Figure 5-9. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

5.13 SVS (Supply Voltage Supervisor and Monitor)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 5-10)		5		150	µs
	dV_{CC}/dt ≤ 30 V/ms				2000	
$t_{d(SVSon)}$	SVS on, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0 (1)				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, V_{CC}/dt ≤ 3 V/s (see Figure 5-10)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 5-10)	VLD = 1	70	120	210	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)}$ × 0.001		$V_{(SVS\_IT-)}$ × 0.016	
	V_{CC}/dt ≤ 3 V/s (see Figure 5-10), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 5-10)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.23	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61 (2)	
		VLD = 13	3.24	3.5	3.76 (2)	
		VLD = 14	3.43	3.7 (2)	3.99 (2)	
	V_{CC}/dt ≤ 3 V/s (see Figure 5-10), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (3)	VLD ≠ 0, V_{CC} = 2.2 V, 3 V			10	15	µA

(1) t_{settle} is the settling time that the comparator output needs to have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value from 2 to 15. The overdrive is assumed to be > 50 mV.
(2) The recommended operating voltage range is limited to 3.6 V.
(3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

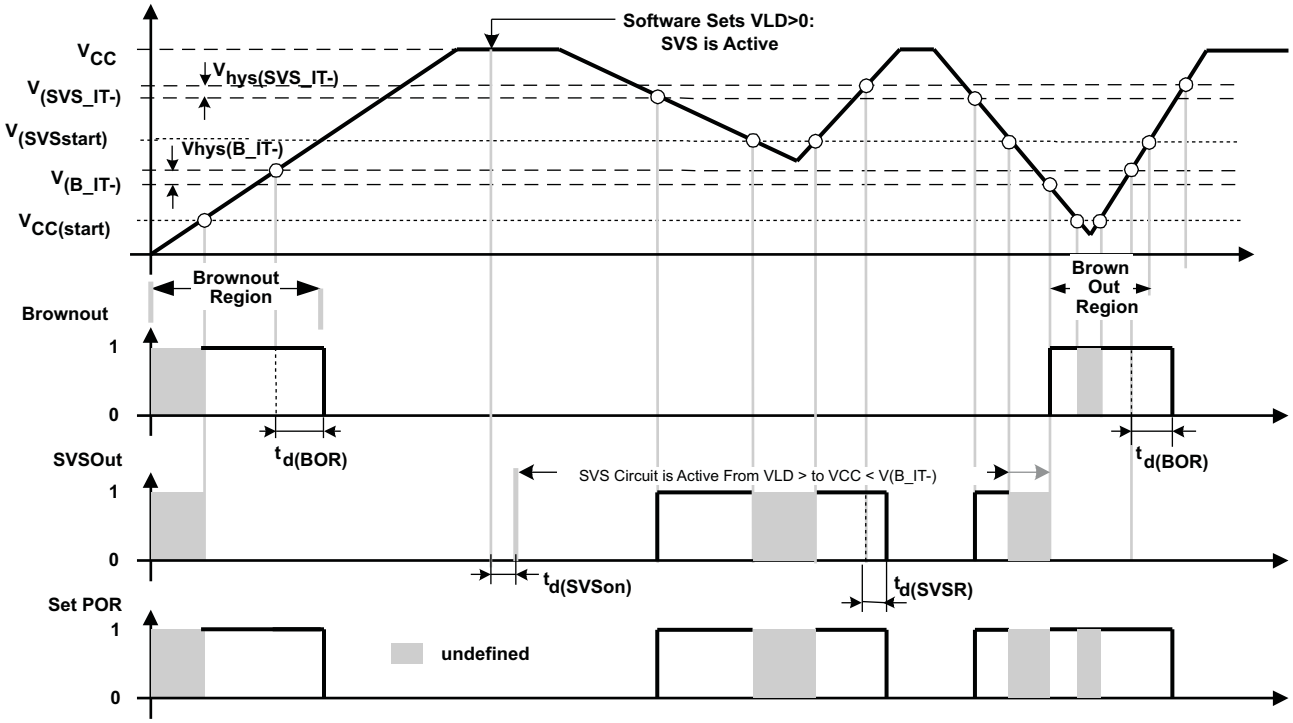


Figure 5-10. SVS Reset (SVSR) vs Supply Voltage

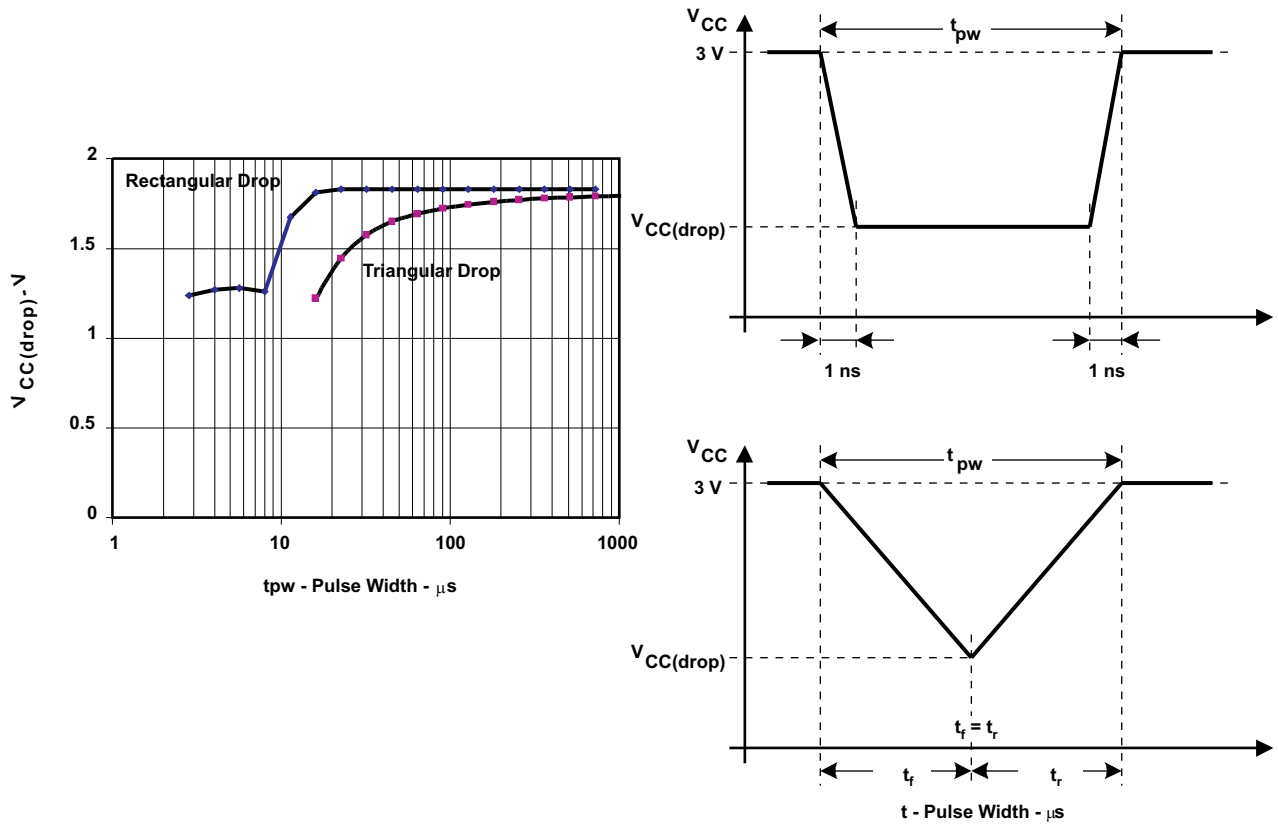


Figure 5-11. $V_{CC(drop)}$ with a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

5.14 DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V, 3 V		1		MHz
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1 (1)	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1 (1)	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO = 2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO = 27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1 (1)	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO = 2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO = 27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1 (1)	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO = 2)}$	FN_8 = 1, FN_4 = 1 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO = 27)}$	FN_8 = 1, FN_4 = 1 = FN_3 = FN_2 = x, DCOPLUS = 1 (1)	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 5-13 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0 (2)	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0 (2)		0	5	15	%/V

(1) Do not exceed the maximum system frequency.
(2) This parameter is not production tested.

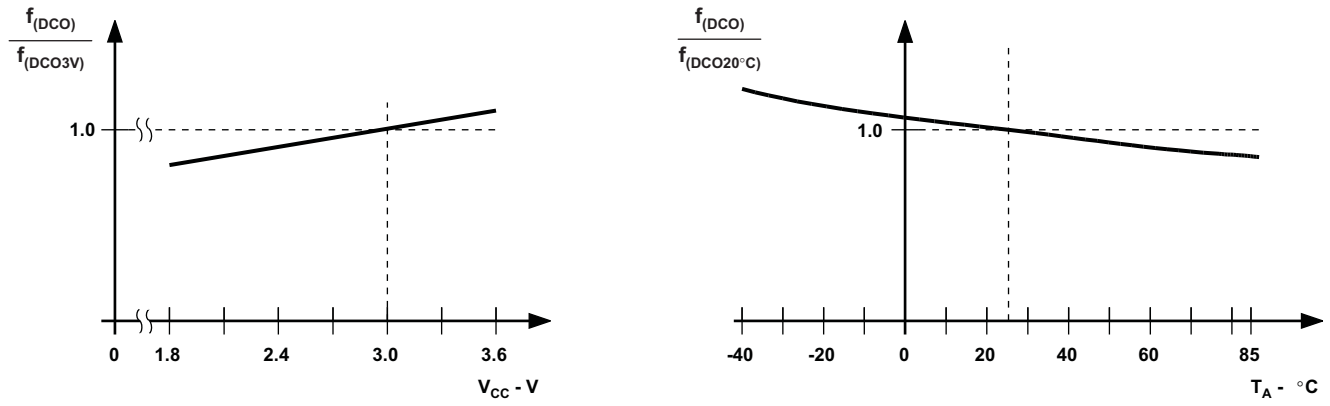


Figure 5-12. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

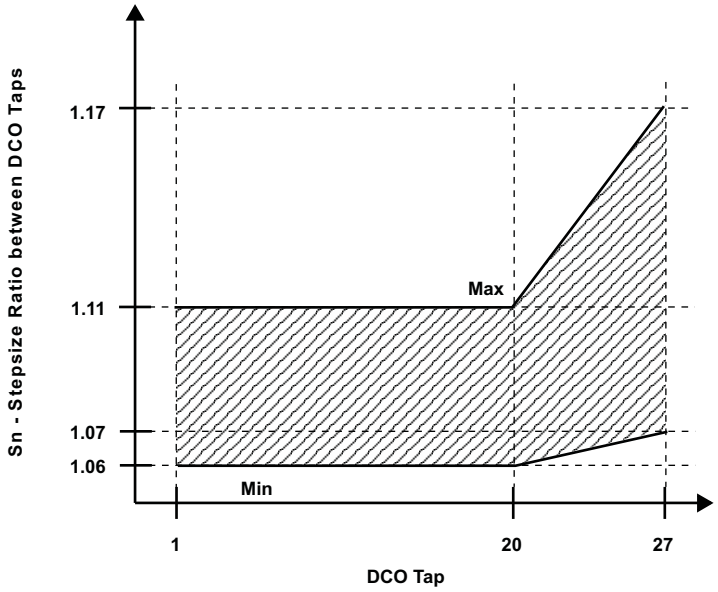


Figure 5-13. DCO Tap Step Size

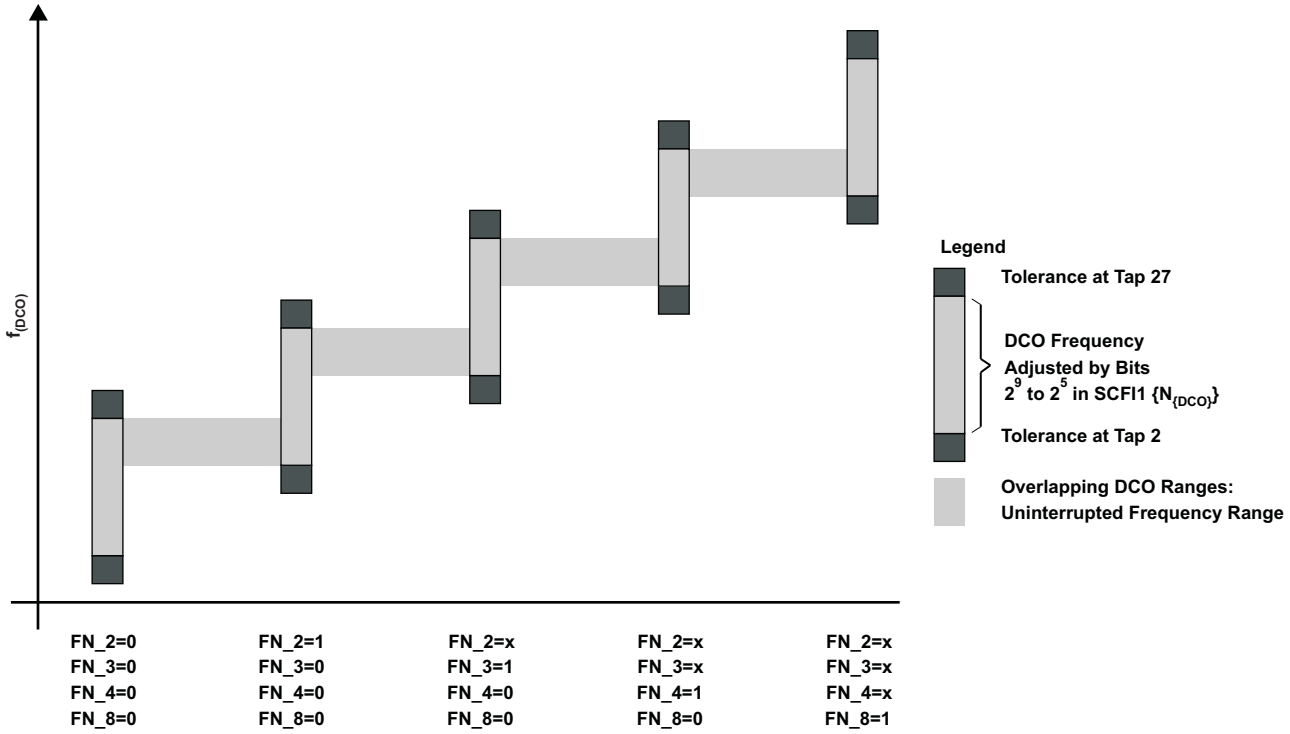


Figure 5-14. Five Overlapping DCO Ranges Controlled by FN_x Bits

5.15 Crystal Oscillator, LFXT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 kHz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode (2)	XTS = 0, XCAPx = 0			1		
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		pF
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P1.5/ACLK, $f_{LFXT1,LF}$ = 32768Hz	2.2 V, 3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (3)	XTS = 0, XCAPx = 0, LFXT1Sx = 3 (4)					
			2.2 V, 3 V	10		10000	Hz

(1) To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
- Keep the trace between the MCU and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.

(3) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(4) Measured with logic level input frequency but also applies to operation with crystals.

5.16 Crystal Oscillator, LFXT1, High-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{LFXT1}	LFXT1 oscillator crystal frequency	Ceramic resonator	1.8 V to 3.6 V	0.45		8	MHz
		Crystal resonator	1.8 V to 3.6 V	1		8	
$C_{L,eff}$	Integrated effective load capacitance, HF mode(1)(2)				1		pF
	Duty cycle	Measured at P1.5/ACLK	2.2 V, 3 V	40	50	60	%

(1) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
(2) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

5.17 Crystal Oscillator, XT2 Oscillator, High-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{XT2}	XT2 oscillator crystal frequency	Ceramic resonator	1.8 V to 3.6 V	0.45		8	MHz
		Crystal resonator	1.8 V to 3.6 V	1		8	
$C_{L,eff}$	Integrated effective load capacitance, HF mode(1)(2)				1		pF
	Duty cycle	Measured at P1.4/SMCLK	2.2 V, 3 V	40	50	60	%

(1) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
(2) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

5.18 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VRAMh	CPU halted(1)	1.6		V

(1) This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

5.19 LCD_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply voltage	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		2.2		3.6	V
C_{LCD}	Capacitor on LCDCAP(1)	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		4.7			µF
$I_{CC(LCD)}$	Average supply current(2)	$V_{LCD(typ)}$ = 3 V, LCDCPEN = 1, VLCDx= 1000, all segments on, $f_{LCD} = f_{ACLK}/32$, no LCD connected(3), T_A = 25°C	2.2 V		3.8		µA
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage	VLCDx = 0000			V_{CC}		V
		VLCDx = 0001			2.60		
		VLCDx = 0010			2.66		
		VLCDx = 0011			2.72		
		VLCDx = 0100			2.78		
		VLCDx = 0101			2.84		
		VLCDx = 0110			2.90		
		VLCDx = 0111			2.96		
		VLCDx = 1000			3.02		
		VLCDx = 1001			3.08		
		VLCDx = 1010			3.14		
		VLCDx = 1011			3.20		
		VLCDx = 1100			3.26		
		VLCDx = 1101			3.32		
		VLCDx = 1110			3.38		
		VLCDx = 1111			3.44	3.60	
R_{LCD}	LCD driver output impedance	V_{LCD}= 3 V, CPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 µA	2.2 V			10	kΩ

(1) Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
(2) Refer to the supply current specifications $I_{(LPM3)}$ for additional current specifications with the LCD_A module active.
(3) Connecting an actual display increases the current consumption depending on the size of the LCD.

5.20 Comparator_A[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = (1, 2, 3), No load at P1.6/CA0 and P1.7/CA1	2.2 V		30	50	µA
			3 V		45	80	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{cc} \text{ node}}{V_{cc}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	2.2 V, 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{cc} \text{ node}}{V_{cc}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	2.2 V, 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 5-15 and Figure 5-16	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V, 3 V	0		V_{CC} – 1	V
$V_p - V_S$	Offset voltage		2.2 V, 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$ $t_{(response\ HL)}$	See [2]	T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	80	165	3..	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 1	2.2 V	1.4	1.9	2.8	µs
			3 V	0.9	1.5	2.2	

(1) The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
(2) The response time is measured at P1.6/CA0 with an input voltage step and the Comparator_A already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

5.21 Typical Characteristics – Comparator_A

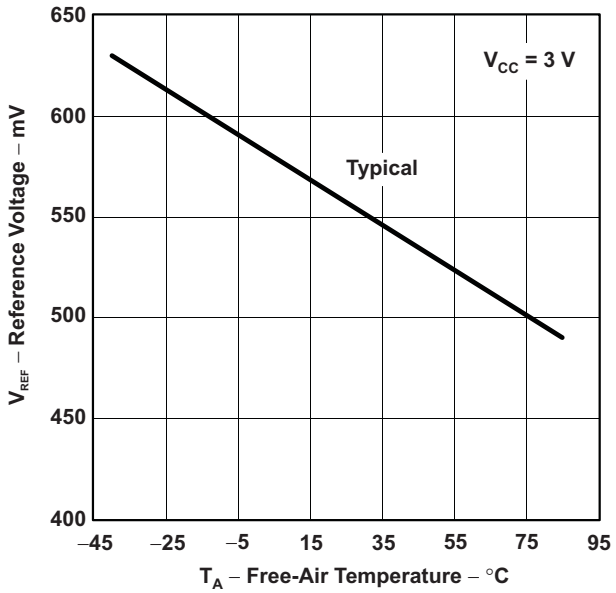


Figure 5-15. Reference Voltage vs Free-Air Temperature

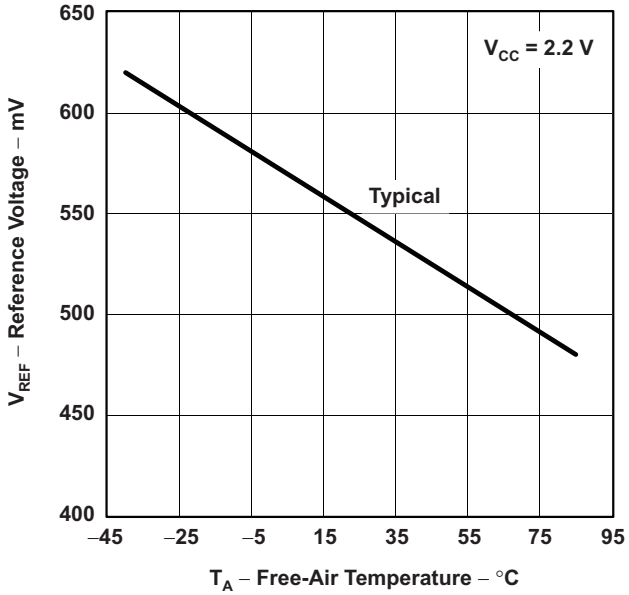


Figure 5-16. Reference Voltage vs Free-Air Temperature

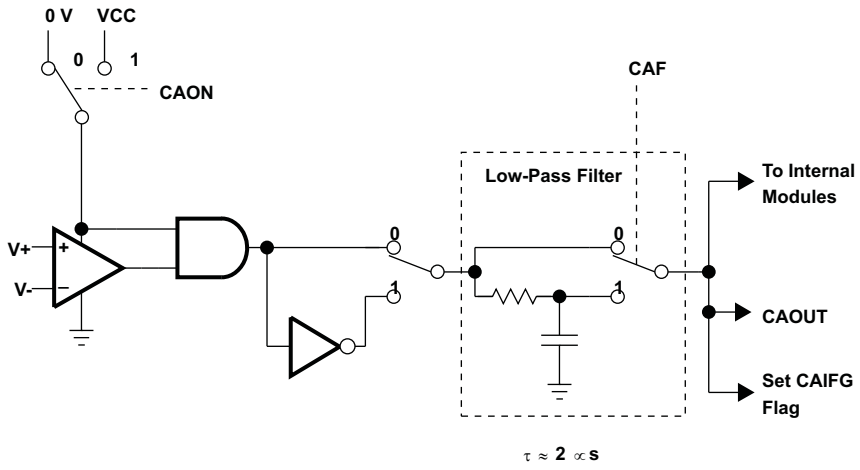


Figure 5-17. Block Diagram of Comparator_A Module

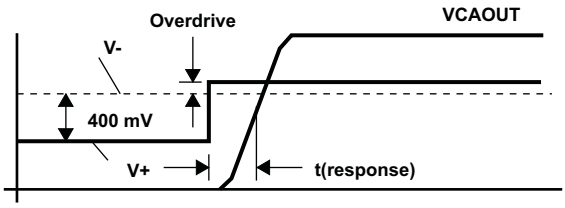


Figure 5-18. Overdrive Definition

5.22 SD16_A, Power Supply and Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage range	$AV_{CC} = DV_{CC} = V_{CC}$, $AV_{SS} = DV_{SS} = V_{SS} = 0$ V			2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1, 2	3 V		750	1050	µA
			SD16BUFx = 00, GAIN: 4, 8, 16			830	1150	
			SD16BUFx = 00, GAIN: 32			1150	1700	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1			730	1030	
			SD16BUFx = 00, GAIN: 32			830	1150	
		SD16LP = 0, SD16OSR = 256	SD16BUFx = 01, GAIN: 1			850		
			SD16BUFx = 10, GAIN: 1			1000		
			SD16BUFx = 11, GAIN: 1			1130		
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)			0.03	0.5		

5.23 SD16_A, Input Range

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_I	Absolute input voltage range	SD16BUFx = 00			AV_{SS} – 0.1		AV_{CC}	V
		SD16BUFx > 00			AV_{SS} + 0.2		AV_{CC} – 1.2 V	
V_{IC}	Common-mode input voltage range	SD16BUFx = 00			AV_{SS} – 0.1		AV_{CC}	V
		SD16BUFx > 00			AV_{SS} + 0.2		AV_{CC} – 1.2 V	
$V_{ID,FSR}$	Differential full scale input voltage range(1)	Bipolar mode, SD16UNI = 0			$-V_{REF}$/2GAIN		$+V_{REF}$/2GAIN	mV
		Unipolar mode, SD16UNI = 1			0		$+V_{REF}$/2GAIN	
V_{ID}	Differential input voltage range for specified performance(1)	SD16REFON = 1	SD16GAINx = 1			±500		mV
			SD16GAINx = 2			±250		
			SD16GAINx = 4			±125		
			SD16GAINx = 8			±62		
			SD16GAINx = 16			±31		
			SD16GAINx = 32			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1 MHz, SD16BUFx = 00	SD16GAINx = 1	3 V		200		kΩ
			SD16GAINx = 32			75		
		f_{SD16} = 1 MHz, SD16BUFx = 01	SD16GAINx = 1			>10		
Z_{ID}	Differential input impedance (IN+ to IN-)	f_{SD16} = 1 MHz, SD16BUFx = 00	SD16GAINx = 1	3 V	300	400		kΩ
			SD16GAINx = 32		100	150		
		f_{SD16} = 1 MHz, SD16BUFx = 01	SD16GAINx = 1			>10		

(1) The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF} / 2) / GAIN$ and $V_{FSR-} = -(V_{REF} / 2) / GAIN$. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

5.24 SD16_A, Performance

f_{SD16} = 30 kHz, SD16REFON = 1, SD16BUFx = 01
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1,Signal Amplitude = 500 mV, SD16OSRx = 256	f_{IN} = 2.8 Hz	3 V		84		dB
		SD16GAINx = 1,Signal Amplitude = 500 mV, SD16OSRx = 512				84		
		SD16GAINx = 1,Signal Amplitude = 500 mV, SD16OSRx = 1024				84		
G	Nominal gain	SD16GAINx = 1, SD16OSRx = 1024			0.97	1.00	1.02	
dG/dT	Gain temperature drift	SD16GAINx = 1, SD16OSRx = 1024				15		ppm/°C
dG/dV_{CC}	Gain supply voltage drift	SD16GAINx = 1, SD16OSRx = 1024, VCC = 2.5 V to 3.6 V				0.35		%/V

5.25 SD16_A, Performance

f_{SD16} = 1 MHz, SD16OSRx = 256, SD16REFON = 1, SD16BUFx = 00
V_{CC} = 3 V, over recommended operating free-air temperature (unless otherwise noted)

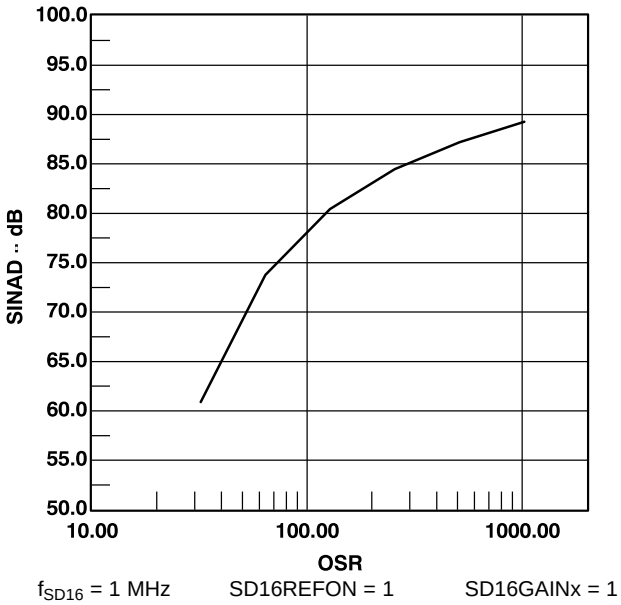
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1, Signal Amplitude = 500 mV	f_{IN} = 50 Hz or 100 Hz	83.5	85		dB
		SD16GAINx = 2, Signal Amplitude = 250 mV		81.5	84		
		SD16GAINx = 4, Signal Amplitude = 125 mV		76	79.5		
		SD16GAINx = 8, Signal Amplitude = 62 mV		73	76.5		
		SD16GAINx = 16, Signal Amplitude = 31 mV		69	73		
		SD16GAINx = 32, Signal Amplitude = 15 mV		62	69		
G	Nominal gain	SD16GAINx = 1		0.97	1.00	1.02	
		SD16GAINx = 2		1.90	1.96	2.02	
		SD16GAINx = 4		3.76	3.86	3.96	
		SD16GAINx = 8		7.36	7.62	7.84	
		SD16GAINx = 16		14.56	15.04	15.52	
		SD16GAINx = 32		27.20	28.35	29.76	
E_{OS}	Offset error	SD16GAINx = 1				±0.2	%FSR
		SD16GAINx = 32				±1.5	
dE_{OS}/dT	Offset error temperature coefficient	SD16GAINx = 1			±4	±20	ppm FSR/°C
		SD16GAINx = 32			±20	±100	
CMRR	Common-mode rejection ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz or 100 Hz			>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz or 100 Hz			>75		
PSRR	Power supply rejection ratio	SD16GAINx = 1			>80		dB

5.26 SD16_A, Linearity

f_{SD16} = 1 MHz, SD16REFON = 1, SD16BUFx = 00
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
INL	Integral nonlinearity	SD16OSR = 256, SD16GAINx = 000b, Signal Amplitude = 500 mV	3 V	1.5	LSB
		SD16OSR = 256, SD16GAINx = 101b, Signal Amplitude = 15 mV		6	
		SD16OSR = 1024, SD16GAINx = 000b, Signal Amplitude = 500 mV		0.8	
		SD16OSR = 1024, SD16GAINx = 101b, Signal Amplitude = 15 mV		3.5	

5.27 Typical Characteristics, SD16_A SINAD Performance Over OSR



f_{SD16} = 1 MHz SD16REFON = 1 SD16GAINx = 1

Figure 5-19. SINAD Performance vs OSR

5.28 SD16_A, Temperature Sensor and Built-in V_{CC} Sense

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient	See (2)		1.18	1.32	1.46	mV/K
$V_{Offset,Sensor}$	Sensor offset voltage	See (2)		–100		100	mV
V_{Sensor}	Sensor output voltage(3)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C		355	395	435	
		Temperature sensor voltage at T_A = 0°C(2)		320	360	400	
$V_{CC,Sense}$	V_{CC} divider at input 5	f_{SD16} = 32 kHz, SD16OSRx = 256, SD16REFON = 1		0.08	1/11	0.1	V

(1) Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.
(2) Not production tested, limits characterized.
(3) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV]

5.29 SD16_A, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0	3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	3 V		175	260	µA
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0(1)	3 V		18	50	ppm/°C
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0(2)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1, SD16VMIDON = 0	3 V			±200	nA
t_{ON}	Turn-on time	SD16REFON = 0 → 1, SD16VMIDON = 0, C_{REF} = 100 nF	3 V		5		ms
PSRR	Line regulation	SD16REFON = 1, SD16VMIDON = 0	3 V		100		µV/V

(1) Calculated using the box method: (MAX(--40...85°C) -- MIN(--40...85°C))/MIN(--40...85°C)/(85C -- (--40°C))
(2) There is no capacitance required on V_{REF}. However, TI recommends a capacitance of at least 100 nF to reduce any reference voltage noise.

5.30 SD16_A, Reference Output Buffer

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1	3 V		1.2		V
$I_{REF,BUF}$	Reference supply + reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	3 V		385	600	µA
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1	3 V			±1	mA
	Maximum voltage variation vs load current	$\|I_{LOAD}\|$ = 0 to 1 mA	3 V	–15		+15	mV
t_{ON}	Turn-on time	SD16REFON = 0 → 1, SD16VMIDON = 1, C_{REF} = 470 nF	3 V		100		µs

5.31 SD16_A, External Reference Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

5.32 12-Bit DAC, Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V		2.20		3.60	V
I_{DD}	Supply current, single DAC channel(1) (2)	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0800h	2.2 V, 3 V		50	110	µA
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			50	110	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			200	440	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			700	1500	
PSRR	Power-supply rejection ratio(3)(4)	DAC12_xDAT = 800h, $V_{REF,DAC12}$ = 1.2 V, ΔAV_{CC} = 100 mV	2.7 V		70		dB

(1) No load at the output pin, DAC12_0, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
(3) PSRR = $20 \times \log\{\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}\}$.
(4) V_{REF} is applied externally. The internal reference is not used.

5.33 12-Bit DAC, Linearity Specifications

over recommended operating free-air temperature (unless otherwise noted) (see Figure 5-20)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
INL	Integral nonlinearity(1)	$V_{REF,DAC12}$ = 1.2 V or $V_{REF,ext}$ = 2.5 V DAC12AMPx = 7, DAC12IR = 1	2.7 V		±2.0	±8.0	LSB
DNL	Differential nonlinearity(1)	$V_{REF,ext}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V	–1	±0.4	±1.3	LSB
		$V_{REF,ext}$ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1			±0.4	±1.0	
		$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1			±0.4	±1.0	
E_O	Offset voltage without calibration(1) (2)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V			±20	mV
	Offset voltage with calibration(1) (2)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1				±2.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient(1)		2.7 V		±30		µV/°C
E_G	Gain error(1)	$V_{REF,DAC12}$ = 1.2 V	2.7 V			±3.50	%FSR
$d_{E(G)}/d_T$	Gain temperature coefficient(1)		2.7 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration(3)	DAC12AMPx = 2	2.7 V			100	ms
		DAC12AMPx = 3, 5				32	
		DAC12AMPx = 4, 6, 7				6	

(1) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + b × x. $V_{DAC12\_xOUT} = E_O + (1 + E_G) \times (Ve_{REF+}/4095) \times DAC12\_xDAT$, DAC12IR = 1.
(2) The offset calibration works on the output operational amplifier. Offset calibration is triggered by setting bit DAC12CALON.
(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. TI recommends that the DAC12 module be configured before initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

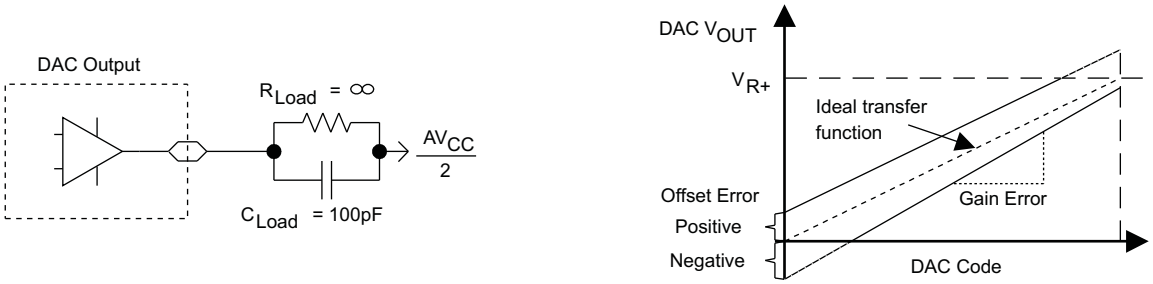


Figure 5-20. Linearity Test Load Conditions and Gain and Offset Definition

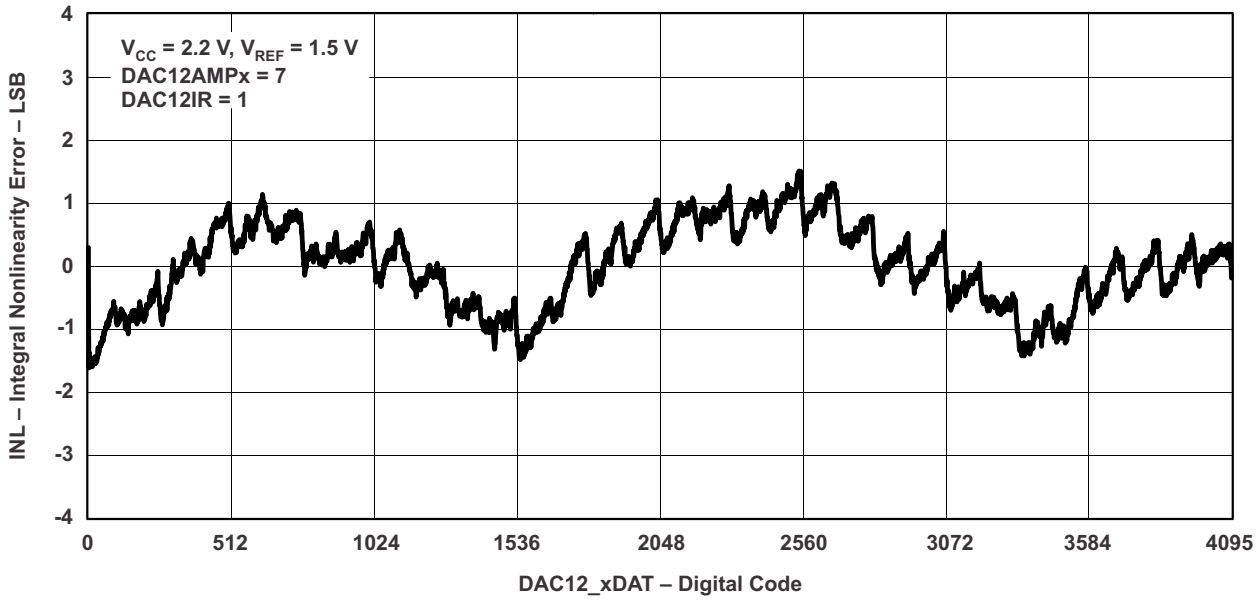


Figure 5-21. Typical INL Error vs Digital Input Data

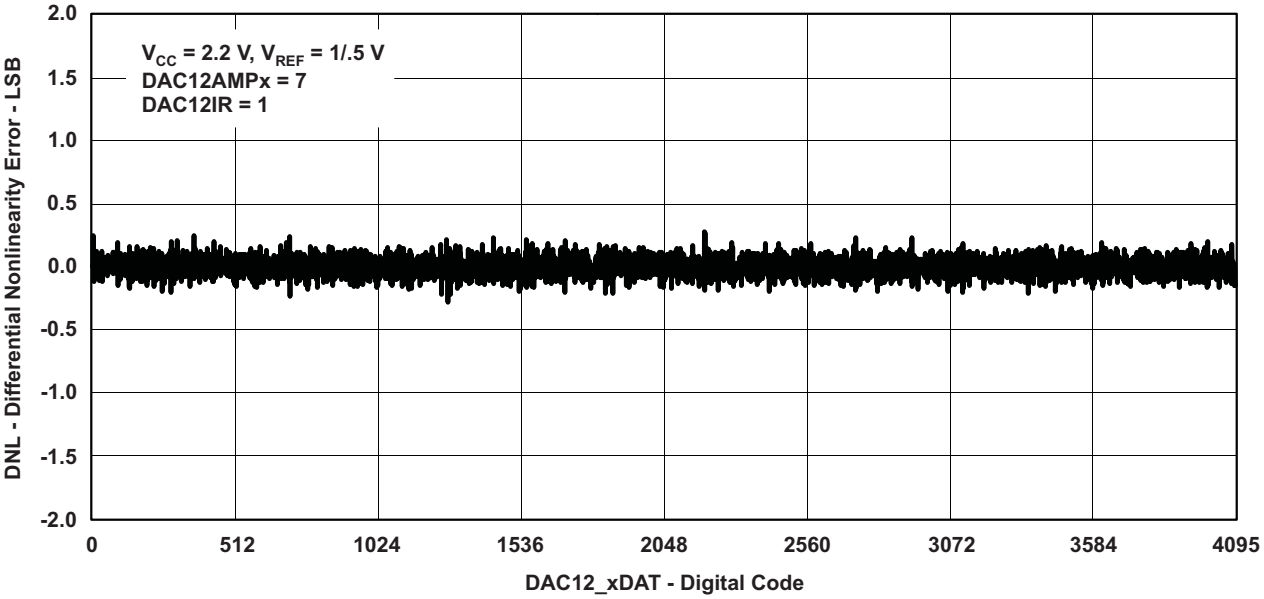


Figure 5-22. Typical DNL Error vs Digital Input Data

5.34 12-Bit DAC, Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range[1] (see Figure 5-23)	No load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V, 3 V	0		0.005	V
		No load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.13		AV_{CC}	
$C_{L(DAC12)}$	Maximum DAC12 load capacitance		2.2 V, 3 V			100	pF
$I_{L(DAC12)}$	Maximum DAC12 load current		2.2 V	–0.5		+0.5	mA
			3 V	–1.0		+1.0	
$R_{O/P(DAC12)}$	Output resistance (see Figure 5-23)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$ – 0.3 V, DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} – 0.3 V			1	4	

(1) Data is valid after the offset calibration of the output amplifier.

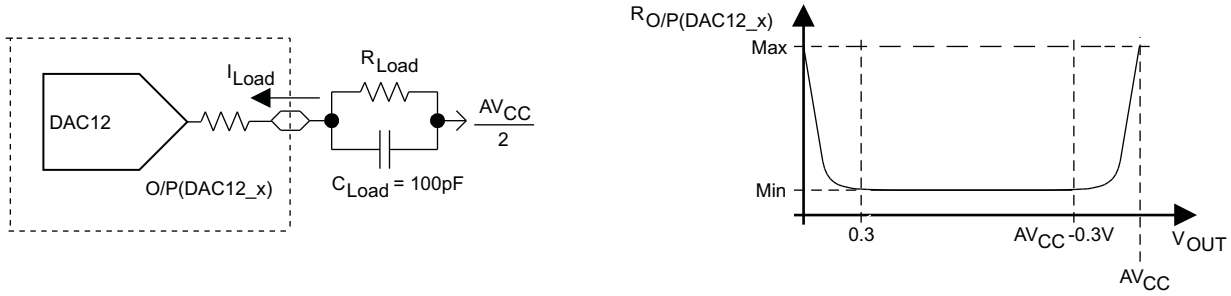


Figure 5-23. DAC12_x Output Resistance Tests

5.35 12-Bit DAC, Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Ve_{REF+}	Reference input voltage range	DAC12IR = 0[1] [2]	2.2 V, 3 V		AV_{CC}/3	AV_{CC} + 0.2	V
		DAC12IR = 1[3] [4]			AV_{CC}	AV_{CC} + 0.2	
$Ri_{(VREF+)}$	Reference input resistance	DAC12IR = 0, SD16VMIDON = 1[5]	2.2 V, 3 V	20			MΩ
		DAC12IR = 1, SD16VMIDON = 1		40	48	56	kΩ

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
(2) The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} – V_{E(O)}] / [3 × (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
(4) The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} – V_{E(O)}] / (1 + E_G)$.
(5) Characterized, not production tested

5.36 12-Bit DAC, Dynamic Specifications

$V_{ref} = V_{CC}$, DAC12IR = 1, over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-24 and Figure 5-25)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB(1) (see Figure 5-24)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V, 3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h→F7Fh→80h	DAC12AMPx = 2	2.2 V, 3 V		100	200	µs
			DAC12AMPx = 3, 5			40	80	
			DAC12AMPx = 4, 6, 7			15	30	
$t_{S(C–C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→408h→3F8h BF8h→C08h→BF8h	DAC12AMPx = 2	2.2 V, 3 V		5		µs
			DAC12AMPx = 3, 5			2		
			DAC12AMPx = 4, 6, 7			1		
SR	Slew rate	DAC12_xDAT = 80h→F7Fh→80h(2)	DAC12AMPx = 2	2.2 V, 3 V	0.05	0.12		V/µs
			DAC12AMPx = 3,5		0.35	0.7		
			DAC12AMPx = 4, 6, 7		1.5	2.7		
	Glitch energy, full-scale	DAC12_xDAT = 80h→F7Fh→80h	DAC12AMPx = 2	2.2 V, 3 V		600		nV-s
			DAC12AMPx = 3,5			150		
			DAC12AMPx = 4, 6, 7			30		

(1) R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 5-24.
(2) Slew rate applies to output voltage steps ≥200 mV.

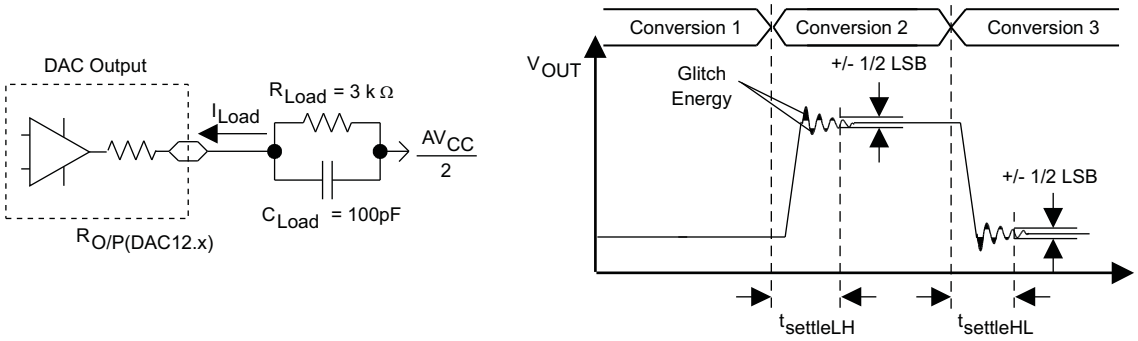


Figure 5-24. Settling Time and Glitch Energy Testing

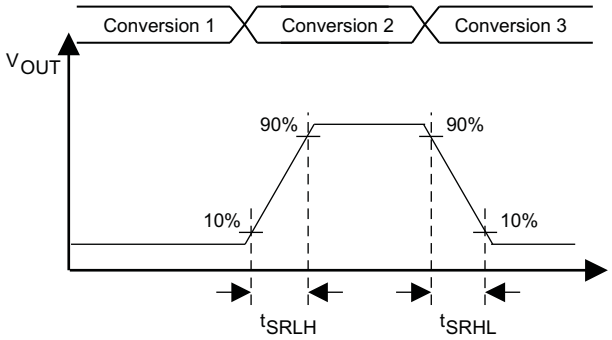


Figure 5-25. Slew Rate Testing

5.37 12-Bit DAC, Dynamic Specifications Continued

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 V_{PP} (see Figure 5-26)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V, 3 V	40		kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		180		
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		550		

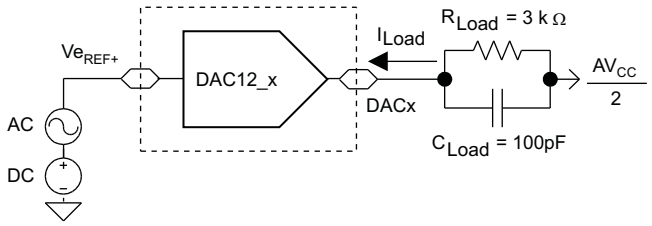


Figure 5-26. Test Conditions for 3-dB Bandwidth Specification

5.38 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ±10%	2.2 V		8	MHz
			3 V		10	
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V, 3 V	20		ns

5.39 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_B clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ±10%	2.2 V		8	MHz
			3 V		10	
$t_{TA,cap}$	Timer_B capture timing	TB0, TB1, TB2	2.2 V, 3 V	20		ns

5.40 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)(1)		2.2 V, 3 V	2			MHz
t_{τ}	UART receive deglitch time UART(2)		2.2 V	50	150	600	ns
			3 V	50	100	600	

(1) The DCO wake-up time must be considered in LPM3 or LPM4 for baud rates above 1 MHz.
(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

5.41 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 5-27 and Figure 5-28)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		
$t_{HD,MI}$	iSOMI input data hold time		2.2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

5.42 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 5-29 and Figure 5-30)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V, 3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V, 3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V, 3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V, 3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

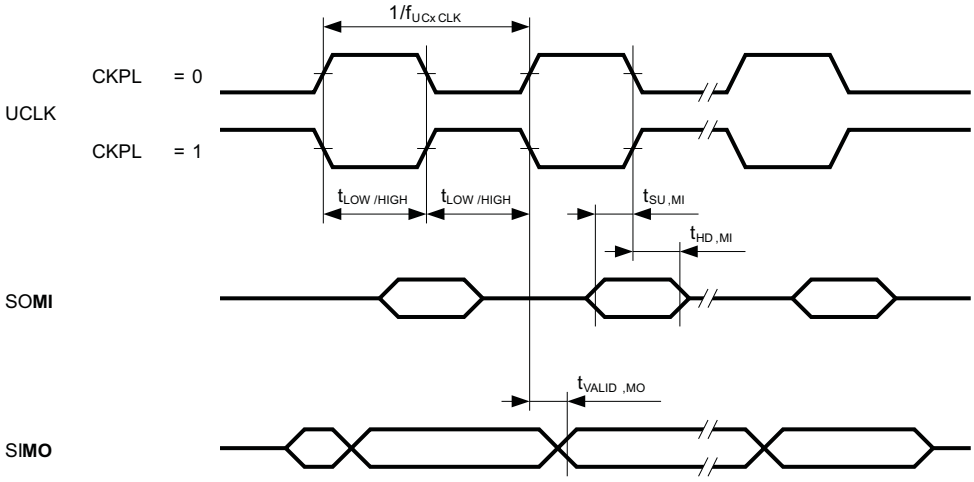


Figure 5-27. SPI Master Mode, CKPH = 0

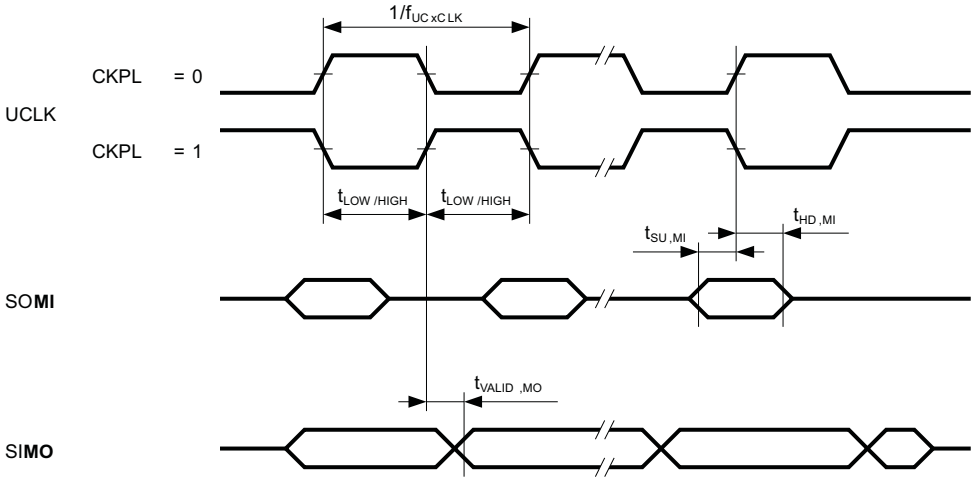


Figure 5-28. SPI Master Mode, CKPH = 1

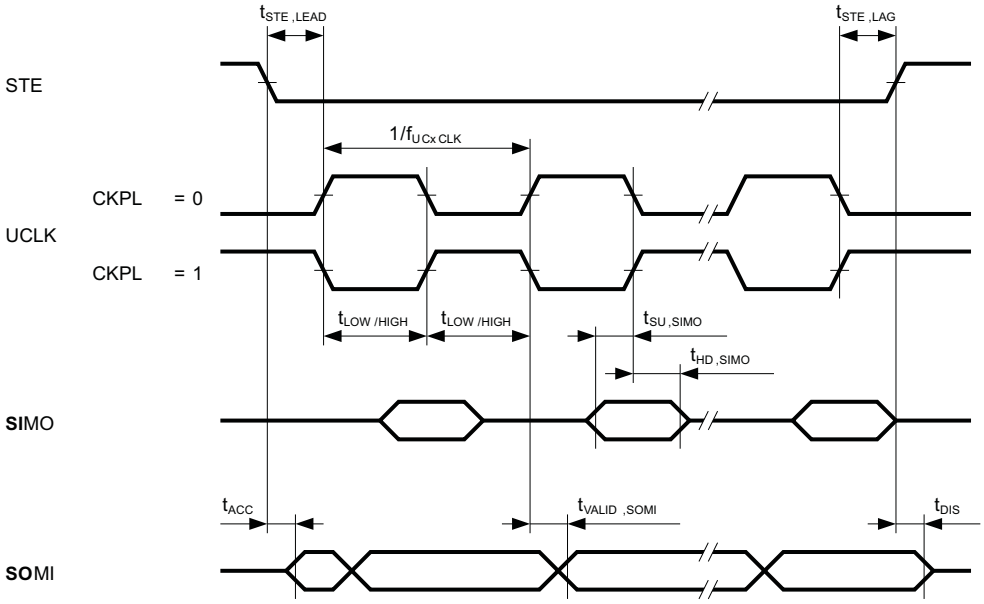


Figure 5-29. SPI Slave Mode, CKPH = 0

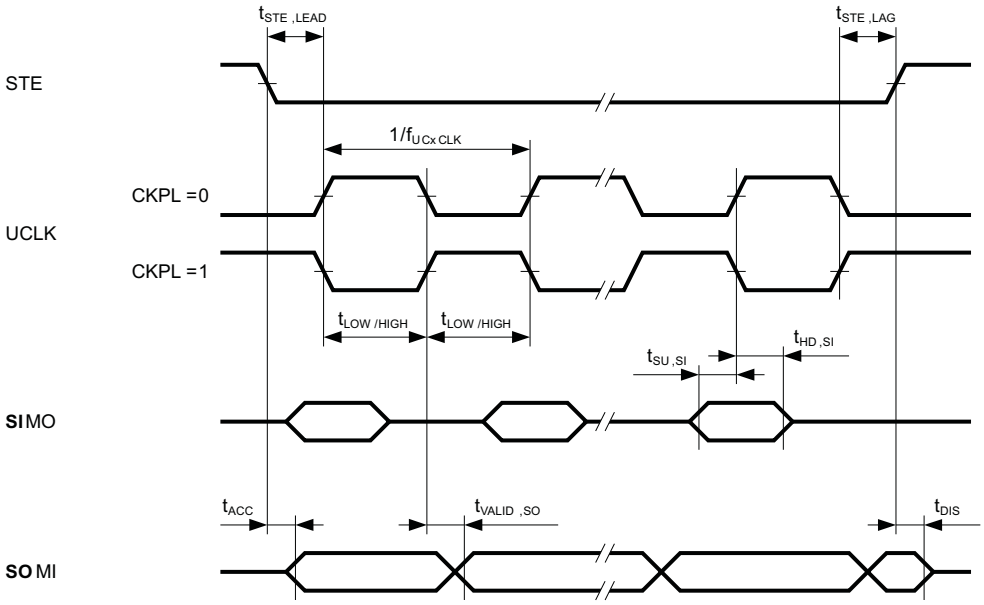


Figure 5-30. SPI Slave Mode, CKPH = 1

5.43 USCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-31)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty Cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.0			µs
		$f_{SCL} > 100$ kHz	2.2 V, 3 V	0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.7			µs
		$f_{SCL} > 100$ kHz	2.2 V, 3 V	0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V, 3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

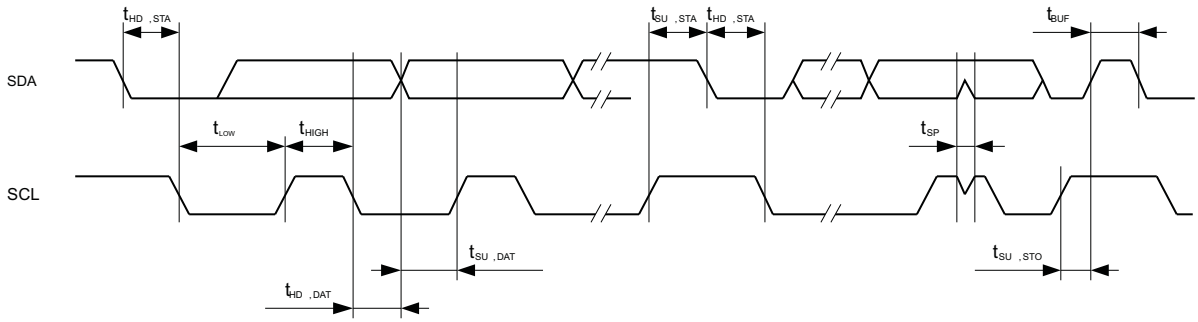


Figure 5-31. I^2C Mode Timing

5.44 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from DVCC during program		2.5 V, 3.6 V		3	5	mA
I_{ERASE}	Supply current from DVCC during erase		2.5 V, 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	(1)	2.5 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.5 V, 3.6 V	200			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

(1) The cumulative program time must not be exceeded when writing to a 64--byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the flash controller' mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).

5.45 JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	(1)	2.2 V	0		5	MHz
			3 V	0		10	
$R_{Internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	(2)	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
(2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

5.46 JTAG Fuse(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow		6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

6 Detailed Description

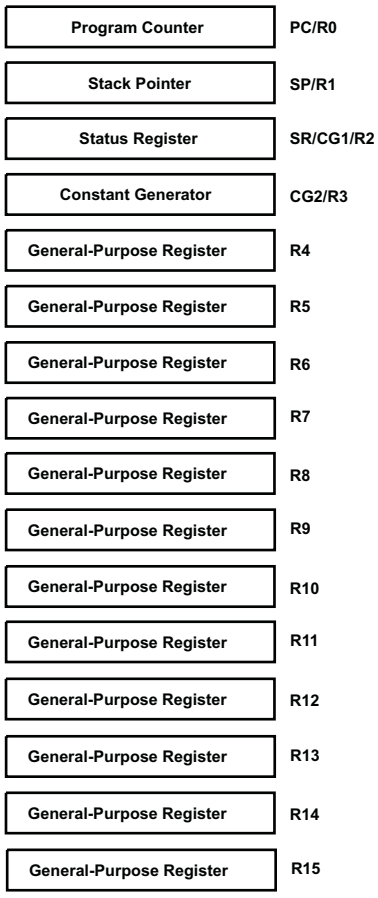
6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 6-1 shows examples of the three types of instruction formats; the address modes are listed in Table 6-2.

Table 6-1. Instruction Word Formats

FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC→ (TOS), R8 → PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	•	•	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	•	•	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)→ M(6+R6)
Symbolic (PC relative)	•	•	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	•	•	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	•		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	•		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2→ R10
Immediate	•		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) NOTE: S = source D = destination

6.3 Operating Modes

These devices have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL+ loop control is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control and DCOCLK are disabled
  - DCO DC generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO DC generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO DC generator is disabled
  - Crystal oscillator is stopped

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

If the reset vector (located at address 0xFFFE) contains 0xFFFF (for example, flash is not programmed) the CPU goes into LPM4 immediately after power-up.

Table 6-3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory PC Out-of-Range (1)	PORIFG RSTIFG WDTIFG KEYV (2)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (2) (3) OFIFG (2) (3) ACCVIFG (2) (4)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B3	TBCCR0 CCIFG0 (4)	Maskable	0FFFAh	13
Timer_B3	TBCCR1 CCIFG1 and TBCCR2 CCIFG2, TBIFG (2) (4)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog Timer+	WDTIFG	Maskable	0FFF4h	10
USCI_A0, USCI_B0 Receive, USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG (2) (5)	Maskable	0FFF2h	9
USCI_A0, USCI_B0 Transmit, USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG (2) (6)	Maskable	0FFF0h	8
SD16_A	SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG (2) (4)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG0 (4)	Maskable	0FFECh	6
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (2) (4)	Maskable	0FFEAh	5
I/O Port P1 (8 Flags)	P1IFG.0 to P1IFG.7 (2) (4)	Maskable	0FFE8h	4
DAC12	DAC12_0IFG	Maskable	0FFE6h	3
		Maskable	0FFE4h	2
I/O Port P2 (8 Flags)	P2IFG.0 to P2IFG.7 (2) (4)	Maskable	0FFE2h	1
Basic Timer 1, RTC	BTIFG	Maskable	0FFE0h	0, lowest

(1) Access and key violations, KEYV and ACCVIFG.
(2) Multiple source flags
(3) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.

6.5 Special Function Registers (SFRs)

The SFRs are in the lowest address space and are organized as byte mode registers. SFRs should be accessed with byte instructions.

Legend

rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), rw-(1)	Bit can be read and written. It is Reset or Set by POR.
	SFR bit is not present in device

6.5.1 Interrupt Enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.

OFIE Oscillator fault-interrupt enable

NMIIE Nonmaskable interrupt enable

ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE				UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
	rw-0				rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI_A0 receive-interrupt enable

UCA0TXIE USCI_A0 transmit-interrupt enable

UCB0RXIE USCI_B0 receive-interrupt enable

UCB0TXIE USCI_B0 transmit-interrupt enable

BTIE Basic timer interrupt enable

6.5.2 Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode

OFIFG Flag set on oscillator fault

RSTIFG External reset interrupt flag. Set on a reset condition at RST/NMI pin in reset mode. Reset on V_{CC} power-up.

PORIFG Power-on interrupt flag. Set on Vcs power-up.

NMIIFG Set by the $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG				UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
	rw-0				rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive-interrupt flag

UCA0TXIFG USCI_A0 transmit-interrupt flag

UCB0RXIFG USCI_B0 receive-interrupt flag

UCB0TXIFG USCI_B0 transmit-interrupt flag

BTIFG Basic timer flag

6.6 Memory Organization

Table 6-4 summarizes the memory organization for the MSP430F47x MCUs.

Table 6-4. Memory Organization

		MSP430F477	MSP430F478	MSP430F479
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32KB 0FFFFh to 0FFE0h 0FFFFh to 08000h	48KB 0FFFFh to 0FFE0h 0FFFFh to 04000h	60KB 0FFFFh to 0FFE0h 0FFFFh to 01100h
Information memory	Size Flash	256 Byte 010FFh to 01000h	256 Byte 010FFh to 01000h	256 Byte 010FFh to 01000h
Boot memory	Size ROM	1KB 0FFFh to 0C00h	1KB 0FFFh to 0C00h	1KB 0FFFh to 0C00h
RAM	Size	2KB 09FFh to 0200h	2KB 09FFh to 0200h	2KB 09FFh to 0200h
Peripherals	16 bit 8 bit 8-bit SFR	01FFh to 0100h 0FFh to 010h 0Fh to 00h	01FFh to 0100h 0FFh to 010h 0Fh to 00h	01FFh to 0100h 0FFh to 010h 0Fh to 00h

6.7 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using a UART serial interface. Access to the MCU memory through the BSL is protected by user-defined password. A bootloader security key is provided at address 0FFBEh to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. The BSL is optional for ROM-based devices. For complete description of the features of the BSL and its implementation, see the MSP430™ Flash Devices Bootloader (BSL) User's Guide.

BSL FUNCTION	PN PACKAGE	ZCA OR ZQW PACKAGE
Data Transmit	58 - P1.0	C11 - P1.0
Data Receiver	57 - P1.1	C12 - P1.1

6.8 Flash Memory

The flash memory can be programmed by the JTAG port, the bootloader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called information memory.
- Segment A might contain calibration data. After reset, segment A is protected against programming or erasing. It can be unlocked, but care should be taken not to erase this segment if the calibration data is required.
- Flash content integrity check with marginal read modes.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*.

6.9.1 Oscillator and System Clock

The clock system is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO), and a 8-MHz high-frequency crystal oscillator (XT1), plus a 8-MHz high-frequency crystal oscillator (XT2). The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 s. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Submain clock (SMCLK), the subsystem clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

6.9.2 Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit provides the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must make sure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

6.9.3 Digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions

6.9.4 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.5 Basic Timer1 and Real-Time Clock

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for months with less than 31 days and includes leap-year correction.

6.9.6 LCD_A Drive With Regulated Charge Pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore, it is possible to control the level of the LCD voltage and, thus, contrast in software.

6.9.7 Timer_A3

Timer_A3 is a 16-bit timer or counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-5. Timer_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZCA OR ZQW					PN	ZCA OR ZQW
P1.5 - 51	F11	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.5 - 51	F11	TAINCLK	INCLK				
P1.0 - 58	C11	TA0	CCI0A	CCR0	TA0	P1.0 - 58	C11
P1.1 - 57	C12	TA0	CCI0B			P1.1 - 57	C12
		DVSS	GND				
		DVCC	VCC				
P1.2 - 56	D11	TA1	CCI1A	CCR1	TA1	P1.2 - 56	D11
		CAOUT (internal)	CCI1B				
		DVSS	GND				
		DVCC	VCC				
P2.0 - 4	C2	TA2	CCI2A	CCR2	TA2	P2.0 - 4	C2
		ACLK (internal)	CCI2B				
		DVSS	GND				
		DVCC	VCC				

6.9.8 Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-6. Timer_B3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZCA OR ZQW					PN	ZCA OR ZQW
P1.4 - 54	E11	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.4 - 54	E11	$\overline{\text{TBCLK}}$ (1)	INCLK				
P2.1 - 3	C1	TB0	CCI0A	CCR0	TB0	P2.1 - 3	C1
P2.1 - 3	C1	TB0	CCI0B				
		VSS	GND				
		VCC	VCC				
P2.2 - 2	B1	TB1	CCI1A	CCR1	TB1	P2.2 - 2	B1
P2.2 - 2	B1	TB1	CCI1B				
		VSS	GND				
		VCC	VCC				
P2.3 - 77	B4	TB2	CCI2A	CCR2	TB2	P2.3 - 77	B4
		ACLK (internal)	CCI2B				
		VSS	GND				
		VCC	VCC				

(1) The inversion of TBCLK is done inside the module.

6.9.9 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3-pin or 4-pin), I^2C, and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection, and IrDA.

The USCI_A0 module provides support for SPI (3-pin or 4-pin), UART, enhanced UART and IrDA.

The USCI_B0 module provides support for SPI (3-pin or 4-pin) and I^2C.

6.9.10 Comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

6.9.11 SD16_A

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and a reference generator. In addition to external analog inputs, an internal VCC sense and temperature sensor are also available.

6.9.12 DAC12

The DAC12 module is a 12-bit R-ladder voltage-output DAC. The DAC12 can be used in 8-bit or 12-bit mode and can be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

6.9.13 Peripheral File Map

Table 6-7 lists the registers and addresses for peripherals with word access. Table 6-8 lists the registers and addresses for peripherals with byte access.

Table 6-7. Peripherals With Word Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B3	Capture/compare register 2	TBCCR2	0 96h
	Capture/compare register 1	TBCCR1	0 94h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Capture/compare register 2	TACCR1	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash	Flash control 4	FCTL4	01BEh
	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DAC12	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
SD16_A (also see Table 6-8)	General control	SD16CTL	0100h
	Channel 0 control	SD16CCTL0	0102h
	Channel 0 conversion memory	SD16MEM0	0112h
	Interrupt vector word register	SD16IV	0110h

Table 6-8. Peripherals With Byte Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
SD16_A (also see Table 6-7)	Channel 0 input control Analog enable	SD16INCTL0 SD16AE	0B0h 0B7h
LCD_A	LCD Voltage Control 1 LCD Voltage Control 0 LCD Voltage Port Control 1 LCD Voltage Port Control 0 LCD memory 20 : LCD memory 16 LCD memory 15 : LCD memory 1 LCD control and mode	LCDAVCTL1 LCDAVCTL0 LCDAPCTL1 LCDAPCTL0 LCDM20 : LCDM16 LCDM15 : LCDM1 LCDCTL	0AFh 0AEh 0ADh 0ACh 0A4h : 0A0h 09Fh : 091h 090h
USCI_A0, USCI_B0	USCI A0 auto baud rate control USCI A0 transmit buffer USCI A0 receive buffer USCI A0 status USCI A0 modulation control USCI A0 baud rate control 1 USCI A0 baud rate control 0 USCI A0 control 1 USCI A0 control 0 USCI A0 IrDA receive control USCI A0 IrDA transmit control	UCA0ABCTL UCA0TXBUF UCA0RXBUF UCA0STAT UCA0MCTL UCA0BR1 UCA0BR0 UCA0CTL1 UCA0CTL0 UCA0IRRCTL UCA0IRTCTL	0x005D 0x0067 0x0066 0x0065 0x0064 0x0063 0x0062 0x0061 0x0060 0x005F 0x005E
	USCI B0 transmit buffer USCI B0 receive buffer USCI B0 status USCI B0 I2C Interrupt enable USCI B0 baud rate control 1 USCI B0 baud rate control 0 USCI B0 control 1 USCI B0 control 0 USCI B0 I2C slave address USCI B0 I2C own address	UCB0TXBUF UCB0RXBUF UCB0STAT UCB0CIE UCB0BR1 UCB0BR0 UCB0CTL1 UCB0CTL0 UCB0SA UCB0OA	0x006F 0x006E 0x006D 0x006C 0x006B 0x006A 0x0069 0x0068 0x011A 0x0118
Comparator_A	Comparator_A port disable Comparator_A control 2 Comparator_A control 1	CAPD CACTL2 CACTL1	05Bh 05Ah 059h
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	056h
FLL+ Clock	FLL+ Control 1 FLL+ Control 0 System clock frequency control System clock frequency integrator System clock frequency integrator	FLL_CTL1 FLL_CTL0 SCFQCTL SCFI1 SCFI0	054h 053h 052h 051h 050h
RTC (Basic Timer 1)	Real Time Clock Year High Byte Real Time Clock Year Low Byte Real Time Clock Month Real Time Clock Day of Month Basic Timer1 Counter 2 Basic Timer1 Counter 1 Real Time Counter 4 (Real Time Clock Day of Week) Real Time Counter 3 (Real Time Clock Hour) Real Time Counter 2 (Real Time Clock Minute) Real Time Counter 1 (Real Time Clock Second) Real Time Clock Control Basic Timer1 Control	RTCYEARH RTCYEARL RTCMON RTCDAY BTCNT2 BTCNT1 RTCNT4 (RTCDOW) RTCNT3 (RTCHOUR) RTCNT2 (RTCMIN) RTCNT1 (RTCSEC) RTCCTL BTCTL	04Fh 04Eh 04Dh 04Ch 047h 046h 045h 044h 043h 042h 041h 040h
Port P6	Port P6 selection Port P6 direction Port P6 output Port P6 input	P6SEL P6DIR P6OUT P6IN	037h 036h 035h 034h
Port P5	Port P5 selection Port P5 direction Port P5 output Port P5 input	P5SEL P5DIR P5OUT P5IN	033h 032h 031h 030h

Table 6-8. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Port P4	Port P4 selection Port P4 direction Port P4 output Port P4 input	P4SEL P4DIR P4OUT P4IN	01Fh 01Eh 01Dh 01Ch
Port P3	Port P3 selection Port P3 direction Port P3 output Port P3 input	P3SEL P3DIR P3OUT P3IN	01Bh 01Ah 019h 018h
Port P2	Port P2 selection Port P2 interrupt enable Port P2 interrupt-edge select Port P2 interrupt flag Port P2 direction Port P2 output Port P2 input	P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN	02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h
Port P1	Port P1 selection Port P1 interrupt enable Port P1 interrupt-edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	026h 025h 024h 023h 022h 021h 020h
Special functions	SFR module enable 2 SFR module enable 1 SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	ME2 ME1 IFG2 IFG1 IE2 IE1	005h 004h 003h 002h 001h 000h

6.10 Input/Output Schematics

6.10.1 Port P1, P1.0, Input/Output With Schmitt Trigger

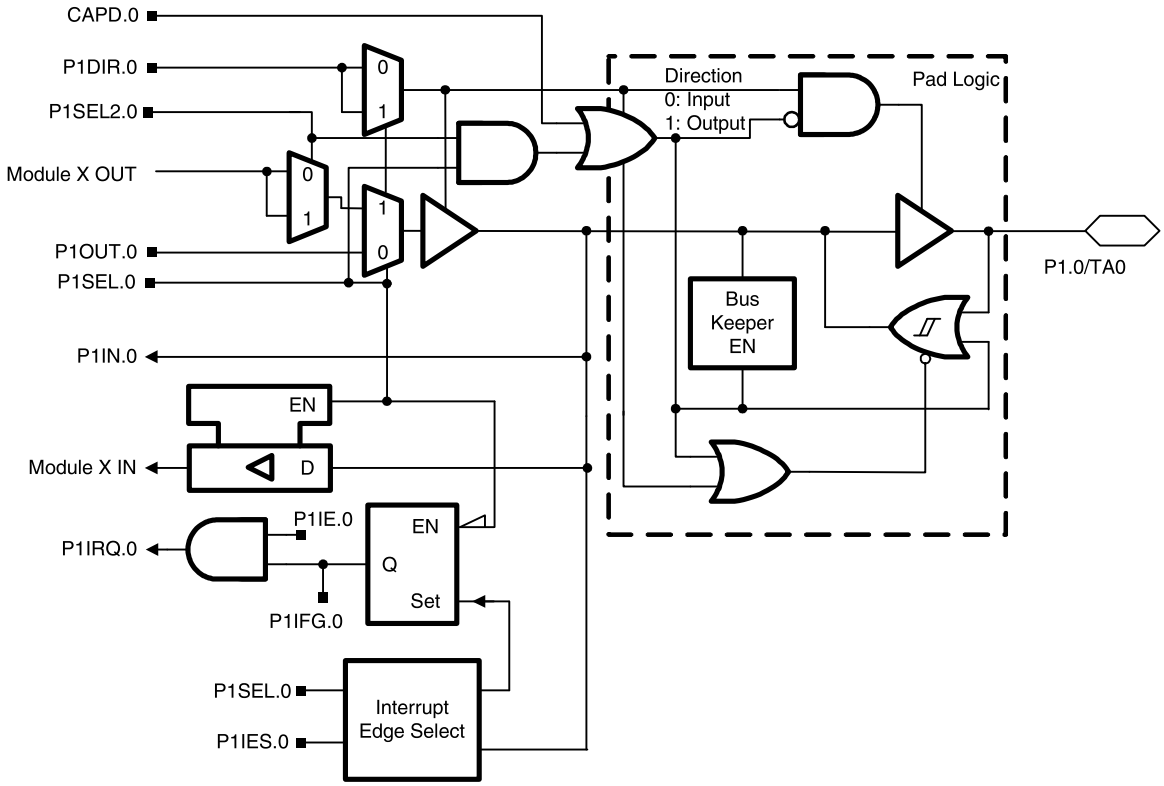


Table 6-9. Port P1 (P1.0) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.0/TA0	0	P1.x (I/O)	0	I: 0, O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0

(1) x = don't care

6.10.2 Port P1, P1.1, Input/Output With Schmitt Trigger

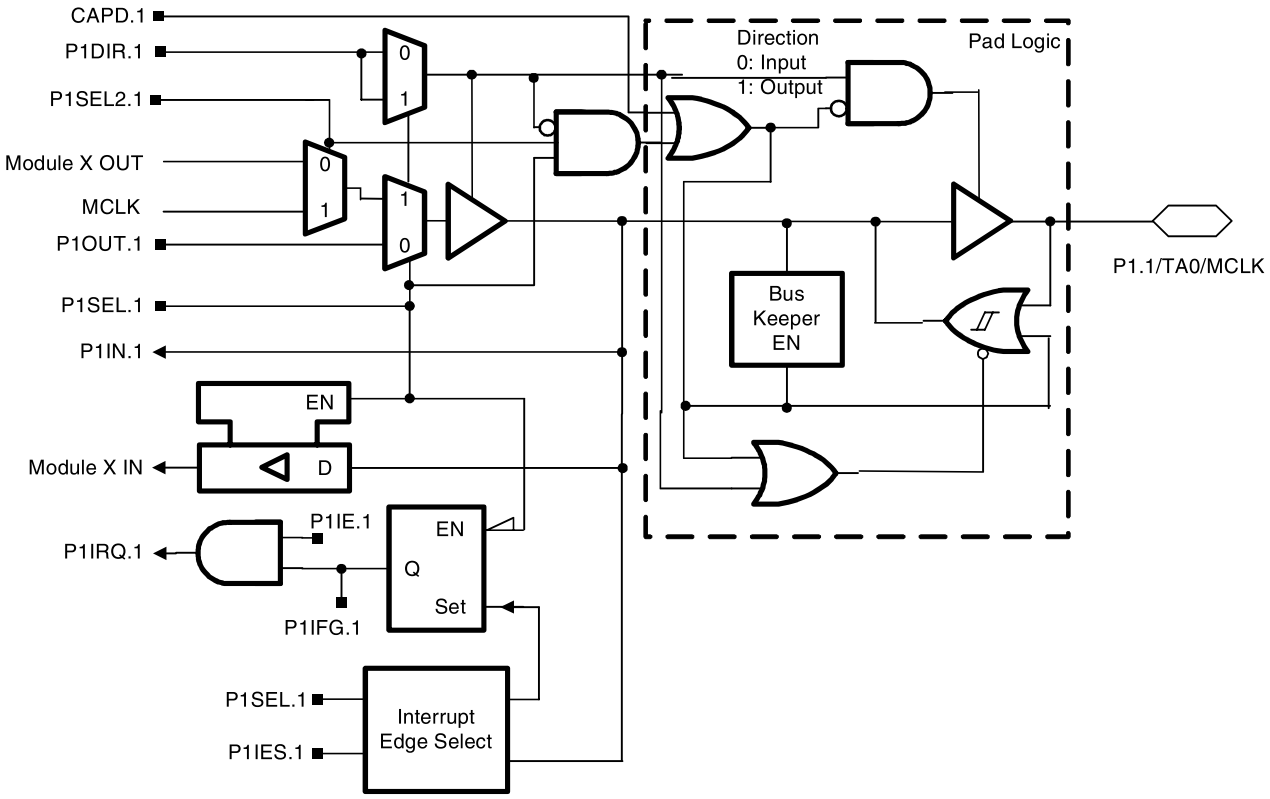


Table 6-10. Port P1 (P1.1) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.1/TA0/MCLK	1	P1.x (I/O)	0	I: 0, O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0
		MCLK	0	1	1	1

(1) x = don't care

6.10.3 Port P1, P1.2, Input/Output With Schmitt Trigger

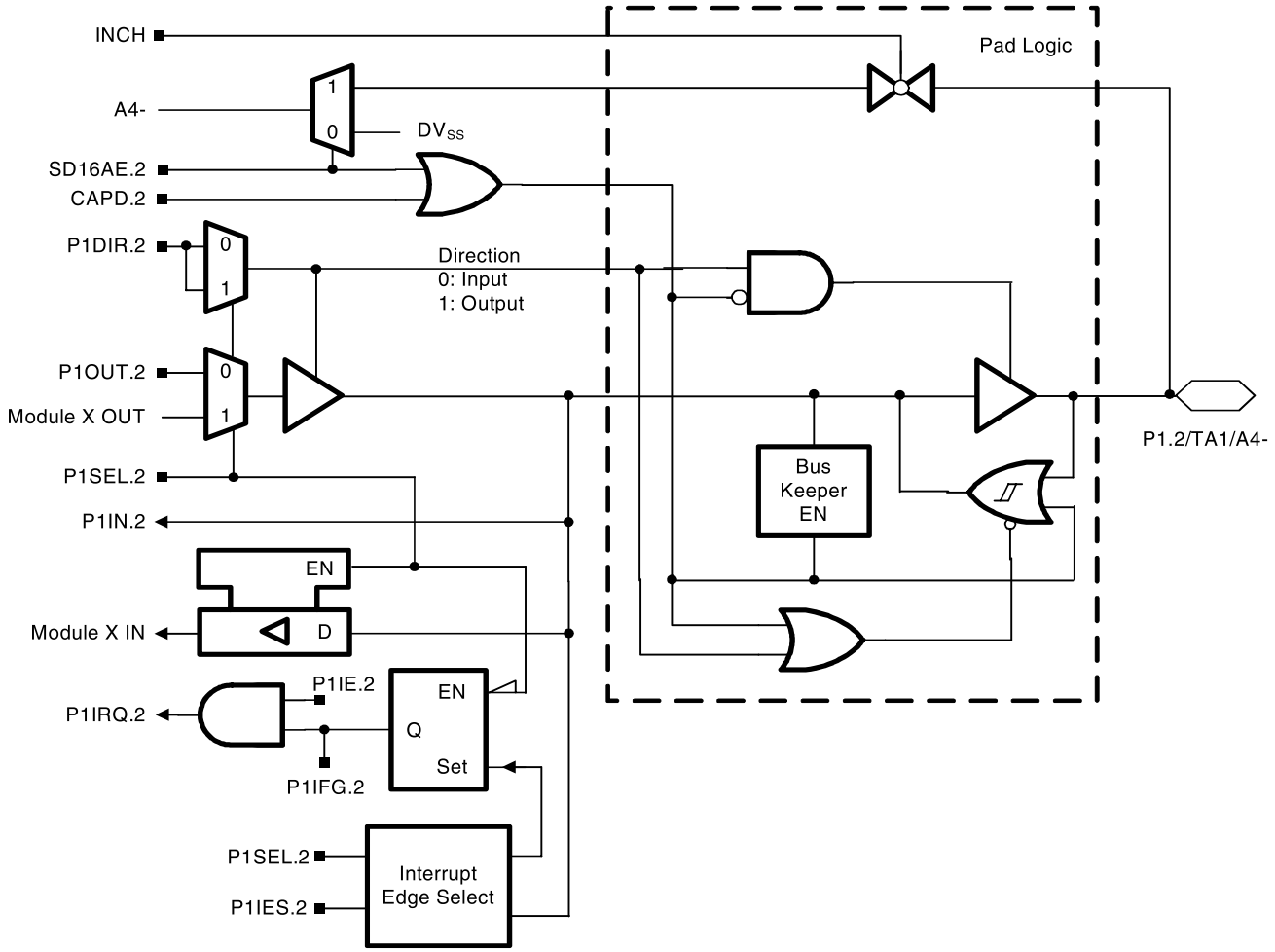


Table 6-11. Port P1 (P1.2) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.2/TA1/A4-	2	P1.x (I/O)	0	I: 0, O: 1	0	0
		Timer_A3.CCI1A	0	0	1	0
		Timer_A3.TA1	0	1	1	0
		A4-	x	x	x	1

(1) x = don't care

6.10.4 Port P1, P1.3, Input/Output With Schmitt Trigger

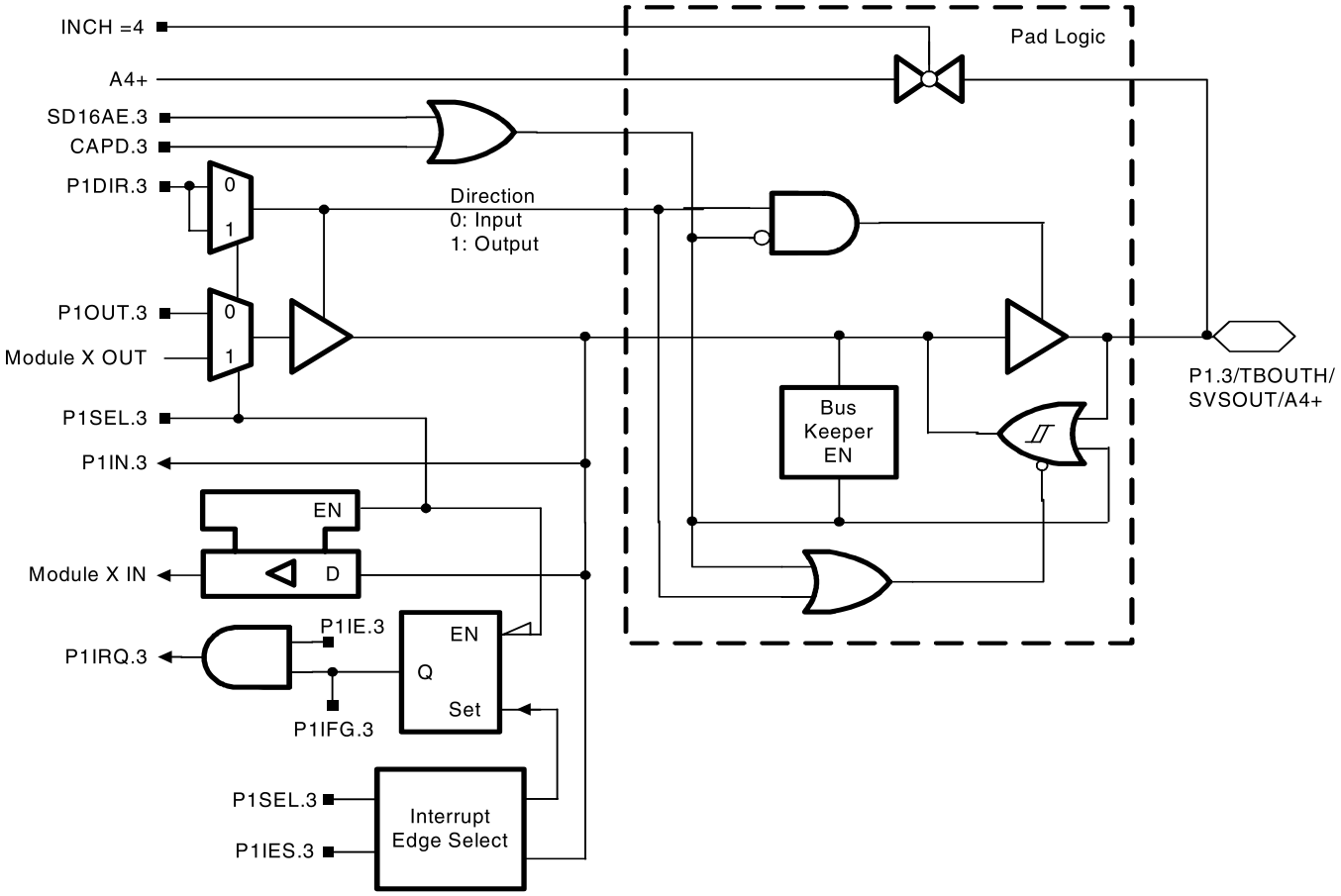


Table 6-12. Port P1 (P1.3) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.3/TBOUTH/ SVSOUT/A4+	3	P1.x (I/O)	0	I: 0, O: 1	0	0
		TBOUTH	0	0	1	0
		SVSOUT	0	1	1	0
		A4+	x	x	x	1

(1) x = don't care

6.10.5 Port P1, P1.4, Input/Output With Schmitt Trigger

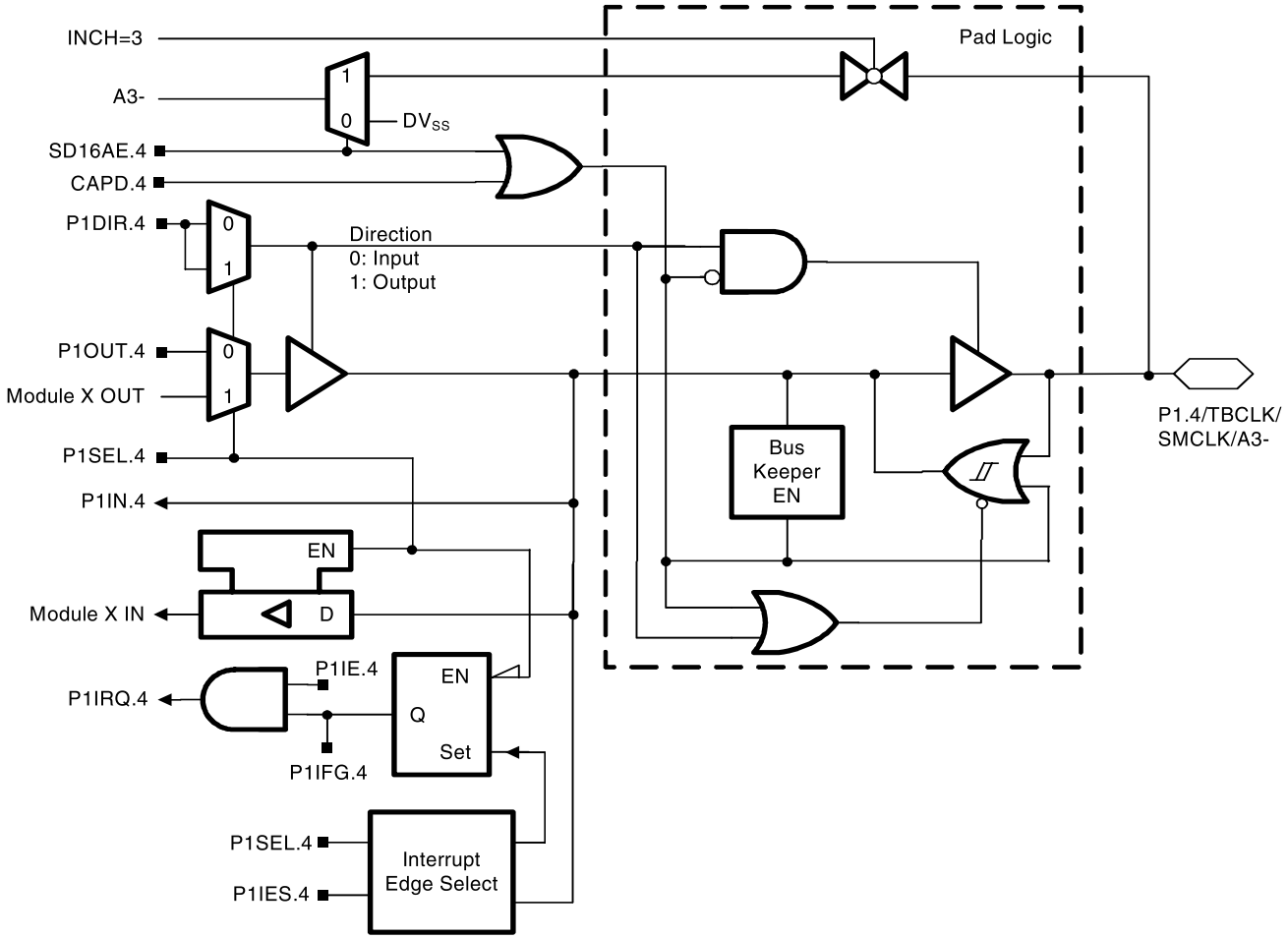


Table 6-13. Port P1 (P1.4) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.4/TBCLK/SMCLK/A3-	4	P1.x (I/O)		I: 0, O: 1	0	0
		TBCLK		0	1	0
		SMCLK		1	1	0
		A3-		x	x	1

(1) x = don't care

6.10.6 Port P1, P1.5, Input/Output With Schmitt Trigger

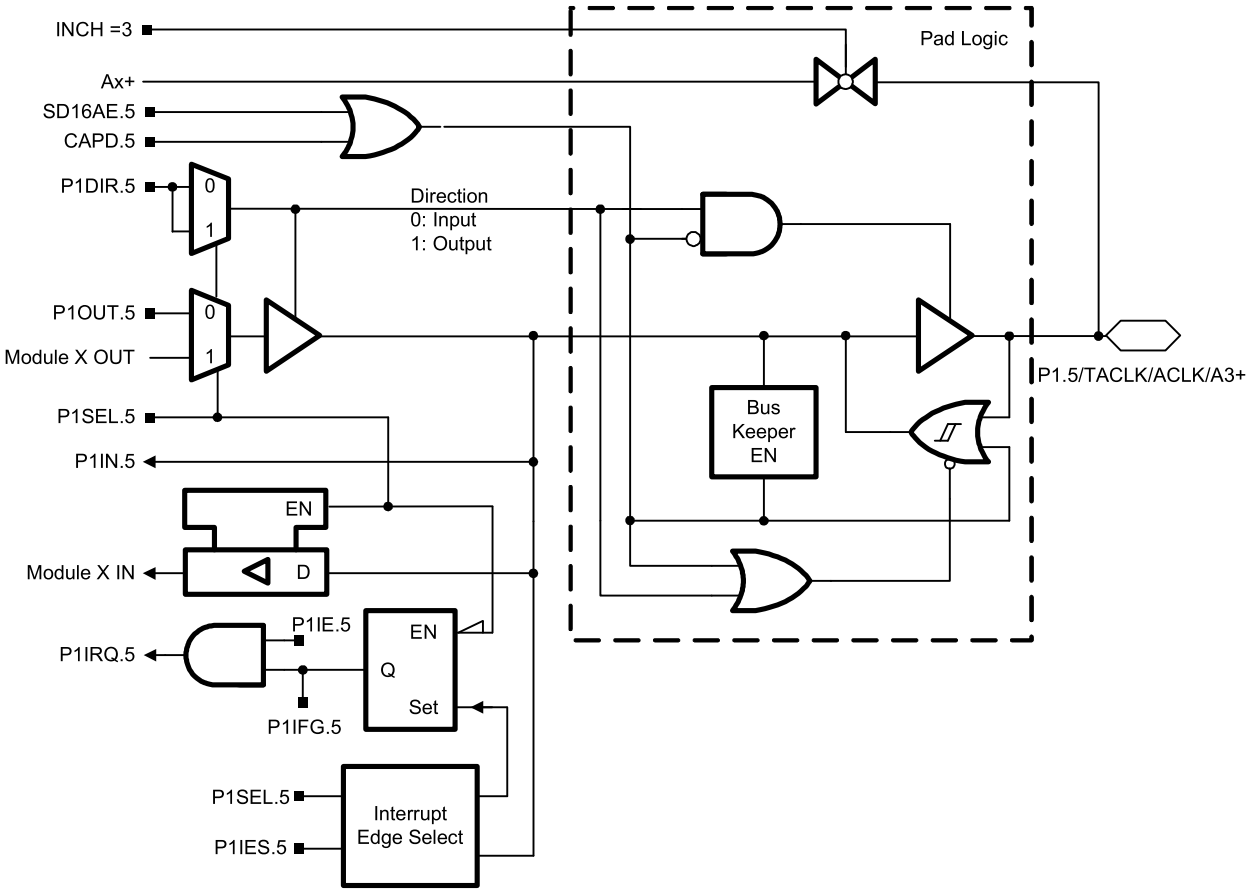


Table 6-14. Port P1 (P1.5) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.5/ACLK/ACLK/A3+	5	P1.x (I/O)	0	I: 0, O: 1	0	0
		TACLK	0	0	1	0
		ACLK	0	1	1	0
		A3+	x	x	x	1

(1) x = don't care

6.10.7 Port P1, P1.6, Input/Output With Schmitt Trigger

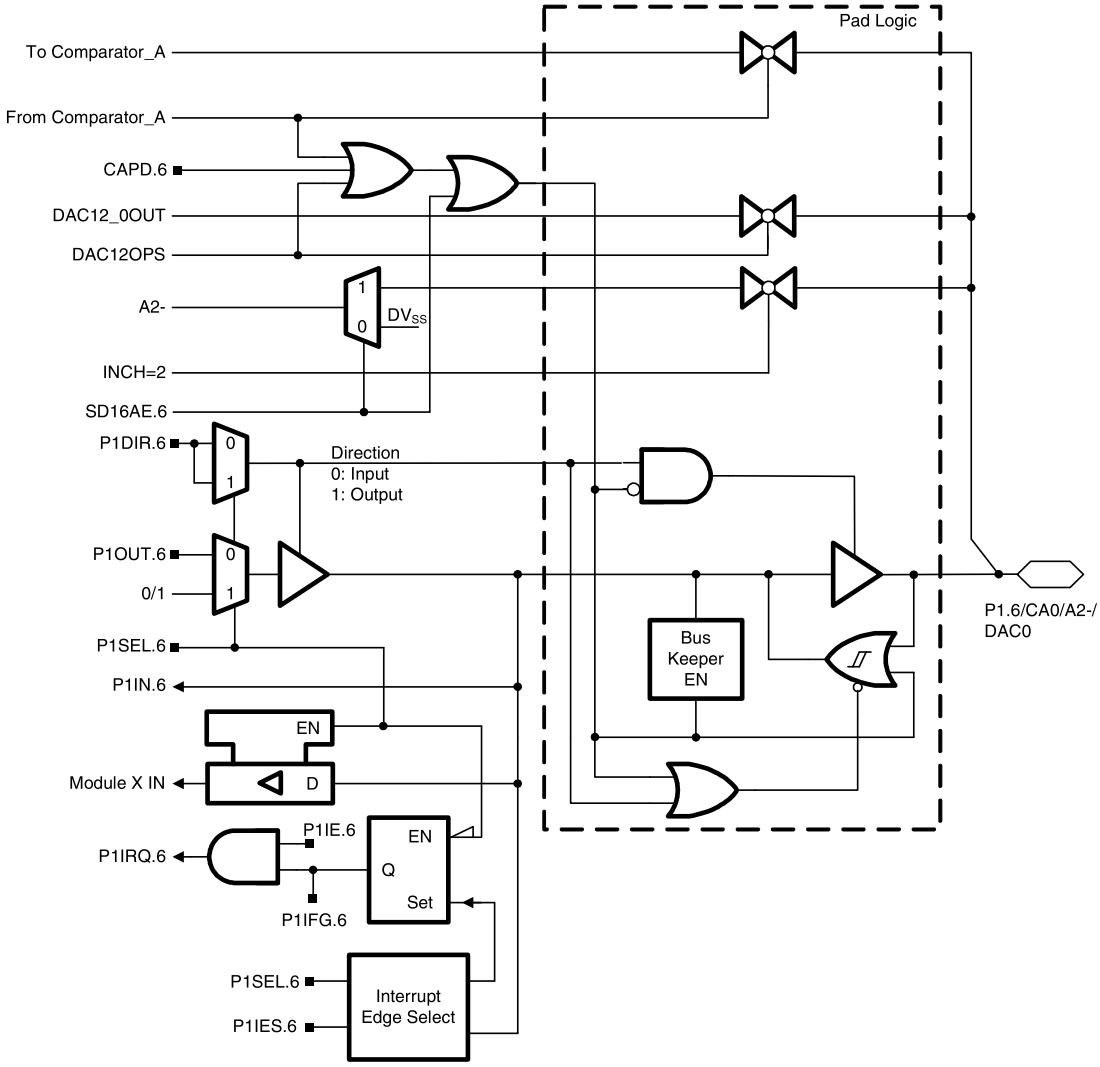


Table 6-15. Port P1 (P1.6) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)				
			P1DIR.x	P1SEL.x	P1SEL2.x = 0 CAPD.x	P1SEL2.x = 0 SD16AE.x	P1SEL2.x = 0 DAC12OPS (DAC12_0)
P1.6/CA0/A2-/DAC0	6	P1.x (I/O)	I: 0, O: 1	0	0	0	0
		CA0	x	x	1 or selected	x	x
		A2-	x	x	x	1	x
		DAC0	x	x	x	x	1

(1) x = don't care

6.10.8 Port P1, P1.7, Input/Output With Schmitt Trigger

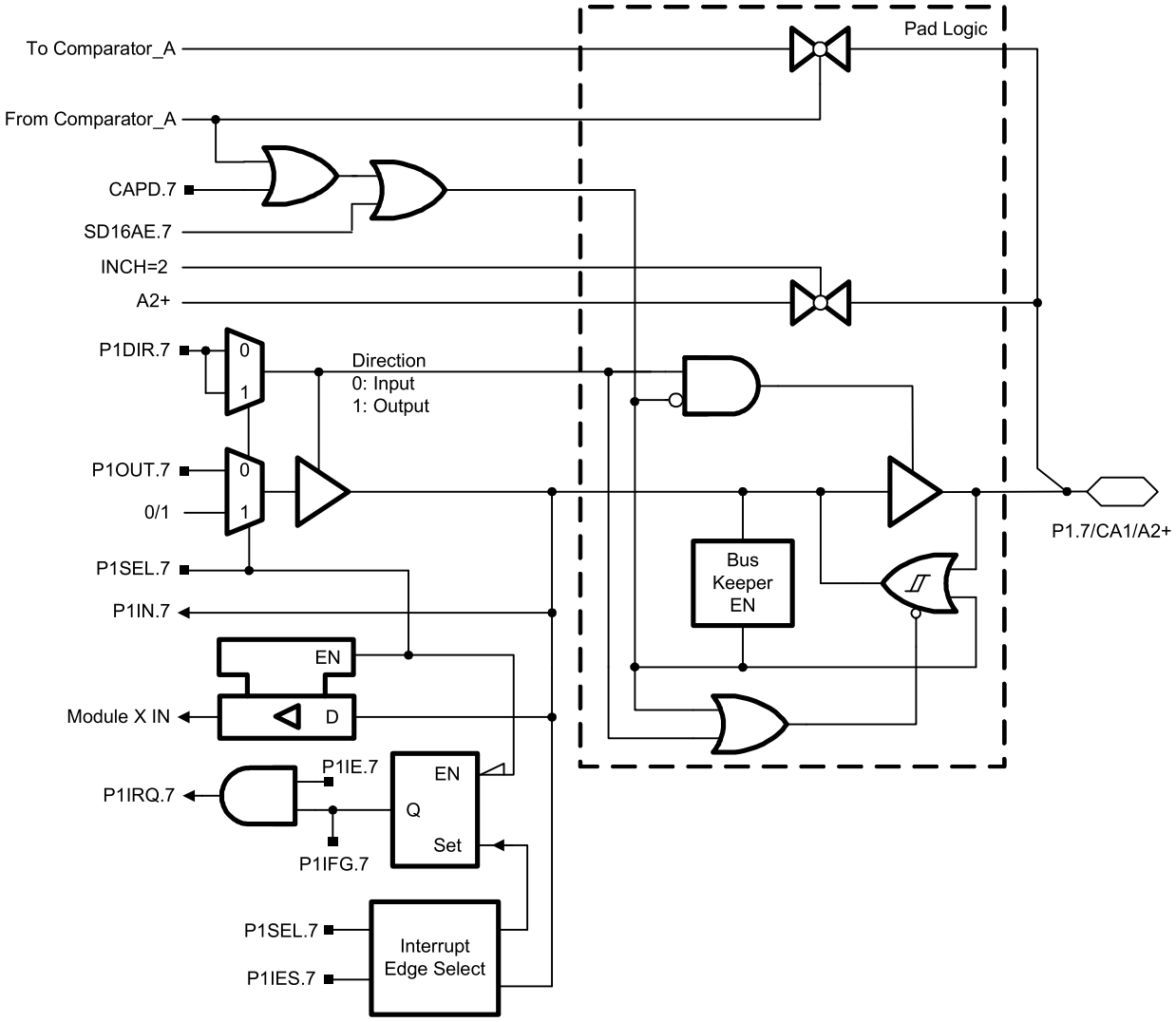


Table 6-16. Port P1 (P1.7) Pin Functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)			
			P1DIR.x	P1SEL.x	P1SEL2.x = 0 CAPD.x	P1SEL2.x = 0 SD16AE.x
P1.7/CA1/A2+	7	P1.x (I/O)	I: 0, O: 1	0	0	0
		CA1	x	x	1 or selected	x
		A2+	x	x	x	1

(1) x = don't care

6.10.9 Port P2, P2.0 and P2.1, Input/Output With Schmitt Trigger

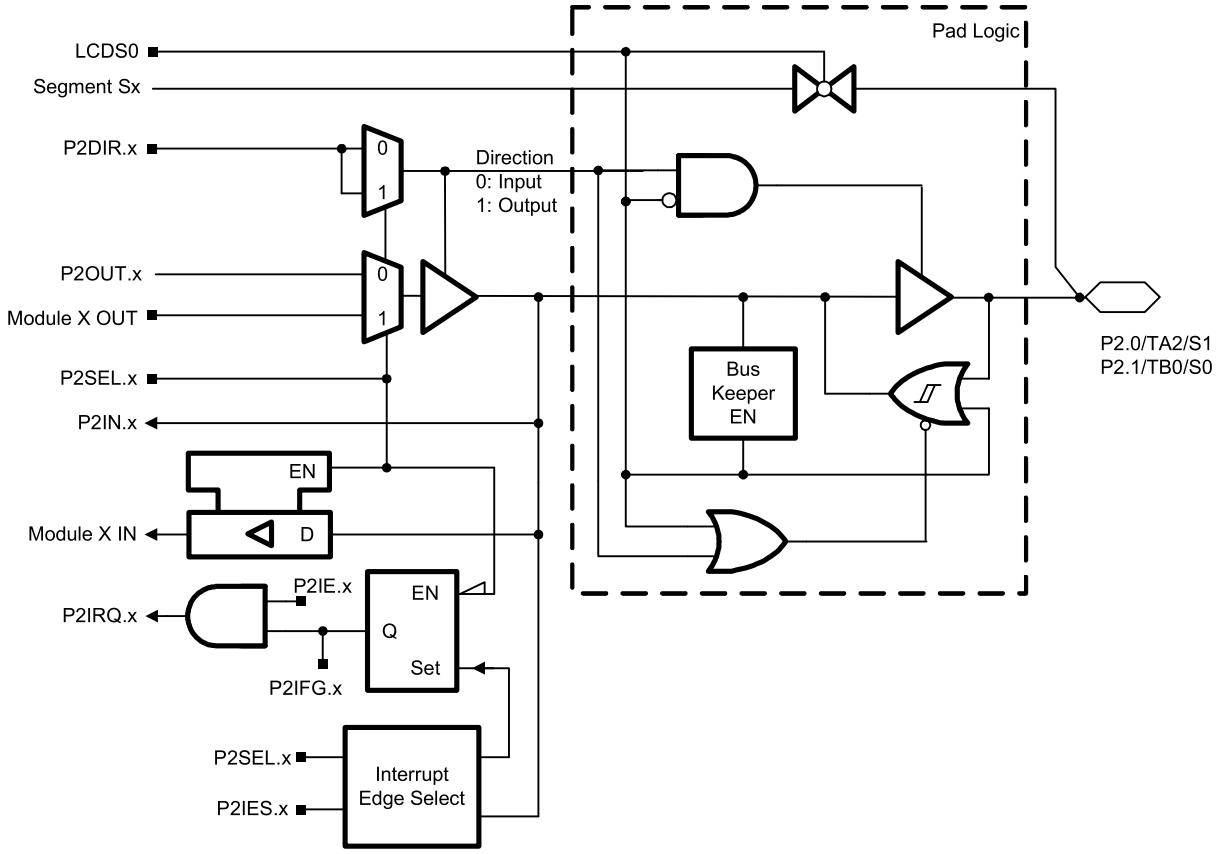


Table 6-17. Port P2 (P2.0 and P2.1) Pin Functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)		
			P2DIR.x	P2SEL.x	LCDS0
P2.0/TA2/S1	0	P2.x (I/O)	I: 0, O: 1	0	0
		Timer_A3.CCI2A	0	1	0
		Timer_A3.TA2	1	1	0
		S1	x	x	1
P2.1/TB0/S0	1	P2.x (I/O)	I: 0, O: 1	0	0
		Timer_B3.CCI0A	0	1	0
		Timer_B3.TB0	1	1	0
		S0	x	x	1

(1) x = don't care

6.10.10 Port P2, P2.2 and P2.3, Input/Output With Schmitt Trigger

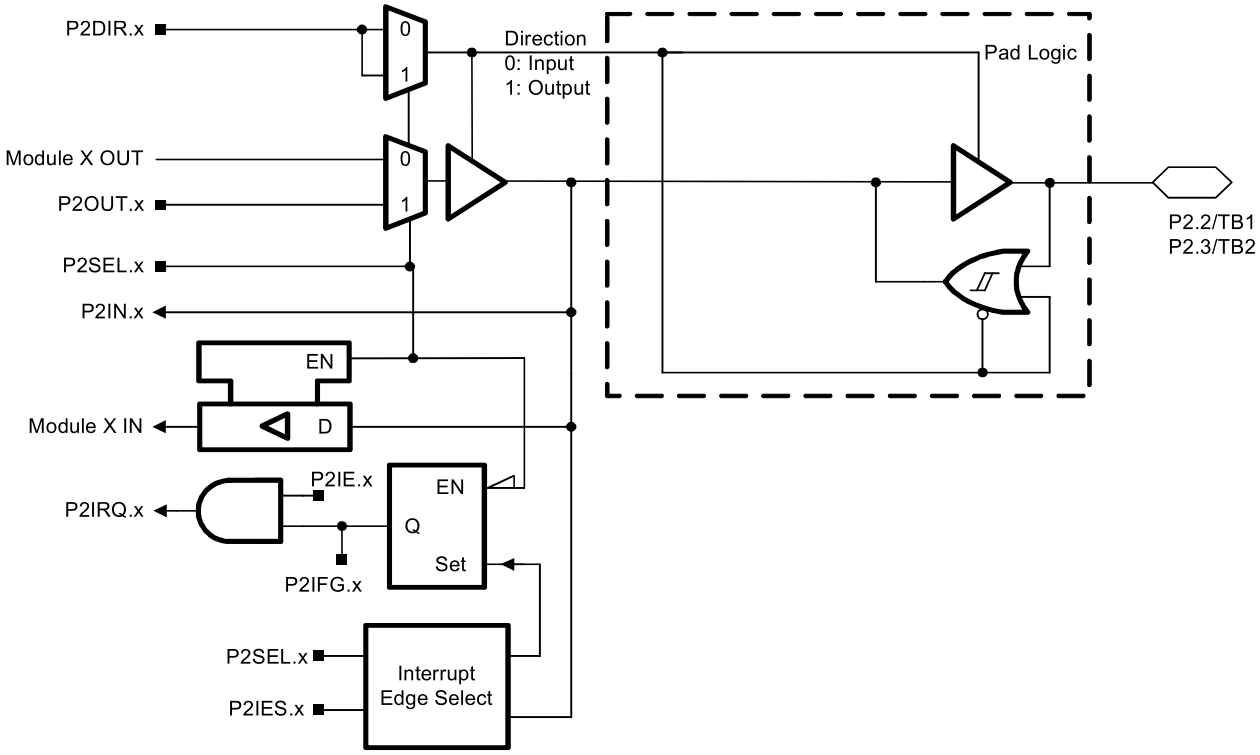


Table 6-18. Port P2 (P2.2 and P2.3) Pin Functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.2/TB1	2	P2.x (I/O)	I: 0, O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P2.3/TB2	3	P2.x (I/O)	I: 0, O: 1	0
		Timer_B3.CCI2A	0	1
		TimerB3.TB2	1	1

6.10.11 Port P2, P2.4 and P2.5, Input/Output With Schmitt Trigger

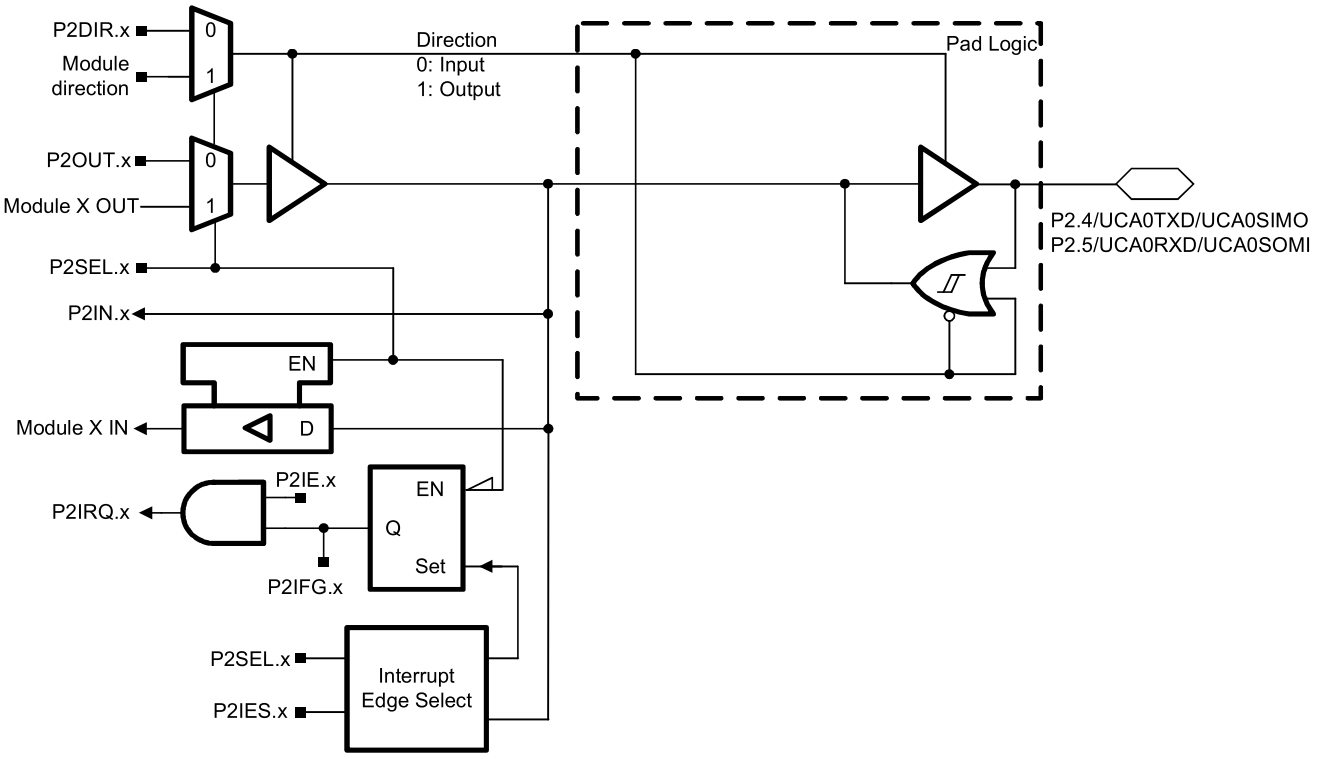


Table 6-19. Port P2 (P2.4 and P2.5) Pin Functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P2DIR.x	P2SEL.x
P2.4/UCA0TXD/UCA0SIMO	4	P2.x (I/O)	I: 0, O: 1	0
		UCA0TXD/UCA0SIMO(2)	x	1
P2.5/UCA0RXD/UCA0SOMI	5	P2.x (I/O)	I: 0, O: 1	0
		UCA0RXD/UCA0SOMI(2)	x	1

(1) x = don't care
(2) The pin direction is controlled by the USCI module.

6.10.12 Port P2, P2.6 and P2.7, Input/Output With Schmitt Trigger

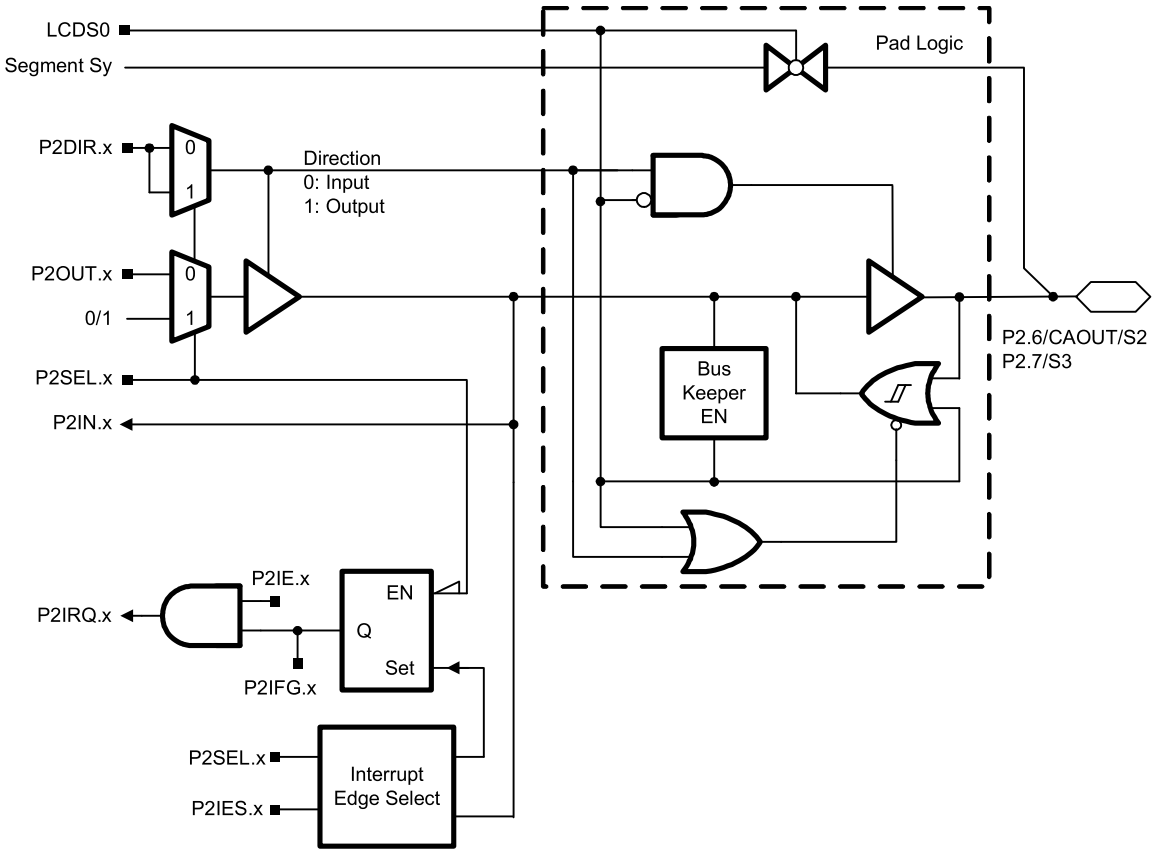


Table 6-20. Port P2 (P2.6 and P2.7) Pin Functions

PIN NAME (P2.X)	X		CONTROL BITS / SIGNALS[1]		
		FUNCTION	P2DIR.x	P2SEL.x	LCDS0
P2.6/CAOUT/S2	6	P2.x (I/O)	I: 0, O: 1	0	0
		CAOUT	1	1	0
		S2	x	x	1
P2.7/S3	7	P2.x (I/O)	I: 0, O: 1	0	0
		Vss	1	1	0
		S3	x	x	1

(1) x = don't care

6.10.13 Port P3, P3.0 and P3.3, Input/Output With Schmitt Trigger

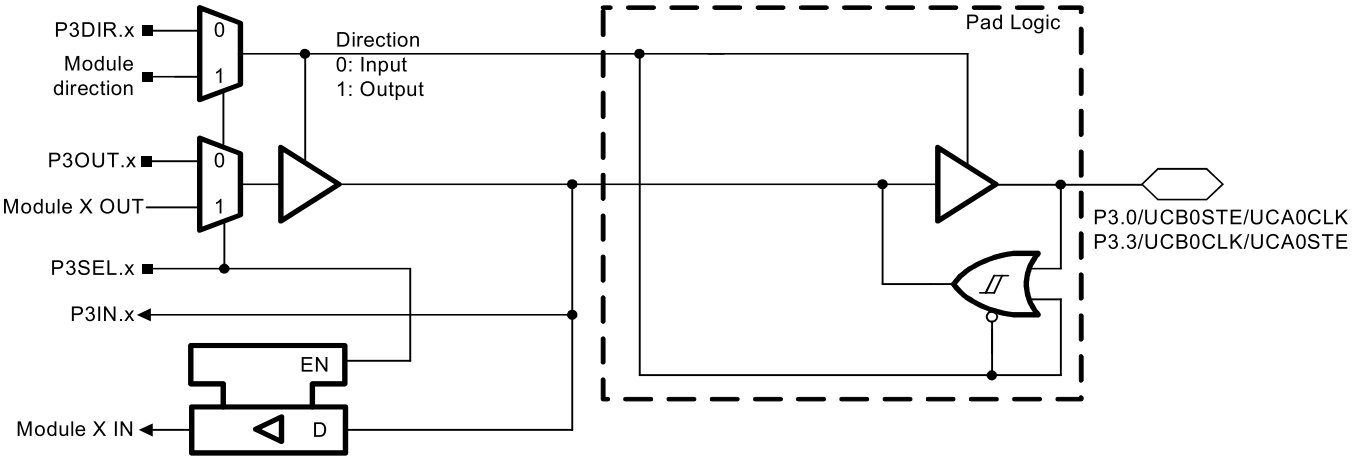


Table 6-21. Port P3 (P3.0 and P3.3) Pin Functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/UCA0CLK	0	P3.x (I/O)	I: 0, O: 1	0
		UCB0STE/UCA0CLK(2)	x	1
P3.3/UCB0CLK/UCA0STE	3	P3.x (I/O)	I: 0, O: 1	0
		UCB0CLK/UCA0STE(2)	x	1

(1) x = don't care
(2) The pin direction is controlled by the USCI module.

6.10.14 Port P3, P3.1 and P3.2, Input/Output With Schmitt Trigger

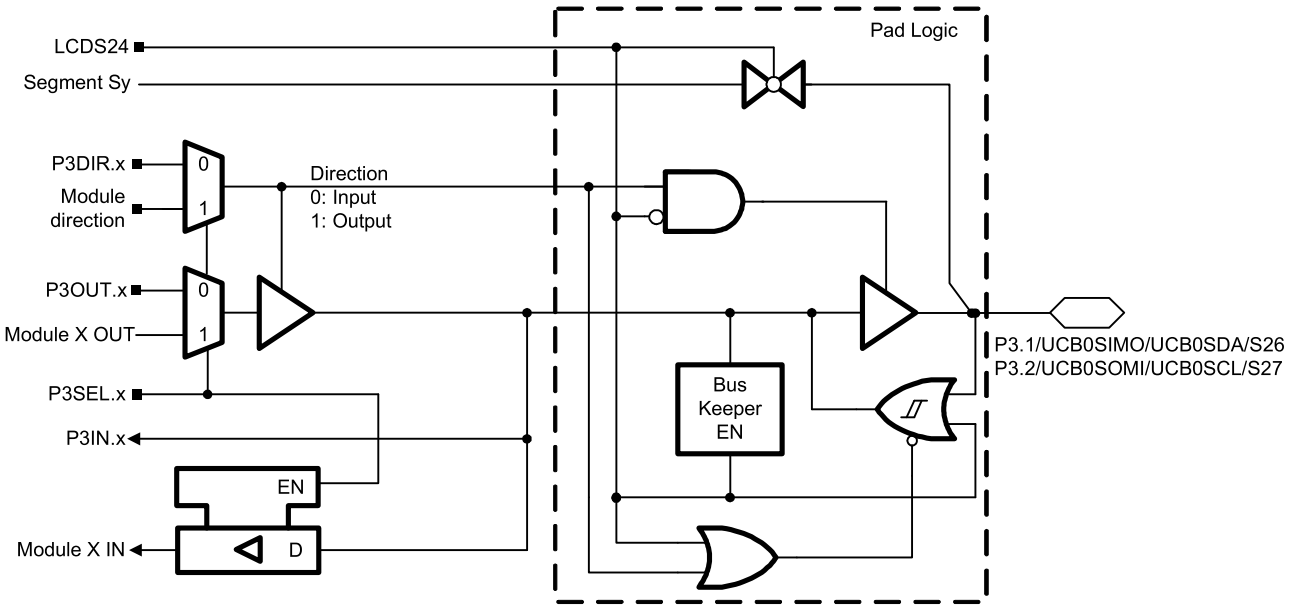


Table 6-22. Port P3 (P3.1 and P3.2) Pin Functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)		
			P3DIR.x	P3SEL.x	LCDS24
P3.1/UCB0SIMO/UCB0SDA/S26	1	P3.x (I/O)	I: 0, O: 1	0	0
		UCB0SIMO/UCB0SDA(2)(3)	x	1	0
		S26	x	x	1
P3.2/UCB00SOMI/UCB0SCL/S27	2	P3.x (I/O)	I: 0, O: 1	0	0
		UCB0SOMI/UCB0SCL(2)(3)	x	1	0
		S27	x	x	1

(1) x = don't care
(2) The pin direction is controlled by the USCI module.
(3) In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.

6.10.15 Port P3, P3.4 to P3.7, Input/Output With Schmitt Trigger

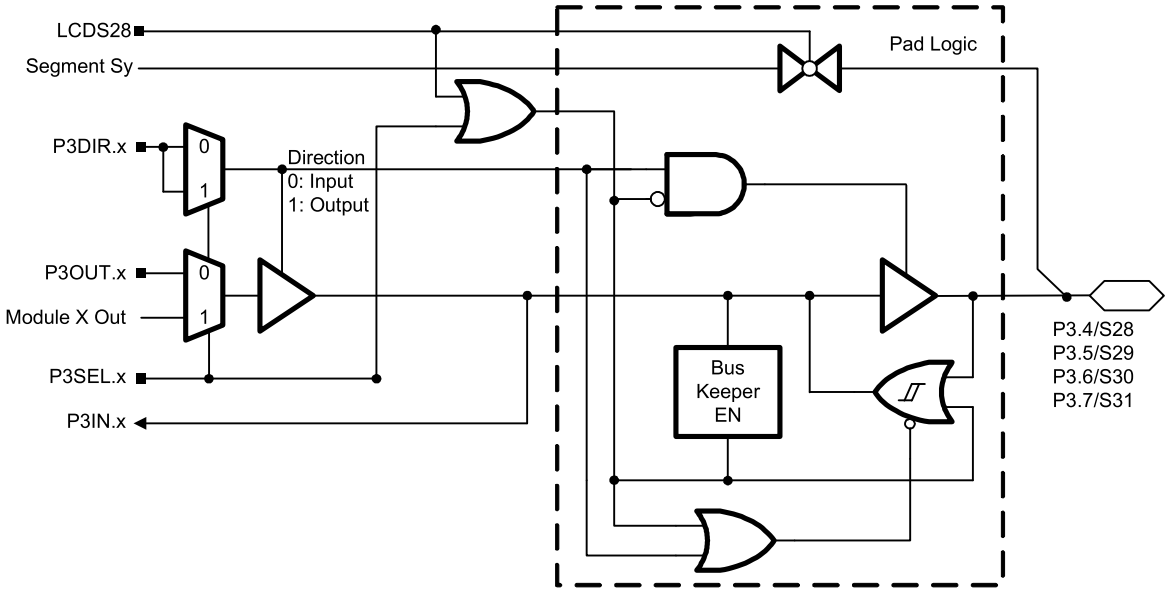


Table 6-23. Port P3 (P3.4 to P3.7) Pin Functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P3DIR.x	P3SEL.x	LCDS28
P3.4/S28	4	P3.x (I/O)	I: 0, O: 1	0	0
		S28	x	x	1
P3.5/S29	5	P3.x (I/O)	I: 0, O: 1	0	0
		S29	x	x	1
P3.6/S30	6	P3.x (I/O)	I: 0, O: 1	0	0
		S30	x	x	1
P3.7/S31	7	P3.x (I/O)	I: 0, O: 1	0	0
		S31	x	x	1

(1) x: Don't care

6.10.16 Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

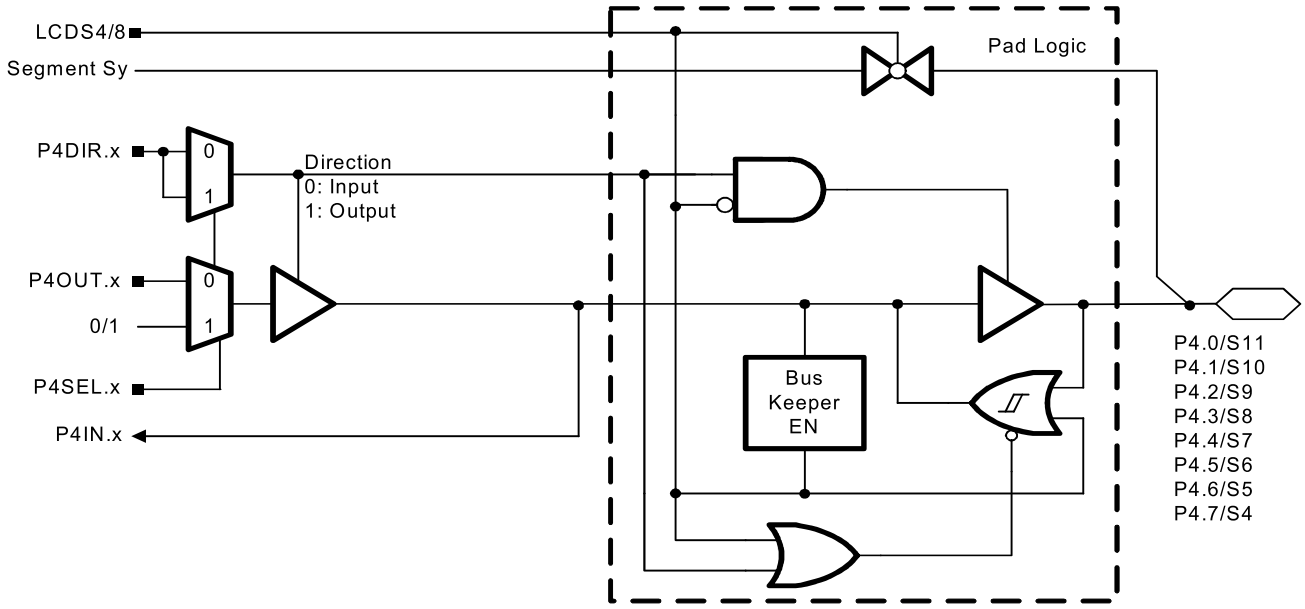


Table 6-24. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P4DIR.x	P4SEL.x	LCDS4/8
P4.0/S11	0	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S11	x	x	1 (LCDS8)
P4.1/S10	1	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S10	x	x	1 (LCDS8)
P4.2/S9	2	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S9	x	x	1 (LCDS8)
P4.3/S8	3	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S8	x	x	1 (LCDS8)
P4.4/S7	4	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S7	x	x	1 (LCDS4)
P4.5/S6	5	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S6	x	x	1 (LCDS4)
P4.6/S5	6	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S5	x	x	1 (LCDS4)
P4.7/S4	7	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S4	x	x	1 (LCDS4)

(1) x = don't care

6.10.17 Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

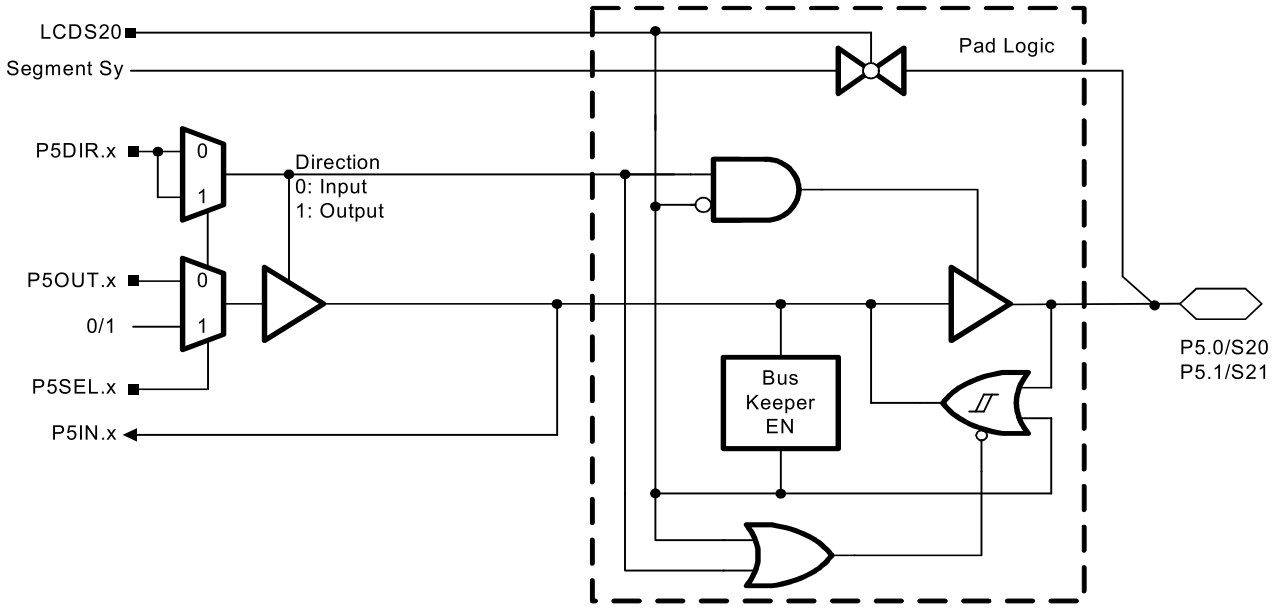


Table 6-25. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS (1)		
			P5DIR.x	P5SEL.x	LCDS20
P5.0/S20	0	P5.x (I/O)	I: 0, O: 1	0	0
		S20	x	x	1
P5.1/S21	1	P5.x (I/O)	I: 0, O: 1	0	0
		S21	x	x	1

(1) x = don't care

6.10.18 Port P5, P5.2 to P5.7, Input/Output With Schmitt Trigger

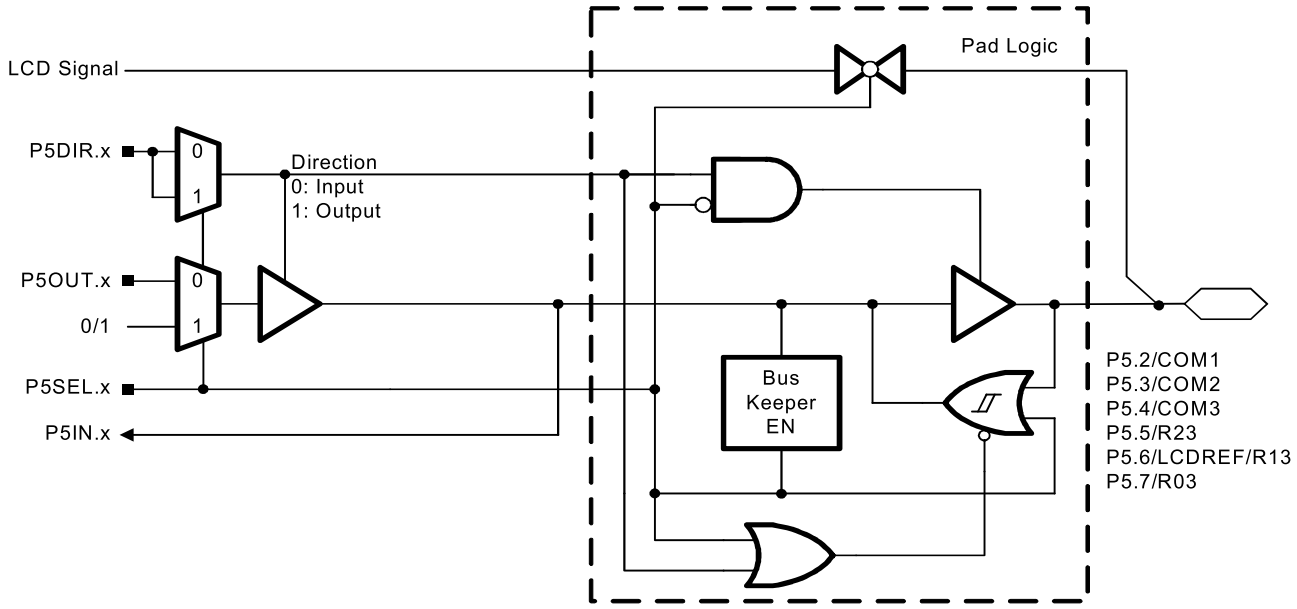


Table 6-26. Port P5 (P5.2 to P5.7) Pin Functions

PIN NAME (P5.X)	X	FUNCTION	CONTOL BITS / SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.x (I/O)	I: 0, O: 1	0
		COM1	x	1
P5.3/COM2	3	P5.x (I/O)	I: 0, O: 1	0
		COM2	x	1
P5.4/COM3	4	P5.x (I/O)	I: 0, O: 1	0
		COM3	x	1
P5.5/R23	5	P5.x (I/O)	I: 0, O: 1	0
		R23	x	1
P5.6/LCDREF/R13	6	P5.x (I/O)	I: 0, O: 1	0
		R13 or LCDREF	x	1
P5.7/R03	7	P5.x (I/O)	I: 0, O: 1	0
		R03	x	1

(1) x = don't care

6.10.19 Port P6, P6.0 and P6.3, Input/Output With Schmitt Trigger

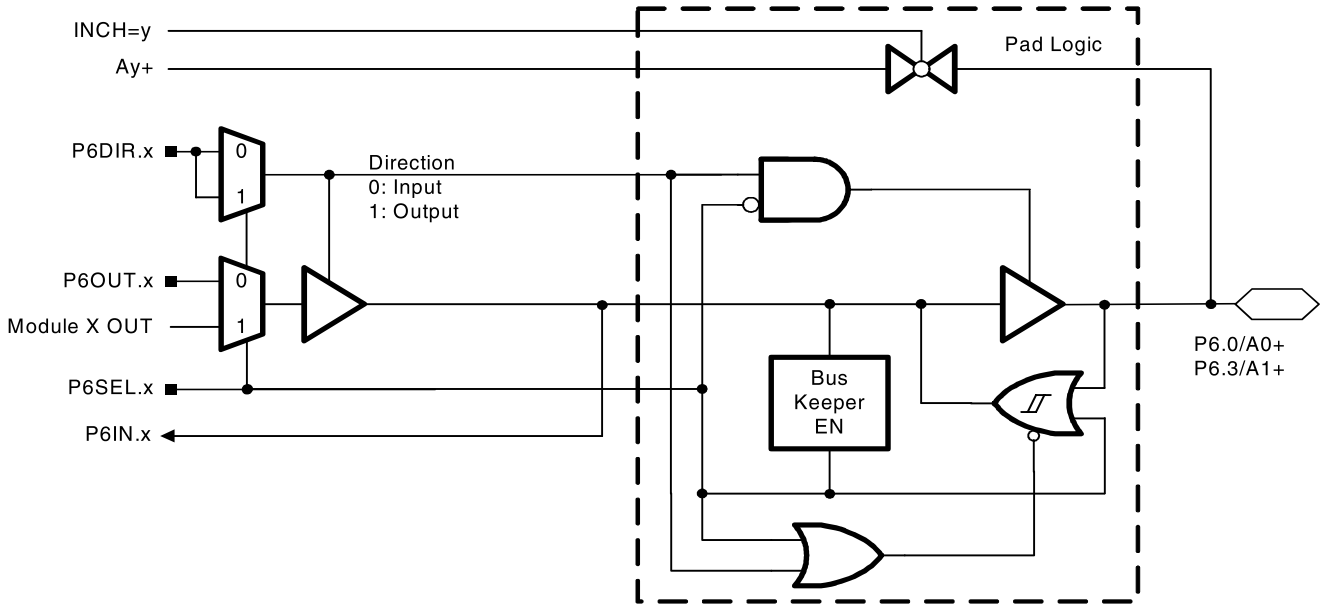


Table 6-27. Port P6 (P6.0 and P6.3) Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P6DIR.x	P6SEL.x
P6.0/A0+	0	P6.x (I/O)	I: 0, O: 1	0
		A0+	x	1
P6.3/A1+	3	P6.x (I/O)	I: 0, O: 1	0
		A1+	x	1

(1) x = don't care

6.10.20 Port P6, P6.1 and P6.4, Input/Output With Schmitt Trigger

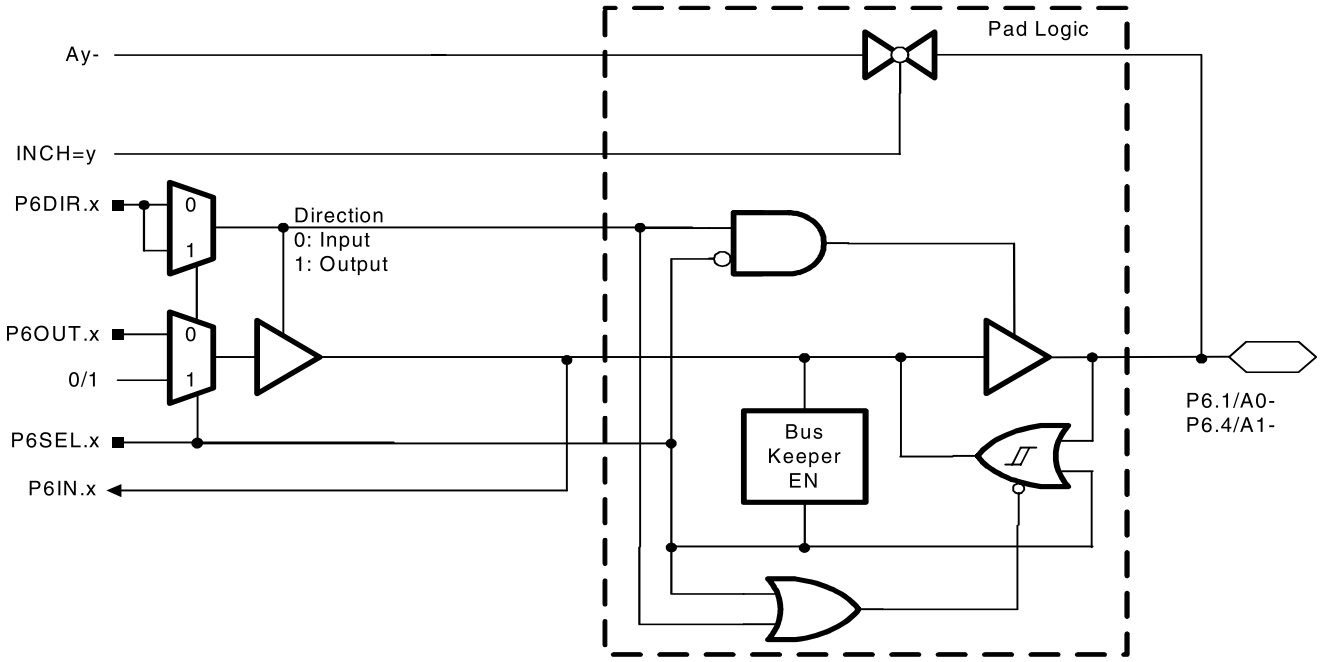


Table 6-28. Port P6 (P6.1 and P6.4) Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P6DIR.x	P6SEL.x
P6.1/A0-	1	P6.x (I/O)	I: 0, O: 1	0
		A0-	x	1
P6.4/A1-	4	P6.x (I/O)	I: 0, O: 1	0
		A1-	x	1

(1) x = don't care

6.10.21 Port P6, P6.2, P6.5, and P6.6, Input/Output With Schmitt Trigger

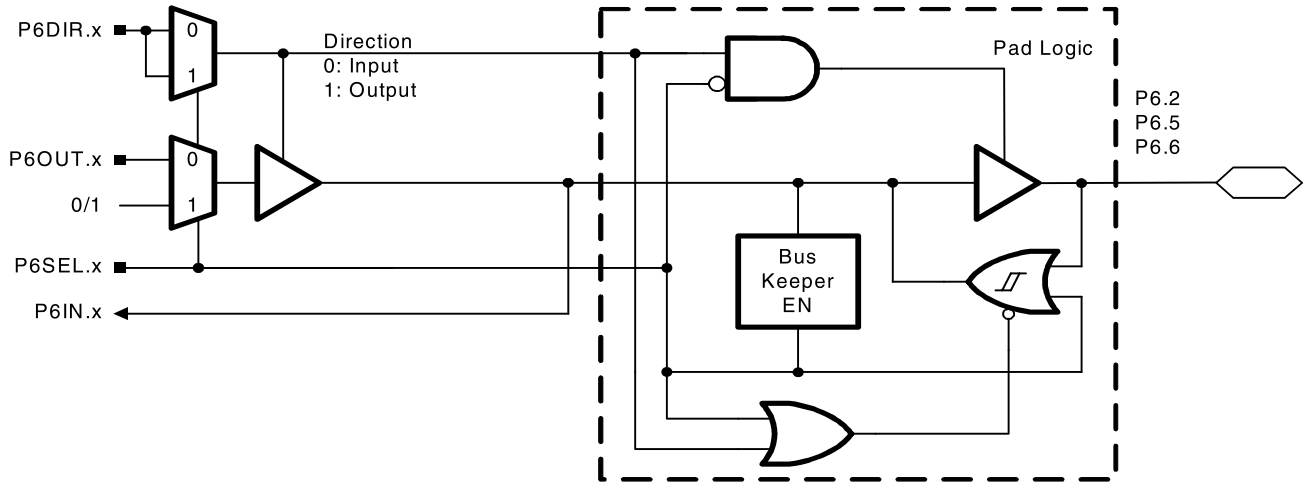


Table 6-29. Port P6 (P6.2, P6.5, and P6.6) Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P6DIR.x	P6SEL.x
P6.2	2	P6.x (I/O)	I: 0, O: 1	0
P6.5	5	P6.x (I/O)	I: 0, O: 1	0
P6.6	6	P6.x (I/O)	I: 0, O: 1	0

(1) x = don't care

6.10.22 Port P6, P6.7, Input/Output With Schmitt Trigger

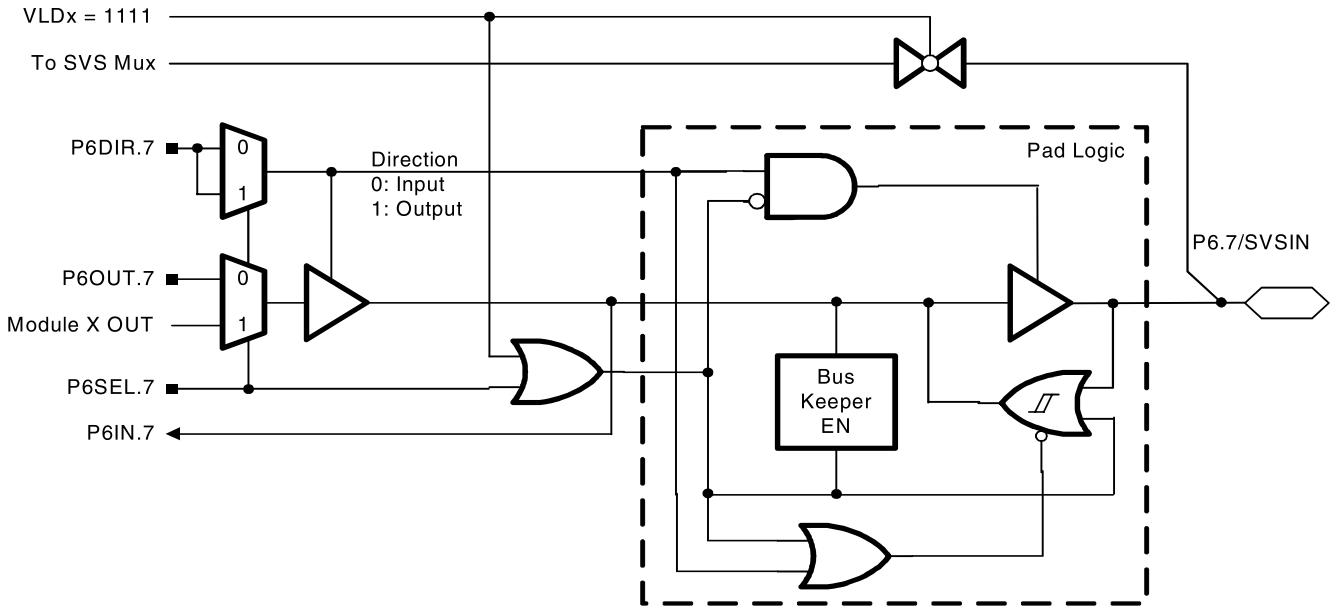


Table 6-30. Port P6 (P6.7) Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P6DIR.x	P6SEL.x	VLDx
P6.7/SVSIN	7	P6.x (I/O)	I: 0, O: 1	0	x
		SVSIN	x	1	1111

6.10.23 Segment Pin Schematic: Sx, Dedicated Segment Pins

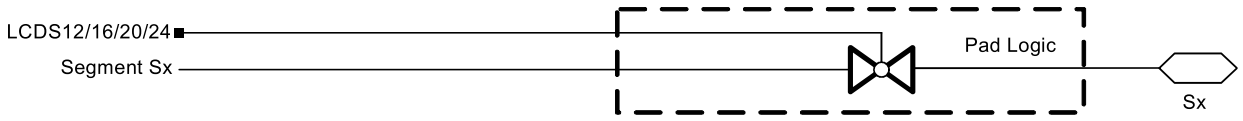


Table 6-31. Sx Pin Functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS
			LCDSy
Sx	12	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	13	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	14	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	15	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	16	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	17	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	18	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	19	Sx	1 (LCDS16)
		3-state	0 (LCDS16)
Sx	22	Sx	1 (LCDS20)
		3-state	0 (LCDS20)
Sx	23	Sx	1 (LCDS20)
		3-state	0 (LCDS20)
Sx	24	Sx	1 (LCDS24)
		3-state	0 (LCDS24)
Sx	25	Sx	1 (LCDS24)
		3-state	0 (LCDS24)

6.10.24 Segment Pin Schematic: COM0, Dedicated COM0 Pin

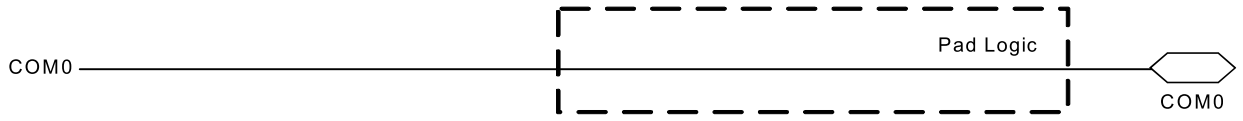
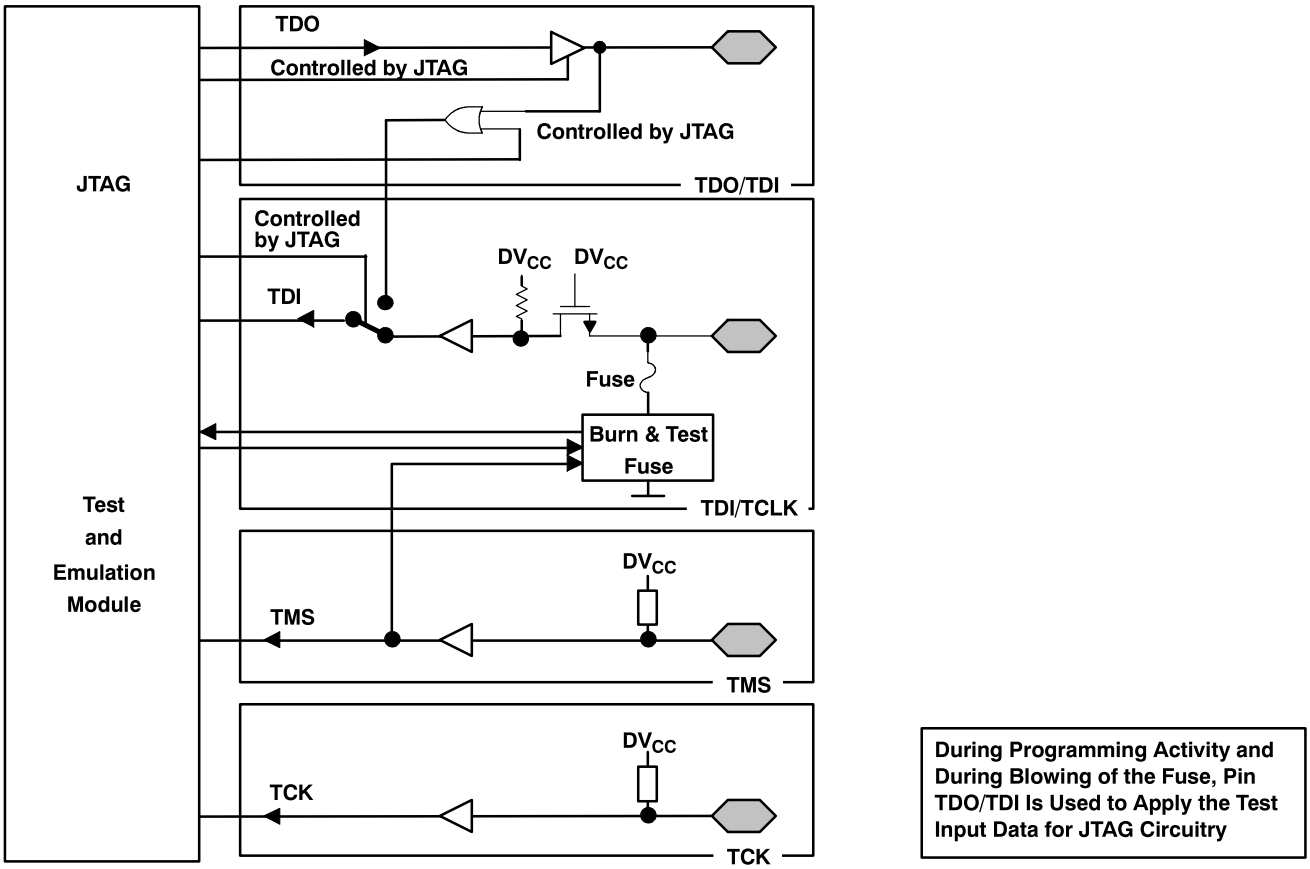


Table 6-32. COM0 Pin Functions

PIN NAME	X	FUNCTION
COM0	--	COM0

6.10.25 JTAG Pins TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt Trigger or Output



6.10.26 JTAG Fuse Check Mode

For details on the JTAG fuse check mode, see the MSP430x4xx Family User's Guide.

7 Device and Documentation Support

7.1 Device Support

7.1.1 Getting Started and Next Steps

For more information on the MSP430F4x family of devices and the tools and libraries that are available to help with your development, visit the MSP430™ ultra-low-power sensing & measurement MCUs overview page.

7.1.2 Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

7.1.2.1 Recommended Hardware Options

7.1.2.1.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

Package	Target Board and Programmer Bundle	Target Board Only
80-pin LQFP (PN)	MSP-FET430U80	MSP-TS430PN80

7.1.2.1.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

7.1.2.1.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

7.1.2.1.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

Part Number	PC Port	Features	Provider
MSP-GANG	Serial and USB	Program up to eight devices at a time. Works with PC or standalone.	Texas Instruments

7.1.2.2 Recommended Software Options

7.1.2.2.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

7.1.2.2.2 MSP430Ware

MSP430Ware is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.

7.1.2.2.3 Command-Line Programmer

MSP430 Flasher is an open-source shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 microcontroller without the need for an IDE.

7.1.3 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

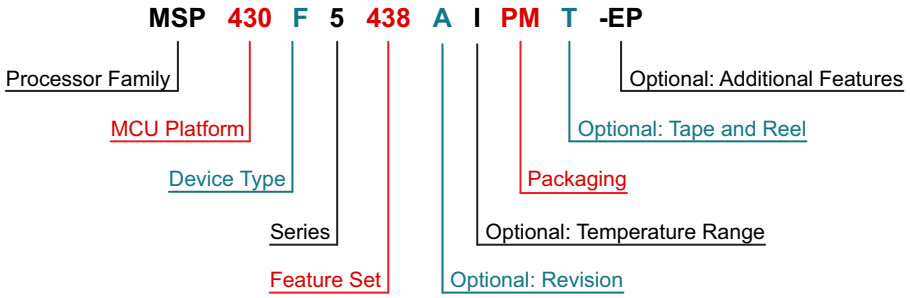
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 7-1 provides a legend for reading the complete device name.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory	**Specialized Application** AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series
Feature Set	Various levels of integration within a series	
Optional: Revision	Updated version of the base part number	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced product (–40°C to 105°C) -HT = Extreme temperature parts (–55°C to 150°C) -Q1 = Automotive Q100 qualified	

Figure 7-1. Device Nomenclature

7.2 Documentation Support

The following documents describe the MSP430F47x devices. Copies of these documents are available on the Internet at www.ti.com.

SLAU056 ***MSP430F4xx Family User's Guide.*** Detailed information on the modules and peripherals available in this device family.

SLAZ243 ***MSP430F479 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.

SLAZ240 ***MSP430F478 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.

SLAZ239 ***MSP430F477 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.

7.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 7-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430F479	Click here	Click here	Click here	Click here	Click here
MSP430F478	Click here	Click here	Click here	Click here	Click here
MSP430F477	Click here	Click here	Click here	Click here	Click here

7.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.5 Trademarks

MicroStar Junior, MSP430, Code Composer Studio, TI E2E are trademarks of Texas Instruments.

7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F477IPN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F477	Samples
MSP430F477IPNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F477	Samples
MSP430F477IZCA	ACTIVE	NFBGA	ZCA	113	260	RoHS & Green	Call TI	Call TI	-40 to 85	F477	Samples
MSP430F477IZCAR	ACTIVE	NFBGA	ZCA	113	2500	RoHS & Green	Call TI	Call TI	-40 to 85	F477	Samples
MSP430F478IPN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F478	Samples
MSP430F478IPNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F478	Samples
MSP430F478IZCA	ACTIVE	NFBGA	ZCA	113	2500	RoHS & Green	Call TI	Call TI	-40 to 85	F478	Samples
MSP430F478IZCAR	ACTIVE	NFBGA	ZCA	113	2500	RoHS & Green	Call TI	Call TI	-40 to 85	F478	Samples
MSP430F479IPN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F479	Samples
MSP430F479IPNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F479	Samples
MSP430F479IZCAR	ACTIVE	NFBGA	ZCA	113	2500	RoHS & Green	Call TI	Call TI	-40 to 85	F479	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

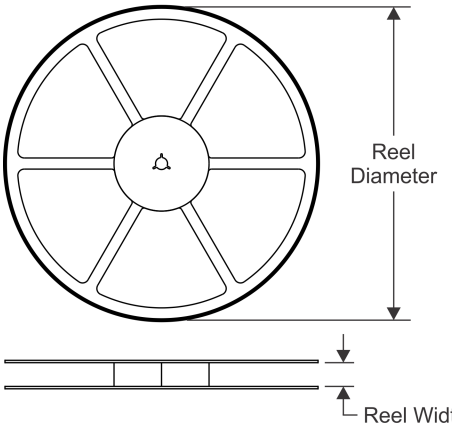
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

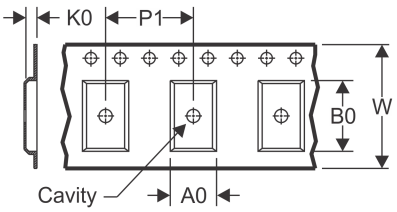
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

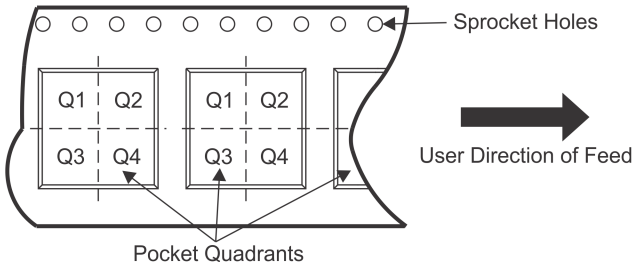


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

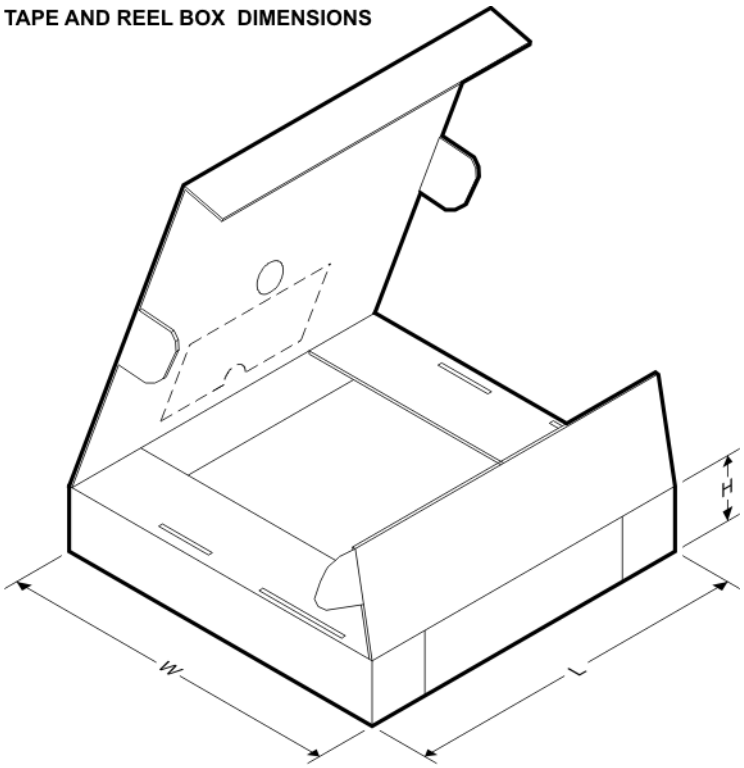
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F477IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F478IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F479IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

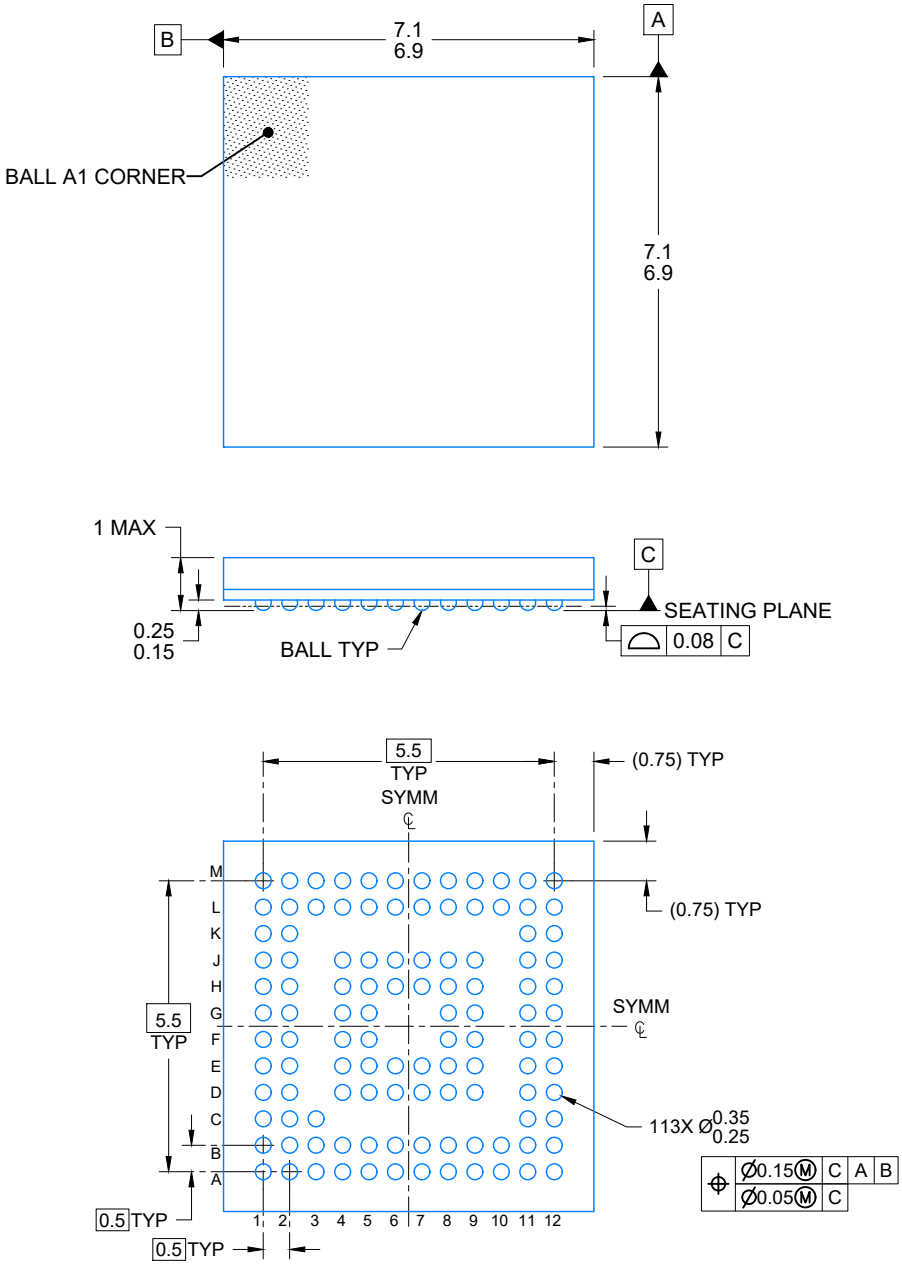
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F477IZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F478IZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F479IZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0

PACKAGE OUTLINE

ZCA0113A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



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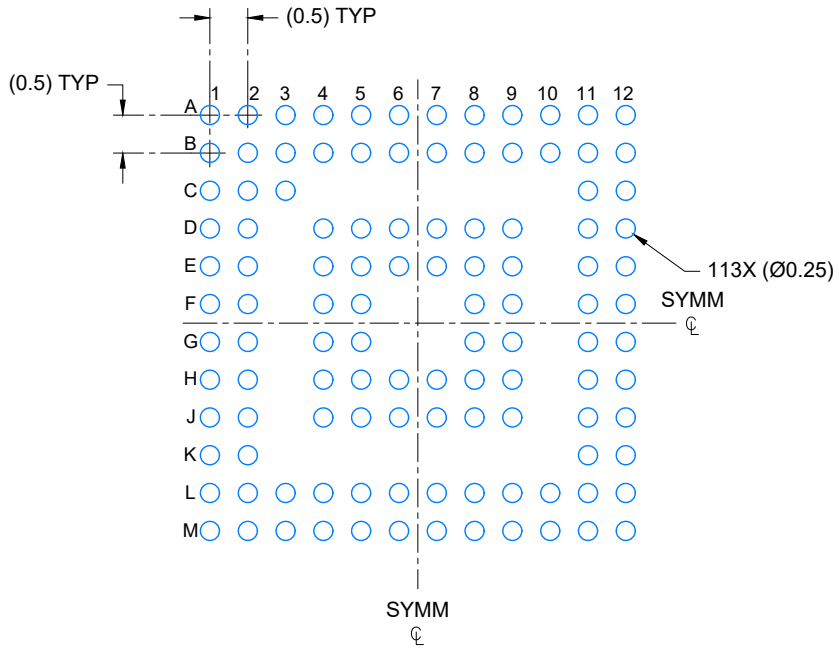
NOTES:

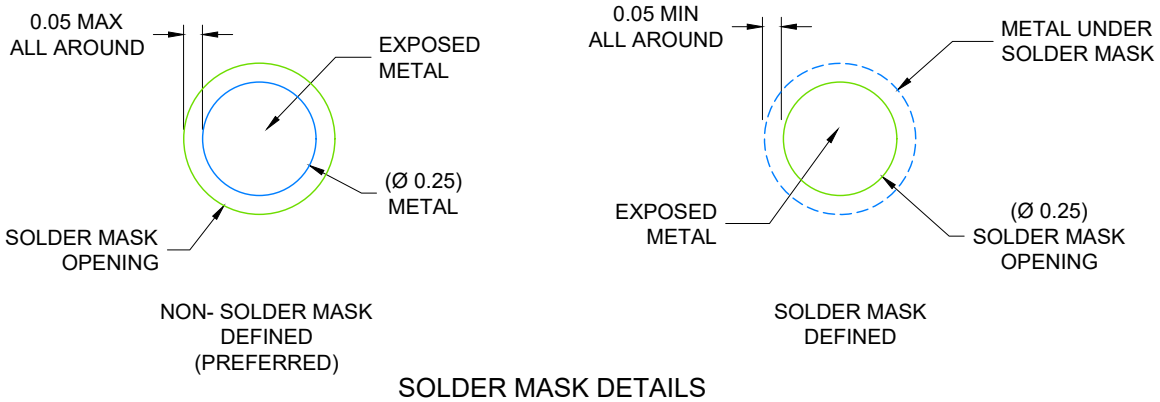
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 10X



SOLDER MASK DETAILS

NOT TO SCALE

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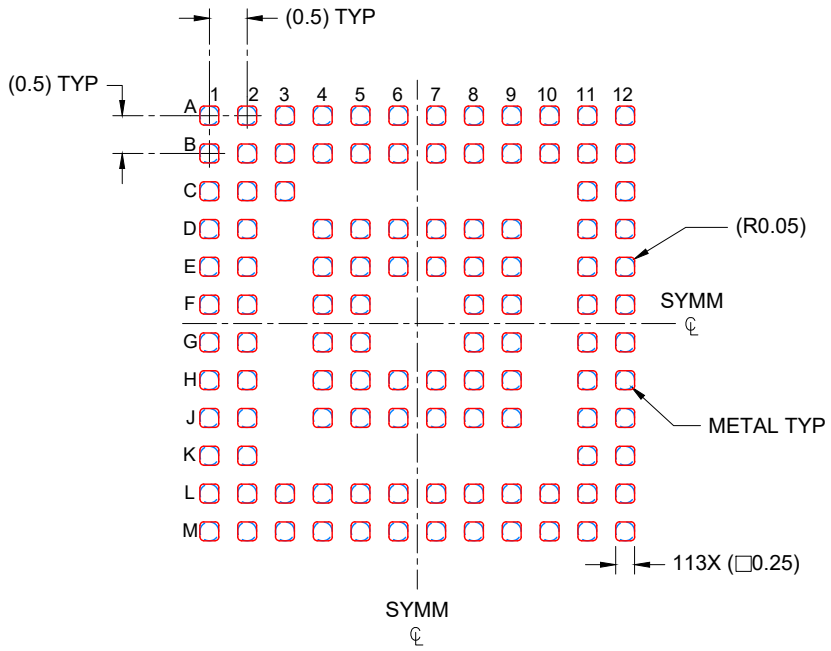
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

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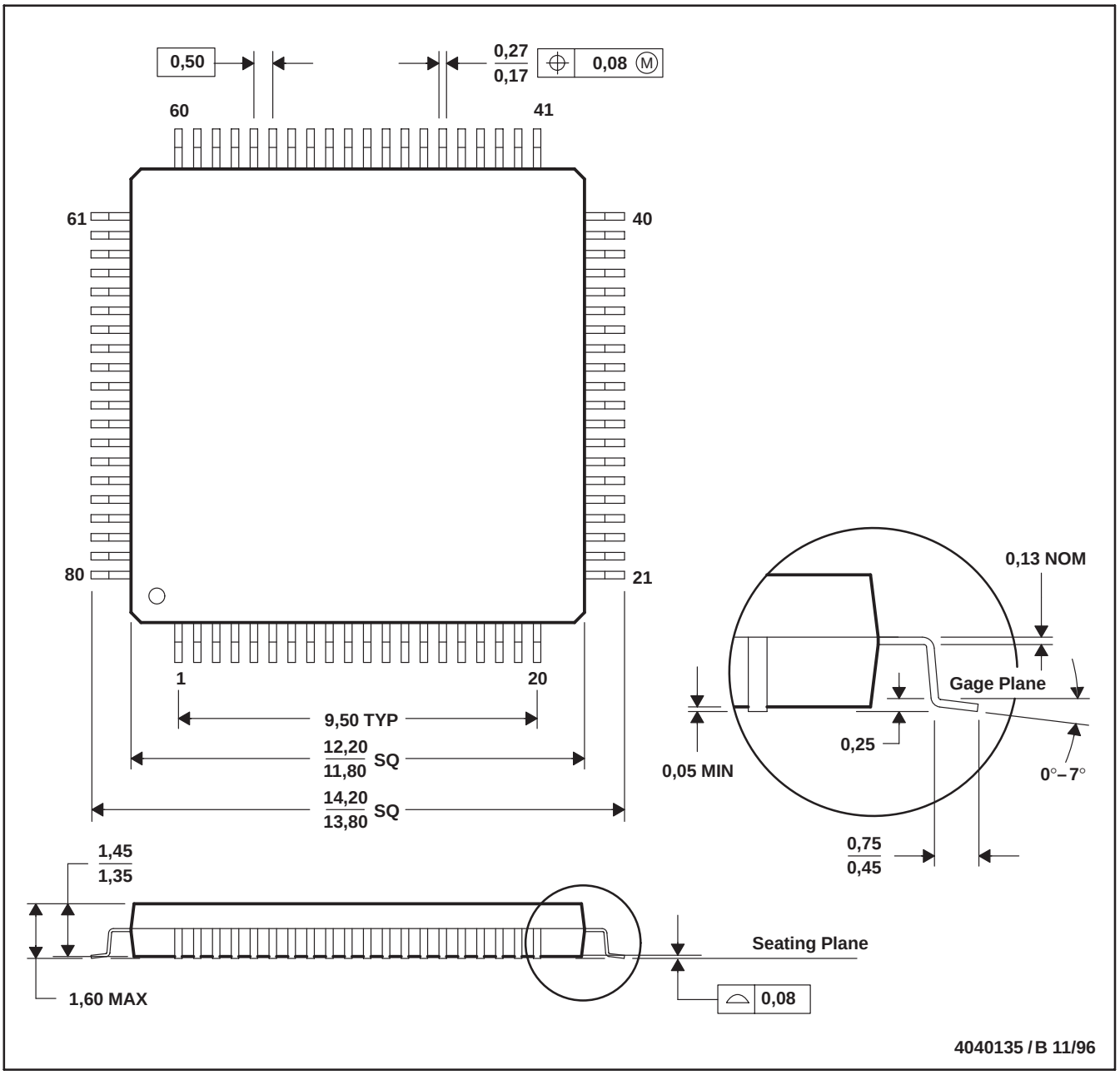
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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