SN74LVC2G241 带三态输出的双路缓冲器和驱动器

1 特性

- 采用德州仪器 (TI) 的 NanoFree™封装
- 支持 5V V_{CC} 运行
- 输入电压高达 5.5V
- 电压为 3.3V 时，t_{pd} 最大值为 4.1ns
- 低功耗，I_{CC} 最大值为 10μA
- 电压为 3.3V 时，输出驱动为 ±24mA
- V_{CC} = 3.3 V，T_A = 25°C 时，V_{OLP}（输出地弹反射）
  典型值小于 0.8V
- V_{CC} = 3.3V，T_A = 25°C 时，V_{OHV}（输出 V_{OH} 下冲）
  典型值大于 2V
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 可用于下行转换器，将最高 5.5V 的输入电压下行转换
  至 V_{CC} 电平
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)

2 应用

- AV 接收机
- 蓝光播放器和家庭影院
- DVD 录像机和播放器
- 台式机或笔记本电脑
- 数字音频广播或互联网广播播放器
- 数码摄像机 (DVC)
- 嵌入式计算机
- GPS：个人导航设备
- 移动互联网设备
- 网络投影仪前端
- 便携式媒体播放器
- 专业音频混合器

3 说明

此双路缓冲器和线路驱动器适用于 1.65V 至 5.5V V_{CC} 运行环境。

SN74LVC2G241 器件设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发射器的性能和密度。

NanoFree 封装技术是 IC 封装概念的一项重大突破，它将硅晶片用作封装。

SN74LVC2G241 器件被组织为两个具有独立输出使能（$1\overline{OE}$，2OE）输入的 1 位线路驱动器。当 $1\overline{OE}$ 为低电平，2OE 为高电平时，该器件将来自 A 输入的数据传递到 Y 输出。当 $1\overline{OE}$ 为高电平，2OE 为低电平时，输出处于高阻抗状态。

为了确保在上电或断电期间处于高阻抗状态，应通过上拉电阻器将 $\overline{OE}$ 接到 V_{CC}，通过下拉电阻器将 OE 接地；此电阻器的最小值由驱动器的灌电流能力或拉电流能力决定。

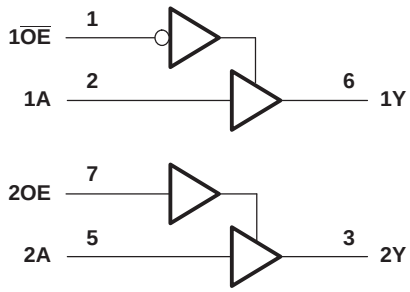
该器件完全 适用于 使用 I_{off} 的不完全断电应用。I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74LVC2G241DCT	SM8 (8)	2.95mm × 2.80mm
SN74LVC2G241DCU	VSOOP (8)	2.30mm × 2.00mm
SN74LVC2G241YZP	DSBGA (8)	1.91mm × 0.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

逻辑图（正逻辑）



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics ... 6
6.7 Operating Characteristics ... 6
6.8 Typical Characteristic ... 6
7 Parameter Measurement Information ... 7
8 Detailed Description ... 8
8.1 Overview ... 8
8.2 Functional Block Diagram ... 8
8.3 Feature Description ... 8
8.4 Device Functional Modes ... 8
9 Application and Implementation ... 9
9.1 Application Information ... 9
9.2 Typical Application ... 9
10 Power Supply Recommendations ... 10
11 Layout ... 10
11.1 Layout Guidelines ... 10
11.2 Layout Example ... 10
12 器件和文档支持 ... 11
12.1 文档支持 ... 11
12.2 社区资源 ... 11
12.3 商标 ... 11
12.4 静电放电警告 ... 11
12.5 术语表 ... 11
13 机械、封装和可订购信息 ... 11

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision O (December 2015) to Revision P — **Page**

- Changed Electrical Characteristics table format ... 5
- Changed Switching Characteristics tables format. ... 6

Changes from Revision N (November 2013) to Revision O — **Page**

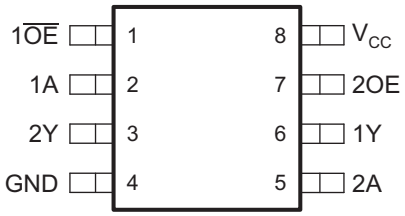
- 添加了*应用*部分、*器件信息表*、*ESD 额定值*表、*热性能信息表*、*典型特性*、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1

Changes from Revision M (February 2007) to Revision N — **Page**

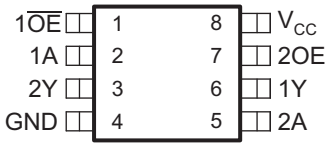
- 将文档更新为新的 TI 数据表格式。 ... 1
- 删除了订购信息表。 ... 1
- 更新了 特性 中删除了“最高传播延迟低于 1.5ns”。 ... 1
- Updated operating temperature range. ... 4

5 Pin Configuration and Functions

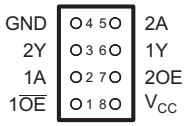
DCT Package
8-Pin SM8
Top View



DCU Package
8-Pin VSSOP
Top View



YZP Package
8-Pin DSBGA
Bottom View



Pin Functions[1][2]

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	Input
$\overline{1OE}$	1	I	Output enable (Active low)
1Y	6	O	Output
2A	5	I	Input
2Y	3	O	Output
2OE	7	I	Output enable (Active high)
GND	4	—	Ground
V_{CC}	8	—	Power pin

(1) N.C. – No internal connection
(2) See for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Recommended Operating Conditions(1) (continued)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC2G241			UNIT
		DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, T_A = –40ºC to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	–40°C to 85°C			–40°C to 125°C (Recommended)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –4 mA	1.65 V	1.2			1.2			
		I_{OH} = –8 mA	2.3 V	1.9			1.9			
		I_{OH} = –16 mA	3 V	2.4			2.4			
		I_{OH} = –24 mA		2.3			2.3			
		I_{OH} = –32 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45			0.45	
		I_{OL} = 8 mA	2.3 V			0.3			0.3	
		I_{OL} = 16 mA	3 V			0.4			0.4	
		I_{OL} = 24 mA				0.55			0.55	
		I_{OL} = 32 mA	4.5 V			0.55			0.75	
I_I	A or $\overline{OE}$ inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10			±10	µA
I_{OZ}		V_O = 0 to 5.5 V	3.6 V			10			10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	µA
C_i	Data Inputs	V_I = V_{CC} or GND	3.3 V		3.5					pF
	Control Inputs				4					
C_o		V_O = V_{CC} or GND	3.3 V		6.5					pF

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.3	9.1	1.5	5.5	1.4	4.3	1.0	4.0	ns
t_{en}	$\overline{OE}$	Y	4.0	9.9	1.3	6.6	1.2	4.7	1.1	5.0	ns
t_{dis}	$\overline{OE}$	Y	1.5	11.6	1.0	5.7	1.4	4.6	0.5	4.2	ns

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C (Recommended)								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.3	10.1	1.5	5.6	1.4	5.3	1.0	4.2	ns
t_{en}	$\overline{OE}$	Y	4.0	10.9	1.3	6.6	1.2	5.7	1.2	4.3	ns
t_{dis}	$\overline{OE}$	Y	1.5	12.6	1.0	6.6	1.4	5.6	1.0	3.9	ns

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	V_{CC} = 1.8 V	19	pF
			V_{CC} = 2.5 V	19	
			V_{CC} = 3.3 V	20	
			V_{CC} = 5 V	22	
	Outputs disabled		V_{CC} = 1.8 V	2	pF
			V_{CC} = 2.5 V	2	
			V_{CC} = 3.3 V	2	
			V_{CC} = 5 V	3	

6.8 Typical Characteristic

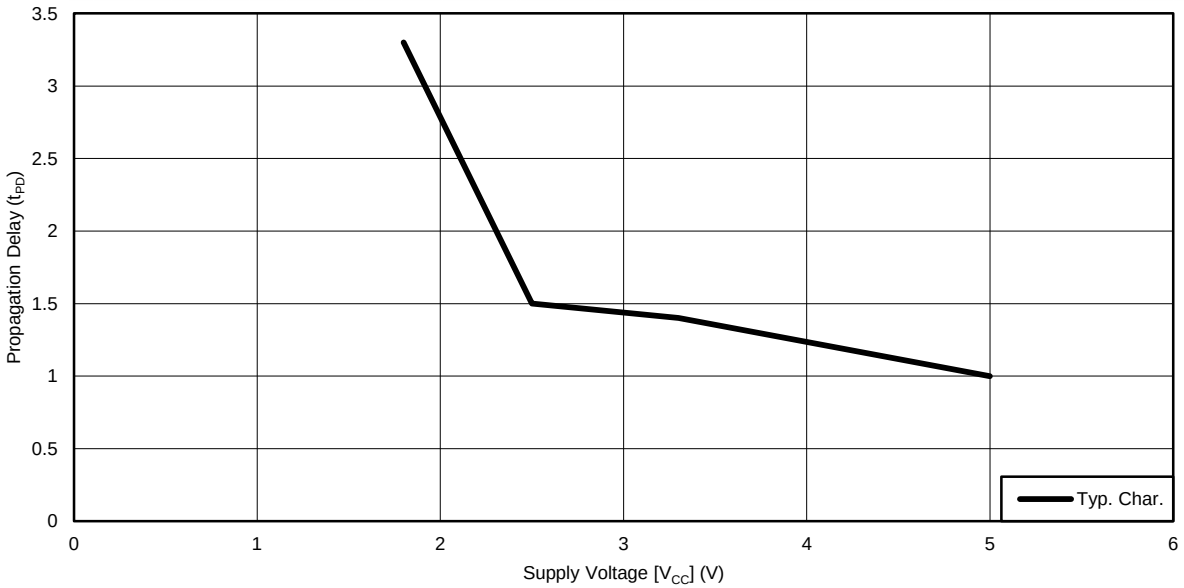
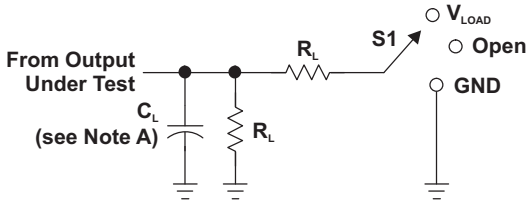


Figure 1. tpd vs Vcc Over Full Temperature Range

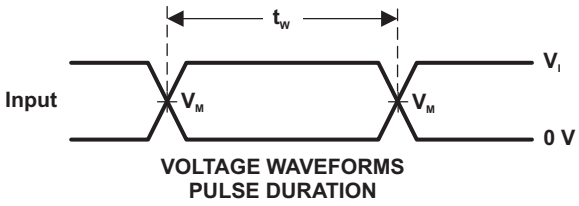
7 Parameter Measurement Information



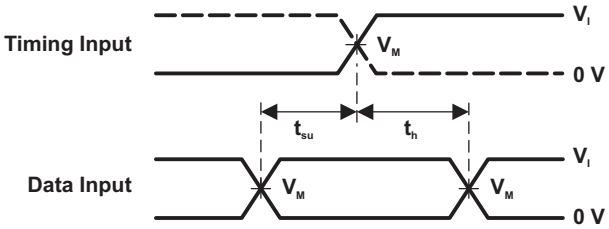
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

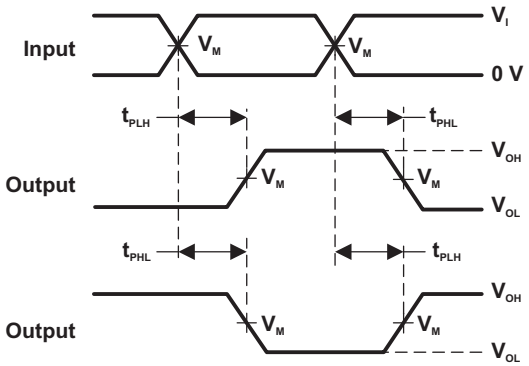
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



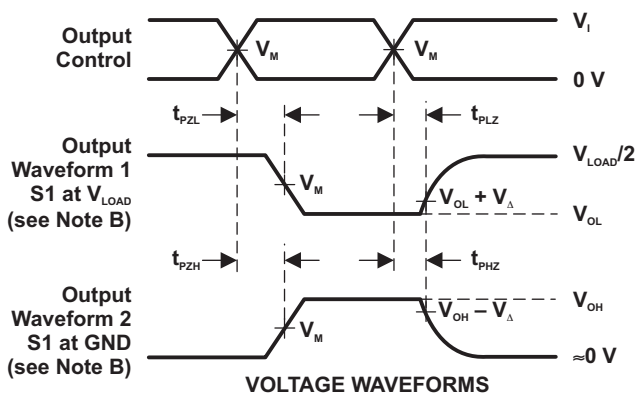
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC2G241 device is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters. The SN74LVC2G241 device is organized as two 1-bit line drivers with separate output-enable ($1\overline{OE}$, 2OE) inputs. When $1\overline{OE}$ is low and 2OE is high, the device passes data from the A inputs to the Y outputs. When $1\overline{OE}$ is high and 2OE is low, the outputs are in the high-impedance state.

The SN74LVC2G241 is also an effective redriver, with a maximum output current drive of 32 mA.

8.2 Functional Block Diagram

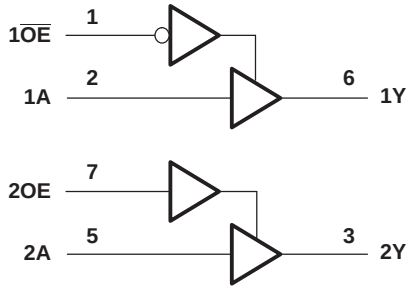


Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.4 Device Functional Modes

Table 1 and Table 2 list the functional modes of the SN74LVC2G241.

Table 1. Gate 1 Functional Table

INPUTS		OUTPUT 1Y
$1\overline{OE}$	1A	
L	H	H
L	L	L
H	X	Z

Table 2. Gate 2 Functional Table

INPUTS		OUTPUT 2Y
2OE	2A	
H	H	H
H	L	L
L	X	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Typical Application shows a simple application where a physical push button is connected to the SN74LVC2G241. The push button is in a physical location far enough away from the processor that the input signal is weak and needs to be redriven. The SN74LVC2G241 acts as a redriver, providing a strong input signal to the processor with as little as 1 ns of propagation delay.

9.2 Typical Application

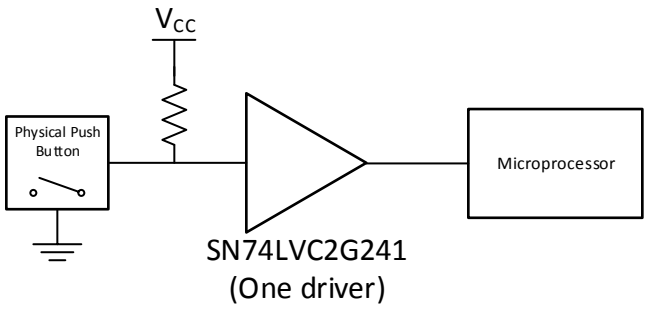


Figure 4. SN74LVC2G241 Application

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in *Recommended Operating Conditions* at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
   - Outputs must not be pulled above V_{CC} during normal operation or 5.5 V in high-z state.

Typical Application (continued)

9.2.3 Application Curve

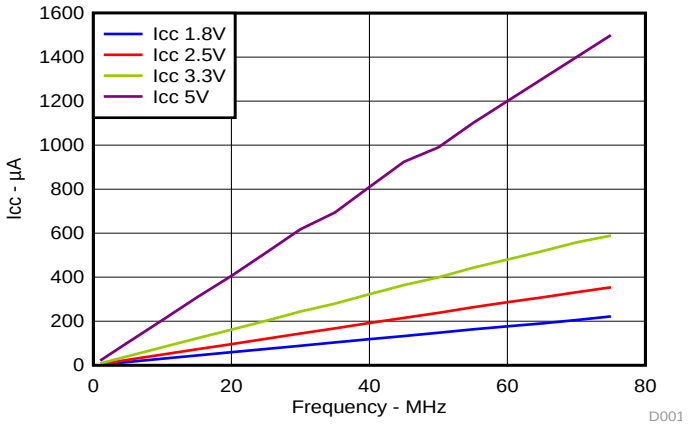


Figure 5. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever make more sense or is more convenient.

11.2 Layout Example

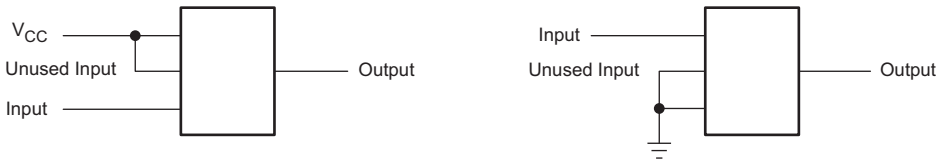


Figure 6. Layout Diagram

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅：

《CMOS 输入缓慢变化或悬空的影响》，SCBA004

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.3 商标

NanoFree, E2E are trademarks of Texas Instruments.
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12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC2G241DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z	Samples
74LVC2G241DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z	Samples
74LVC2G241DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41R	Samples
SN74LVC2G241DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z	Samples
SN74LVC2G241DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)	Samples
SN74LVC2G241DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)	Samples
SN74LVC2G241YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(C2, C27)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

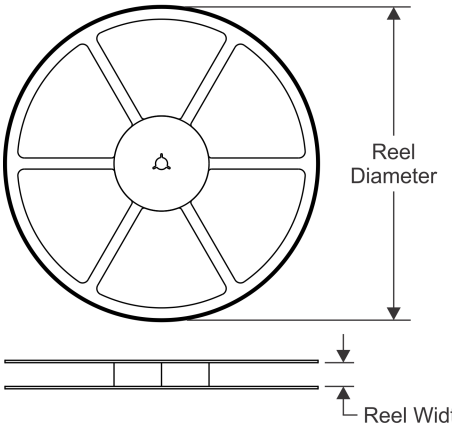
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

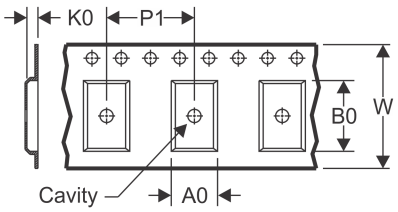
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

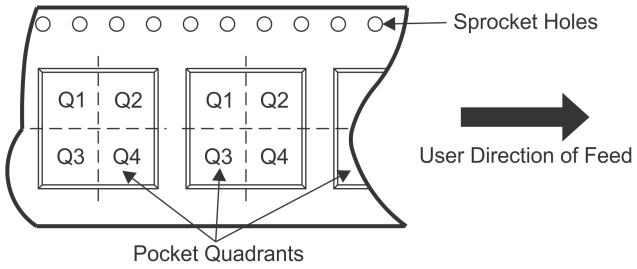


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

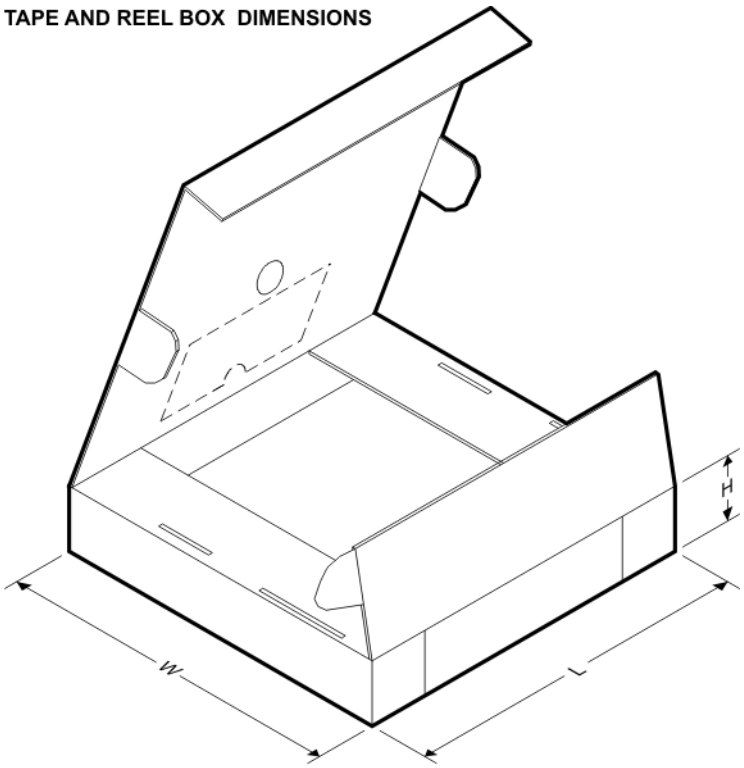
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2G241DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

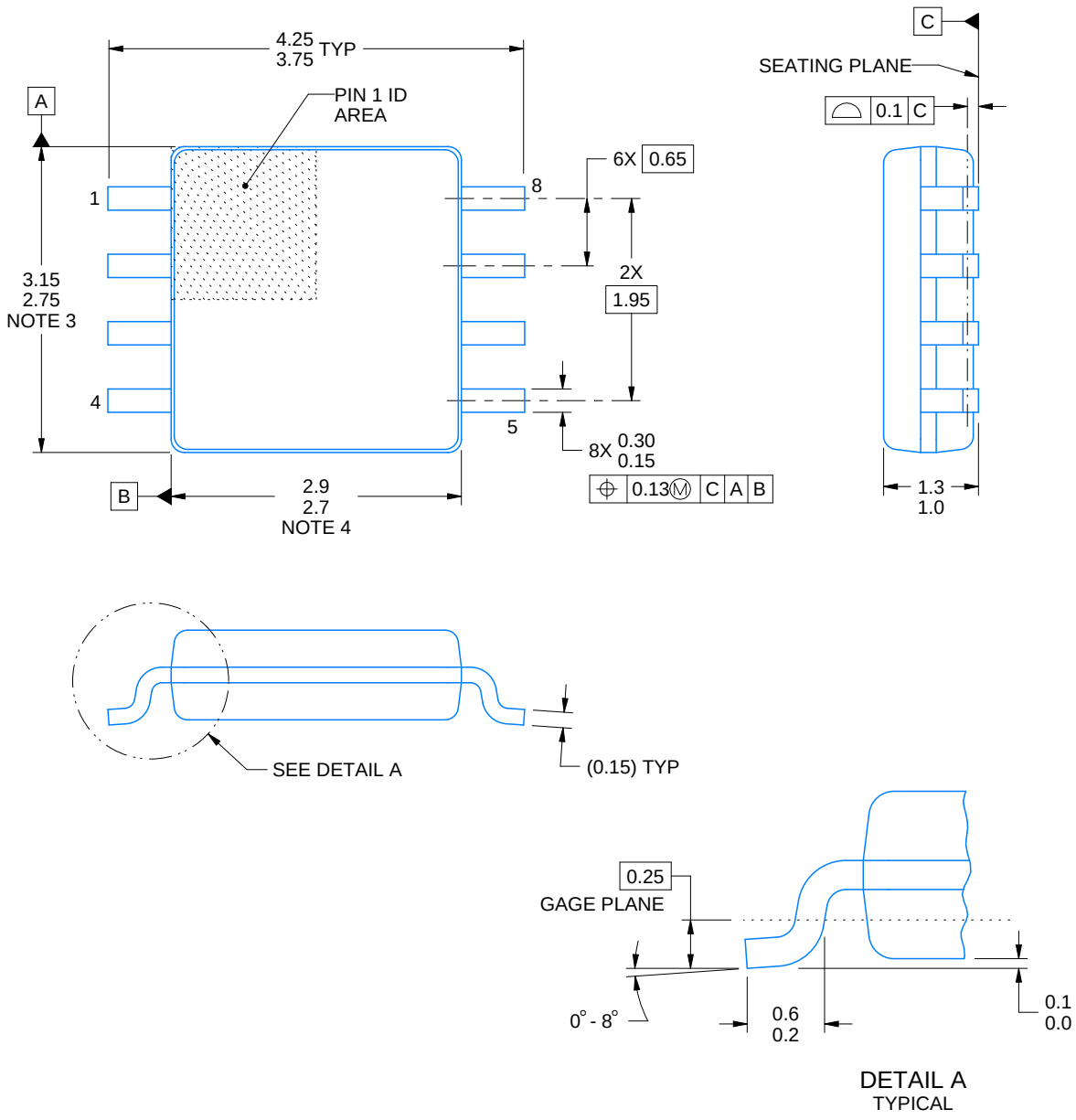
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2G241DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G241DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G241DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G241DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G241YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

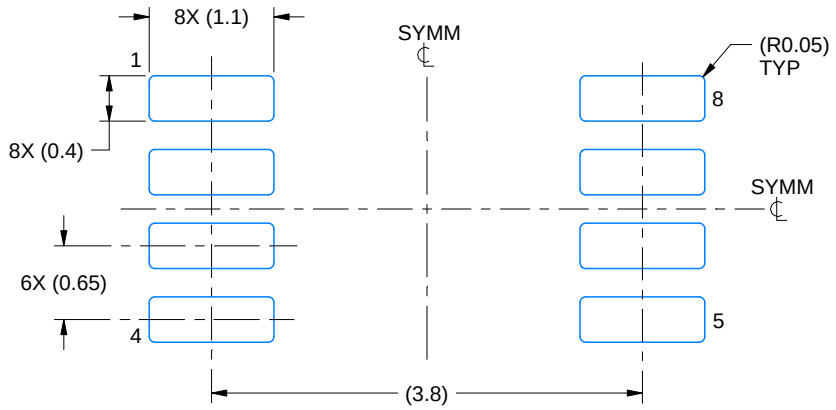
SMALL OUTLINE PACKAGE



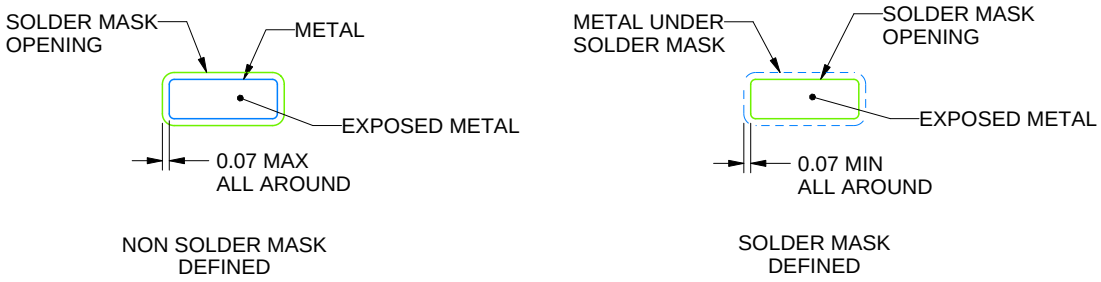
4220784/B 07/2020

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

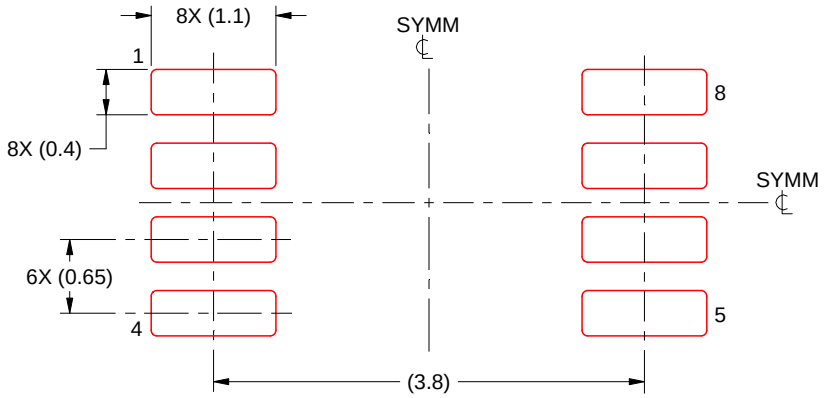


SOLDER MASK DETAILS

4220784/B 07/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/B 07/2020

NOTES: (continued)

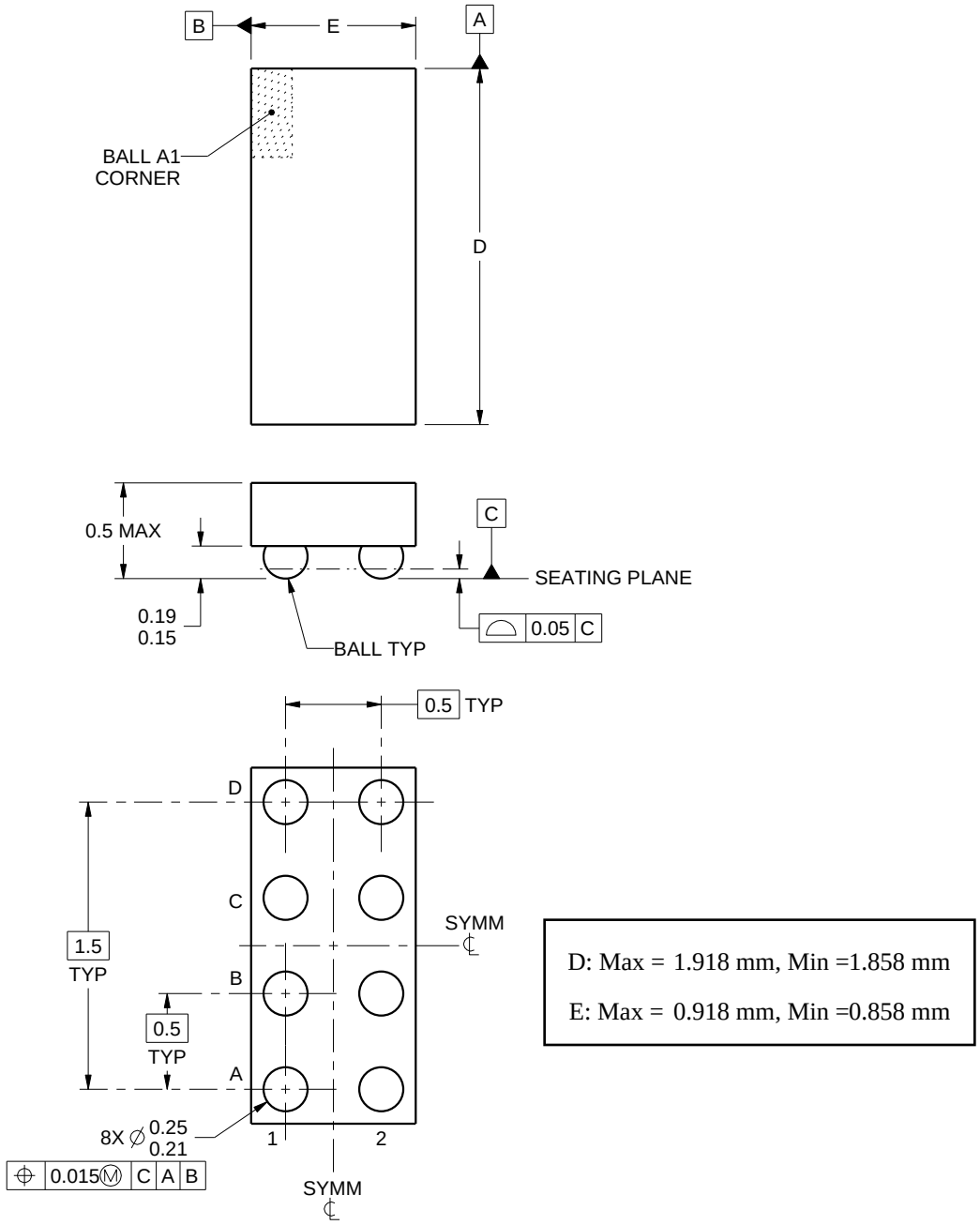
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

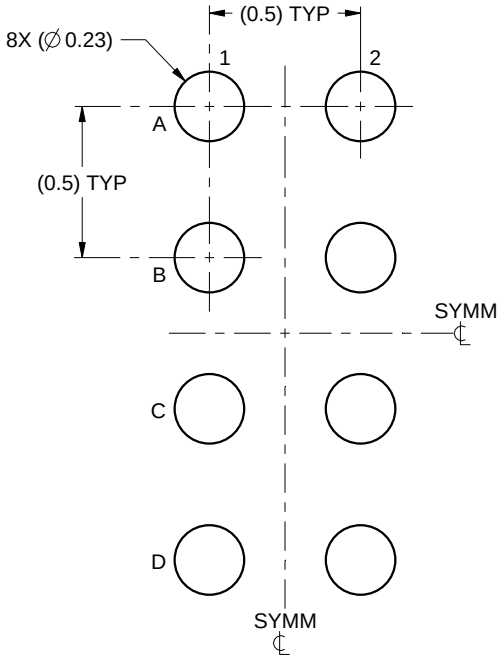
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

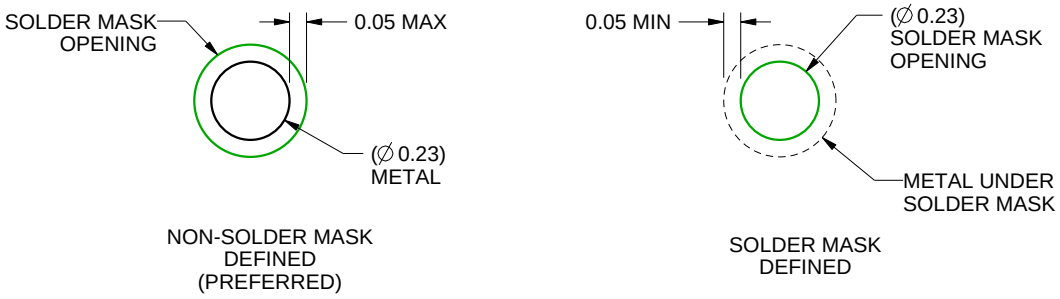


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

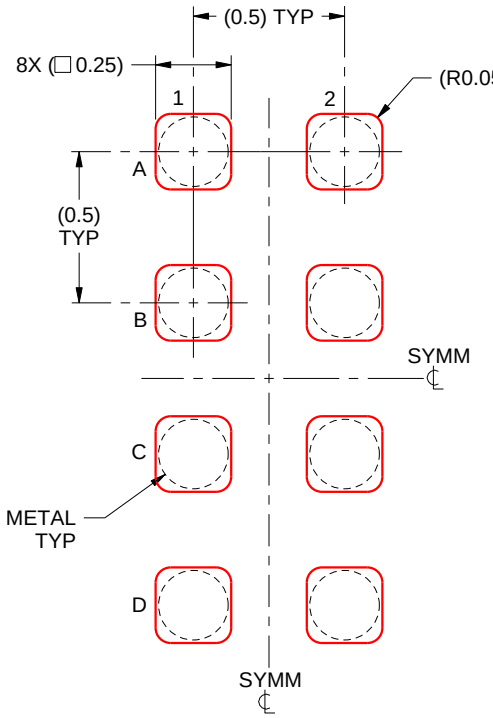


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



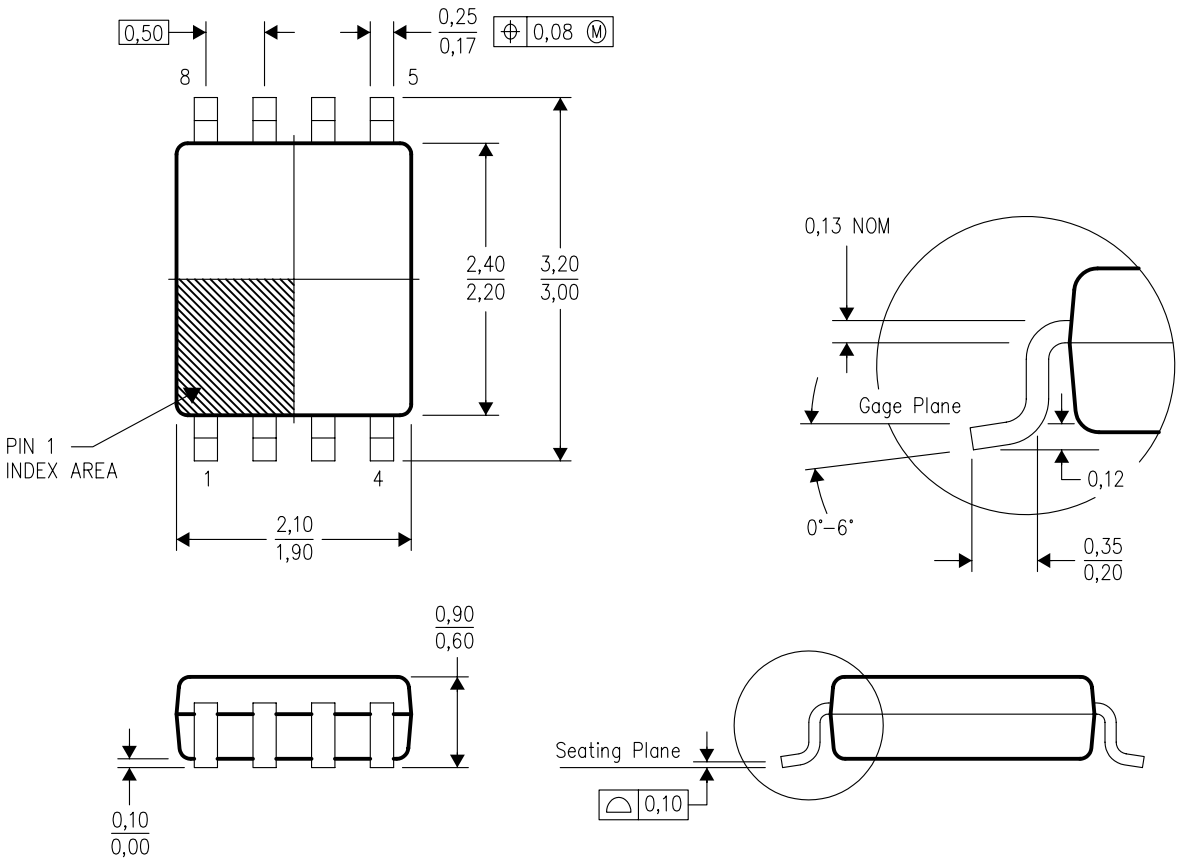
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

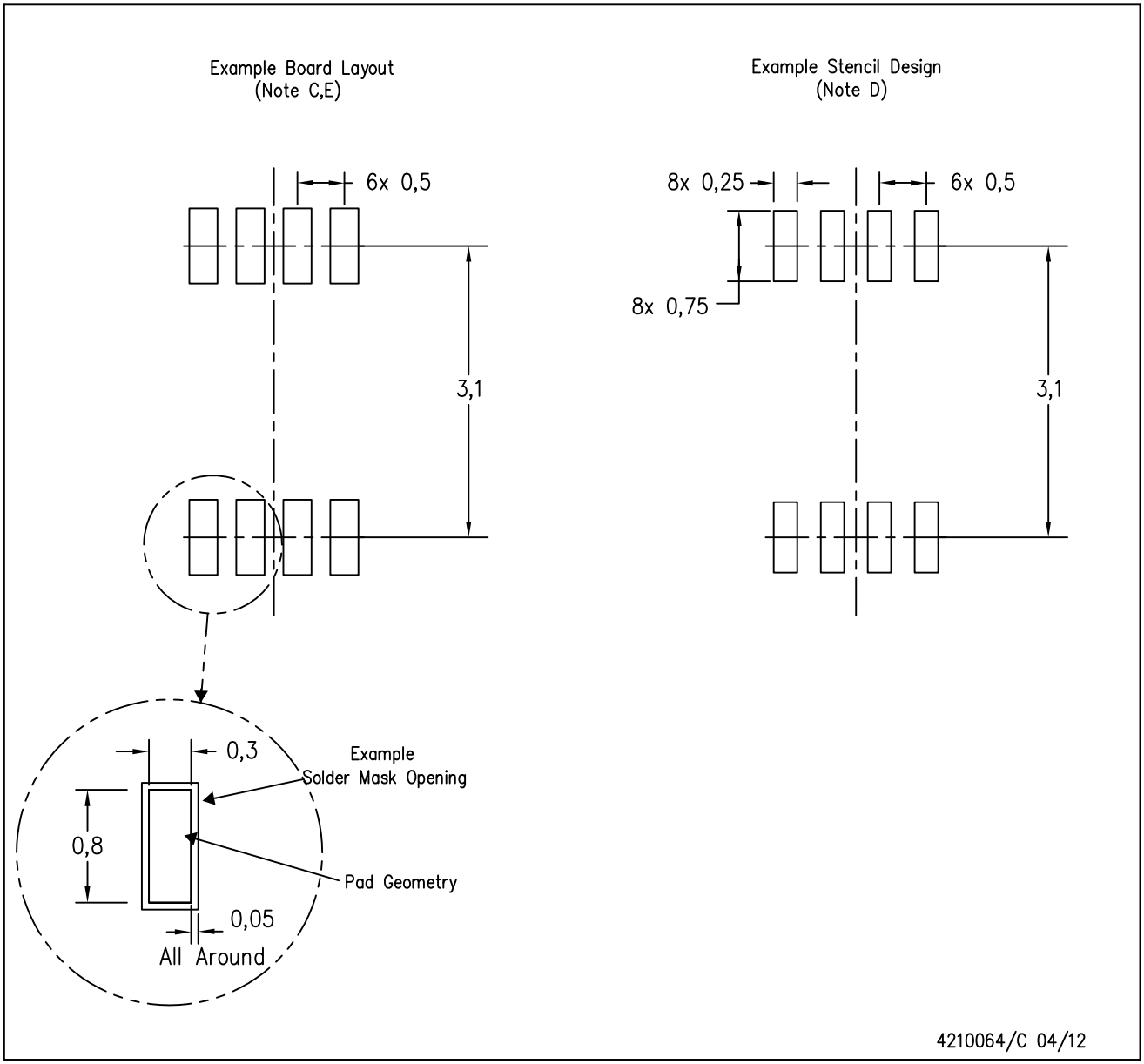
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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