具有三态输出的 SN74LVC2G126 双路总线缓冲门

1 特性

- 可采用德州仪器 (TI) 的 NanoFree™ 封装
- 支持 5V V_{CC} 运行
- 输入电压高达 5.5V
- 电压为 3.3V 时，t_{pd} 最大值为 4ns
- 低功耗，10μA 最大 I_{CC}
- 电压为 3.3V 时，输出驱动为 ±24mA
- V_{CC} = 3.3V、T_A = 25°C 时，V_{OLP}（输出接地反弹）典型值小于 0.8V
- V_{CC} = 3.3V、T_A = 25°C 时，V_{OHV}（输出 VOH 下冲）典型值大于 2V
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 可作为下行转换器，将最高 5.5V 的输入电压下行转换至 V_{CC} 电平
- 闩锁性能超过 100mA，符合 {53}JESD 78 II 类规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型
  - 1000V 充电器件模型

2 应用

- 线缆调制解调器终端系统
- 高速数据采集和生成
- 军用：雷达和声纳
- 电机控制：高电压
- 电力线通信调制解调器
- SSD：内部或外部
- 视频广播与基础设施：可扩展平台
- 视频广播：基于 IP 的多格式转码器
- 视频通信系统

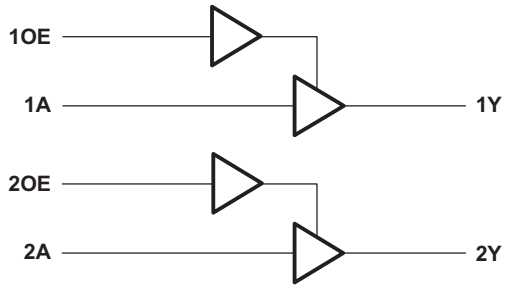
3 说明

这些总线收发器专为 1.65V 至 3.6V V{3}CC{4} 工作电压设计。SN74LVC2G126 器件是一款具有三态输出的双路线路驱动器。当输出使能输入为低电平时，输出被禁用。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SN74LVC2G126DCT	SM8 (8)	2.95mm × 2.80mm
SN74LVC2G126DCU	VSSOP (8)	2.30mm x 2.00mm
SN74LVC2G126YZP	DSBGA (8)	1.91mm × 0.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (September 2016) to Revision N (September 2020) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式。.....1

Changes from Revision L (December 2014) to Revision M (September 2016) — **Page**

- 删除了*特性*中的机器模型.....1
- 更新了*器件信息*表.....1
- Updated pinout images and *Pin Functions* table.....3
- Added Operating junction temperature, T_J in *Absolute Maximum Ratings*.....4

Changes from Revision K (November 2013) to Revision L (December 2014) — **Page**

- 添加了*应用*、*器件信息*表、*ESD 等级*表，*典型特性*、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分。.....1
- 更新了{23}特性{24}.....1

Changes from Revision J (January 2007) to Revision K (November 2013) — **Page**

- 删除了*订购信息*表.....1
- Updated operating temperature range.....5

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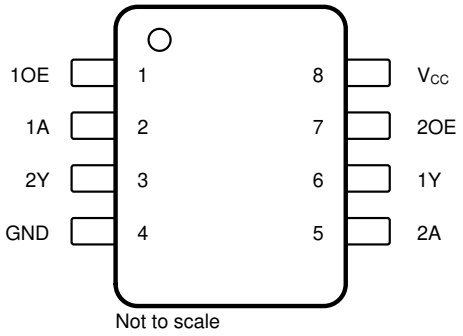
5 Pin Configuration and Functions



See mechanical drawings for dimensions.

图 5-1. DCT or DCU Package 8-Pin SM8 or VSSOP Top View

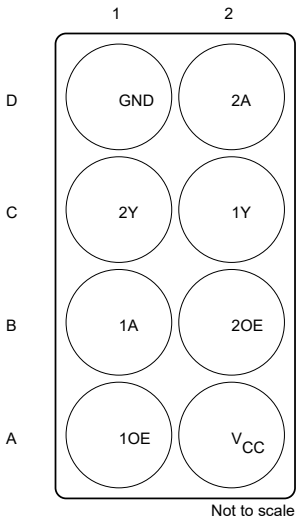


图 5-2. YZP Package 8-Pin DSBGA Bottom View

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SM8, VSSOP	DSBGA		
1A	2	B1	I	1A Input
1OE	1	A1	I	1OE Enable/Input
1Y	6	C2	O	1Y Output
2A	5	D2	I	2A Input
2OE	7	B2	I	2OE Enable/Input
2Y	3	C1	O	2Y Output
GND	4	D1	—	Ground Pin
V_{CC}	8	A2	—	Power Pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Operating junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The value of V_{CC} is provided in the 节 6.3 table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*,SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC2G126			UNIT
		DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			−40°C to +85°C		−40°C to +125°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −100 µA	1.65 V to 5.5 V	V_{CC} − 0.1			V_{CC} − 0.1		V_{CC} − 0.1		V
		I_{OH} = −4 mA	1.65 V	1.2			1.2		1.2		
		I_{OH} = −8 mA	2.3 V	1.9			1.9		1.9		
		I_{OH} = −16 mA	3 V	2.4			2.4		2.4		
		I_{OH} = −24 mA		2.3			2.3		2.3		
		I_{OH} = −32 mA	4.5 V	3.8			3.8		3.8		
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1		0.1		0.1	V
		I_{OL} = 4 mA	1.65 V			0.45		0.45		0.45	
		I_{OL} = 8 mA	2.3 V			0.3		0.3		0.3	
		I_{OL} = 16 mA	3 V			0.4		0.4		0.4	
		I_{OL} = 24 mA				0.55		0.55		0.55	
		I_{OL} = 32 mA	4.5 V			0.55		0.55		0.75	
I_I	A or OE inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5		±5		±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10		±10		±10	µA
I_{OZ}		V_O = 0 to 5.5 V	3.6 V			10		10		10	µA
I_{CC}		V_I = 5.5 V or GND I_O = 0	1.65 V to 5.5 V			10		10		10	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500		500		500	µA
C_I	Data inputs	V_I = V_{CC} or GND	3.3 V		3.5						pF
	Control inputs				4						
C_o		V_O = V_{CC} or GND	3.3 V		6.5						pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, −40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−40°C to +85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.5	9.8	1.7	4.9	1.4	4	1	3.2	ns
t_{en}	OE	Y	3.5	10	1.7	5	1.5	4.1	1	3.1	ns
t_{dis}	OE	Y	1.7	12.6	1	5.7	1	4.4	1	3.3	ns

6.7 Switching Characteristics, −40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−40°C to +125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.5	10.8	1.7	5.9	1.4	5	1	3.7	ns
t_{en}	OE	Y	3.5	11	1.7	6	1.5	5.1	1	3.6	ns
t_{dis}	OE	Y	1.7	13.6	1	6.7	1	5.4	1	3.8	ns

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6.8 Operating Characteristics

T_A = 25°

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
				TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	19	19	20	22	pF
		Outputs disabled		2	2	2	3	

6.9 Typical Characteristics

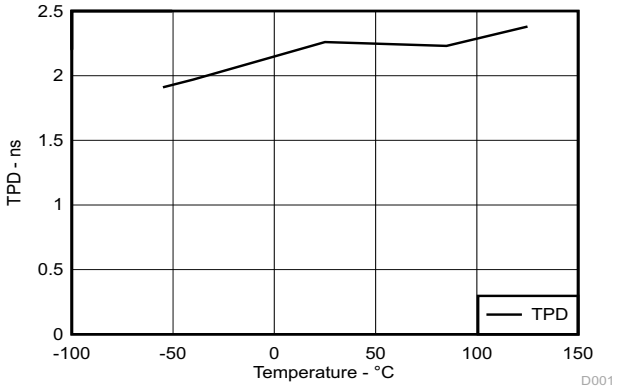


图 6-1. TPD Across Tempearture at 3.3 V_{CC}

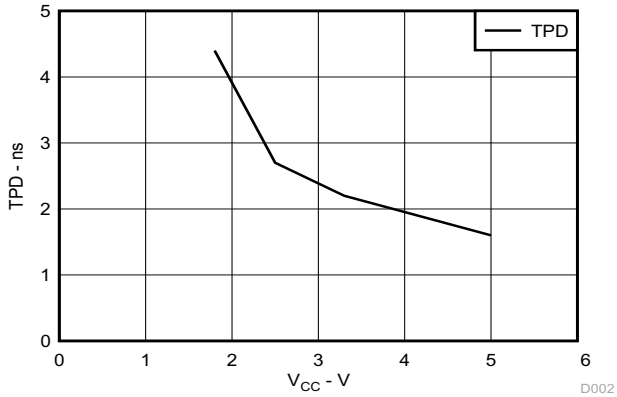
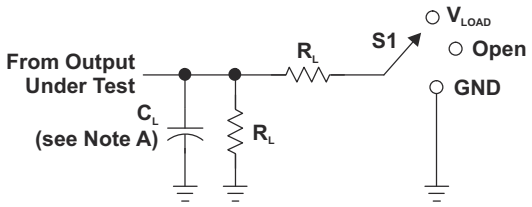


图 6-2. TPD Across V_{CC} at 25°C

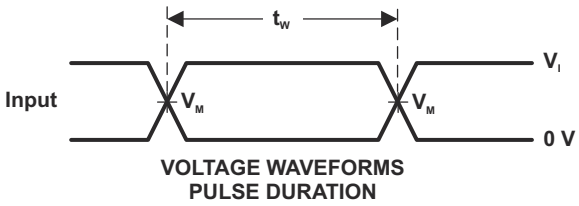
7 Parameter Measurement Information



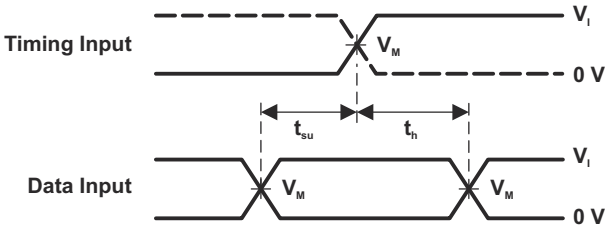
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

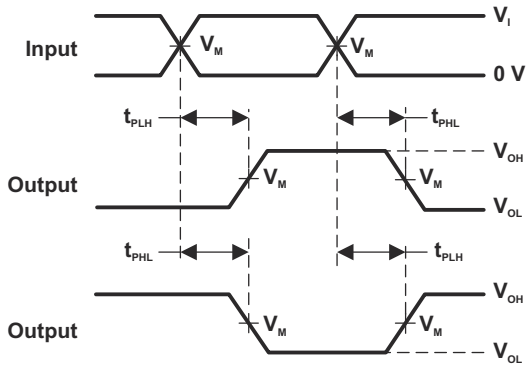
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



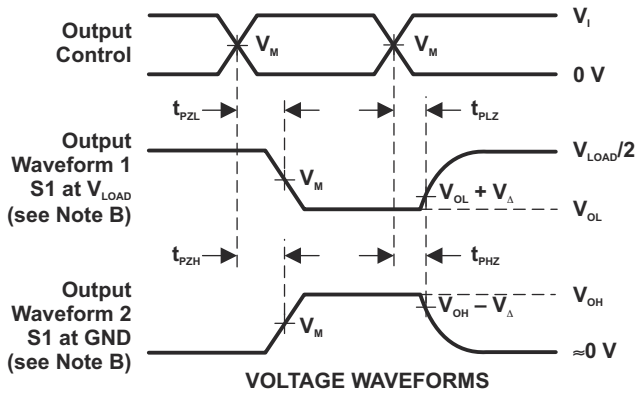
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

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8 Detailed Description

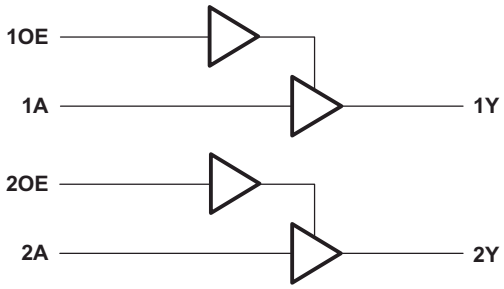
8.1 Overview

The SN74LVC2G126 device contains a dual buffer gate with output enable control and performs the Boolean function Y = A.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

- 1.65 V to 5.5 V operating voltage range
- Allows down voltage translation
  - 5 V to 3.3 V
  - 5 V or 3.3 V to 1.8V
- Inputs accept voltages to 5.5 V
  - 5-V tolerance on input pin
- I_{off} feature
  - Allows voltage on the inputs and outputs when V_{CC} is 0 V
  - Able to prevent leakage when V_{CC} is 0 V

8.4 Device Functional Modes

表 8-1 lists the functional modes of SN74LVC2G126.

Table 8-1. Function Table

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G126 device is a high-drive CMOS device that can be used as an output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V, making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC}.

9.2 Typical Application

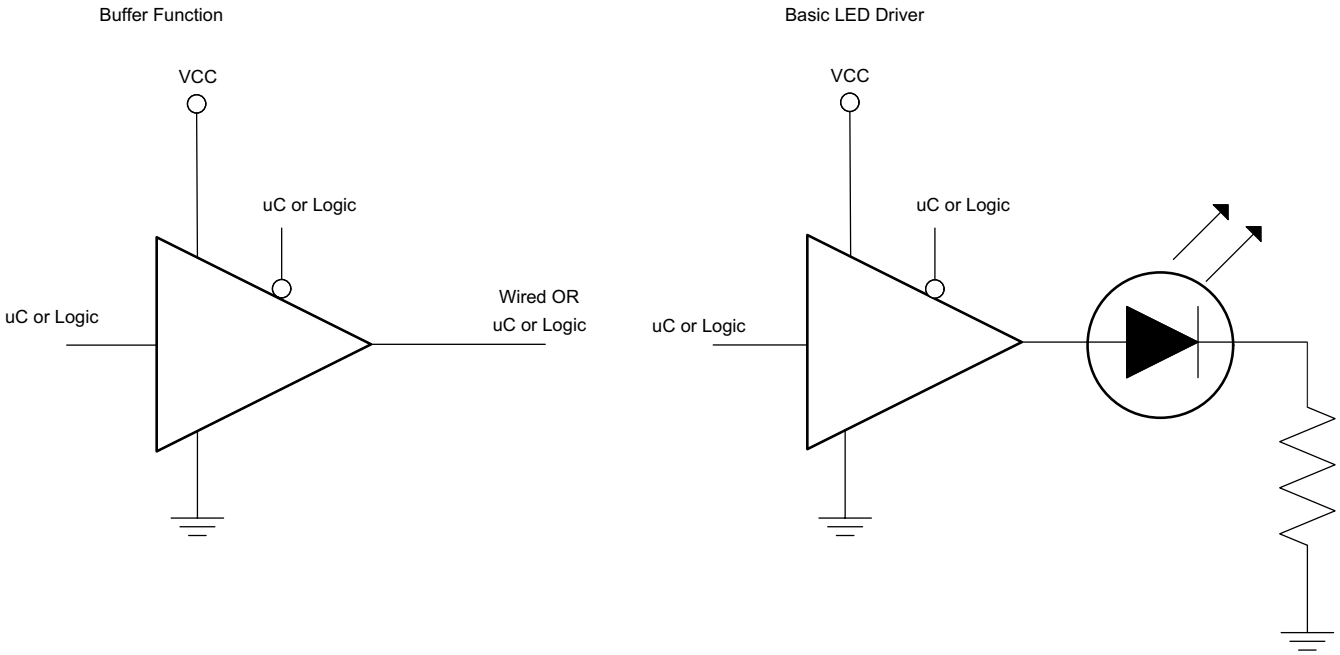

图 9-1. Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive also creates faster edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the *节 6.3* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *节 6.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.

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9.2.3 Application Curve

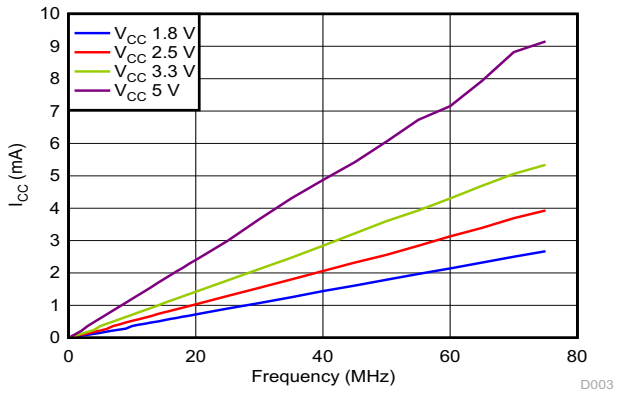

图 9-2. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the 节 6.3 table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01-μF or 0.022-μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. Install the bypass capacitor as close to the power terminal as possible for the best results.

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11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 图 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This does not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

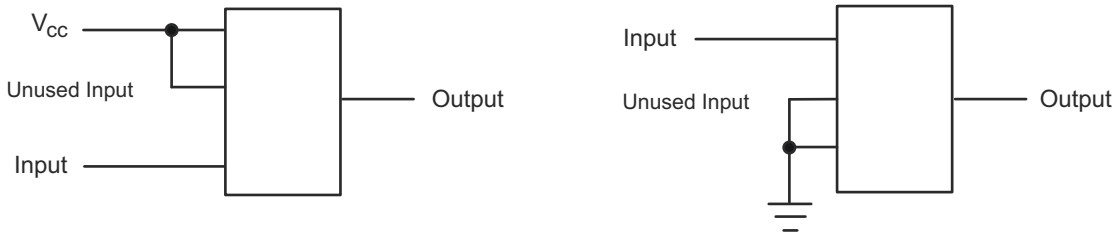

图 11-1. Layout Diagram

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC2G126DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C26 Z	Samples
74LVC2G126DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C26R	Samples
SN74LVC2G126DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C26 Z	Samples
SN74LVC2G126DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C26J, C26Q, C26R)	Samples
SN74LVC2G126DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C26J, C26Q, C26R)	Samples
SN74LVC2G126YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(CN7, CNN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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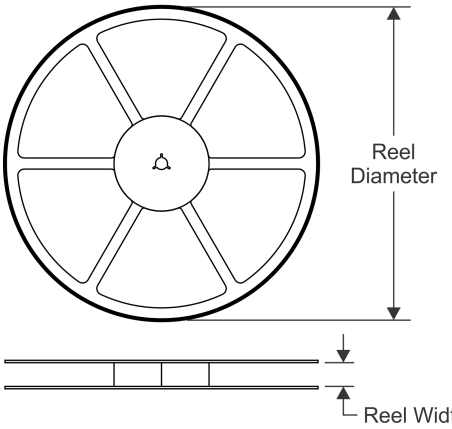
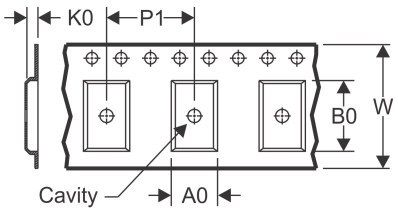
TAPE AND REEL INFORMATION

REEL DIMENSIONS

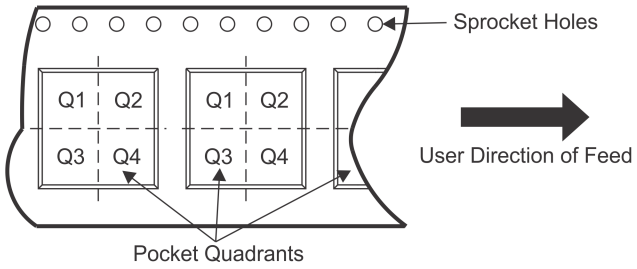


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

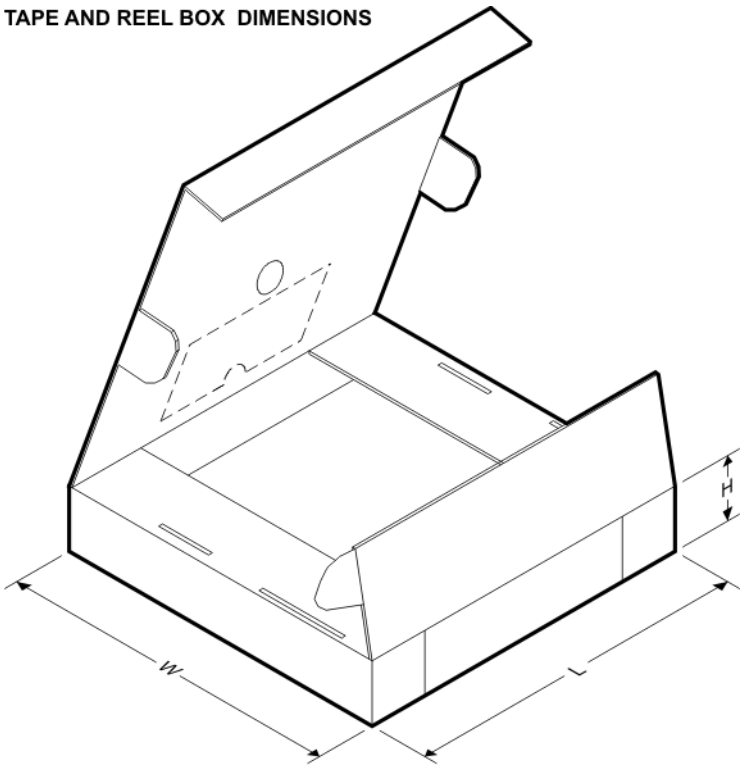
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2G126DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G126DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G126DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G126DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G126DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G126DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G126DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G126YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

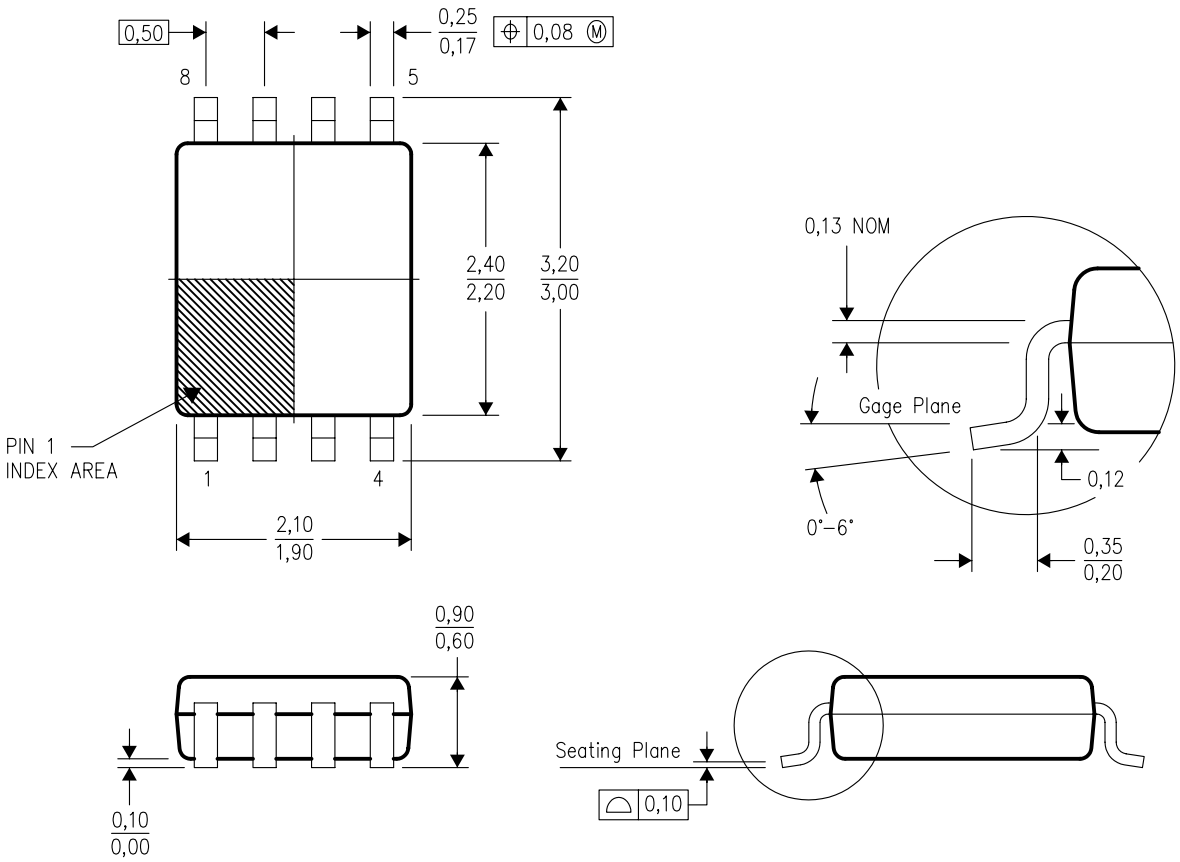
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2G126DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G126DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G126DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G126DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G126DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G126DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G126DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G126YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

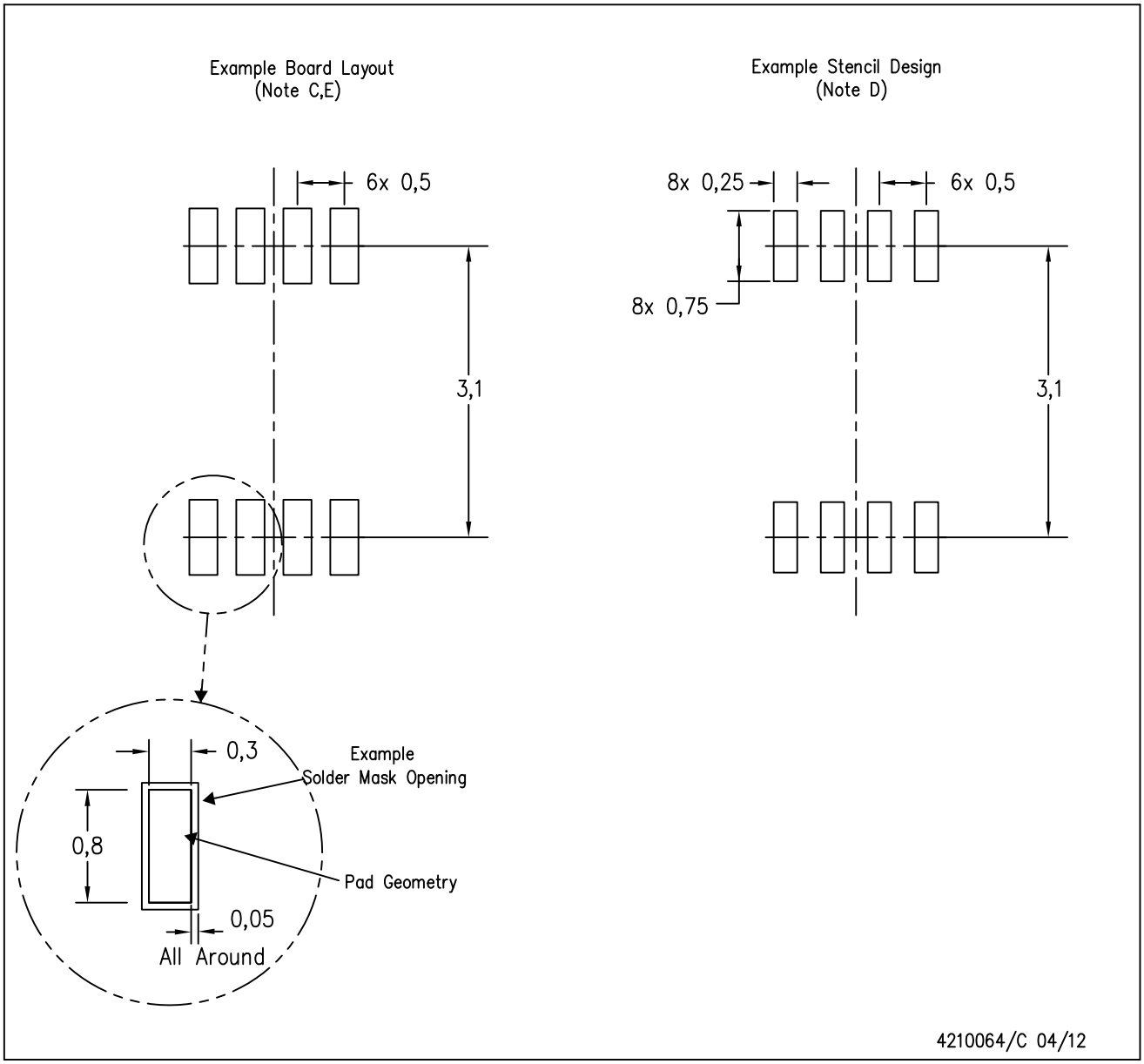
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



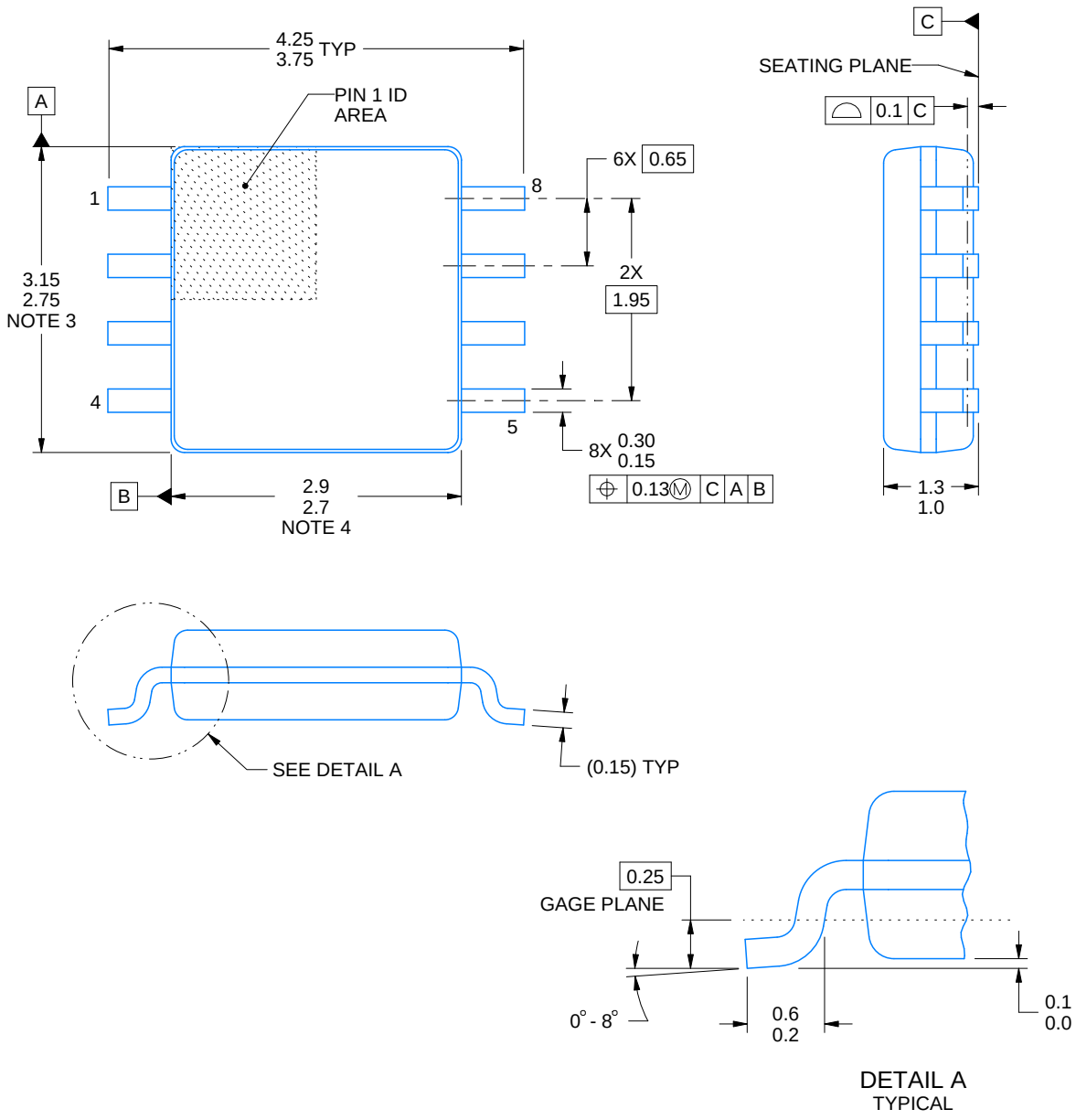
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

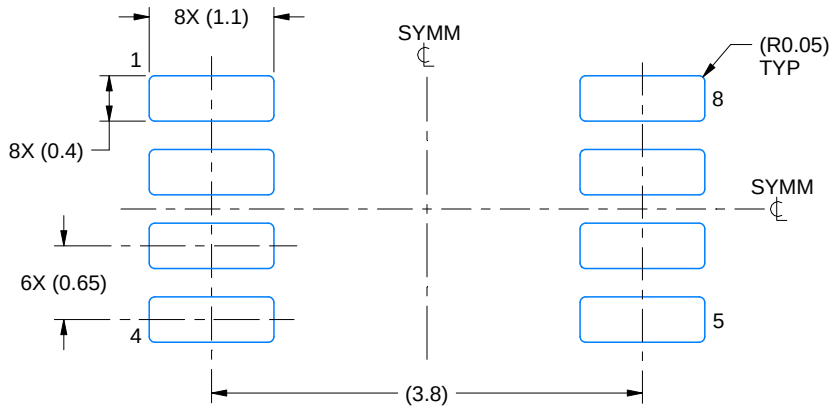
SMALL OUTLINE PACKAGE



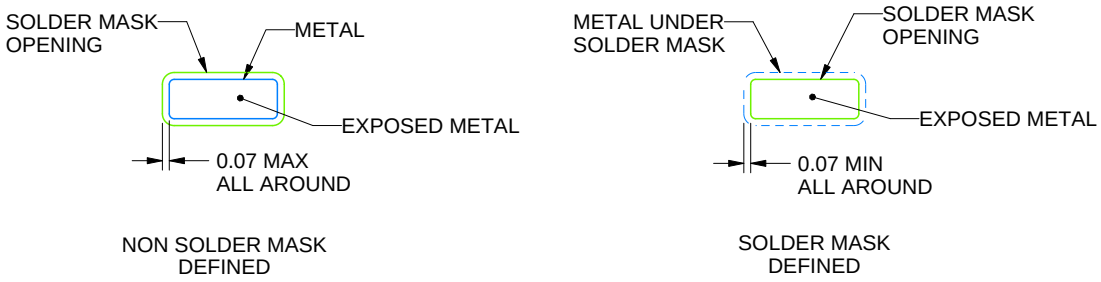
4220784/B 07/2020

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

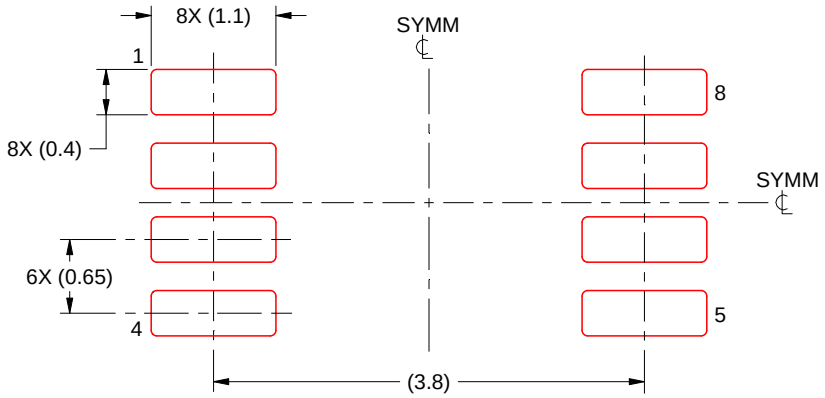


SOLDER MASK DETAILS

4220784/B 07/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/B 07/2020

NOTES: (continued)

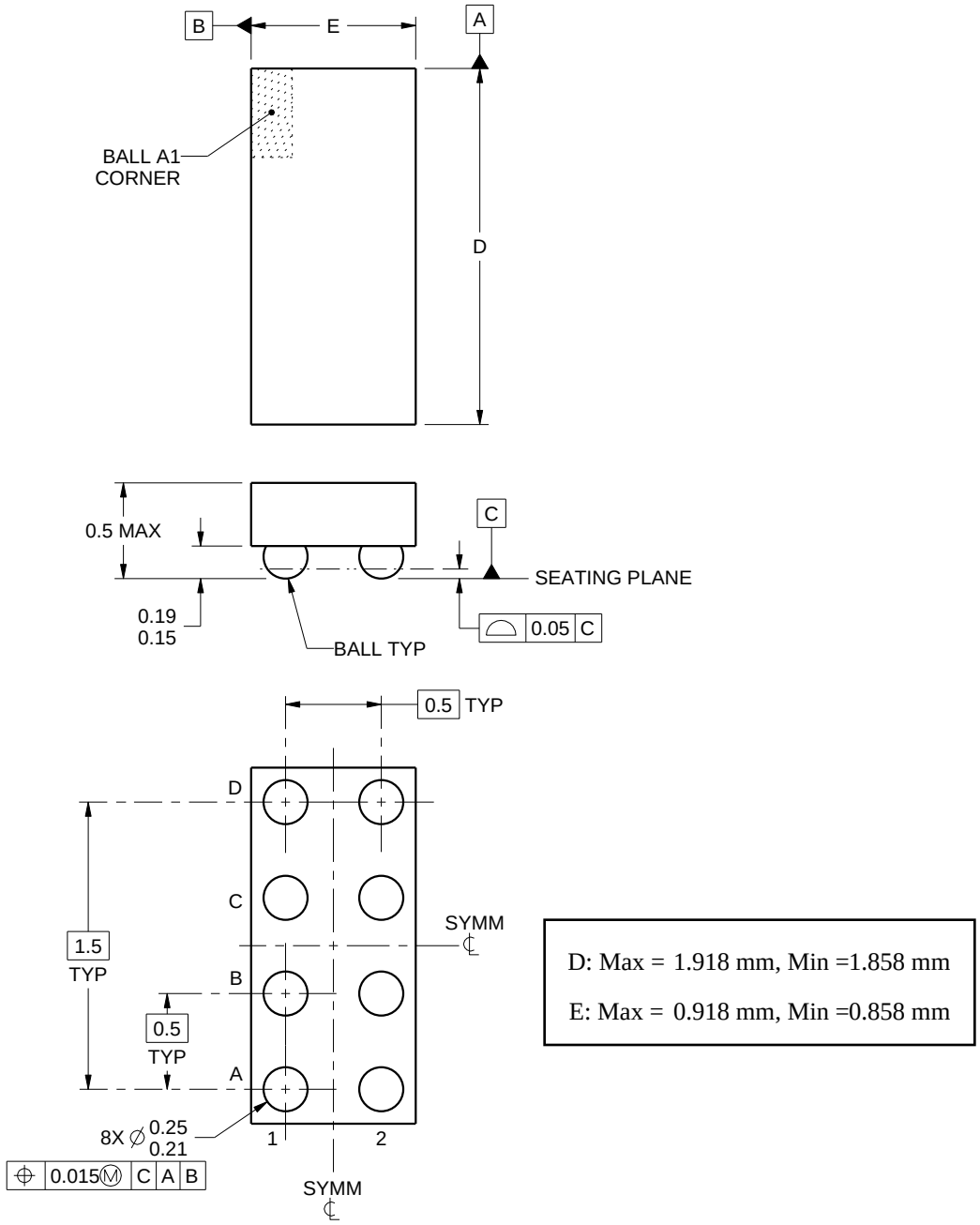
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

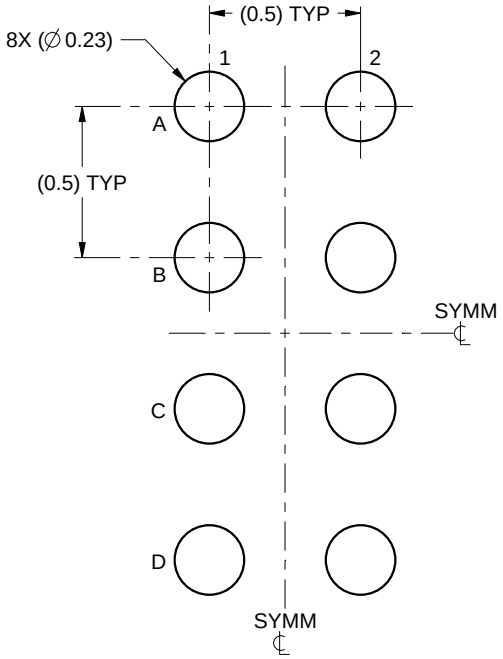
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

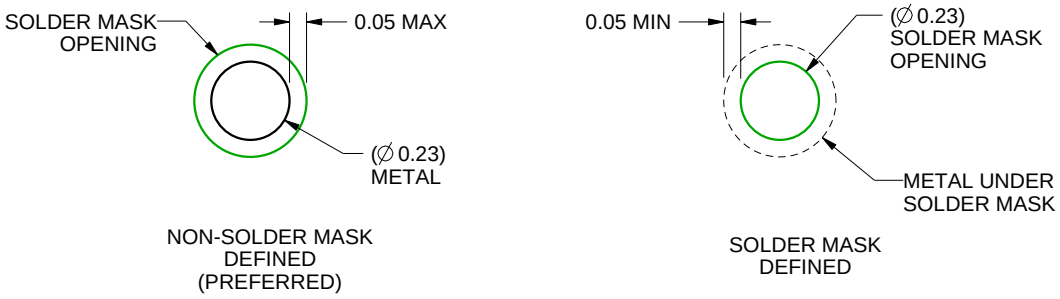


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

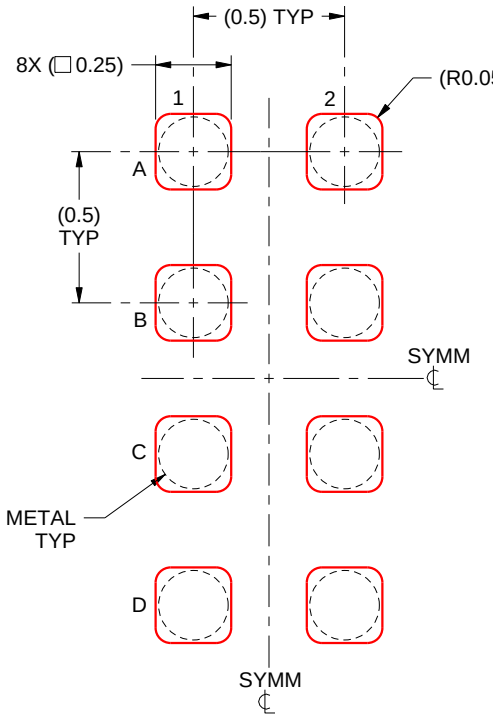


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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