

CSD25481F4 20V P 通道 FemtoFET™ MOSFET

1 特性

- 超低导通电阻
- 超低 Q_g 和 Q_{gd}
- 高运行漏极电流
- 超小封装尺寸 (0402 外壳尺寸)
 - 1mm x 0.6mm
- 超薄
 - 最大高度 0.35mm
- 集成型静电放电 (ESD) 保护二极管
 - 额定值 > 4kV 人体放电模式 (HBM)
 - 额定值 > 2kV 充电器件模型 (CDM)
- 无铅且无卤素
- 符合 RoHS 环保标准

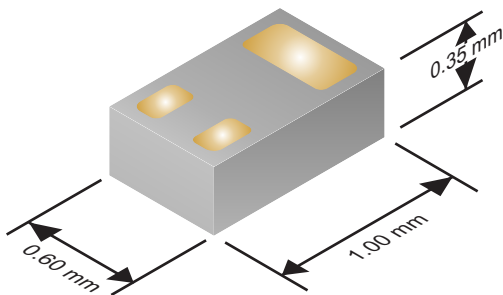
2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 电池应用
- 手持式和移动类电感式触控不锈钢键盘参考设计应用

3 说明

这款 90mΩ, 20V P 通道 FemtoFET™ MOSFET 的设计经过了优化, 能够最大限度地减小许多手持式和移动类应用的尺寸。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小 60% 以上。

典型部件尺寸



产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	-20	V
Q_g	栅极电荷总量 (-4.5V)	913	pC
Q_{gd}	栅极电荷 (栅极到漏极)	153	pC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = -1.8\text{V}$	395 mΩ
		$V_{GS} = -2.5\text{V}$	145 mΩ
		$V_{GS} = -4.5\text{V}$	90 mΩ
$V_{GS(th)}$	阈值电压	-0.95	V

订购信息⁽¹⁾

器件	数量	介质	封装	出货
CSD25481F4	3000	7 英寸卷带	Femto (0402) 1.0mm x 0.6mm 焊盘栅格阵列 (LGA)	卷带封装
CSD25481F4T	250	7 英寸卷带		

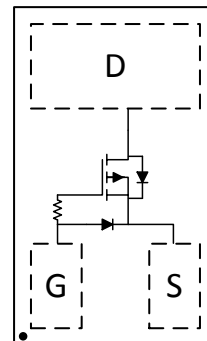
(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

绝对最大额定值

$T_A = 25^\circ\text{C}$ 时测得, 除非另外注明		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-12	V
I_D	持续漏极电流 ⁽¹⁾	-2.5	A
I_{DM}	脉冲漏极电流 ⁽²⁾	-13.1	A
I_G	持续栅极钳位电流	-35	mA
	脉冲栅极钳位电流 ⁽²⁾	-350	
P_D	功率耗散 ⁽¹⁾	500	mW
$V_{(ESD)}$	人体放电模式 (HBM)	4	kV
	充电器件模型 (CDM)	2	kV
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C

(1) 典型 $R_{\theta JA} = 90^\circ\text{C/W}$ (当在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上将其安装在 1 平方英寸 (6.45 cm²) 2 oz (0.071mm 厚) 的铜焊盘上时)。

(2) 顶视图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (October 2014) to Revision E	Page
• 将绝对最大额定值表中的脉冲漏极电流值从 $-10A$ 更改成了 $-13.1A$	1
• 将备注 1 从“典型 $R_{\theta JA} = 85^{\circ}C/W$ ”更改成了“ $R_{\theta JA} = 90^{\circ}C/W$ ”	1
• 将备注 2 从“脉冲持续时间 $\leq 300\mu s$ ，占空比 $\leq 2\%$ ”更改成了“脉冲持续时间 $\leq 100\mu s$ ，占空比 $\leq 1\%$ ”。	1
• Changed the typical $R_{\theta JA}$ values in the <i>Thermal Information</i> table	3
• Updated Figure 1	4
• Updated Figure 10 with newly measured data.	5
• 已添加 社区资源 。	7
• 更新了所有机械制图，在 推荐的模版布局 部分增加了焊盘尺寸。	8

Changes from Revision C (February 2014) to Revision D	Page
• Corrected timing V_{DS} to read $-10 V$	3

Changes from Revision B (February 2013) to Revision C	Page
• Corrected capacitance units to read pF in Figure 5	5

Changes from Revision A (December 2013) to Revision B	Page
• 更新了特性中的无铅且无卤素特性。	1
• 添加了 I_G 参数。	1
• Lowered I_{DSS} limit.	3
• Lowered I_{GSS} limit.	3

Changes from Original (September 2013) to Revision A	Page
• 删除了大型卷带信息并添加了小卷带信息。	1
• Removed UIS graph.	5

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = −250 μA	−20			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = −16 V	−100			nA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = −12 V	−50			nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = −250 μA	−0.7	−0.95	−1.2	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = −1.8 V, I _{DS} = −0.1 A		395	800	mΩ
		V _{GS} = −2.5 V, I _{DS} = −0.5 A		145	174	mΩ
		V _{GS} = −4.5 V, I _{DS} = −0.5 A		90	105	mΩ
		V _{GS} = −8 V, I _{DS} = −0.5 A		75	88	mΩ
g _{fs}	Transconductance	V _{DS} = −10 V, I _{DS} = −0.5 A		3.3		S
DYNAMIC CHARACTERISTICS						
C _{iSS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = −10 V, f = 1 MHz		189		pF
C _{oss}	Output Capacitance			78		pF
C _{rSS}	Reverse Transfer Capacitance			5.5		pF
R _G	Series Gate Resistance			20		Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = −10 V, I _{DS} = −0.5 A		913		pC
Q _{gd}	Gate Charge Gate-to-Drain			153		pC
Q _{gs}	Gate Charge Gate-to-Source			240		pC
Q _{g(th)}	Gate Charge at V _{th}			116		pC
Q _{oss}	Output Charge	V _{DS} = −10 V, V _{GS} = 0 V		1030		pC
t _{d(on)}	Turn On Delay Time	V _{DS} = −10 V, V _{GS} = −4.5 V, I _{DS} = −0.5 A, R _G = 2 Ω		4.1		ns
t _r	Rise Time			3.6		ns
t _{d(off)}	Turn Off Delay Time			16.9		ns
t _f	Fall Time			6.7		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = −0.5 A, V _{GS} = 0 V		−0.75		V
Q _{rr}	Reverse Recovery Charge	V _{DS} = −10 V, I _F = −0.5 A, di/dt = 100 A/μs		1010		pC
t _{rr}	Reverse Recovery Time			7.5		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾	90	°C/W
	Junction-to-Ambient Thermal Resistance ⁽²⁾	250	

(1) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

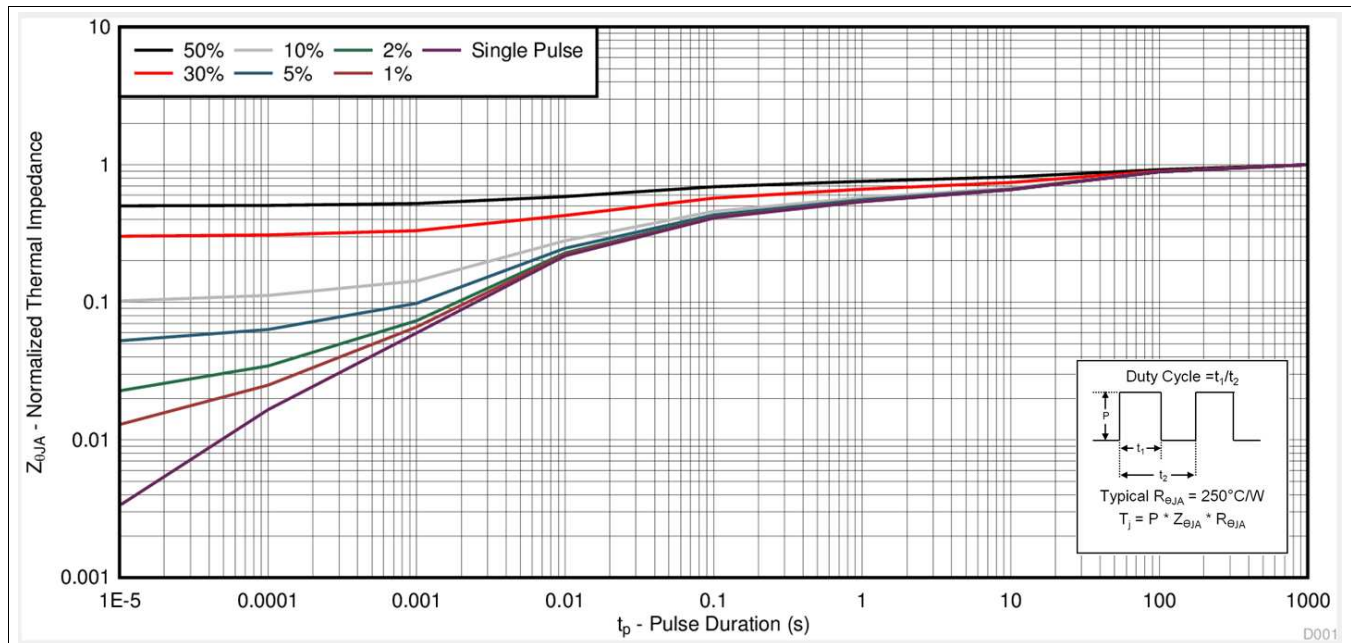


Figure 1. Transient Thermal Impedance

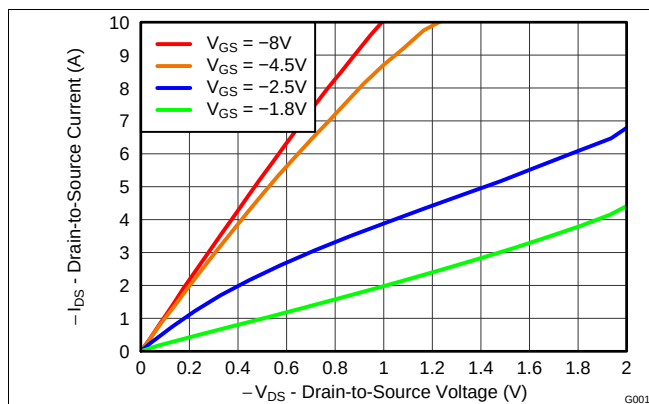


Figure 2. Saturation Characteristics

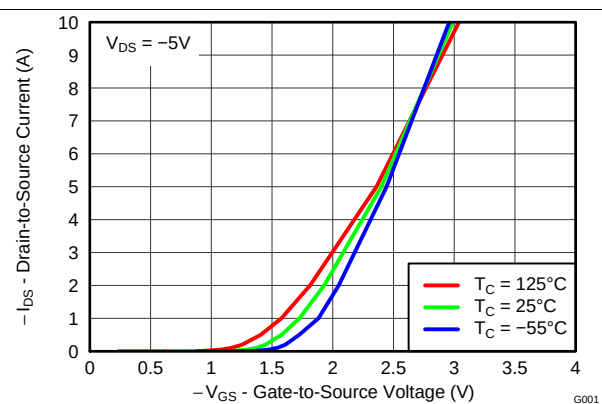


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

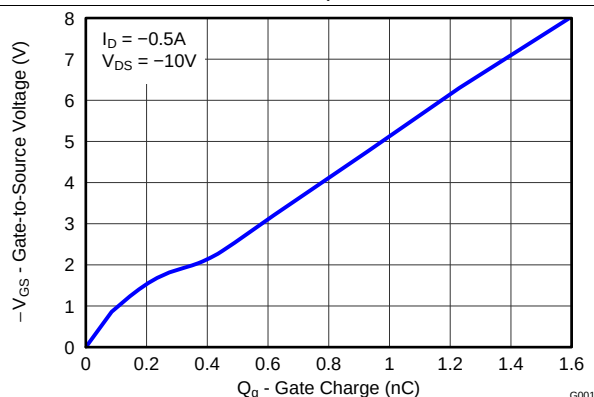


Figure 4. Gate Charge

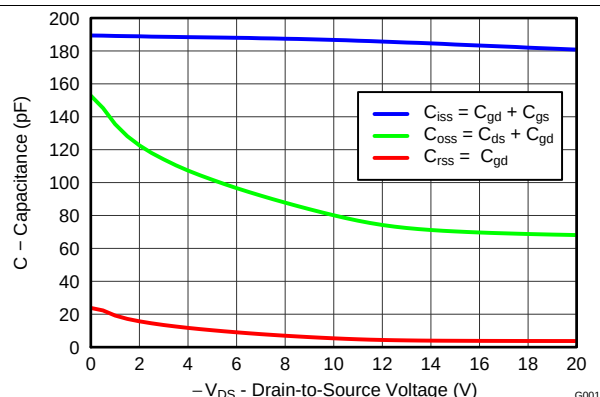


Figure 5. Capacitance

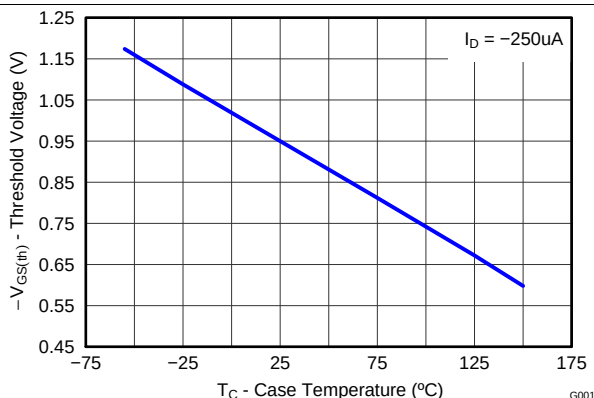


Figure 6. Threshold Voltage vs Temperature

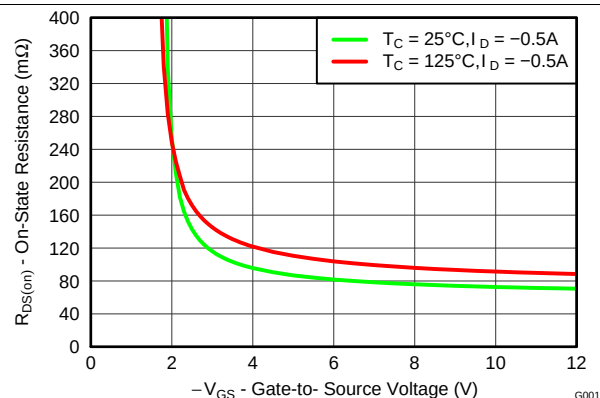


Figure 7. On-State Resistance vs Gate-to-Source Voltage

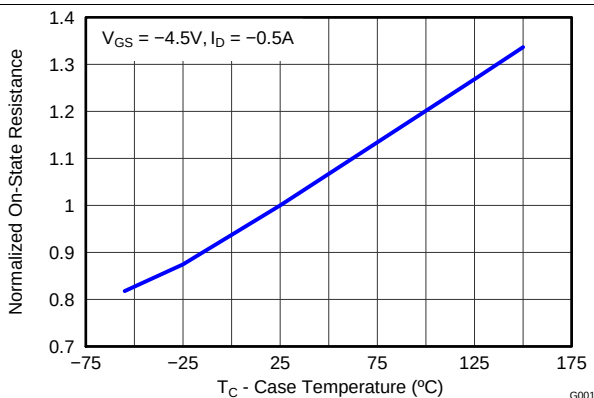


Figure 8. Normalized On-State Resistance vs Temperature

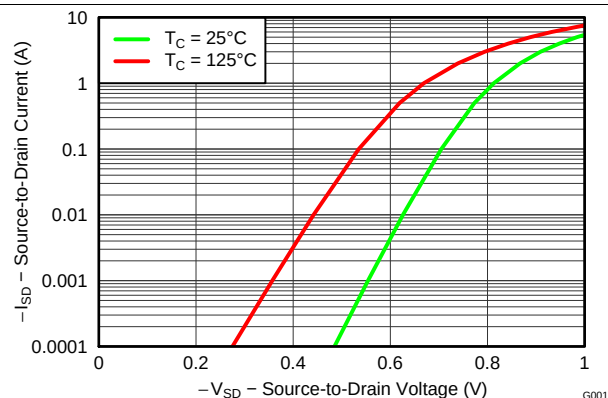
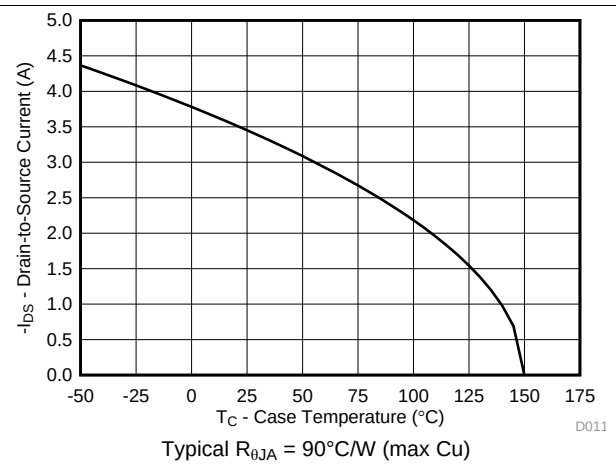
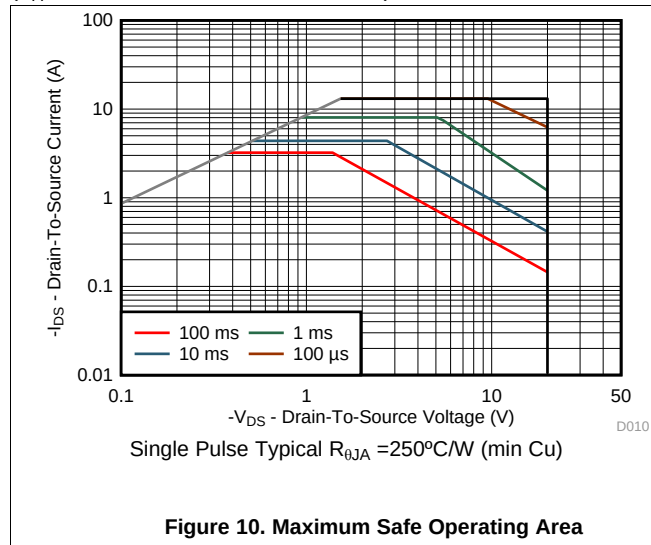


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



6 器件和文档支持

6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.2 商标

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 Glossary

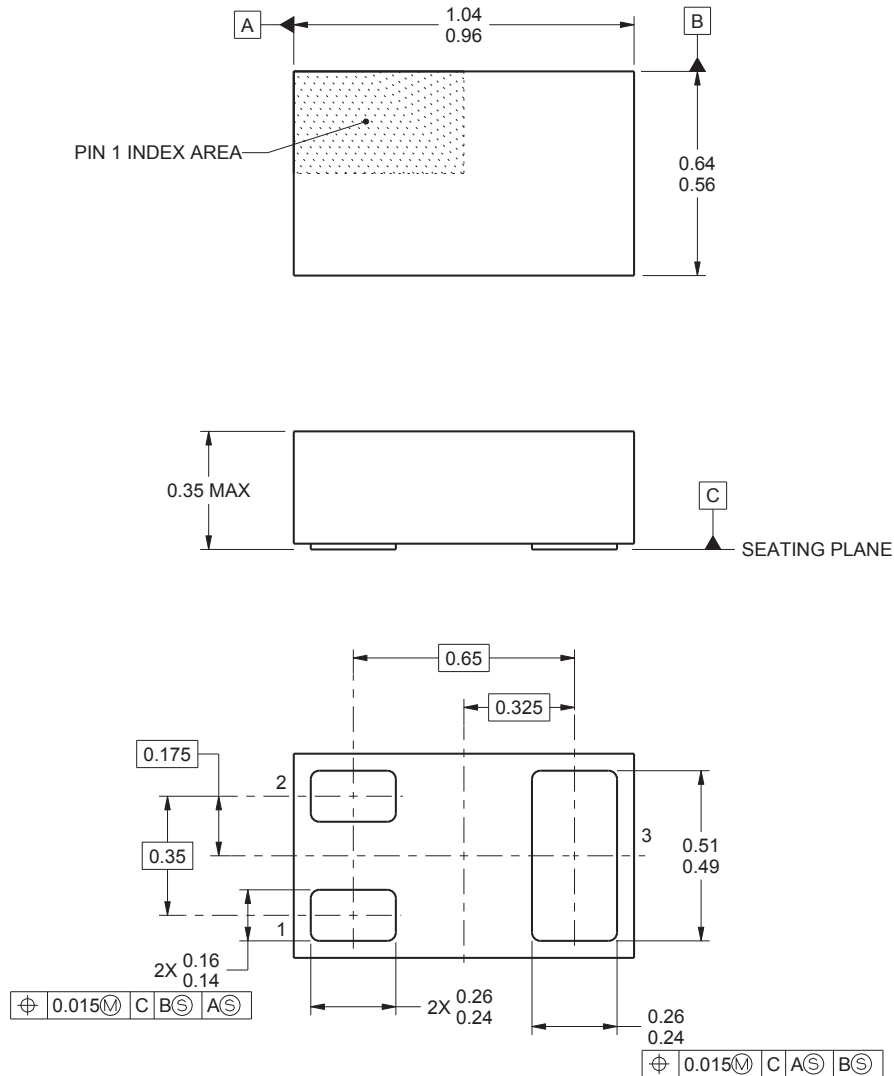
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

7.1 机械尺寸

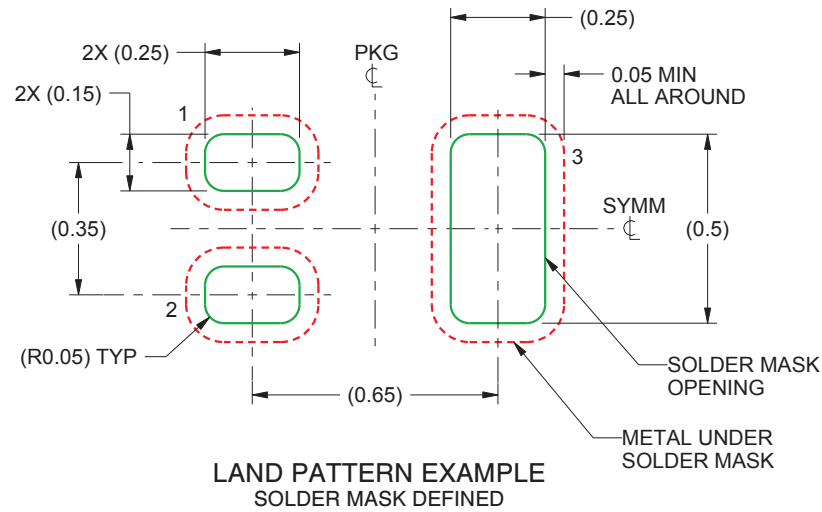


- (1) 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
- (2) 本图如有变更，恕不另行通知。
- (3) 此封装为无铅凸点设计。凸点涂料可能有所不同。要确定确切的涂料，请参阅器件数据表或联系当地的 TI 代表。

表 1. 引脚配置

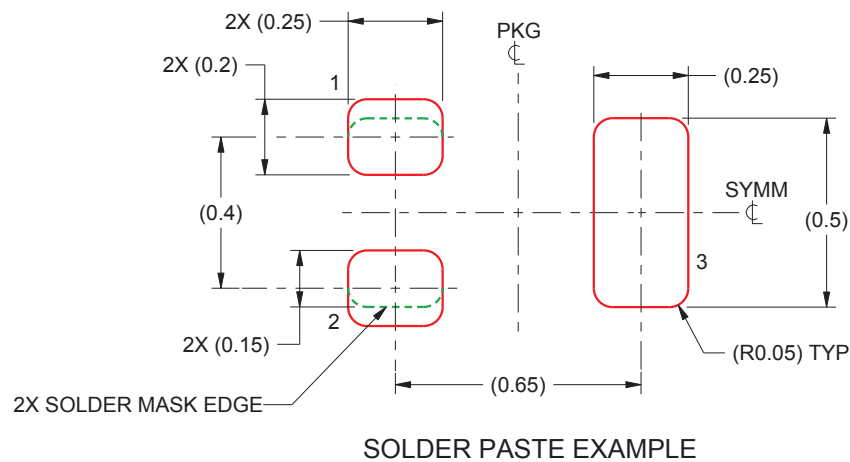
位置	名称
引脚 1	栅极
引脚 2	源极
引脚 3	漏极

7.2 建议的最小 PCB 布局



- (1) 所有尺寸的单位均为毫米。
- (2) 有关更多信息，请参阅《QFN/SON PCB 连接》(SLUA271)。

7.3 推荐的模版布局



- (1) 所有尺寸的单位都是毫米。
- (2) 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25481F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	CS	Samples
CSD25481F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	CS	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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