LMH1982 Multi-Rate Video Clock Generator With Genlock

1 Features

- Two Simultaneous LVDS Output Clocks with Selectable Frequencies and Hi-Z Capability:
  - SD Clock: 27 MHz or 67.5 MHz
  - HD Clock: 74.25 MHz, 74.25/1.001 MHz, 148.5 MHz or 148.5/1.001 MHz
- Low-Jitter Output Clocks May Be Directly Connected to an FPGA Serializer to Meet SMPTE SDI Jitter Specifications
- Top of Frame (TOF) Pulse with Programmable Output Format Timing and Hi-Z Capability
- Two reference ports (A and B) With H and V Sync Inputs
- Supports Cross-Locking of Input and Output Timing
- External Loop Filter Allows Control of Loop Bandwidth, Jitter Transfer, and Lock Time Characteristics
- Free Run or Holdover Operation on Loss of Reference
- User-Defined Free Run Control Voltage Input
- I^2C Interface and Control Registers
- 3.3-V and 2.5-V Supplies

2 Applications

- Video Genlock and Synchronization
- FPGA SDI SerDes Recovered Clock Generation
- Triple Rate 3G/HD/SD-SDI SerDes
- Video Capture, Conversion, Editing and Distribution
- Video Displays and Projectors
- Broadcast and Professional Video Equipment

3 Description

The LMH1982 device is a multi-rate video clock generator ideal for use in a wide range of 3-Gbps (3G), high-definition (HD), and standard-definition (SD) video applications, such as video synchronization, serial digital interface (SDI) serializer and deserializer (SerDes), video conversion, video editing, and other broadcast and professional video systems.

The LMH1982 can generate two simultaneous SD and HD clocks and a Top of Frame (TOF) pulse. In genlock mode, the device's phase locked loops (PLLs) can synchronize the output signals to H sync and V sync input signals applied to either of the reference ports. The input reference can have analog timing from Texas Instrument's LMH1981 multi-format video sync separator or digital timing from an SDI deserializer and should conform to the major SD and HD standards. When a loss of reference occurs, the device can default to free run operation where the output timing accuracy will be determined by the external bias on the free run control voltage input.

The LMH1982 can replace discrete PLLs and field-programmable gate array (FPGA) PLLs with multiple voltage controlled crystal oscillators (VCXOs). Only one 27.0000 MHz VCXO and loop filter are externally required for genlock mode. The external loop filter as well as programmable PLL parameters can provide narrow loop bandwidths to minimize jitter transfer. HD clock output jitter as low as 40 ps peak-to-peak can help designers using FPGA SerDes meet stringent SDI output jitter specifications.

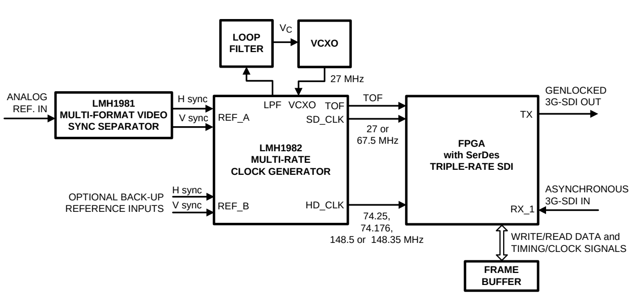
The LMH1982 is offered in a space-saving 5 mm x 5 mm 32-pin WQFN package and provides low total power consumption of about 250 mW (typical).

Device Information(1)

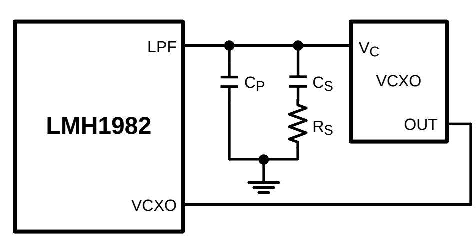
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH1982	WQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Genlock Application



Typical Loop Filter Topology



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D — **Page**

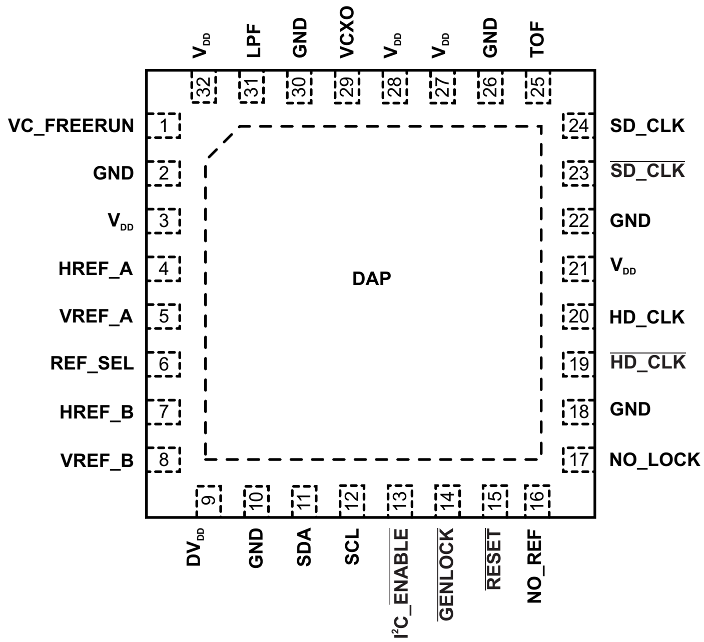
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision B (March 2009) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format 38

5 Pin Configuration and Functions

RTV Package
32-Pin WQFN
Top View



Pin Functions

PIN		I/O	SIGNAL LEVEL	DESCRIPTION
NO.	NAME			
–	DAP	—	Supply	Die Attach Pad (Connect to GND)
1	VC_FREERUN	I	Analog	Free Run Control Voltage Input
2, 10, 18, 22, 26, 30	GND	—	Supply	Ground
3, 21, 27, 28, 32	V_{DD}	—	Supply	3.3-V Supply(1)
4	HREF_A	I	LVCMOS	H sync Input, Reference A
5	VREF_A	I	LVCMOS	V sync Input, Reference A
6	REF_SEL	I	LVCMOS	Reference Select(2)(3)
7	HREF_B	I	LVCMOS	H sync Input, Reference B
8	VREF_B	I	LVCMOS	V sync Input, Reference B
9	DV_{DD}	—	Supply	2.5-V Supply(4)
11	SDA	I/O	I^2C	I^2C Data(5)
12	SCL	I	I^2C	I^2C Clock(5)
13	$I^2C\_\overline{\text{ENABLE}}$	I	LVCMOS	I^2C Enable
14	$\overline{\text{GENLOCK}}$	I	LVCMOS	Mode Select(6)
15	$\overline{\text{RESET}}$	I	LVCMOS	Device Reset
16	NO_REF	O	LVCMOS	Reference Status Flag
17	NO_LOCK	O	LVCMOS	Lock Status Flag
19, 20	$\overline{\text{HD\_CLK}}$, HD_CLK	O	LVDS	HD Clock Output

(1) Refer to *Power Supply Sequencing*.
(2) To control reference selection via the REF_SEL pin instead of the I^2C interface (default), program I^2C_RSEL = 0 (register 00h).
(3) To override reference control through pin 6 and instead use pin 6 as an logic input for output initialization, program PIN6_OVRD = 1 (register 02h); accordingly, the TOF_INIT bit (register 0Ah) will be ignored and reference selection must be controlled through I^2C.
(4) Must be ≤ V_{DD} + 0.3 V. Refer to *Power Supply Sequencing*.
(5) SDA and SCL pins each require a 4.7-kΩ (typical) pullup resistor to the V_{DD} supply.
(6) To control mode selection through the $\overline{\text{GENLOCK}}$ pin instead of the I^2C interface (default), program I^2C_GNLK = 0 (register 00h).

Pin Functions (continued)

PIN		I/O	SIGNAL LEVEL	DESCRIPTION
NO.	NAME			
23, 24	$\overline{SD\_CLK}$, SD_CLK	O	LVDS	SD Clock Output
25	TOF	O	LVCMOS	Top of Frame Pulse
29	VCXO	I	LVCMOS	VCXO Clock Input
31	LPF	O	Analog	VCXO PLL Loop Filter

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)]

	MIN	MAX	UNIT
Supply Voltage, V_{DD}		3.6	V
Supply Voltage, DV_{DD}		2.75	V
Input Voltage (any input)	−0.3	V_{DD} +0.3	V
Lead Temperature (Soldering 10 sec.)		300	°C
Junction Temperature, T_{JMAX}		150	°C
Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{DD}	3.135	3.465	V
DV_{DD}	2.375	2.625	V
Input Voltage	0	V_{DD}	V
Temperature, T_A	0	70	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		LMH1982	UNIT
		RTV (WQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 3.3 V, DV_{DD} = 2.5 V.

PARAMETER		TEST CONDITIONS		MIN [(1)]	TYP [(2)]	MAX [(1)]	UNIT
I_{VDD}	V_{DD} Supply Current	Default register settings, no input reference, 27-MHz VCXO and loop filter connected, 100-Ω differential load on SD_CLK and HD_CLK outputs; no load on all other outputs			47		mA
I_{DVDD}	DV_{DD} Supply Current				39		mA
I_{VDD}	V_{DD} Supply Current	V_{DD} = 3.465 V, DV_{DD} = 2.625 V, Genlock mode, 1080p/59 output timing, HD_CLK = 148.35 MHz, SD_CLK = 67.5 MHz, 100-Ω differential load on SD_CLK and HD_CLK outputs; no load on all other outputs			57		mA
			At the temperature extremes			70	
I_{DVDD}	DV_{DD} Supply Current				44		mA
			At the temperature extremes			60	
FREE RUN VOLTAGE CONTROL INPUT (PIN 1)							
V_{IL}	Low Analog Input Voltage	See [(3)]			0		V
V_{IH}	High Analog Input Voltage	See [(3)]			V_{DD}		V
REFERENCE INPUTS (PINS 4, 5, 7, 8)							
V_{IL}	Low Input Voltage	I_{IN} = ±10 µA		0		0.3 V_{DD}	V
V_{IH}	High Input Voltage	I_{IN} = ±10 µA		0.7 V_{DD}		V_{DD}	V
$ΔT_{HV}$	H-V Sync Timing Offset	Input timing offset measured from H sync to V sync pulse leading edges [(4)]				2.0	µs
DIGITAL CONTROL INPUTS (PINS 6, 13, 14, 15)							
V_{IL}	Low Input Voltage	I_{IN} = ±10 µA		0		0.3 V_{DD}	V
V_{IH}	High Input Voltage	I_{IN} = ±10 µA		0.7 V_{DD}		V_{DD}	V
I^2C INTERFACE (PINS 11, 12)							
V_{IL}	Low Input Voltage			0		0.3 V_{DD}	V
V_{IH}	High Input Voltage			0.7 V_{DD}		V_{DD}	V
I_{IN}	Input Current	V_{IN} between 0.1 V_{DD} and 0.9 V_{DD}		−10		+10	µA
I_{OL}	Low Output Sink Current	V_{OL} = 0 V or 0.4 V			3		mA
STATUS FLAG OUTPUTS (PIN 16, 17)							
V_{OL}	Low Output Voltage	I_{OUT} = +10 mA				0.4	V
V_{OH}	High Output Voltage	I_{OUT} = −10 mA		V_{DD} −0.4V			V
TOP OF FRAME OUTPUT (PIN 25)							
V_{OL}	Low Output Voltage	I_{OUT} = +10 mA				0.4	V
V_{OH}	High Output Voltage	I_{OUT} = −10 mA		V_{DD} −0.4V			V
I_{OZ}	Output Hi-Z Leakage Current	TOF output in Hi-Z mode, output pin connected to V_{DD} or GND			0.4	10	|µA|
t_R	Rise Time	15-pF load			1.5		ns
t_F	Fall Time	15-pF load			1.5		ns

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) The input voltage to VC_FREERUN (pin 1) should also be within the input range of the external VCXO. The input voltage should be clean from noise that may significantly modulate the VCXO control voltage and consequently produce output jitter during free run operation.
(4) $ΔT_{HV}$ is a required specification that allows for proper frame decoding and subsequent output initialization (alignment). For interlace formats, the H-V sync timing offset must be within $ΔT_{HV}$ for all even fields and be outside $ΔT_{HV}$ for odd fields. For progressive formats, the H-V sync timing offset must be within $ΔT_{HV}$ for all frames. See sections *Reference Frame Decoder* and *Output Frame Line Offset*.

Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 3.3 V, DV_{DD} = 2.5 V.

PARAMETER		TEST CONDITIONS	MIN [1]	TYP [2]	MAX [1]	UNIT
t_{D_TOF}	TOF Output Delay Time [5]	Specified for any SD or HD format generated from 27-MHz TOF clock [6], outputs initialized [7], 15 pF load		2		ns
CLOCK OUTPUTS (PINS 19, 20, 23, 24)						
$Jitter_{SD}$	27-MHz TIE Peak-to-Peak Output Jitter [8]	HD_CLK = Hi-Z		23		ps
		HD_CLK = 74.176 MHz		40		ps
	67.5-MHz TIE Peak-to-Peak Output Jitter [8]	HD_CLK = Hi-Z		40		ps
		HD_CLK = 74.176 MHz		50		ps
$Jitter_{HD}$	74.176-MHz TIE Peak-to-Peak Output Jitter [8]	SD_CLK = Hi-Z		55		ps
		SD_CLK = 27 MHz		65		ps
	74.25-MHz TIE Peak-to-Peak Output Jitter [8]	SD_CLK = Hi-Z		40		ps
		SD_CLK = 27 MHz		50		ps
	148.35-MHz TIE Peak-to-Peak Output Jitter [8]	SD_CLK = Hi-Z		60		ps
		SD_CLK = 27 MHz		70		ps
	148.5-MHz TIE Peak-to-Peak Output Jitter [8]	SD_CLK = Hi-Z		45		ps
		SD_CLK = 27 MHz		55		ps
t_{D_SD}	27-MHz Output Delay Time [9]	SD_CLK = 27 MHz, Any valid output timing, outputs initialized [7]		4		ns
	67.5-MHz Output Delay Time [9]	SD_CLK = 67.5 MHz, 525i output timing [6], outputs initialized [7]		6		ns
t_{D_HD}	74.176-MHz Output Delay Time [10]	HD_CLK = 74.176 MHz, 1080i/59 output timing [6], outputs initialized [7]		4.5		ns
	74.25-MHz Output Delay Time [10]	HD_CLK = 74.25 MHz, 1080i/50 output timing [6], outputs initialized [7]		–0.6		ns
	148.35-MHz Output Delay Time [10]	HD_CLK = 148.35 MHz, 1080p/59 output timing [6], outputs initialized [7]		1.5		ns
	148.5-MHz Output Delay Time [10]	HD_CLK = 148.5 MHz, 1080p/50 output timing [6], outputs initialized [7]		4.5		ns
V_{OD}	Differential Signal Output Voltage [11]	100-Ω differential load	247	350	454	mV
V_{OS}	Common Signal Output Voltage [11]	100-Ω differential load	1.125	1.250	1.375	V
$\|V_{OD}\|$	|Change to V_{OD}| for Complementary Output States [11]	100-Ω differential load			50	|mV|
$\|V_{OS}\|$	|Change to V_{OS}| for Complementary Output States [11]	100-Ω differential load			50	|mV|

(5) t_{D_TOF} is measured from the TOF pulse (leading negative edge) to the 27 MHz SD_CLK output (positive edge) using 50% levels.
(6) For any SD and HD output formats, the TOF pulse can be generated using 27 MHz as the TOF clock by programming TOF_CLK = 0, SD_FREQ = 0, and the alternative output counter values shown in Table 2. See *HD Format TOF Generation Using a 27-MHz TOF Clock*.
(7) Output initialization refers to the initial alignment of the output frame clock and TOF signals to the input reference frame. See *Programming the Output Initialization Sequence*.
(8) The SD and HD clock output jitter is based on VCXO clock (pin 29) with 20 ps peak-to-peak using a time interval error (TIE) jitter measurement. The typical TIE peak-to-peak jitter was measured on the LMH1982 evaluation bench board using TDSJIT3 jitter analysis software on a Tektronix DSA70604 oscilloscope and 1 GHz active differential probe. TDSJIT3 Clock TIE Measurement Setup: 10^{-12} bit error rate (BER), >1 Meg samples recorded using multiple acquisitions Oscilloscope Setup: 20 mV/div vertical scale, 100 µs/div horizontal scale, and 25 GS/s sampling rate
(9) t_{D_SD} is measured from the VCXO clock input (pin 29) to the SD_CLK output (pins 23, 24) using positive edges and 50% levels. The measurement is taken at the leading edge of the TOF pulse, where the input and output clocks are phase aligned at the start of frame.
(10) t_{D_HD} is measured from the VCXO clock input (pin 29) to the HD_CLK output (pins 19, 20) using positive edges and 50% levels. The measurement is taken at the leading edge of the TOF pulse, where the input and output clocks are phase aligned at the start of frame.
(11) This parameter is specified for the SD_CLK output only. This parameter is ensured by design for the HD_CLK output.

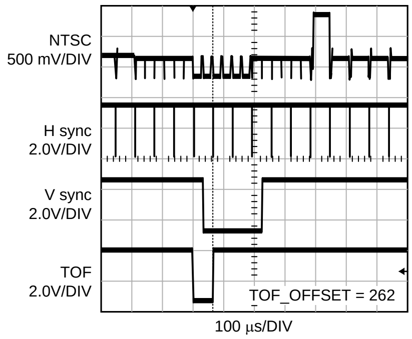
Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 3.3 V, DV_{DD} = 2.5 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
I_{OS}	Output Short Circuit Current	Differential clock output pins connected to GND			24	|mA|
I_{OZ}	Output Hi-Z Leakage Current	Output clock in Hi-Z mode, differential clock output pins connected to V_{DD} or GND		1	10	|µA|

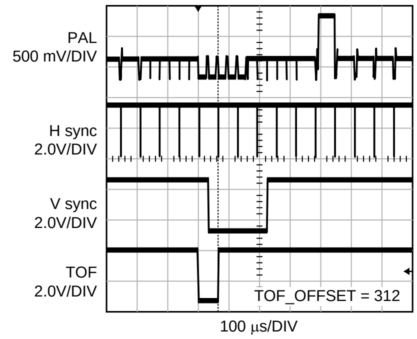
6.6 Typical Characteristics

Test conditions: V_{DD} = 3.3V, D_{VDD} = 2.5V, Genlock mode, outputs initialized. H sync and V sync signals to REF_A inputs are from the LMH1981 sync separator, which receives an analog video reference signal from a Tektronix TG700 AVG7/AWVG7 (SD/HD) video signal generator. See the table notes below for register settings (in decimal):



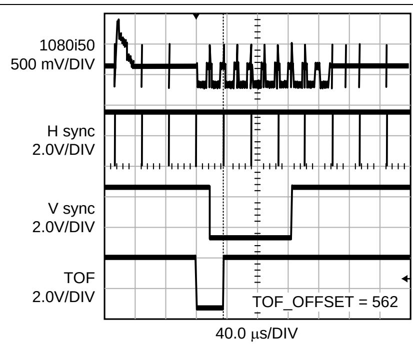
GNLK = 1, REF_DIV_SEL = 1, FB_DIV = 1716, SD_FREQ = 0, TOF_CLK = 0, TOF_PPL = 1716, TOF_LPFM = 525, REF_LPFM = 525, TOF_OFFSET = 262; all other register settings are default

Figure 1. NTSC TOF Pulse



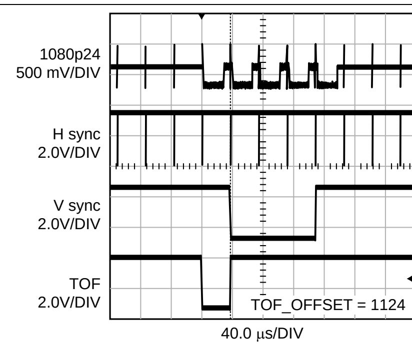
GNLK = 1, REF_DIV_SEL = 1, FB_DIV = 1728, SD_FREQ = 0, TOF_CLK = 0, TOF_PPL = 1728, TOF_LPFM = 625, REF_LPFM = 625, TOF_OFFSET = 312; all other register settings are default

Figure 2. PAL TOF Pulse



GNLK = 1, REF_DIV_SEL = 1, FB_DIV = 960, SD_FREQ = 0, HD_FREQ = 0, TOF_CLK = 0, TOF_PPL = 960, TOF_LPFM = 1125, REF_LPFM = 1125, TOF_OFFSET = 562; all other register settings are default

Figure 3. 1080i/50 TOF Pulse



GNLK = 1, REF_DIV_SEL = 1, FB_DIV = 1000, SD_FREQ = 0, HD_FREQ = 0, TOF_CLK = 0, TOF_PPL = 1000, TOF_LPFM = 1125, REF_LPFM = 1125, TOF_OFFSET = 1124; all other register settings are default

Figure 4. 1080p/24 TOF Pulse

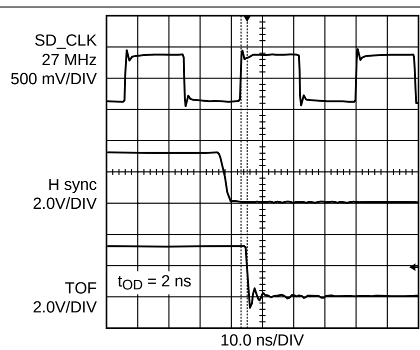


Figure 5. 525i TOF Output Delay Using 27 MHz TOF Clock

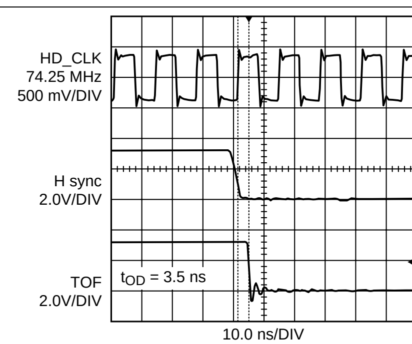


Figure 6. 1080i/50 TOF Output Delay Using 74.25 MHz TOF Clock

7 Detailed Description

7.1 Overview

The LMH1982 is an analog phase locked loop (PLL) clock generator that can output simultaneous SD and HD video clocks synchronized or "genlocked" to H sync and V sync input reference timing. The LMH1982 features an output Top of Frame (TOF) pulse generator with programmable timing that can also be synchronized to the reference frame. Two reference ports are provided to allow a secondary input to be selected.

The clock generator uses a two-stage PLL architecture. The first stage is a VCXO-based PLL (PLL 1) that requires an external 27 MHz VCXO and loop filter. In Genlock mode, PLL 1 can phase lock the VCXO clock to the input reference after programming the PLL divider ratio. The use of a VCXO provides a low phase noise clock source even when the LMH1982 is configured with a low loop bandwidth, which is necessary to attenuate input timing jitter for minimum jitter transfer. The combination of the external VCXO, external loop filter, and programmable PLL parameters can provide flexibility for the system designer to optimize the loop bandwidth and loop response for the application.

The second stage consists of three PLLs (PLL 2, 3, 4) with integrated VCOs and loop filters. These PLLs will attempt to continually track the reference VCXO clock phase from PLL 1 regardless of the device mode. The second stage PLLs have pre-configured divider ratios to provide frequency multiplication or translation from the VCXO clock frequency. The VCO PLLs use a high loop bandwidth to assure PLL stability, so the VCXO must provide a stable low-jitter clock reference to ensure optimal output jitter performance.

Any unused clock output can be put in Hi-Z mode, which can be useful for reducing power dissipation as well as reducing jitter or phase noise on the active clock output.

The TOF pulse can be programmed to indicate the start (top) of frame and even provide format cross-locking. The output format registers should be programmed to specify the output timing (output clocks and TOF pulse), the output timing offset relative to the reference, and the output initialization (alignment) to the reference frame. If unused, the TOF output can also be put in Hi-Z mode.

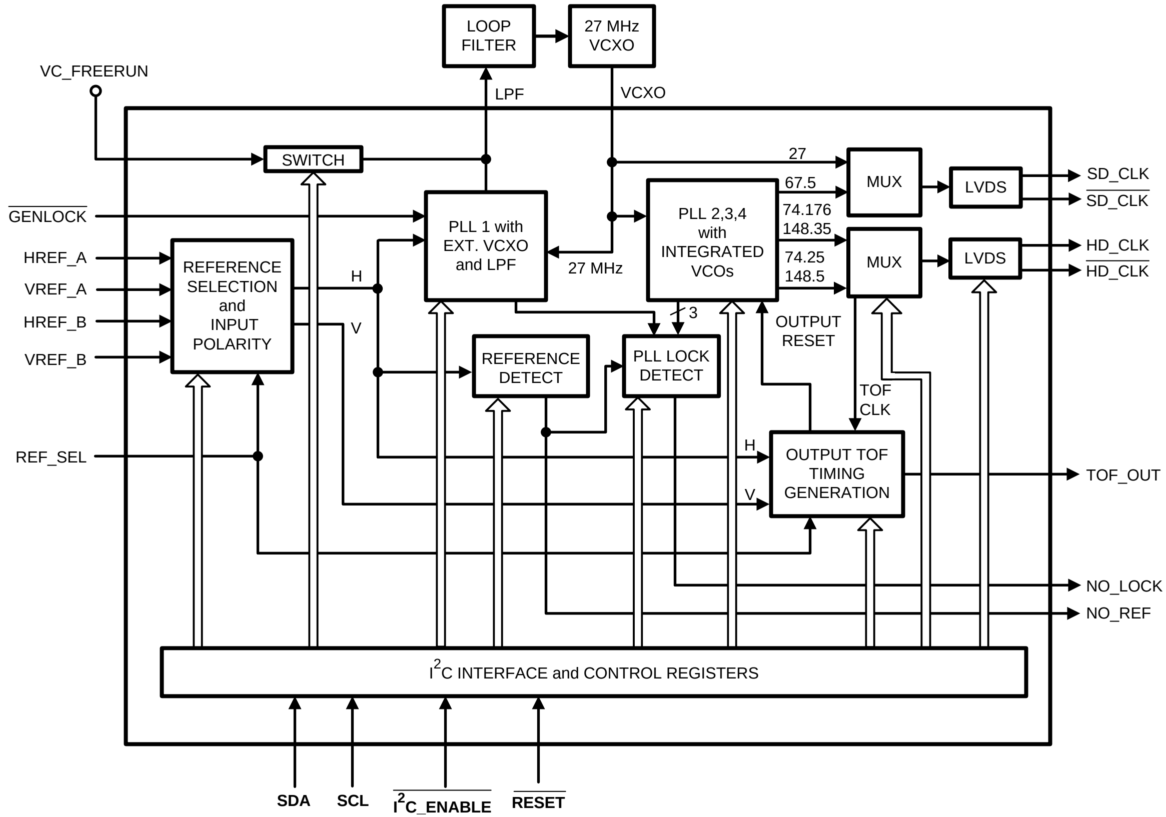
When a loss of reference occurs during genlock, PLL 1 can default to either Free run or Holdover operation. When free run is selected, the output frequency accuracy will be determined by the external bias on the free run control voltage input pin, VC_FREERUN. When Holdover is selected, the loop filter can hold the control voltage to maintain short-term output phase accuracy for a brief period in order to allow the application to select the secondary input reference and re-lock the outputs. These options in combination with proper PLL 1 loop response design can provide flexibility to manage output clock behavior during loss and re-acquisition of the reference.

The reference status and PLL lock status flags can provide real-time status indication to the application system. The loss of reference and lock detection thresholds can also be configured.

Table 1. LMH1982 PLL and Clock Summary

PLL	Input Reference	Divider Ratio (reduced)	Output Clock Frequency (MHz)	Output Port
PLL 1	H sync	Programmable	27	SD_CLK
PLL 2	VCXO clock	11/4 or 11/2	74.25 or 148.5	HD_CLK
PLL 3	VCXO clock	250/91 or 500/91	74.25/1.001 (74.176) or 148.5/1.001 (148.35)	HD_CLK
PLL 4	VCXO clock	5/2	67.5	SD_CLK

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supported Standards and Timing Formats

Table 2 lists the known supported standard timing formats and includes the relevant parameters that can be used to configure the LMH1982 for the input reference and output timing. For the related programming instructions, see sections *Input Reference* and *Output Clocks and TOF*.

Table 2. Input Reference and Output Timing Parameters (1)(2)

Format	INPUT TIMING PARAMETERS (1)				OUTPUT TIMING PARAMETERS (2)			
	PLL 1 Reference Divider[1](3)	PLL 1 Feedback Divider	PLL 1 Phase Comparison Frequency (kHz)	Total Lines per Frame Counter	Clock Frequency (MHz)	Total Clocks per Line Counter	Total Lines per Frame Counter	Frame Rate (Hz)
NTSC, 525i	1	1716	15.7343	525	27.0	1716	525	29.97
PAL, 625i	1	1728	15.625	625	27.0	1728	625	25
525p	1 [5]	858 [4290]	31.4685 [6.2937]	525 [105]	27.0	858	525	59.94
625p	1 [5]	864 [4320]	31.25 [6.25]	625 [125]	27.0	864	625	50

(1) For some input reference formats, an alternative set of values for PLL 1 dividers and total lines per frame (REF_LPFM) is also shown in **brackets "[ ]"**. This alternative set of values may be programmed if a lower PLL 1 phase comparison frequency is desired. The corresponding counter values for REF_LPFM needs to be programmed for proper reference frame and output timing generation. See *Reference Frame Timing*.
(2) For any output HD format, an alternative set of counter values for total clocks per line (TOF_PPL) and total lines per frame (TOF_LPFM) is shown in **parenthesis "( )"**. This alternative set of values can be programmed to generate any HD format TOF pulse using the 27 MHz SD_CLK instead of using the native 74.xx or 148.xx MHz HD_CLK. See *HD Format TOF Generation Using a 27-MHz TOF Clock*.
(3) The PLL 1 reference divider value is not the same as the programming value for REF_DIV_SEL. See Table 8.

Feature Description (continued)

Table 2. Input Reference and Output Timing Parameters (1)(2) (continued)

Format	INPUT TIMING PARAMETERS (1)				OUTPUT TIMING PARAMETERS (2)			
	PLL 1 Reference Divider1(3)	PLL 1 Feedback Divider	PLL 1 Phase Comparison Frequency (kHz)	Total Lines per Frame Counter	Clock Frequency (MHz)	Total Clocks per Line Counter	Total Lines per Frame Counter	Frame Rate (Hz)
720p/60	1 [5]	600 [3000]	45.0 [9.0]	750 [150]	74.25 (27.0)	1650 (600)	750 (750)	60
720p/59.94	5	3003	8991.0090	750	74.176 (27.0)	1650 (3003)	750 (150)	59.94
720p/50	1 [5]	720 [3600]	37.5 [7.5]	750 [150]	74.25 (27.0)	1980 (720)	750 (750)	50
720p/30	1 [5]	1200 [6000]	22.5 [4.5]	750 [150]	74.25 (27.0)	3300 (1200)	750 (150)	30
720p/29.97	5	6006	4.4955	750	74.176 (27.0)	3300 (6006)	750 (150)	29.97
720p/25	1 [5]	1440 [7200]	18.75 [3.75]	750 [150]	74.25 (27.0)	3960 (1440)	750 (750)	25
720p/24	1 [5]	1500 [7500]	18.0 [3.6]	750 [150]	74.25 (27.0)	4125 (1500)	750 (750)	24
720p/23.98	2	3003	8991.0090	750	74.176 (27.0)	4125 (3003)	750 (375)	23.98
1080p/60	1 [5]	400 [2000]	67.5 [13.5]	1125 [225]	148.5 (27.0)	2200 (400)	1125 (1125)	60
1080p/59.94	5	2002	13.4865	1125	148.35 (27.0)	2200 (2002)	1125 (225)	59.94
1080p/50	1 [5]	480 [2400]	56.25 [11.25]	1125 [225]	148.5 (27.0)	2640 (480)	1125 (1125)	50
1080p/30	1 [5]	800 [4000]	33.75 [6.75]	1125 [225]	74.25 (27.0)	2200 (800)	1125 (1125)	30
1080p/29.97	5	4004	6.7433	1125	74.176 (27)	2200 (4004)	1125 (225)	29.97
1080p/25	1 [5]	960 [4800]	28.125 [5.625]	1125 [225]	74.25 (27.0)	2640 (960)	1125 (1125)	25
1080p/24	1 [5]	1000 [5000]	27.0 [5.4]	1125 [225]	74.25 (27.0)	2750 (1000)	1125 (1125)	24
1080p/23.98	1 [5]	1001 [5005]	26.9730 [5.3946]	1125 [225]	74.176 (27.0)	2750 (1001)	1125 (1125)	23.98
1080i/60	1 [5]	800 [4000]	33.75 [6.75]	1125 [225]	74.25 (27.0)	2200 (800)	1125 (1125)	30
1080i/59.94	5	4004	6.7433	1125	74.176 (27.0)	2200 (4004)	1125 (225)	29.97
1080i/50	1 [5]	960 [4800]	28.125 [5.625]	1125 [225]	74.25 (27.0)	2640 (960)	1125 (1125)	25
48 kHz AES sample clock	2	1125	24.0	96	27.0	1125	96	250

7.4 Device Functional Modes

7.4.1 Modes of Operation

The mode of operation describes the operation of PLL 1, which can operate in either Free Run mode or Genlock mode depending on the GNLK bit setting. If desired, the GENLOCK input pin can be instead used to control the mode of operation by initially setting I^2C_GNLK = 0 (register 00h).

7.4.1.1 Free Run Mode

The LMH1982 will enter Free Run mode when GNLK is set to 0. In Free Run mode, the VCXO will be free-running and independent of the input reference, and the output clocks will maintain phase lock to the VCXO clock reference. Therefore, the output clocks will have the same accuracy as the VCXO clock reference.

The LMH1982 provides the designer with the option to define the VCXO's free run control voltage by external biasing of the VC_FREERUN input (pin 1). The analog bias voltage applied to the VC_FREERUN input will be connected to the LPF output (pin 31) though an internal switch (non-buffered, low impedance), as shown in the *Functional Block Diagram*. The resultant voltage at the LPF output will drive the control input of the VCXO to set its free run output frequency. Thus, the pull range of the VCXO imparts the same pull range on the free run output clocks.

If VC_FREERUN is left floating, the VCXO control voltage will be pulled to GND potential as the residual charge stored across the loop filter will discharge through any existing leakage path.

7.4.1.2 Genlock Mode

The LMH1982 will enter Genlock mode when GNLK is set to 1. In Genlock mode, PLL 1 can be phase locked to the reference H sync input of the selected port; once the VCXO clock reference is locked and stable, the output clocks and TOF pulse can be aligned and phase locked to the reference. The LMH1982 supports cross-locking, which allows the outputs to be frame-locked to a reference format that is different from the output format.

To genlock the outputs, the following programming sequence is suggested:

1. Program the output clock frequency for the desired output format. See *Programming the Output Clock Frequencies* for more information.
2. Program the output TOF timing for the desired output format. See *Programming the Output Format Timing* for more information. It is required to complete this step for proper output clock initialization (alignment) even if the TOF pulse is not required.
3. Program the PLL 1 divider registers for the input reference format. See *Programming the PLL 1 Dividers* for more information.
4. Program GNLK = 1 to enable Genlock mode.

NOTE

When Genlock mode is enabled, the LMH1982 will attempt to phase lock the PLLs to the input reference regardless of input timing stability. Timing errors or instability on the inputs will cause the PLLs and outputs to also have instability. If output stability is a consideration during periods of input uncertainty, it is suggested to gate off the input signals from the LMH1982 until they are completely stable. Input signal gating can be achieved externally using a discrete or FPGA logic buffer with Hi-Z (tri-state) output and a pull-up or pull-down resistor, depending on the input pulse signal polarity.

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5. Program the output initialization to the desired reference frame. See *Programming the Output Initialization Sequence* for more information.

7.4.1.2.1 Genlock Mode State Diagram

Figure 7 shows the Genlock mode state diagram for different input reference and PLL lock conditions. It also includes Free Run and Holdover states for the loss of reference operation, specified by the HOLDOVER bit (register 00h). Each state indicates the NO_REF and NO_LOCK status flag output conditions.

Device Functional Modes (continued)

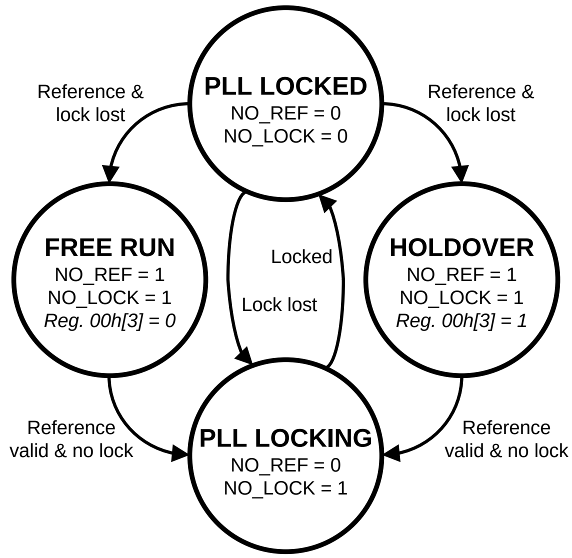

Figure 7. Genlock Mode State Diagram

7.4.1.2.1.1 Loss of Reference (LOR)

By configuring the HOLDOVER bit, the LMH1982 can default to either Free Run or Holdover operation when a loss of reference (LOR) occurs in Genlock mode.

If HOLDOVER = 0 when a LOR occurs, the LMH1982 will default to Free run operation (*Free Run during LOR*) until a reference is reapplied.

If HOLDOVER = 1 when a LOR occurs, the LMH1982 will default to Holdover operation (*Holdover during LOR*) until a reference is reapplied.

When the input reference is reapplied, the LMH1982 will immediately attempt to phase lock the output clocks to the reference.

7.4.1.2.1.1.1 Free Run during LOR

Free Run mode (GNLK = 0) differs from Free Run operation due to LOR in Genlock mode (GNLK = 1) in the following way:

- In Free Run mode, the outputs will free run regardless of the presence or loss of reference.
- In Genlock mode, the outputs will free run only during LOR; once a reference is present, free run operation will cease as the PLLs will immediately attempt to phase lock the output clocks to the reference.

7.4.1.2.1.1.2 Holdover during LOR

In Holdover operation, the LPF output is put into high impedance mode, which allows the loop filter to temporarily hold the residual charge stored across it (i.e. the control voltage) immediately after LOR is indicated by the NO_REF status flag. Holdover operation can help to temporarily sustain the output clock accuracy upon LOR. The duration that the residual control voltage level can be sustained within a tolerable level depends primarily on the charge leakage on the loop filter. A typical VCXO has an input impedance of several tens of kΩ, which will be the dominant leakage path seen by the loop filter. As the leakage current discharges the residual control voltage to GND, the output frequencies of the VCXO and LMH1982 will drift accordingly. If a longer time constant is required, a precision op amp with low input bias current and rail-to-rail input and output (e.g. LMP7701) can be used to buffer the control voltage. The buffer will isolate the relatively low input impedance of the VCXO and reduce the charge leakage on the loop filter during Holdover.

Device Functional Modes (continued)

The output frequency accuracy will degrade as the VCXO accuracy drifts with the decaying control voltage. Moreover, because the H_ERROR setting (register 00h) affects the reference error threshold for LOR indication, a higher setting for H_ERROR may result in reduced output accuracy upon LOR indication compared to when H_ERROR = 0. For more information on programming H_ERROR, see *Programming the Loss of Reference (LOR) Threshold*.

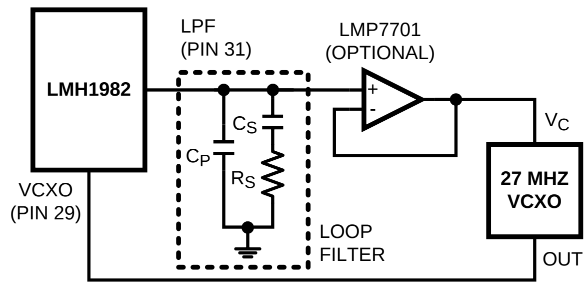

Figure 8. Loop Filter with Optional Op Amp to Isolate VCXO's Low Input Impedance

7.5 Programming

7.5.1 I²C Interface Protocol

The protocol of the I^2C interface begins with the start pulse followed by a byte comprised of a seven-bit slave device address and a read/write bit as the LSB. Therefore, the address of the LMH1982 for write sequences is DCh (1101 1100) and the address for read sequences is DDh (1101 1101). Figure 9, Figure 10, and Figure 11 show a write and read sequence across the I^2C interface.

7.5.1.1 Write Sequence

The write sequence begins with a start condition, which consists of the master pulling SDA low while SCL is held high. The slave device address is sent next. The address byte is made up of an address of seven bits (7:1) and the read/write bit (0). Bit 0 is low to indicate a write operation. Each byte that is sent is followed by an acknowledge (ACK) bit. When SCL is high the master will release the SDA line. The slave must pull SDA low to acknowledge. The address of the register to be written to is sent next. Following the register address and the ACK bit, the data byte for the register is sent. When more than one data byte is sent, it is automatically incremented into the next address location. See Figure 9. Note that each data byte is followed by an ACK bit.

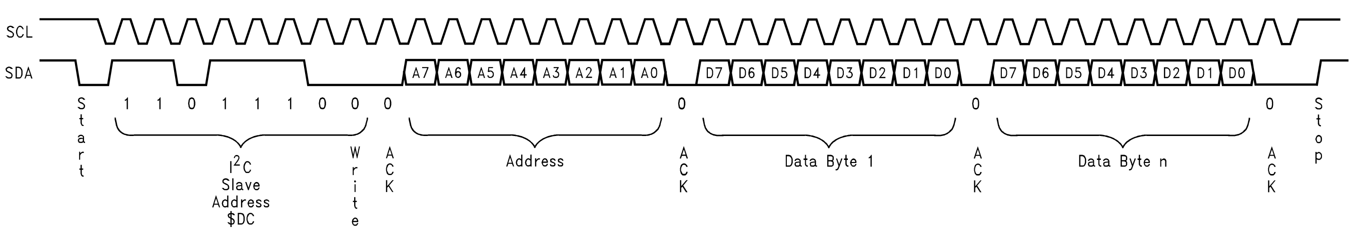

Figure 9. LMH1982 Write Sequence

7.5.1.2 Read Sequence

Read sequences are comprised of two I^2C transfers. The first is the address access transfer, which consists of a write sequence that transfers only the address to be accessed. The second is the data read transfer, which starts at the address accessed in the first transfer and increments to the next address per data byte read until a stop condition is encountered.

The address access transfer shown in Figure 10 consists of a start pulse, the slave device address including the read/write bit (a zero, indicating a write), then its ACK bit. The next byte is the address to be accessed, followed by the ACK bit and the stop bit to indicate the end of the address access transfer.

Programming (continued)

The subsequent read data transfer shown in Figure 11 consists of a start pulse, the slave device address including the read/write bit (a one, indicating a read) and the ACK bit. The next byte is the data read from the initial access address. Subsequent read data bytes will correspond to the next increment address locations. Each data byte is separated from the other data bytes by an ACK bit.

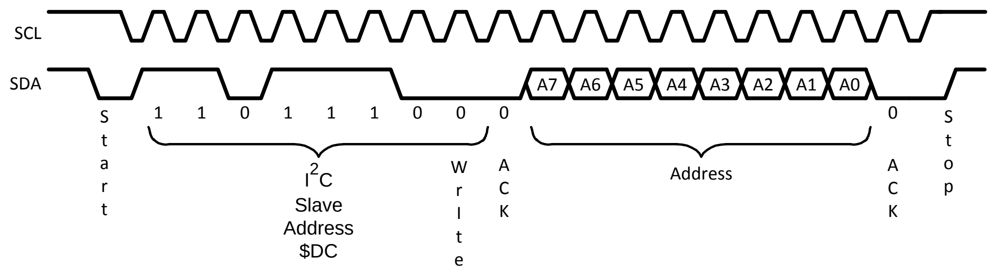

Figure 10. LMH1982 Read Sequence – Address Access Transfer

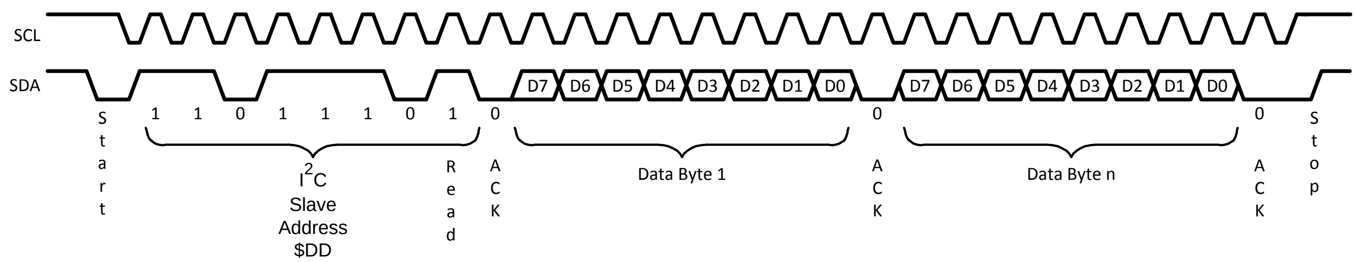

Figure 11. LMH1982 Read Sequence – Data Read Transfer

7.5.1.3 I²C Enable Control Pin

When the active low input $\overline{\text{I2C\_ENABLE}}$ = 0, the LMH1982 will enable I²C communication via its fixed slave address; otherwise, the LMH1982 will not respond. For applications with multiple LMH1982 devices on the same I²C bus, the I²C enable function can be useful for writing data to a specific device(s) and for reading data from an individual device to prevent bus contention. For single chip applications, the $\overline{\text{I2C\_ENABLE}}$ input can be tied to GND to keep the I²C interface enabled.

7.6 Register Maps

7.6.1 I^{2}C Interface Control Register Definitions

Table 3. I^{2}C Interface Control Register Map(1)

Register Address	Default Data	D7	D6	D5	D4	D3	D2	D1	D0
00h	A3h	GNLK_I^{2}C	GNLK	RSEL_I^{2}C	RSEL	HOLD-OVER	H_ERROR [2:0]		
01h	86h	LOCK_CTRL [7:3]					HD_LOCK	SD_LOCK	REF_VALID
02h	00h	RSV	RSV	PIN6_ OVRD	REF_27	POL_HA	POL_VA	POL_HB	POL_VB
03h	01h	RSV	RSV	RSV	RSV	RSV	RSV	REF_DIV_SEL [1:0]	
04h	B4h	FB_DIV [7:0]							
05h	06h	0	0	0	FB_DIV [12:8]				
06h	00h	RSV	RSV	RSV	RSV	ICP4 [3:0]			
07h	00h	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
08h	04h	RSV	RSV	TOF_HIZ	HD_HIZ	HD_FREQ [3:2]		SD_HIZ	SD_FREQ
09h	01h	TOF_RST [7:0]							
0Ah	00h	EN_TOF_ RST	POL_TOF	TOF_INIT	TOF_RST [12:8]				
0Bh	B4h	TOF_PPL [7:0]							
0Ch	06h	0	0	TOF_CLK	TOF_PPL [12:8]				
0Dh	0Dh	TOF_LPFM [7:0]							
0Eh	02h	0	0	0	0	TOF_LPFM [11:8]			
0Fh	0Dh	REF_LPFM [7:0]							
10h	02h	0	0	0	0	REF_LPFM [11:8]			
11h	00h	TOF_OFFSET [7:0]							
12h	00h	0	0	0	0	TOF_OFFSET [11:8]			
13h	88h	RSV	RSV	RSV	ICP1 [4:0]				
14h	88h	ICP2 [7:4]				ICP3 [3:0]			

(1) When writing to registers containing reserved bits (RSV), make sure the RSV bits are programmed with their original default data shown in column 2 of Table 3; otherwise, improper device operation may result.

7.6.1.1 Genlock and Input Reference Control Registers

Register 00h

Bits 2-0: H Input Error Max Count (H_ERROR)

The H_ERROR bits control the reference detector's error threshold, which determines the maximum number of missing H sync pulses before indicating a LOR. See *Programming the Loss of Reference (LOR) Threshold* for more information.

Bit 3: Holdover on Loss of Reference (HOLDOVER)

The HOLDOVER bit controls the operating mode when a loss of reference occurs. See *Loss of Reference (LOR)* for more information.

Bit 4: Reference Select (RSEL)

The RSEL bit selects either REF_A or REF_B inputs as the reference to genlock the outputs when I^{2}C_RSEL = 1.

RSEL = 0: Select REF_A inputs.

RSEL = 1: Select REF_B inputs.

If PIN6_OVRD = 1 (register 02h), then reference selection must be controlled by programming RSEL, regardless of I^2C_RSEL. When PIN6_OVRD = 0 and I^2C_RSEL = 0, then reference selection is controlled using the REF_SEL input pin and the RSEL bit is ignored.

Bit 5: Reference Select Control via I^2C (I^2C_RSEL)

By programming I^2C_RSEL, reference selection can be controlled either via I^2C or the REF_SEL input pin.

I^2C_RSEL = 1: Control reference selection by programming RSEL.

I^2C_RSEL = 0: Control reference selection via the REF_SEL input pin.

NOTE

If PIN6_OVRD = 1, then reference selection must be controlled by programming RSEL regardless of I^2C_RSEL.

Bit 6: Mode Select (GNLK)

The GNLK bit selects the operating mode when I^2C_GNLK = 1. See *Modes of Operation* for more information.

GNLK = 0: Selects Free Run mode.

GNLK = 1: Selects Genlock mode.

If I^2C_GNLK = 0, then the operating mode will be controlled using the $\overline{\text{GENLOCK}}$ input pin and the GNLK bit will be ignored.

Bit 7: Mode Select via I^2C (I^2C_GNLK)

By programming I^2C_GNLK, mode selection can be controlled either via I^2C or the $\overline{\text{GENLOCK}}$ input pin.

I^2C_GNLK = 1: Control mode selection by programming GNLK.

I^2C_GNLK = 0: Control mode selection through the $\overline{\text{GENLOCK}}$ input pin.

7.6.1.2 Genlock Status And Lock Control Register

Register 01h

Bit 0: Reference Status (REF_VALID)

REF_VALID is a read-only bit and indicates the presence or loss of reference on the selected reference port in Genlock mode. The NO_REF output flag is an inverted copy of REF_VALID. See *Reference Detection* for more information.

REF_VALID = 0: Indicates loss of reference (LOR).

REF_VALID = 1: Indicates valid reference.

In Free Run mode, REF_VALID will be set to 0 to indicate the absence of any input pulses at the selected HREF port.

Bit 1: SD Clock PLL Lock Status (SD_LOCK)

SD_LOCK is a read-only bit and indicates PLL lock status of the selected SD clock. See *PLL Lock Detection* for more information.

SD_LOCK = 0: Indicates loss of lock.

SD_LOCK = 1: Indicates valid lock.

Bit 2: HD Clock PLL Lock Status (HD_LOCK)

HD_LOCK is a read-only bit and indicates PLL lock status of the selected HD clock. See *PLL Lock Detection* for more information.

HD_LOCK = 0: Indicates loss of lock.

HD_LOCK = 1: Indicates valid lock.

Bits 7-3: Lock Control (LOCK_CTRL)

LOCK_CTRL controls the phase error threshold of PLL 1's lock detector. A larger value for LOCK_CTRL will yield shorter lock indication time (although not actual lock time) at the expense of higher output phase error when lock is initially indicated, whereas a smaller value will yield the opposite effect. See *Programming the PLL Lock Threshold* for more information.

7.6.1.3 Input Control Register

Register 02h

Bit 0: VREF_B Input Signal Polarity (POL_VB)

This bit should be programmed to match the input signal polarity at the VREF_B input pin.

POL_VB = 0: Negative polarity or active low signal.

POL_VB = 1: Positive polarity or active high signal.

Bit 1: HREF_B Input Signal Polarity (POL_HB)

This bit should be programmed to match the input signal polarity at the HREF_B input pin. The positive edge of the output clock will be phase locked to the active edge of the H sync input signal.

POL_HB = 0: Negative polarity or active low signal.

POL_HB = 1: Positive polarity or active high signal.

Bit 2: VREF_A Input Signal Polarity (POL_VA)

This bit should be programmed to match the input signal polarity at the VREF_A input pin.

POL_VA = 0: Negative polarity or active low signal.

POL_VA = 1: Positive polarity or active high signal.

Bit 3: HREF_A Input Signal Polarity (POL_HA)

This bit should be programmed to match with the input signal polarity at HREF_A input pin. The positive edge of the output clock will be phase locked to the active edge of the H sync input signal.

POL_HA = 0: Negative polarity or active low signal.

POL_HA = 1: Positive polarity or active high signal.

Bit 4: 27 MHz Reference Control (27M_REF)

Instead of an H sync signal, a 27 MHz clock signal can be applied to the selected HREF input to phase lock the output clocks. If a 27 MHz clock is used as a reference, then a value of 1 should be programmed to 27M_REF, REF_DIV_SEL, and FB_DIV.

27M_REF = 0: H sync input signal.

27M_REF = 1: 27 MHz clock input signal. Also, set REF_DIV_SEL =1 and FB_DIV = 1

NOTE

Because the loop gain, K, for 27 MHz clock input is much larger than for an H sync input (due to the large difference in FB_DIV), the loop filter design will be necessarily different between the 27 MHz input and H sync inputs. Alternatively, it's possible to use an external counter circuit to divide the 27 MHz clock to a lower frequency (e.g. like H sync) input, so only one loop filter design could support both types of inputs.

Bit 5: Pin 6 Override (PIN6_OVRD)

The PIN6_OVRD bit can be programmed to override the default reference selection capability on pin 6 and instead use pin 6 as an logic pulse input to initialize or reset the internal counters for output initialization.

PIN6_OVRD = 0: Allows a logic level input to be applied to pin 6 for reference selection if RSEL_I^{2}C = 0 (register 00h). If RSEL_I^{2}C = 1, then pin 6 is ignored and reference selection is controlled via I^{2}C; additionally, outputs must be initialized via I^{2}C by programming TOF_INIT and EN_TOF_RST (register 0Ah).

PIN6_OVRD = 1: Allows an TOF Init pulse to be applied to pin 6 for output initialization if EN_TOF_RST = 1. If EN_TOF_RST = 0, then any TOF Init pulse received at pin 6 will be ignored. Additionally, reference selection must be controlled via I^2C, regardless of I^2C_RSEL.

Bits 7-6: Reserved (RSV)

These RSV bits are reserved. When writing to this register, only write the default data to the RSV bits as specified in Table 3.

7.6.1.4 PLL 1 Divider Register

Register 03h

Bits 1-0: Reference Divider Selection (REF_DIV_SEL)

REF_DIV_SEL selects the reference divider value according to the selection table in Table 1. See *Programming the PLL 1 Dividers* for more information.

The reference divider value is the denominator of PLL 1's divider ratio:

Feedback divider value / Reference divider value = 27 MHz / Hsync input frequency

The numerator and denominator values of the divider ratio should be reduced to their lowest factors to be compatible with the range of divider values offered by REF_DIV_SEL and FB_DIV. These registers must be programmed correctly to phase lock the 27 MHz VCXO PLL and output clocks to the input reference. See Table 2 for the suggested divider settings for the supported timing formats.

Bits 7-3: Reserved (RSV)

These RSV bits are reserved. When writing to this register, only write the default data to the RSV bits as specified in Table 3.

Register 04h

Bits 7-0: Feedback Divider (FB_DIV)

This register contains the 8 LSBs of FB_DIV. The feedback divider value is the numerator of PLL 1's divider ratio. FB_DIV should be programmed using the feedback divider value after the divide ratio has been reduced to its lowest factors. Refer to the description for register 03h, and see Table 2 for the suggested divider settings for the supported timing format.

Register 05h

Bits 4-0: Feedback Divider (FB_DIV)

This register contains the 5 MSBs of FB_DIV. See the description for register 04h.

Bits 7-5: These non-programmable bits contain zeros.

7.6.1.5 PLL 4 Charge Pump Current Control Register

Register 06h

Bits 3-0: Charge Pump Current Control for PLL 4 (ICP4)

ICP4 can be programmed to specify charge pump current for PLL 4, which generates the 67.5 MHz SD clock.

NOTE

Bit 3 is inverted internally, so the default ICP4 value of 0000b (0h) actually yields an effective value of 1000b (8h), which is the mid-scale setting.

The PLL 4 charge pump current increases linearly with the effective value. Reducing the effective value of the charge pump current will lower its loop bandwidth at the expense of reduced PLL stability. An effective value of 0 (ICP4 = 1000b) should not be programmed since this corresponds to 0 µA nominal current and will cause PLL 4 to lose phase lock.

Bits 7-4: Reserved (RSV)

These RSV bits are reserved. When writing to this register, only write the default data to the RSV bits as specified in Table 3.

Register 07h

Bits 7-0: Reserved (RSV)

This register is reserved. If necessary, only write the default data (00h) to register 07h as specified in Table 3.

7.6.1.6 Output Clock and TOF Control Register

Register 08h

Bit 0: SD Clock Output Frequency Select (SD_FREQ)

This bit sets the clock frequency of the SD_CLK output pair.

SD_FREQ = 0: Selects 27 MHz from PLL 1.

SD_FREQ = 1: Selects 67.5 MHz from PLL 4.

Bit 1: SD Clock Output Mode (SD_HIZ)

Set the SD_HIZ bit to 1 to put the SD_CLK output pair in high-impedance (Hi-Z) mode; otherwise, the SD_CLK output will be enabled.

Bit 3-2: HD Clock Output Frequency Select (HD_FREQ)

These bits set the clock frequency of the HD_CLK output pair.

HD_FREQ = 0h: Selects 74.25 MHz from PLL 2.

HD_FREQ = 1h: Selects 74.176 MHz from PLL 3.

HD_FREQ = 2h: Selects 148.5 MHz from PLL 2.

HD_FREQ = 3h: Selects 148.35 MHz from PLL 3.

NOTE

When selecting the 148.35 MHz clock, you must also program the PLL 3 initialization sequence as described in *148.35 MHz PLL Initialization Sequence*.

Bit 4: HD Clock Output Mode (HD_HIZ)

Set the HD_HIZ bit to 1 to put the HD_CLK output pair in high-impedance (Hi-Z) mode; otherwise, the HD_CLK output will be enabled.

Bit 5: Top of Frame Output Mode (TOF_HIZ)

Set the TOF_HIZ bit to 1 to put the TOF output pin in high-impedance (Hi-Z) mode; otherwise, the output will be enabled.

Bits 7-6: Reserved (RSV)

These RSV bits are reserved. When writing to this register, only write the default data to the RSV bits as specified in Table 3.

7.6.1.7 TOF Configuration Registers

Register 09h

Bits 7-0: TOF Reset (TOF_RST)

This register contains the 8 LSBs of TOF_RST. When PLL 1 is phase locked to the reference, both H sync and V sync inputs are used to reset the frame-based counters used for output TOF generation. The numerator value of the reduced frame rate ratio should be programmed to TOF_RST. See *Input-Output Frame Rate Ratio* for more information.

Once TOF_RST is programmed, the outputs must be properly initialized by either programming TOF_INIT or otherwise using an external TOF Init pulse (when PIN6_OVRD = 1).

Register 0Ah

Bits 4-0: TOF Reset (TOF_RST)

This register contains the 5 MSBs of TOF_RST. See the description for register 09h.

Bit 5: Output Initialization (TOF_INIT)

After enabling output alignment mode (EN_TOF_RST = 1), the TOF_INIT bit should be programmed to reset the internal counters and initialize (align) the outputs to the desired reference frame. The output initialization is triggered by programming a positive bit transition (0 to 1) to TOF_INIT. See *Programming the Output Initialization Sequence* for more information.

Bit 6: TOF Pulse Output Polarity (POL_TOF)

This bit should be programmed to the desired TOF pulse polarity at the TOF output.

POL_TOF = 0: Negative polarity or active low signal.

POL_TOF = 1: Positive polarity or active high signal.

Bit 7: Output Alignment Mode (EN_TOF_RST)

This bit must be set (EN_TOF_RST = 1) to enable output alignment mode prior to initialization per *Programming the Output Initialization Sequence*. It is recommended to clear this bit (EN_TOF_RST = 0) immediately after the output initialization sequence has been programmed to prevent excessive output jitter, as described in *Output Disturbance While Output Alignment Mode Enabled*.

Register 0Bh

Bits 7-0: Total Pixels per Line for the Output Format (TOF_PPL)

This register contains the 8 LSBs of TOF_PPL. TOF_PPL should be programmed with total pixels per line for the desired output format. TOF_PPL is used in specifying the output frame rate. This should be specified prior to programming the output initialization sequence. See *Output Frame Timing* for more information.

Register 0Ch

Bits 4-0: MSBs of Total Pixels per Line for the Output Format (TOF_PPL)

This register contains the 5 MSBs of TOF_PPL. See the description for register 0Bh.

Bit 5: Output Clock Select for Output Top of Frame (TOF_CLK)

This bit should be programmed to select the output TOF clock reference according to the desired output format. The selected TOF clock frequency is used in specifying the output frame rate. Any output format, including HD, can use 27 MHz as the TOF clock to generate its TOF pulse by programming the output counter values corresponding to the 27 MHz SD clock as shown in Table 2. See sections *Output TOF Clock* and *Output Frame Timing*.

TOF_CLK = 0: Selects the SD_CLK output as the output clock reference, where the SD frequency is set by SD_FREQ.

TOF_CLK = 1: Selects the HD_CLK output as the output clock reference.

Bit 7-6: These non-programmable bits contain zeros.

Register 0Dh

Bits 7-0: LSBs of Total Lines per Frame for the Output Format (TOF_LPFM)

This register contains the 8 LSBs of TOF_LPFM. TOF_LPFM should be programmed with the total lines per frame for the desired output format. TOF_LPFM is used in specifying the output frame rate. This should be specified prior to programming the output initialization sequence. See *Output Frame Timing* for more information.

Register 0Eh

Bits 3-0: MSBs of Total Lines per Frame for the Output Format (TOF_LPFM)

This register contains the 4 MSBs of TOF_LPFM. See the description for register 0Dh.

Bit 7-5: These non-programmable bits contain zeros.

Register 0Fh

Bits 7-0: LSBs of Total Lines per Frame for the Input Reference Format (REF_LPFM)

This register contains the 8 LSBs of REF_LPFM. REF_LPFM should be programmed with the total lines per frame for the input reference format. REF_LPFM is used in specifying the reference frame rate. This should be specified prior to programming the output initialization sequence (*Reference Frame Timing*).

Register 10h

Bits 3-0: MSBs of Total Lines per Frame for the Input Reference Format (REF_LPFM)

This register contains the 4 MSBs of REF_LPFM. See the description for register 0Fh.

Bit 7-4: These non-programmable bits contain zeros.

Register 11h

Bits 7-0: LSBs of Output Frame Offset (TOF_OFFSET)

This register contains the 8 LSBs of TOF_OFFSET. TOF_OFFSET should be programmed with the desired line offset to delay or advance the output timing relative to the reference frame. This should be specified prior to programming the output initialization sequence. See *Output Frame Line Offset* for more information.

Register 12h

Bits 3-0: MSBs of Line Offset for the Output Top of Frame (TOF_OFFSET)

This register contains the 4 MSBs of TOF_OFFSET. See the description for register 11h.

Bit 7-4: These bits contain zeros (non-programmable)

7.6.1.8 PLL 1, 2, 3 Charge Pump Current Control Registers

Register 13h

Bits 4-0: PLL 1 Charge Pump Current Control (ICP1)

ICP1 can be programmed to specify the charge pump current for PLL 1, which generates 27 MHz from the VCXO output. The PLL 1 charge pump current, or I_{CP1}, is one of the loop gain parameters can be programmed to set and optimize PLL 1's loop response. For more information on setting the loop response, see *Loop Response*.

To minimize lock time, using a large or maximum I_{CP1} can result in faster PLL settling time due to a wider loop bandwidth. Once phase lock has been achieved, using a lower I_{CP1} (that yields sufficient stability) can provide good input jitter rejection due to a narrower loop bandwidth; this can be helpful to minimize low-frequency input jitter from being transferred to the output clocks.

NOTE

An ICP1 value ≤ 2 corresponds to an I_{CP1} current ≤ 62.5 µA. A low I_{CP1} setting or low damping factor (DF) can cause reduced PLL stability and performance (e.g. wander, loss of lock) due to loop filter charge leakage and other secondary factors; therefore, it is not recommended to use an ICP1 value less than 2d nor use an insufficient DF setting.

ICP1 register range = 0 to 31d; 0 to 2d are not recommended

I_{CP1} current = ICP1 x 31.25 µA (nominal current step)

Examples:

ICP1 = 8d (default) gives I_{CP1} = 250 µA nominal

ICP1 = 31d (max) gives I_{CP1} = 968.75 µA nominal

Bits 7-5: Reserved (RSV)

These RSV bits are reserved. When writing to this register, only write the default data to the RSV bits as specified in Table 3.

Register 14h

Bits 3-0: PLL 3 Charge Pump Current Control (ICP3)

ICP3 can be programmed to specify the charge pump current for PLL 3, which generates the 74.176 and 148.35 MHz HD clock outputs. Reducing the value of ICP3 will reduce the PLL 3 charge pump current and lower its loop bandwidth at the expense of reduced PLL stability. An ICP3 value of 0 should not be programmed since this corresponds to 0 µA nominal current, which will cause PLL 3 to lose phase lock or otherwise be unstable.

ICP3 register range = 0 to 15d

Bit 7-4: PLL 2 Charge Pump Current Control (ICP2)

ICP2 can be programmed to specify the charge pump current for PLL 2, which generates the 74.25 and 148.5 MHz HD clock outputs. Reducing the value of ICP2 will reduce the PLL 2 charge pump current and lower its loop bandwidth at the expense of reduced PLL stability. An ICP2 value of 0 should not be programmed since this corresponds to 0 µA nominal current, which will cause PLL 2 to lose phase lock or otherwise be unstable.

ICP2 register range = 0 to 15d

7.6.1.9 Reserved Registers

Register 15h-1Fh

This register is reserved. Do not program any data to these registers.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

For normal operation, the $\overline{\text{RESET}}$ pin must be set high; otherwise, the device cannot be programmed and will not function properly. To reset the control registers to their default values, toggle $\overline{\text{RESET}}$ low for at least 10 µs and then set high.

The LMH1982 can be configured by programming the control registers via the I^{2}C interface. The I^{2}C slave addresses are DCh for write sequences and DDh for read sequences. The I^{2}C_ENABLE pin must be set low or tied to GND to allow I^{2}C communication; otherwise, the LMH1982 will not acknowledge read/write sequences.

For I^{2}C interface control register map and definitions, refer to *I^{2}C Interface Control Register Definitions*.

8.1.1 148.35 MHz PLL Initialization Sequence

The following programming sequence is required to initialize PLL 3 and generate a correct 148.35 MHz output once it is selected as the HD_CLK; otherwise, the clock may have duty cycle errors, frequency errors, and/or high jitter. This PLL initialization sequence must be programmed after switching from another HD clock frequency or Hi-Z mode, as well as after a device reset or power cycle condition. Each programming step below represents a separate write sequence.

1. Program HD_FREQ = 11b and HD_HIZ = 0 (register 08h) to select 148.35 MHz and enable the HD_CLK output.
2. Program a value of 1 to the following register parameters (a single write sequence is valid for this step):
   – FB_DIV = 1 (register 04h-05h)
   – TOF_RST = 1 (register 09h-0Ah)
   – REF_LPFM = 1 (register 0Fh-10h)
   – EN_TOF_RST = 1 (register 0Ah)
3. Wait at least 2 cycles of the 27 MHz VCXO clock, then program EN_TOF_RST = 0.

After this sequence is completed, the 148.35 MHz clock will operate correctly and normal device configuration can resume. All other output clocks do not require this initialization sequence for proper clock operation.

8.1.2 Enabling Genlock Mode

Upon device power up or reset, the default mode of operation is Free Run mode. To enable Genlock mode, set GNLK = 1 (register 00h). Refer to *Genlock Mode* for more information.

8.1.3 Output Disturbance While Output Alignment Mode Enabled

When the output alignment mode is enabled (EN_TOF_RST = 1) for a longer period than is required by the output initialization sequence, the output signals can be abruptly phase-aligned to the reference on every output frame. Continual alignment can cause excessive phase "jumps" or jitter on the output clock edge coinciding with the TOF pulse; this effect is unavoidable and can be caused by slight differences in the internal counter reset timing for the TOF generation and also large input jitter. The characteristic of the output jitter can also vary in severity from process variation, part variation, and the selected clock reference frequency. This output jitter can only be inhibited by setting EN_TOF_RST = 0 immediately following the output initialization and before the subsequent output frame.

8.1.4 Evaluating the LMH1982

For information about SDI jitter performance using the LMH1982 with the LMH1981 sync separator, please refer to the following application notes:

- AN-1893: Demonstrating SMPTE-compliant SDI Output Jitter using the LMH1982 and Virtex-5 GTP

Application Information (continued)

Transmitter (SNLA110)

- AN-1841: LMH1982 Evaluation Board User Guide (SNVA343)

The LMH1982SQEEVAL Evaluation Board can be ordered from Texas Instrument's website.

8.1.5 Input Reference

The LMH1982 features two reference ports (A and B) with H sync and V sync inputs which are used for phase locking the outputs in Genlock mode. The reference port can be selected by programming RSEL (register 00h). If desired, REF_SEL input can be used instead to select the reference port by initially setting I^2C_RSEL = 0 (register 00h).

The reference signals should be 3.3V LVCMOS signals within the input voltage range specified in *Electrical Characteristics* . The H sync and V sync input signals may have analog timing, such as from the LMH1981 multi-format analog video sync separator, or digital timing, such as from an FPGA SDI deserializer.

8.1.5.1 Reference Frame Decoder

The LMH1982 features an internal frame decoder to determine the reference frame timing from only the H and V sync input timing, which eliminates an extra input pin for an odd/even field timing. The reference frame timing is required to allow for output frame initialization (output TOF and clock alignment) to the reference frame.

To allow for proper frame decoding and subsequent output initialization, the H sync and V sync inputs must comply with the H-V sync timing offset specification, ΔT_{HV}. For interlace formats, the H-V sync timing offset must be within ΔT_{HV} for even fields and be outside ΔT_{HV} for odd fields. Compliance with this specification will ensure the internal frame counters are reset only once per frame. For progressive formats, the H-V timing offset must be within ΔT_{HV} for all frames.

Since the LMH1982 was designed for compatibility with the LMH1981 sync separator, its H and V sync pulses will comply with the ΔT_{HV} specification for any input reference format.

For digital timing from an FPGA SDI deserializer, the recovered H and V sync pulses may be co-timed and be within ΔT_{HV} for **both** odd and even fields. This will cause the internal frame counters to reset twice per frame and thus preclude proper frame decoding and output initialization. As a simple work-around, the designer may choose to configure the FPGA to gate the V sync signal, allowing only the even field V pulses and gating off the odd field V pulses.

8.1.6 Output Clocks and TOF

The LMH1982 has simultaneous LVDS output SD and HD clocks and an output TOF pulse. For proper output format timing generation and subsequent output initialization, it is highly recommended to follow the programming sequence below:

1. Program the output clock frequencies (section *Programming the Output Clock Frequencies*).
2. Program the output format timing (section *Output Frame Timing*).
3. Program the output initialization sequence (section *Programming the Output Initialization Sequence*).

8.1.6.1 Programming the Output Clock Frequencies

The SD clock frequency can be selected from Table 4 and programmed to SD_FREQ (register 08h). PLL 1 and PLL 4 are used to generate the two SD clock rates but only one SD clock can be selected at a time. If the SD_CLK output is not needed, it can be put in Hi-Z mode by setting SD_HIZ = 1 (register 08h).

If 27 MHz is selected, the VCXO clock is directly converted from a 3.3V single-ended clock at the VCXO input (pin 29) to an LVDS clock at the SD_CLK output port (pins 23 and 24). If 67.5 MHz is selected, the VCXO clock is used as an input reference for PLL 4 to generate this SD clock frequency. In some FPGA SD-SDI SerDes applications, the 67.5 MHz frequency may be required as an SD reference clock instead of the standard 27 MHz frequency.

Application Information (continued)

Table 4. SD Clock Frequency Selection

SD_CLK (MHz)	SD_FREQ Register 08h	PLL#
27	0	1
67.5	1	4

The HD clock frequency can be selected from Table 5 and programmed to HD_FREQ (register 08h). PLL 2 and PLL 3 are used to generate the four different HD clock rates but only one HD clock can be selected at a time. If the HD_CLK output is not needed, it can be put in Hi-Z mode by setting HD_HIZ = 1 (register 08h).

NOTE

If 148.35 MHz is selected, it is required to follow the programming sequence described in *148.35 MHz PLL Initialization Sequence*.

Table 5. HD Clock Frequency Selection

HD_CLK (MHz)	HD_FREQ Register 08h	PLL#
74.25	0h	2
74.25/1.001	1h	3
148.5	2h	2
148.5/1.001	3h	3

8.1.6.2 Programming the Output Format Timing

When PLL 1 is stable and locked to the input reference, the output format timing should be specified. The functional block diagram for TOF generation and output initialization is shown in Figure 12.

For proper output generation and initialization, the reference format and output format timings must be fully and correctly programmed to the output format registers 09h–12h, which specify the following:

- Output TOF Clock
- Output Frame Timing
- Reference Frame Timing
- Input-Output Frame Rate Ratio
- Output Frame Line Offset

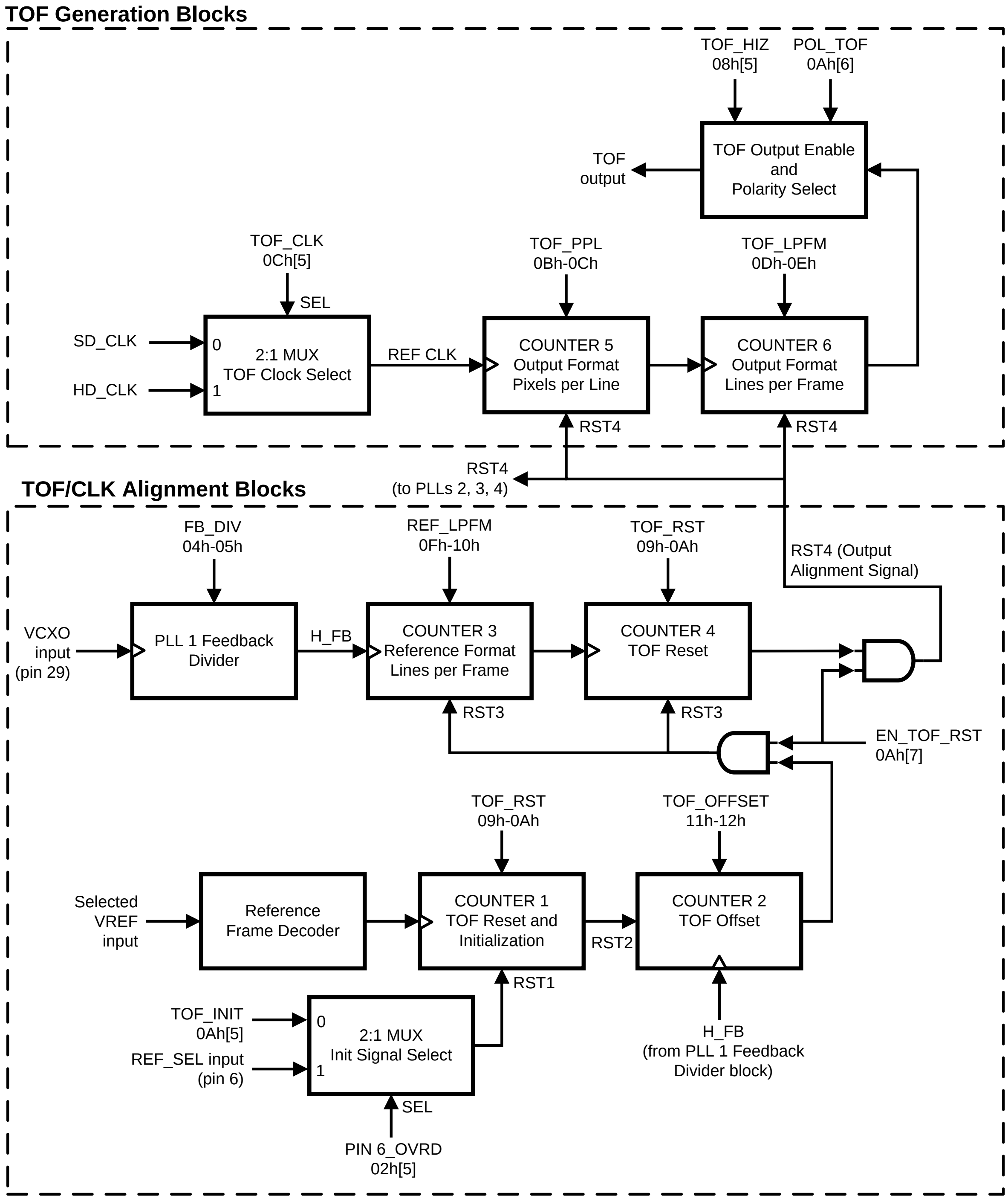

Figure 12. Functional Block Diagram – TOF Generation and Output Initialization Circuitry

8.1.6.2.1 Output TOF Clock

The TOF pulse is derived from a counter chain, which receives either output clock (SD_CLK or HD_CLK) from a 2:1 MUX block, as shown in Figure 12. The TOF clock from the MUX can be selected by programming TOF_CLK (register 0Ch). To select SD_CLK as the TOF clock, set TOF_CLK = 0; otherwise, set TOF_CLK = 1 to select HD_CLK. The selected TOF clock frequency is determined by the SD_FREQ or HD_FREQ register setting.

The TOF output delay time (t_{D_TOF}) for any output format generated from a TOF clock of 27 MHz is specified in *Electrical Characteristics*. The TOF output delay time for 525i and 1080i/50 generated using 27 MHz and 74.25 MHz, respectively, are shown in *Typical Characteristics*. The TOF pulse width can be determined by:

TOF pulse width = (1 / f_{TOF_CLK}) x TOF_PPL

where

- f_{TOF_CLK} = Nominal TOF Clock Frequency
- TOF_PPL = Output Format Total Pixels per Line (1)

8.1.6.2.2 Output Frame Timing

The TOF pulse is specified by programming TOF_CLK, TOF_PPL (register 0Bh-0Ch) and TOF_LPFM (register 0Dh-0Eh). These registers configure the 2:1 MUX and output pixel and line counters in the TOF Generation blocks shown in Figure 12. The output frame or TOF pulse rate is determined by:

TOF rate = f_{TOF_CLK} / (TOF_PPL x TOF_LPFM)

where

- f_{TOF_CLK} = Nominal TOF Clock Frequency
- TOF_PPL = Output Format Total Pixels per Line
- TOF_LPFM = Output Format Total Lines per Frame (2)

Example:

If the output format is 625i, then:

TOF rate = 27 MHz / (1728 x 625) = 25 Hz

where

- f_{TOF_CLK} = 27 MHz (SD_FREQ = 0)
- TOF_PPL = 1728
- TOF_LPFM = 625 (3)

8.1.6.2.2.1 HD Format TOF Generation Using a 27-MHz TOF Clock

Any HD format TOF pulse can be generated using either: Option 1) its native HD clock frequency, or Option 2) the 27 MHz SD clock frequency.

Using Option 1) for HD output formats can result in TOF output delay being offset by more than one TOF clock period, even after output initialization. This is because the very short period of the HD native clock yields little timing margin for the reset signals to propagate through the internal logic in Figure 12. For example, using a TOF clock of 148.5 MHz gives less than 6.7 ns (< 1 clock cycle) for all the logic to completely synchronize and ensure proper output initialization.

To ensure proper output initialization, Option 2) is recommended for HD output formats, especially 1080p at 50, 59.94, and 60 Hz. This is because the longer period of the 27 MHz clock provides ample timing margin for the internal logic to reset. The output parameters for programming the HD output formats using the 27 MHz clock are shown in Table 2.

To illustrate both TOF clock options, an example is given below for 1080p/59.94, which has a native pixel clock frequency of 148.5/1.001 MHz and frame rate of 60/1.001 Hz:

Option 1) 1080p/59.94 TOF generation using 148.35 MHz

TOF rate = 148.5/1.001 MHz / (2200 x 1125) = 60/1.001 Hz

where

- f_{TOF_CLK} = 148.35 MHz (TOF_CLK = 1, HD_FREQ = 3h)
- TOF_PPL = 2200
- TOF_LPFM = 1125 (4)

Option 2) 1080p/59.94 TOF generation using 27 MHz

TOF rate = 27 MHz / 2002 x 225) = 60/1.001 Hz

where

- f_{TOF_CLK} = 27 MHz (TOF_CLK = 0, SD_FREQ = 0)
- TOF_PPL = 2002
- TOF_LPFM = 225 (5)

As an example, Figure 13 shows a timing illustration for 1080p/59 TOF and clock outputs. Once the outputs are initialized, the SD clock and TOF pulse will have a fixed delay, and the SD clock and HD clock will have a fixed timing offset relative to each other. Therefore, the timing offset between the TOF pulse and HD clock, or $t_{TOF\text{-}HD}$, will also be fixed and can be determined by:

$t_{TOF\text{-}HD} = t_{D\_TOF} + t_{D\_SD} - t_{D\_HD}$

where

- t_{D_TOF} = TOF Output Delay Time referenced to SD_CLK
- t_{D_SD} = SD_CLK Output Delay Time
- t_{D_HD} = HD_CLK Output Delay Time (6)

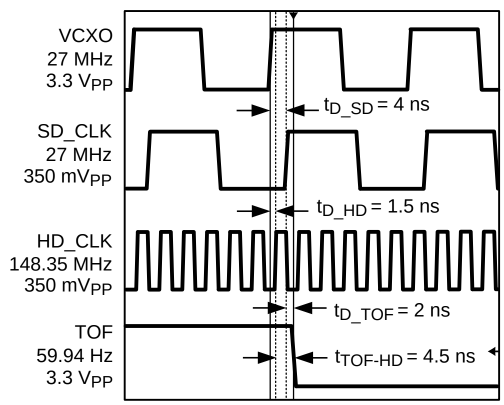

Figure 13. Timing Illustration Showing 1080p/59.94 TOF and CLK Output Delays Using Option 2

8.1.6.2.3 Reference Frame Timing

The reference format frame timing is generated internally and used for resetting the internal counters for output initialization. The reference frame rate should be specified by programming the reference format total lines per frame to REF_LPFM (register 0Fh-10h) as well as the PLL 1 dividers. See Table 2 for programming the parameter values according to each reference format. The reference frame rate is determined by:

REF rate = (f_{VCXO} x R_DIV) / (FB_DIV x REF_LPFM)

where

- f_{VCXO} = 27 MHz Nominal VCXO Clock Frequency
- R_DIV = Reference Divider (not REF_DIV_SEL)
- FB_DIV = Feedback Divider
- REF_LPFM = Reference Format Total Lines per Frame (7)

8.1.6.2.4 Input-Output Frame Rate Ratio

The input-output frame rate ratio is also used for resetting the internal counters for output initialization. The ratio is the Input Frame Rate / Output Frame Rate, in which the numerator and denominator values are reduced to lowest integer factors. The numerator value of this reduced ratio should be programmed to TOF_RST (register 09h-0Ah), and the denominator value is discarded.

Example:

If the input reference is 525i with a frame rate of 30/1.001 Hz and the output format is 625i with a frame rate of 25 Hz, then:

Frame rate ratio = (30/1.001) / 25 = **1200** / 1001

Therefore, the numerator, 1200, should be programmed to TOF_RST.

8.1.6.2.5 Output Frame Line Offset

The output clock and TOF pulse can be aligned to any line of the reference frame by programming TOF_OFFSET (register 11h-12h) and subsequently programming the output initialization sequence. The line offset value should be directly programmed to TOF_OFFSET to delay or advance the outputs' alignment relative to the decoded reference frame timing (see *Reference Frame Decoder*).

The TOF_OFFSET value must be greater than zero but less than or equal to the programmed value for REF_LPFM (i.e. 0 < TOF_OFFSET ≤ REF_LPFM). If no line offset is required, then program TOF_OFFSET equal to REF_LPFM instead of zero (invalid value).

Example:

If an input reference with PAL timing comes from the LMH1981, the H and V pulses will be aligned to within ΔT_{HV} which occurs on line 313 of the reference. In this case, TOF_OFFSET can be set to 312d (138h) so the output frame will align to Line 1 of the PAL reference (start of frame) after the outputs are initialized. This example is illustrated in Figure 14.

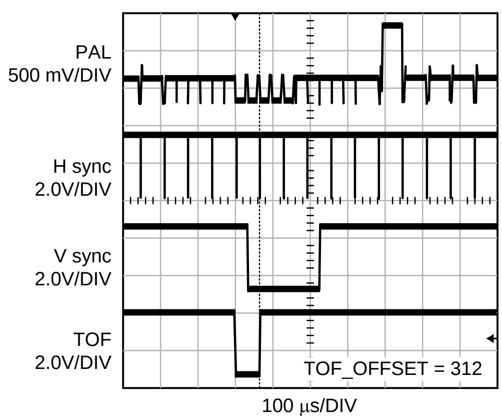

Figure 14. PAL Reference and Output TOF Pulse (TOF_OFFSET = 312)

NOTE

If the alternative set of divider and REF_LPFM values are programmed per [(1)] for a lower PLL 1 phase comparison frequency, then the output frame cannot be offset to any horizontal line of the reference. Instead, the output frame can only be aligned to the reference in 5 lines steps per 1 step of the TOF_OFFSET value, up to a maximum of reference's total lines per frame divided by 5 (i.e. REF_LPFM). This is because the phase comparison frequency (H_FB signal in Figure 12) will be lower than the H sync input frequency by 5x due to the use of the alternative divider values.

8.1.6.3 Programming the Output Initialization Sequence

Before programming the output initialization (alignment) sequence, the following prerequisites must be met:

1. PLL 1 must be stable and locked to the input reference.
2. The desired output clock and TOF pulse timing must be fully specified to the output format registers.

(1) For some input reference formats, an alternative set of values for PLL 1 dividers and total lines per frame (REF_LPFM) is also shown in **brackets "[ ]"**. This alternative set of values may be programmed if a lower PLL 1 phase comparison frequency is desired. The corresponding counter values for REF_LPFM needs to be programmed for proper reference frame and output timing generation. See *Reference Frame Timing*.

To ensure that the output clock and TOF pulse are properly aligned and subsequently phase locked to the reference frame, the output initialization sequence should be programmed accordingly.

During the output frame immediately prior to the frame the initialization is to occur:

1. Set EN_TOF_RST = 1(register 0Ah) to enable output alignment mode.
2. Toggle TOF_INIT (register 0Ah) from 0 to 1 to reset the internal counters. On the next frame, the output clock and TOF pulse will be initialized (aligned) to the reference frame with line offset programmed to TOF_OFFSET.
3. Immediately after the initialization and before the next output frame occurs, clear EN_TOF_RST and TOF_INIT to 0. Otherwise, the output clock will be continually aligned on every output frame while EN_TOF_RST = 1. Continual alignment which may cause excessive jitter on the output clock (from PLL 2, 3, or 4) due to slight differences in the delay paths of the internal logic. This occurrence of excessive clock jitter can be avoided by disabling output alignment mode (EN_TOF_RST = 0) immediately after the initialization sequence.

8.1.6.3.1 TOF Output Delay Considerations

Due to the following conditions, the TOF pulse may be delayed or offset by more than one TOF clock period (t_{D_TOF} > 1 pixel) even after output initialization:

1. The delay paths of the internal logic used to generate and align the TOF pulse is greater than one period of the TOF clock. This can occur for HD format TOF pulses generated using the 148 MHz native pixel clock. For HD format TOF generation, it is recommended to use the 27 MHz SD clock as the TOF clock instead of the native HD pixel clock as shown in *Output Frame Timing*.
2. The H sync and/or V sync input pulses have excessive jitter equal to or larger than half of a pixel period of the selected output clock. Input sync jitter less than 3 ns peak-to-peak is recommended.
3. PLL 1 is not completely phase locked or stable when the output initialization is performed. The VCXO clock phase error with respect to the H sync input should less than one period of the selected TOF clock.

8.1.6.3.2 Output Clock Initialization Without TOF

For applications that do not require the TOF pulse, it is still necessary to program all output format registers prior to the output initialization sequence. This is because the output initialization circuitry relies on the full and correct specification of the output format. If the TOF output is not needed, it can be put in Hi-Z mode by setting TOF_HIZ = 1 (register 08h).

8.1.6.4 Output Behavior Upon Loss Of Reference

After loss of reference (LOR), the LMH1982 will maintain the TOF pulse without the input reference according to the terminal counts of the reference clock; however, output frequency accuracy will be determined by the VCXO, which may be in Free Run or Holdover operation.

To disable output alignment to an arbitrary reference frame when the reference is reapplied, set EN_TOF_RST = 0 before the reference returns. After PLL 1 has re-locked to the reference, the outputs can be initialized to the desired reference frame.

8.1.7 Reference And Pll Lock Status

The LMH1982 features a reference detector and PLL lock detector that can be used to indicate genlock status of the input reference and device PLLs. Genlock status can be sampled via the NO_REF and NO_LOCK status flag output pins and the REF_VALID, SD_LOCK, and HD_LOCK status bits (register 01h). Both the reference and PLL lock detectors may be programmed for their respective detection thresholds according to the needs of the application system. See Table 7 for a summary of the genlock status bits and status outputs for different conditions.

The NO_REF and NO_LOCK outputs are derived from the genlock status bits and given by the following two logic equations:

$$\text{NO\_REF} = \overline{\text{REF\_VALID}}$$

$$\text{NO\_LOCK} = \overline{(\text{REF\_VALID})\ (\text{SD\_LOCK})\ (\text{HD\_LOCK})}$$

8.1.7.1 Reference Detection

In Genlock mode, a valid reference will be indicated by NO_REF = 0 when all the criteria below are met. Otherwise, a loss of reference (LOR) will be indicated by NO_REF = 1.

- An H sync signal is applied to the input reference and conforms to one of the standard formats in Table 2. A V sync signal is not used in reference detection.
- The PLL divide registers are programmed according to the input reference format.
- The control voltage of the VCXO is not within about 500 mV of the GND or V_{DD} supplies.

8.1.7.1.1 Programming the Loss of Reference (LOR) Threshold

The reference detector's error threshold can be programmed to H_ERROR (register 00h), which determines the maximum number of missing H sync pulses before indicating an LOR. The LOR threshold will be the H_ERROR value multiplied by the PLL 1 reference divider value, as shown in Table 6.

Table 6. LOR Threshold Selection

REF_DIV_SEL Register 03h	Reference Divider	LOR Threshold
0h	2	2 x H_ERROR
1h	1	1 x H_ERROR
2h	5	5 x H_ERROR

If H_ERROR = 0, then the device will react after the first missing pulse. When the LOR threshold is exceeded, the NO_REF output will indicate LOR, and the device will default to either Free Run or Holdover operation for as long as the reference is lost. As the LOR threshold value is increased, the accuracy for counting the actual number of missing H pulses may diminish due to frequency drifting by PLL 1.

NOTE

If the input reference is missing H pulses periodically, for example every vertical interval period, the PLL may not indicate a valid reference nor achieve lock regardless of the H_ERROR value programmed. This is because periodically missing pulses will translate to a lower average frequency than expected. When the average input frequency falls outside of the absolute pull range (APR) of the VCXO, the PLL will not be able to frequency lock to the input reference.

8.1.7.2 PLL Lock Detection

In Genlock mode, PLL lock will be indicated by NO_LOCK = 0 when all the criteria below are met. Otherwise, a loss of lock will be indicated by NO_LOCK = 1.

- A valid reference is indicated (REF_VALID = 1).
- PLL 1 or PLL 4 is phase locked to the input reference (SD_LOCK = 1).
- PLL 2 or PLL 3 is phase locked to the VCXO clock reference (HD_LOCK = 1).

PLLs 2, 3, and 4 have high loop bandwidths, which allow them to achieve lock quickly and concurrently while PLL 1 achieves lock. Because PLL 1 has a much lower loop bandwidth, it will dictate the overall lock indication time.

8.1.7.2.1 Programming the PLL Lock Threshold

PLL 1's lock detector threshold can be programmed to LOCK_CTRL (register 01h), which determines the maximum phase error between PLL 1's phase detector (PD) inputs before indicating an unlock or lock condition. The PD inputs are the reference signal (H sync input / reference divider) and the feedback signal (VCXO clock / feedback divider).

The lock detector will indicate loss of lock when the phase error between the PD inputs is greater than the lock threshold for three consecutive phase comparison periods. Conversely, it will indicate valid lock when the phase error is less than the lock threshold for three consecutive phase comparison periods.

A larger value for LOCK_CTRL will yield shorter lock indication time (although not actual lock time) at the expense of higher output phase error when lock is initially indicated, whereas a smaller value will yield the opposite effect.

8.1.7.2.2 PLL Lock Status Instability

It is possible for excessive jitter on the H input to indicate lock instability through the NO_LOCK output, even if the VCXO and output clocks are properly phase locked and no system-level errors are occurring (e.g. bit errors). To reduce the probability of false loss of lock indication or lock status instability, LOCK_CTRL can be increased to improve the lock detector's ability to tolerate a larger amount of input phase jitter or phase error. This can help to ensure the NO_LOCK output and SD_LOCK bit are stable when the reference signal has large input jitter.

Table 7. Summary of Genlock Status Bits and Flag Outputs[(1)]

	Mode Control Bits Register 00h		Status Flag Outputs		Status Bits Register 01h		
Conditions	GNLK	HOLD-OVER	NO_REF [1] (pin 16)	NO_LOCK [2] (pin 17)	HD_LOCK bit 2	SD_LOCK bit 1	REF_VALID bit 0
Genlock mode, Reference valid, PLLs locking	1	X	0	1	0	0	1
Genlock mode, Reference valid, PLLs locked	1	X	0	0	1	1	1
Genlock mode, Reference lost, Free Run operation	1	0	1	1	1	0	0
Genlock mode, Reference lost, Holdover operation	1	1	1	1	1	0	0

(1) Status flag output logic equations:
1. NO_REF = $\overline{\text{REF\_VALID}}$
2. NO_LOCK = $\overline{\text{(REF\_VALID) (SD\_LOCK) (HD\_LOCK)}}$

8.1.8 Loop Response

The overall loop response of the LMH1982 is determined by the design of the VCXO PLL (PLL 1). Because the integrated VCO PLLs use the VCXO clock as the input reference to phase lock the output clocks, the ability of PLL 1 to attenuate the input jitter is critical to output jitter performance, especially low-frequency jitter that occurs at the video line and field rates. The loop response of the LMH1982 can be characterized by PLL 1's loop bandwidth and damping factor.

The loop response is primarily determined by the loop filter components and the loop gain. A passive second-order loop filter consisting of R_S, C_S, and C_P components can provide sufficient input jitter attenuation for most applications, although a higher order passive filter or active filter may also be used. The loop gain is a function of the VCXO gain and programmable PLL parameters.

A lower loop bandwidth will provide higher input jitter attenuation (reduced jitter transfer) for improved output jitter performance; however, increased lock time (or settling time) and larger external component values are a couple trade-offs to a lower loop bandwidth.

8.1.8.1 Loop Response Design Equations

The following equations can be used to design the loop response of PLL 1.

The -3 dB loop bandwidth, BW, can be approximated by:

$BW = I_{CP1} * R_S * K_{VCO} / FB\_DIV$

where

- I_{CP1} = Nominal VCXO PLL charge pump current (in amps) programmed by setting ICP1 (register 13h).
  For example:
  I_{CP1} = 250 µA: ICP1 = 08h (default value)
  I_{CP1} = 0 µA: ICP1 = 00h (min)
  I_{CP1} = 62.5 µA; ICP1 = 02h (practical min)
  I_{CP1} = 968.75 µA; ICP1 = 1Fh (max)
  I_{CP1} step size = 31.25 µA
- R_S = Nominal value of series resistor (in Ω)
- K_{VCO} = Nominal 27 MHz VCXO gain (in Hz/V)
  Nominal 27 MHz VCXO gain (in Hz/V)
  K_{VCO} = Pull_range * 27 MHz/Vin_range
  For the recommended VCXO (Mftr: CTS, P/N: 357LB3C027M0000): K_{VCO} = 100 ppm * 27 MHz/(3.0V- 0.3V) = 1000 Hz/V
- FB_DIV = Feedback Divider value
  For example:
  FB_DIV =1716 for NTSC timing (8)

Note that this BW approximation does not take into account the effects of the damping factor or the second pole introduced by Cp.

At frequencies far above the −3 dB loop bandwidth, the closed-loop frequency response of PLL 1 will roll off at about −40 dB/decade, which is useful attenuating input jitter at frequencies above the loop bandwidth. Near the −3 dB corner frequency, the roll-off characteristic will depend on other factors, such as damping factor and filter order.

To prevent output jitter due to the modulation of the VCXO by the PLL's phase comparison frequency:

$BW \leq (27\ MHz / FB\_DIV) / 20$

PLL 1's damping factor, DF, can be approximated by:

$DF = (R_S / 2) * sqrt\ (I_{CP1} * C_S * K_{VCO} / FB\_DIV)$

where

- C_S = Nominal value of the series capacitor (in farads) (9)

A typical design target for DF is between 0.707 to 1, which can often yield a good trade-off between reference spur attenuation and lock time. DF is related to the phase margin, which is a measure of the PLL stability.

A secondary parallel capacitor, C_P, is needed to filter the reference spurs introduced by the PLL which may modulate the VCXO input voltage and also cause output jitter. The following relationship should be used to determine C_P:

$C_P = C_S / 20$ (10)

The PLL loop gain, K, can be calculated as:

$K = I_{CP1} * K_{VCO} / FB\_DIV$ (11)

Therefore, the BW and DF can be expressed in terms of K:

$BW = R_S * K$

$DF = (R_S/2) * sqrt\ (C_S * K)$

8.1.8.1.1 Loop Response Optimization Tips

The need to support various input reference formats will usually require a diverse range of PLL divider values, which can each yield a different loop response assuming all other PLL parameters are kept the same. Typically, it is desired to design and optimize the loop response across all supported input formats without modification to the loop filter circuit. This requires that the loop gain, K, be kept constant across all supported divider values because K affects both BW and DF equations. To keep a narrow range for K, the ratio (I_{CP1} / feedback divider) should be kept relatively constant. This can be achieved by programming ICP1, so that I_{CP1} is scaled with FB_DIV for each supported input format.

It is suggested to start designing the loop filter component values from the BW and DF equations with initial assumptions of FB_DIV = 1716 (NTSC) and I_{CP1} = 250 µA (default setting). Once reasonable component values are achieved under these initial assumptions, it is necessary to check that K can be maintained over the expected range of FB_DIV by adjusting I_{CP1}. The usable current range of I_{CP1} is limited to a practical minimum of 94 µA (ICP1 = 3d) to a maximum of 969 µA (ICP1 = 31d), which should provide adequate range to maintain a narrow range for K assuming the suggested initial values for FB_DIV and I_{CP1} were followed. If a narrow range for K cannot be maintained within the usable range of I_{CP1}, then the loop filter design may need to be modified. Some trial-and-error and iterative calculations may be necessary to find an optimal loop filter.

In some loop filter designs, the calculated I_{CP1} current that is required for a target K value may be near or below the practical minimum of the I_{CP1} current range. In this scenario, it may also be possible to leverage the programmable reference and feedback dividers by scaling up the values in proportion (i.e. same reduced divider ratio). This would allow I_{CP1} to be scaled up by the same proportion to be within the usable I_{CP1} current range and maintain the same K value, since I_{CP1} and FB_DIV would be scaled by the same factor. For example, by scaling the divider values by a factor of 5x, I_{CP1} can also be scaled up by 5x such that its within the usable current range. This technique of scaling FB_DIV and I_{CP1} assumes that the input format has an alternative set of compatible divider values as shown in Table 2.

8.1.8.1.2 Loop Filter Capacitors

It is suggested to use tantalum capacitors for C_S and C_P instead of ceramic capacitors in the PLL loop filter, which is a sensitive analog circuit. Ferroelectric ceramics, such as X7R, X5R, Y5V, Y5U, etc., exhibit piezoelectric effects that generate electrical noise in response to mechanical vibration and shock. This electrical noise can modulate the VCXO control voltage and consequently induce clock jitter at high amplitudes when the board and ceramic components are subjected to vibration or shock. Tantalum capacitors can be used to mitigate this effect.

8.1.8.2 Lock Time Considerations

The LMH1982 lock time or settling time is determined by the loop response of PLL 1, which has a much lower loop bandwidth compared to the integrated PLLs used to derive the other output clock frequencies. Generally, the lock time is inversely proportional to the loop bandwidth; however, if the loop response is not designed or programmed for sufficient PLL stability, the lock time may not be predicted from the loop bandwidth alone. Therefore, any parameter that affects the loop response can also affect the overall lock time.

One way to reduce lock time is to widen the loop bandwidth by programming a larger or maximum value for I_{CP1} while PLL 1 is locking; after PLL 1 is locked, I_{CP1} can be reduced to provide a narrower loop bandwidth while maintaining a reasonable damping factor.

8.1.8.3 VCXO Considerations

The recommended VCXO manufacturer part number is CTS 357LB3C027M0000, which has an absolute pull range (APR) of ±50 ppm and operating temperature range of -20°C to +70°C. A VCXO with a tighter APR can provide better output frequency accuracy in Free Run operation; however, the APR must be wider than the worst-case input frequency error in order to achieve phase lock.

8.1.8.4 Free Run Output Jitter

The input voltage to VC_FREERUN (pin 1) should have sufficient filtering to minimize noise over the frequency bands of interest (i.e. SMPTE SDI jitter frequency bands) which can cause VCXO input voltage modulation and thus free run output clock jitter.

8.2 Typical Applications

8.2.1 Analog Reference Genlock for Triple-Rate SDI Video

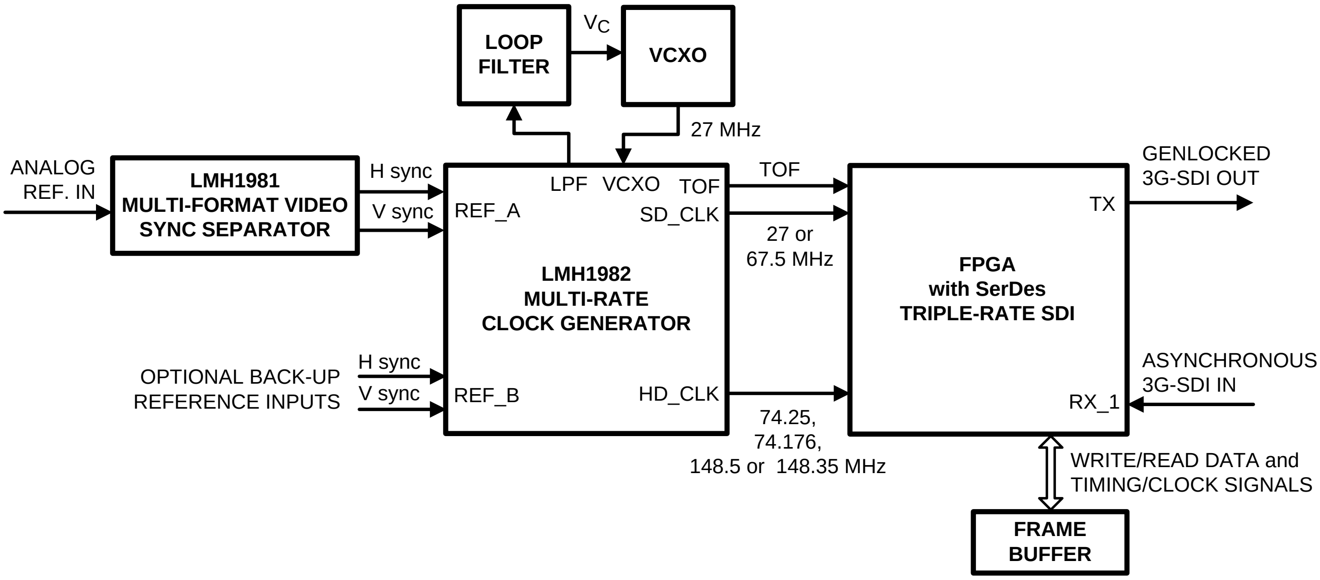

Figure 15. Analog Reference Genlock for Triple-Rate SDI Video

8.2.1.1 Design Requirements

8.2.1.1.1 Programming the PLL 1 Dividers

To genlock the outputs to the reference, it is necessary to phase lock the VCXO clock (PLL 1) to the H sync input signal by programming the PLL dividers. The PLL divider values for each supported input reference format are given in Table 2. The divider values can be determined by reducing the following ratio to its lowest integer factors:

$$f_{VCXO} / f_{HSYNC} = \text{Feedback Divider} / \text{Reference Divider}$$

where

- f_{VCXO} = 27 MHz VCXO frequency
- f_{HSYNC} = H sync input frequency
- Feedback Divider = 1 to 8191 (0 is invalid)
- Reference Divider = 1, 2 or 5 (12)

Table 8 shows the selection table with compatible PLL 1 reference divider values to program REF_DIV_SEL (register 03h). The PLL 1 feedback divider value can be directly programmed to FB_DIV (register 04h-05h).

Table 8. PLL 1 Reference Divider Selection

REF_DIV_SEL Register 03h	Reference Divider
0h	2
1h	1
2h	5

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Procedure for Designing the PLL 1 Dividers

Some supported input formats in Table 2 have two sets of compatible divider values: reduced dividers and non-reduced dividers. See Examples 2A and 2B below. Because the loop response of PLL 1 is dependent on the feedback divider value, a lower loop bandwidth and phase comparison frequency can be achieved by programming the non-reduced divider set (see *Loop Response*).

Examples:

1) For 1080i/59.94 input reference, the dividers are:
- Reference divider = 5 (REF_DIV_SEL = 2h)
- Feedback divider = 4004 (FB_DIV = FA4h)

2A) For 1080i/50 input reference, the reduced dividers are:
- Reference divider = 1 (REF_DIV_SEL = 1h)
- Feedback divider = 960 (FB_DIV = 3C0h)

2B) For 1080i/50 input reference, the non-reduced (alternative) dividers are:
- Reference divider = 5 (REF_DIV_SEL = 2h)
- Feedback divider = 4800 (FB_DIV = 12C0h)

8.2.2 SDI Reference Genlock for Triple-Rate SDI Video

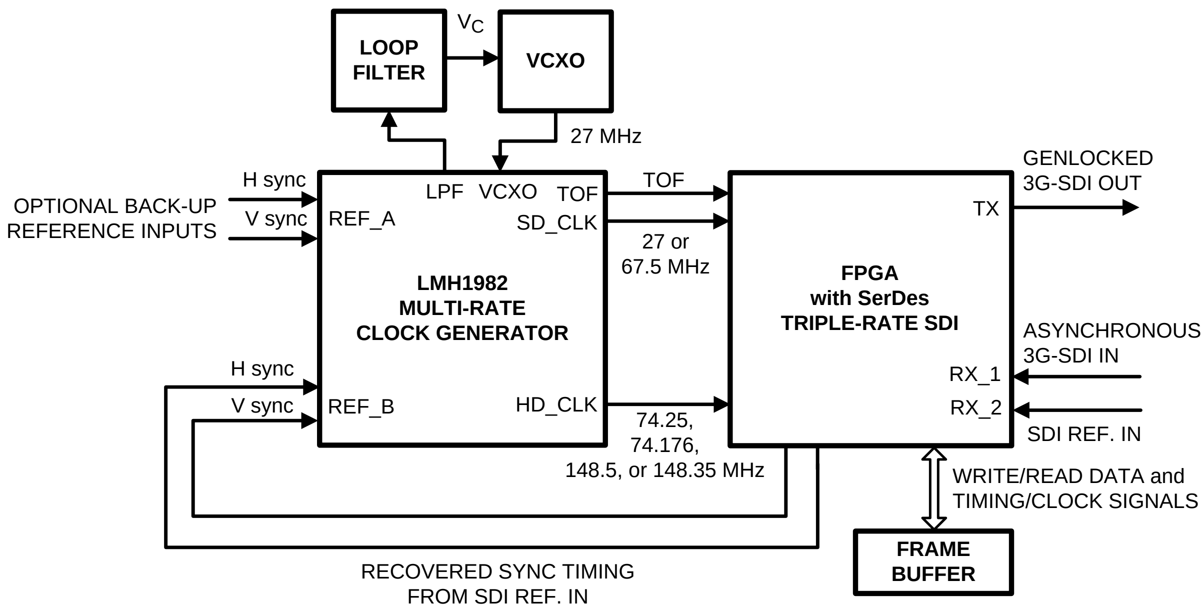

Figure 16. SDI Reference Genlock for Triple-Rate SDI Video

8.2.3 Triple-Rate SDI Loop-through

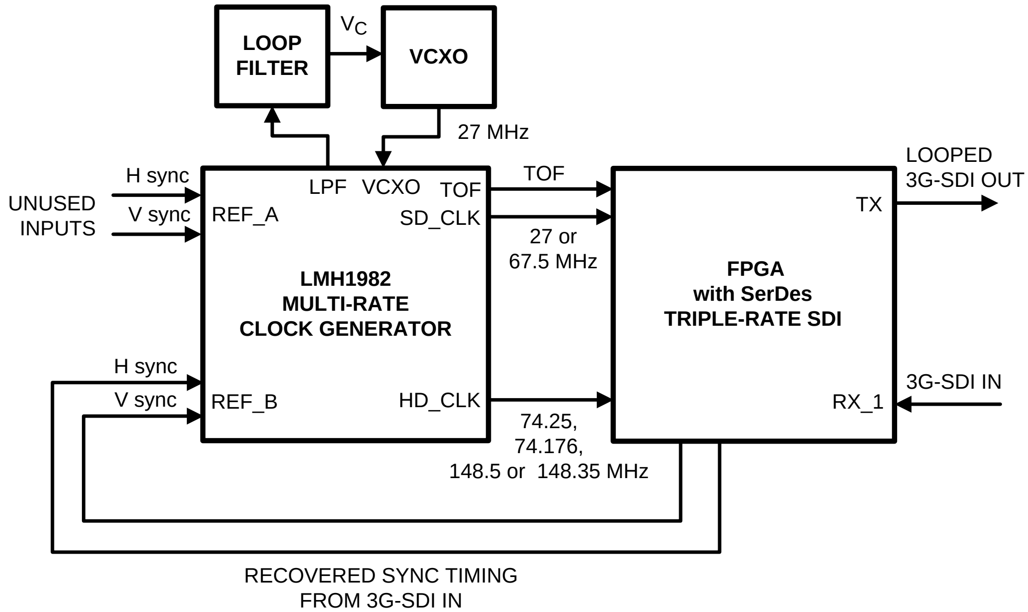

Figure 17. Triple-Rate SDI Loop-through

8.2.4 Combined Genlock or Loop-Through for Triple-Rate SDI Video

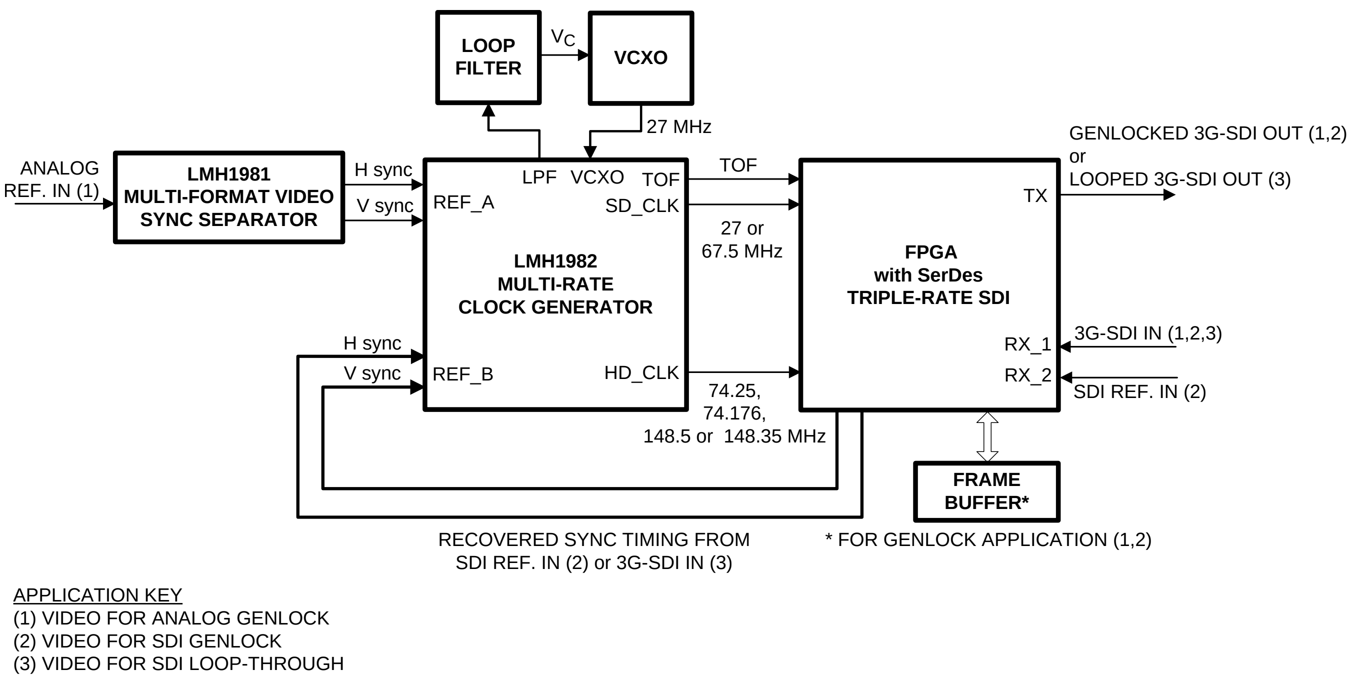

Figure 18. Combined Genlock or Loop-Through for Triple-Rate SDI Video

9 Power Supply Recommendations

9.1 Power Supply Sequencing

The V_{DD} (3.3 V) and DV_{DD} (2.5 V) power supply pins are isolated by internal ESD structures that may become forward biased when DV_{DD} is higher than V_{DD}. Exposure to this condition, when prolonged and excessive, can trigger latch-up and/or reduce the reliability of the device. Therefore, the LMH1982 has a recommended power supply sequence.

On device power-up, the V_{DD} supply must be brought up before the DV_{DD} supply. On power-down, the DV_{DD} supply must be brought down before the V_{DD} supply. The starting points and ramp rates of the supplies should be considered to determine the relative timing of the power-up and power-down sequences such that DV_{DD} does not exceed V_{DD} +0.3 V as shown in the *Absolute Maximum Ratings*.

To minimize the potential for latch-up, a Schottky diode can be externally connected between the DV_{DD} supply (anode) and V_{DD} supply (cathode). If DV_{DD} is brought up first, the Schottky will ensure that V_{DD} is within about 0.3 V of DV_{DD} until V_{DD} is brought up.

Additionally, the device input pins (except for SDA and SCL inputs) should not be driven prior to power-up due to the same reasons provided above for the power pins. Otherwise, a small series resistor should be used on each input pin to protect the device by limiting the current whenever the internal ESD structures become forward biased.

Once both supplies are powered up in the proper sequence, the device has a power on reset sequence that will reset all registers to their default values.

10 Layout

10.1 Layout Guidelines

These are some of the guidelines used in producing the LMH1982 dedicated EVM, for the user's reference:

- The LMH1982 requires that 3.3 V and 2.5 V be regulated to within ±5% and have low noise to ensure optimal output jitter performance. The 27-MHz VCXO also requires a clean 3.3-V supply and proper supply bypassing for optimal performance. Use close-by low noise linear regulators to produce clean 3.3 V and 2.5 V for the application board.
- Route the LVDS output SD and HD clocks from the LMH1982 through controlled 100-Ω differential impedance lines to either edge-mount SMA connectors or to the following stage(s). If a differential probe will be used to measure the clocks directly on the board, then the differential lines should be terminated with 100 Ω.
- Keep the loop filter components (R8, C10, C27, and C28) next to the LMH1982 with a tight layout as shown in Figure 19.

Please consult the LMH1982 EVM for more information.

10.2 Layout Example

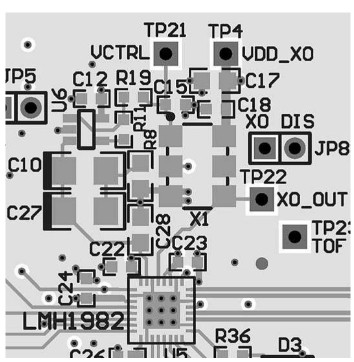

Figure 19. PCB Layout Showing Loop Filter and VCXO

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For more information, please refer to:

- *Demonstrating SMPTE-compliant SDI Output Jitter using the LMH1982 and Virtex-5 GTP Transmitter*, SNLA110
- *LMH1982 Evaluation Board User Guide*, SNVA343

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1982SQ/NOPB	ACTIVE	WQFN	RTV	32	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L1982SQ	Samples
LMH1982SQE/NOPB	ACTIVE	WQFN	RTV	32	250	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L1982SQ	Samples
LMH1982SQX/NOPB	ACTIVE	WQFN	RTV	32	4500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L1982SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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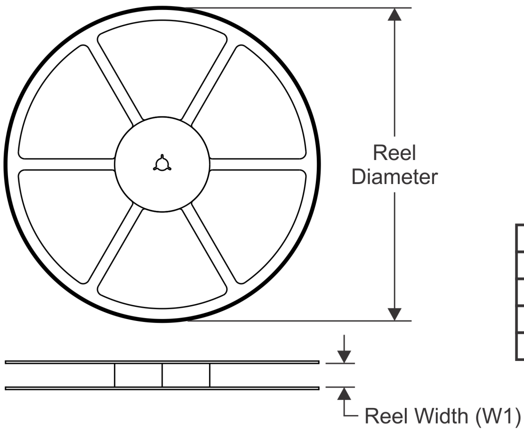
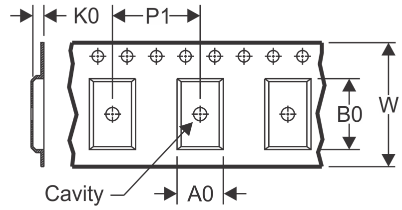
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

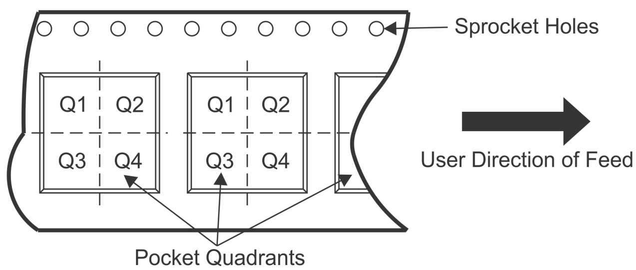


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

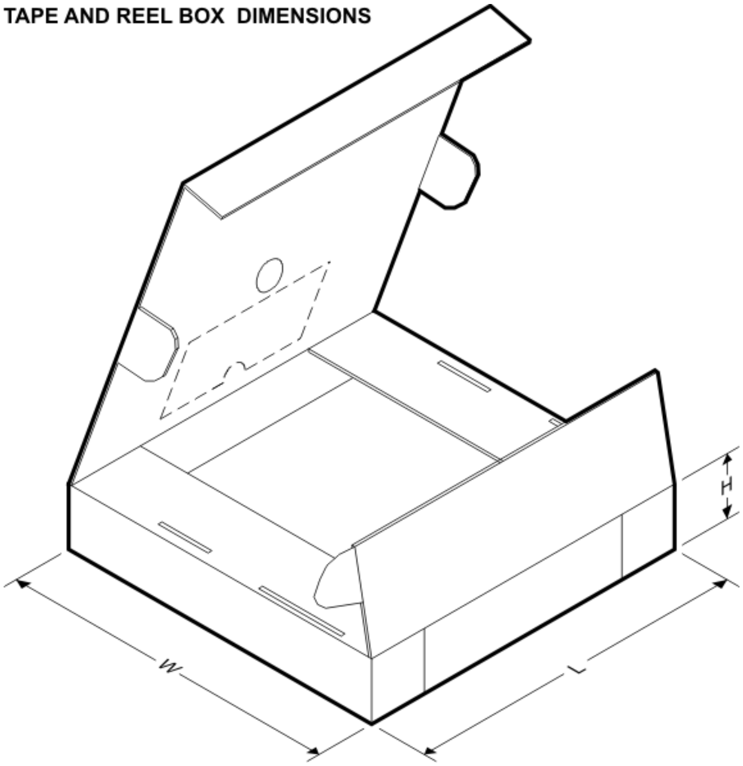
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

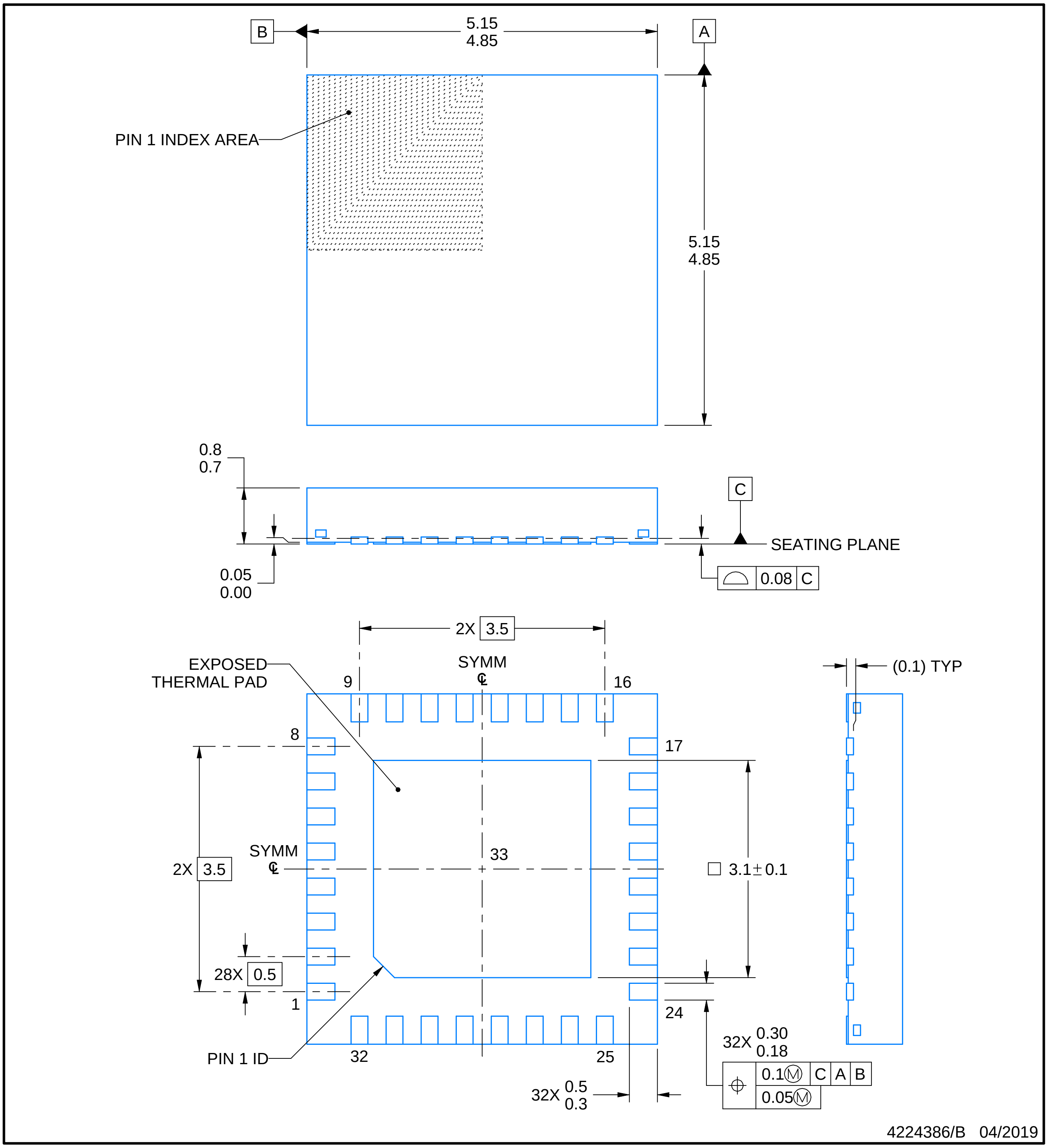
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1982SQ/NOPB	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH1982SQE/NOPB	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH1982SQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



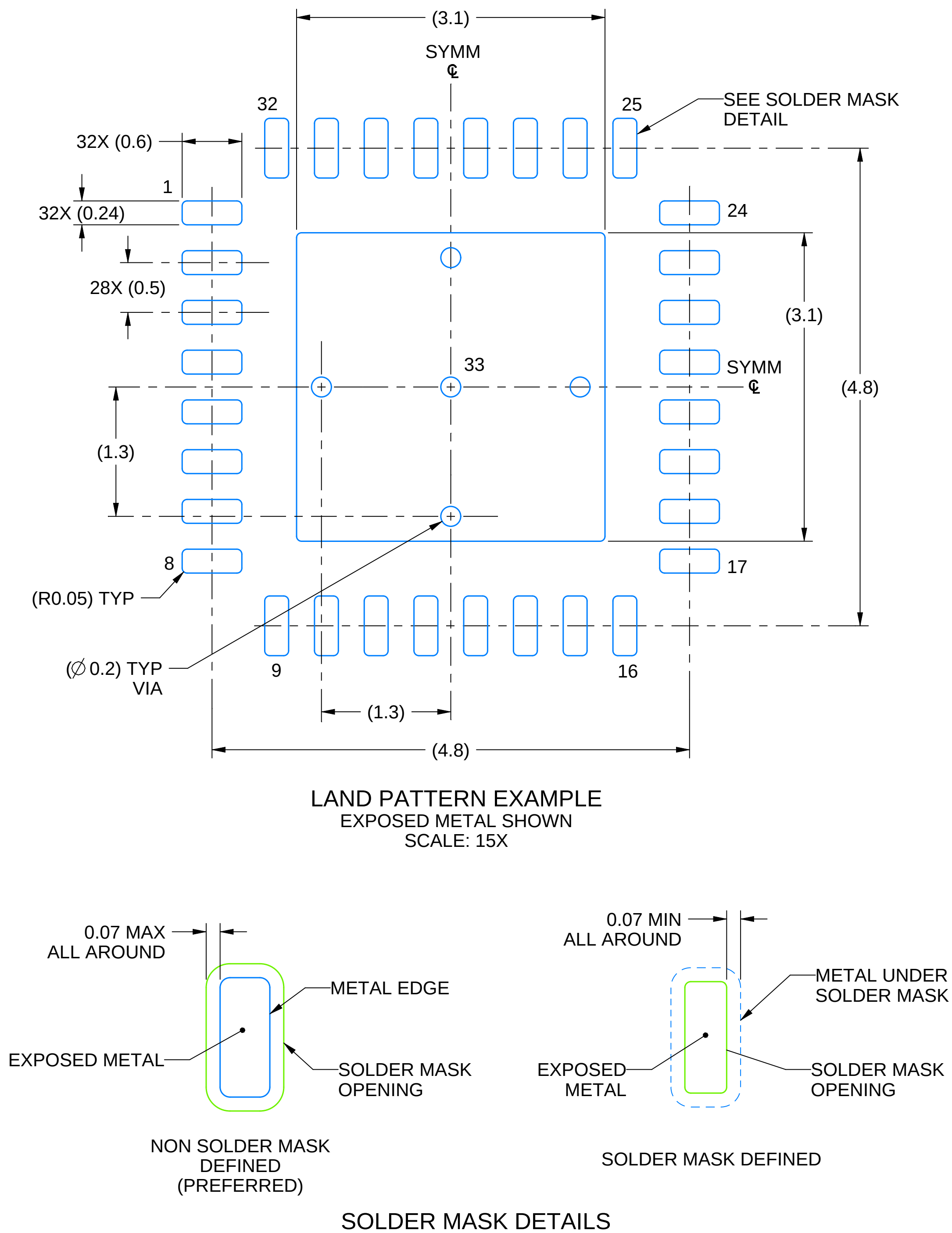
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1982SQ/NOPB	WQFN	RTV	32	1000	210.0	185.0	35.0
LMH1982SQE/NOPB	WQFN	RTV	32	250	210.0	185.0	35.0
LMH1982SQX/NOPB	WQFN	RTV	32	4500	367.0	367.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



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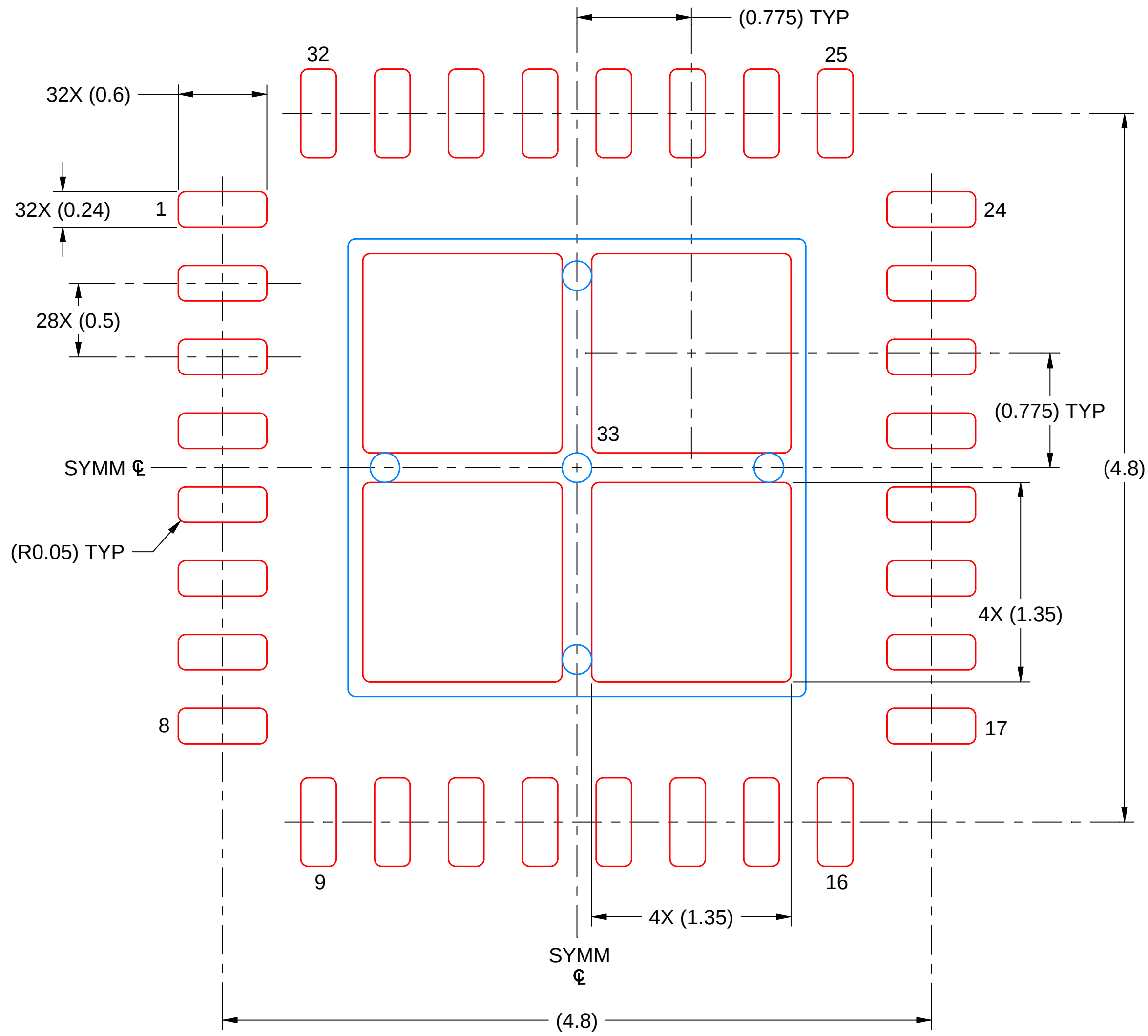
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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