具有动态范围压缩和 AGC 功能、每通道可提供 2.8W 输出驱动功率的立体声 D 类音频放大器

查询样品: TPA2016D2

特性

- 无滤波器 D 类架构
- 在 5V 电压条件下，每个通道可为 8Ω 负载提供 1.7W 的输出驱动功率 (10% THD + N)
- 在 3.6V 电压条件下，每个通道可为 8Ω 负载时提供 750mW 的输出驱动功率 (10% THD + N)
- 在 5V 电压条件下，每个通道可为 4Ω 负载提供 2.8W 的输出驱动功率 (10% THD + N)
- 在 3.6V 电压条件下，每个通道可为 4Ω 负载提供 1.5W 的输出驱动功率 (10% THD + N)
- 电源范围：2.5V 至 5.5V
- 灵活操作（带/不带 I^2C）
- 可编程 DRC/AGC 参数
- 数字I^2C音量控制
- 可选增益范围从－28dB 至 30dB（1dB 步进）（当使用压缩功能时）
- 可选攻击、释放和保持时间
- 4 种可选压缩比率
- 低电源电流：3.5mA
- 低停机电流：0.2 μA
- 高PSRR：80dB
- 快速启动时间：5ms
- AGC 启用/禁用功能
- 限制器启用/禁用功能
- 短路和热保护
- 节省空间的封装
  – 2,2 mm × 2,2 mm Nano-Free™ WCSP (YZH)

应用

- 无线或蜂窝手机及 PDA
- 便携式导航设备
- 便携式 DVD 播放器
- 笔记本 PC
- 便携式收音机
- 便携式游戏机
- 教育玩具
- USB 扬声器

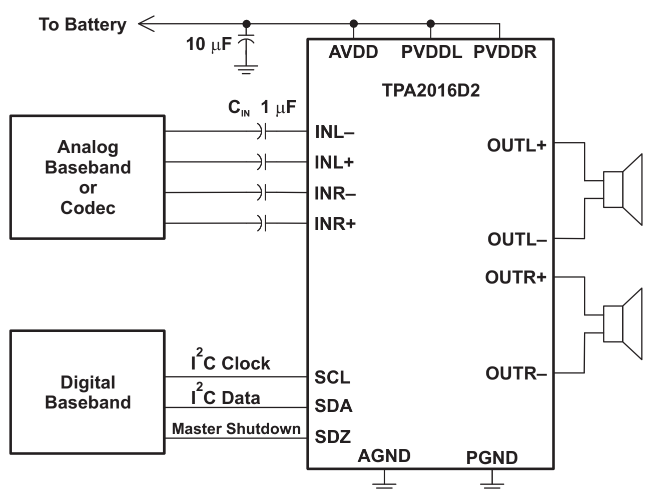
说明

TPS2016D2 是一款立体声、无滤波器的 D 类音频功率放大器，具有音量控制、动态范围压缩 (DRC) 和自动增益控制 (AGC) 功能。 该器件采用 2.2mm x 2.2mm WCSP 封装和 20 引脚 QFN 封装。

TPS2016D2 中的 DRC / AGC 功能可通过一个数字 I^2C 接口来编程。 DRC / AGC 功能可通过配置自动地防止音频信号的失真，并对一般听不到的寂静声音片段进行提升。 另外，还可以通过配置来使 DRC / AGC 功能保护扬声器在高功率电平下不受损坏，并压缩音乐的动态范围以令其处于扬声器的动态范围内。 增益的可选范围从－28dB 至＋30dB（1dB 步进）。 TPS2016D2 能为 8Ω负载提供每通道1.7W（在 5V 电压下）或750mW（在 3.3V 电压下）的驱动功率；或者为 4Ω 负载提供每通道 2.8W（在 5V 电压下）或 1.5W（在 3.3V 电压下）的驱动功率。 该器件具有用于每个通道的独立软件停机控制功能，而且还提供了热保护和短路保护。

除了上述特性之外，快速启动时间和小巧的封装尺寸还使TPS2016D2 成为蜂窝手机、PDA 和其他便携式应用的理想选择。

简化的应用示意图

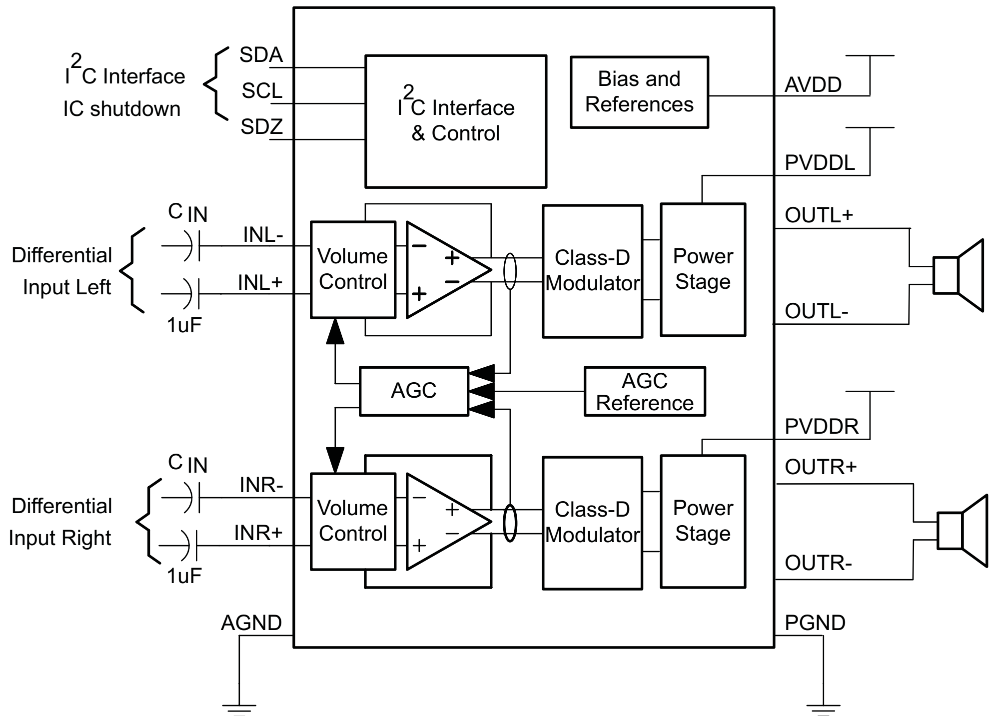


English Data Sheet: SLOS524D

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

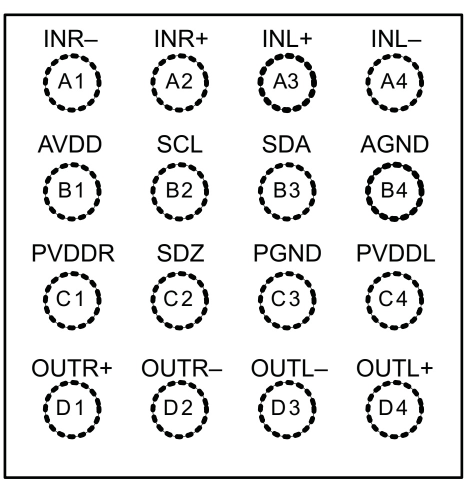
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

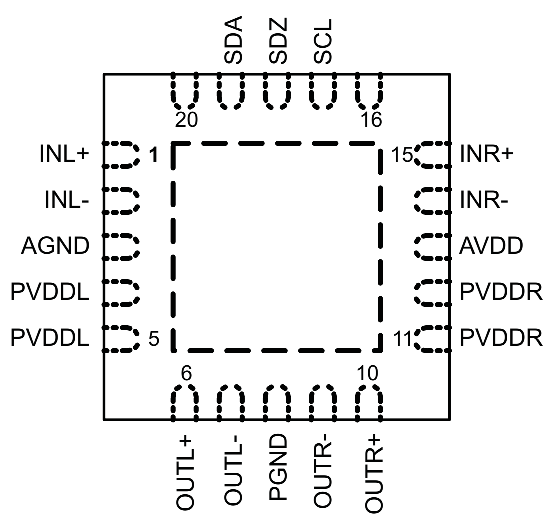


DEVICE PINOUT

YZH (WCSP) PACKAGE (Top View)



RTJ (QFN) PACKAGE (Top View)



PIN FUNCTIONS

PIN			I/O/P	DESCRIPTION
NAME	WCSP	RTJ		
INR+	A2	15	I	Right channel positive audio input
INR–	A1	14	I	Right channel negative audio input
INL+	A3	1	I	Left channel positive audio input
INL–	A4	2	I	Left channel negative audio input
SDZ	C2	18	I	Shutdown terminal (active low)
SDA	B3	19	I/O	I^2C data interface
SCL	B2	17	I	I^2C clock interface
OUTR+	D1	10	O	Right channel positive differential output
OUTR–	D2	9	O	Right channel negative differential output
OUTL+	D4	6	O	Left channel positive differential output
OUTL–	D3	7	O	Left channel negative differential output
AVDD	B1	13	P	Analog supply (must be the same as PVDDR and PVDDL)
AGND	B4	3	P	Analog ground (all GND pins need to be connected)
PVDDR	C1	11, 12	P	Right channel power supply (must be the same as AVDD and PVDDL)
PGND	C3	8	P	Power ground (all GND pins need to be connected)
PVDDL	C4	4, 5	P	Left channel power supply (must be the same as AVDD and PVDDR)
		16, 20		Not connected

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted).

			VALUE / UNIT
V_{DD}	Supply voltage	AVDD, PVDDR, PVDDL	–0.3 V to 6 V
	Input voltage	SDZ, INR+, INR–, INL+, INL–	–0.3 V to V_{DD}+0.3 V
		SDA, SCL	–0.3 V to 6 V
	Continuous total power dissipation		See Dissipation Ratings Table
T_A	Operating free-air temperature range		–40°C to +85°C
T_J	Operating junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
ESD	Electro-Static Discharge Tolerance, all pins	Human Body Model (HBM)	2 KV
		Charged Device Model (CDM)	500 V
R_{LOAD}	Minimum load resistance		3.2 Ω

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE(1)

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
16-ball WCSP	1.25 W	10 mW/°C	0.8 W	0.65 W
20–pin QFN	5.2 W	41.6 mW/°C	3.12 W	2.7 W

(1) Dissipations ratings are for a 2-side, 2-plane PCB.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES(2)	PART NUMBER	SYMBOL
–40°C to 85°C	16-ball, 2,2 mm × 2,2 mm WCSP (+0.01 mm/ -0.09 mm tolerance)	TPA2016D2YZHR	CCJ
		TPA2016D2YZHT	CCJ
–40°C to 85°C	20–pin, 4 mm × 4 mm QFN (RTJ)	TPA2016D2RTJR	–
		TPA2016D2RTJT	–

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com

(2) The YZH packages are only available taped and reeled. The suffix R indicates a reel of 3000; the suffix T indicates a reel of 250.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage	AVDD, PVDDR, PVDDL	2.5	5.5	V
V_{IH}	High-level input voltage	SDZ, SDA, SCL	1.3		V
V_{IL}	Low-level input voltage	SDZ, SDA, SCL		0.6	V
T_A	Operating free-air temperature		–40	+85	°C

ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 3.6 V, SDZ = 1.3 V, and R_L = 8 Ω + 33 μH (unless otherwise noted).

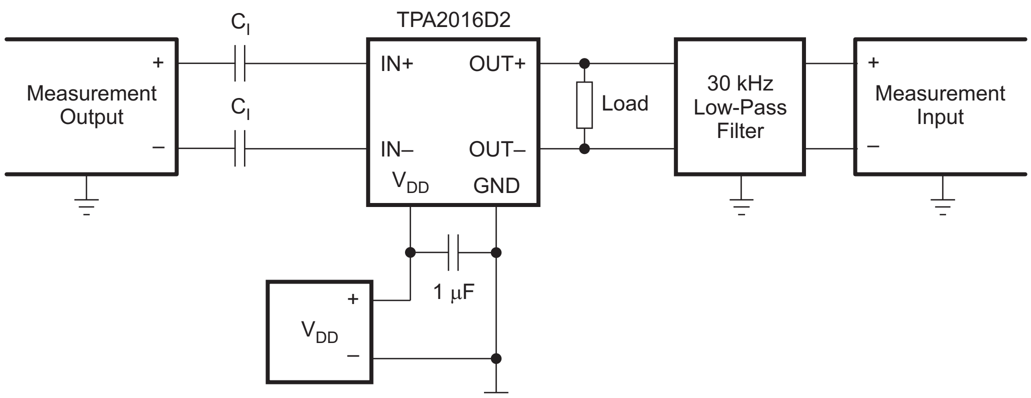
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		2.5	3.6	5.5	V
I_{SDZ}	Shutdown quiescent current	SDZ = 0.35 V, V_{DD} = 2.5 V		0.1	1	μA
		SDZ = 0.35 V, V_{DD} = 3.6 V		0.2	1	
		SDZ = 0.35 V, V_{DD} = 5.5 V		0.3	1	
I_{SWS}	Software shutdown quiescent current	SDZ = 1.3 V, V_{DD} = 2.5 V		35	50	μA
		SDZ = 1.3 V, V_{DD} = 3.6 V		50	70	
		SDZ = 1.3 V, V_{DD} = 5.5 V		75	110	
I_{DD}	Supply current	V_{DD} = 2.5 V		3.5	4.5	mA
		V_{DD} = 3.6 V		3.7	4.7	
		V_{DD} = 5.5 V		4.5	5.5	
f_{SW}	Class D Switching Frequency		275	300	325	kHz
I_{IH}	High-level input current	V_{DD} = 5.5 V, SDZ = 5.8 V			1	μA
I_{IL}	Low-level input current	V_{DD} = 5.5 V, SDZ = –0.3 V	–1			μA
t_{START}	Start-up time	2.5 V ≤ V_{DD} ≤ 5.5 V no pop, C_{IN} ≤ 1 μF		5		ms
POR	Power on reset ON threshold			2	2.3	V
POR	Power on reset hysteresis			0.2		V
CMRR	Input common mode rejection	R_L = 8 Ω, V_{icm} = 0.5 V and V_{icm} = V_{DD} – 0.8 V, differential inputs shorted		–70		dB
V_{oo}	Output offset voltage	V_{DD} = 3.6 V, A_V = 6 dB, R_L = 8 Ω, inputs ac grounded	–10	2	10	mV
Z_{OUT}	Output Impedance in shutdown mode	SDZ = 0.35 V		2		kΩ
	Gain accuracy	Compression and limiter disabled, Gain = 0 to 30 dB	–0.5		0.5	dB
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 4.7 V		-80		dB

OPERATING CHARACTERISTICS

at T_A = 25°C, V_{DD} = 3.6V, SDZ = 1.3 V, R_L = 8 Ω +33 μH, and A_V = 6 dB (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
k_{SVR}	power-supply ripple rejection ratio	V_{DD} = 3.6 Vdc with ac of 200 mV_{PP} at 217 Hz		–68		dB
THD+N	Total harmonic distortion + noise	f_{aud_in} = 1 kHz; P_O = 550 mW; V_{DD} = 3.6 V		0.1%		
		f_{aud_in} = 1 kHz; P_O = 1 W; V_{DD} = 5 V		0.1%		
		f_{aud_in} = 1 kHz; P_O = 630 mW; V_{DD} = 3.6 V		1%		
		f_{aud_in} = 1 kHz; P_O = 1.4 W; V_{DD} = 5 V		1%		
Nfo_{nF}	Output integrated noise	Av = 6 dB		44		μV
Nfo_A	Output integrated noise	Av = 6 dB floor, A-weighted		33		μV
FR	Frequency response	Av = 6 dB	20		20000	Hz
Po_{max}	Maximum output power	THD+N = 10%, V_{DD} = 5 V, R_L = 8 Ω		1.72		W
		THD+N = 10%, V_{DD} = 3.6 V, R_L = 8 Ω		750		mW
		THD+N = 10%, V_{DD} = 5 V, R_L = 4 Ω		2.8		W
		THD+N = 10% , V_{DD} = 3.6 V, R_L = 4 Ω		1.5		mW
η	Efficiency	THD+N = 1%, V_{DD} = 3.6 V, R_L = 8 Ω, P_O= 0.63 W		90%		
		THD+N = 1%, V_{DD} = 5 V, R_L = 8 Ω, P_O = 1.4 W		90%		

Figure 1. TEST SET-UP FOR GRAPHS



(1) All measurements were taken with a 1-μF C_I (unless otherwise noted.)
(2) A 33-μH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.
(3) The 30-kHz low-pass filter is required, even if the analyzer has an internal low-pass filter. An RC low-pass filter (1 kΩ 4.7 nF) is used on each output for the data sheet graphs.
(4) All THD + N graphs are taken with outputs out of phase (unless otherwise noted). All data is taken on left channel.
(5) All data is taken on the WCSP package unless otherwise noted.

I²C TIMING CHARACTERISTICS

For I²C Interface Signals Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states			400	kHz
$t_{W(H)}$	Pulse duration, SCL high		0.6			µs
$t_{W(L)}$	Pulse duration, SCL low		1.3			µs
$t_{SU(1)}$	Setup time, SDA to SCL		100			ns
t_{h1}	Hold time, SCL to SDA		10			ns
$t_{(buf)}$	Bus free time between stop and start condition		1.3			µs
t_{SU2}	Setup time, SCL to start condition		0.6			µs
t_{h2}	Hold time, start condition to SCL		0.6			µs
t_{SU3}	Setup time, SCL to stop condition		0.6			µs

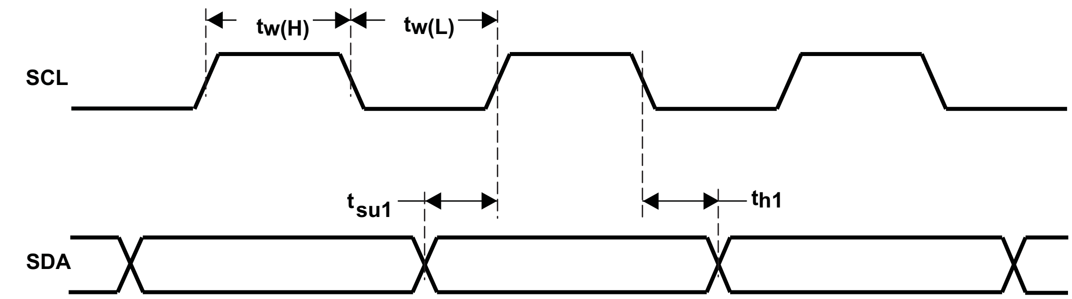


Figure 2. SCL and SDA Timing

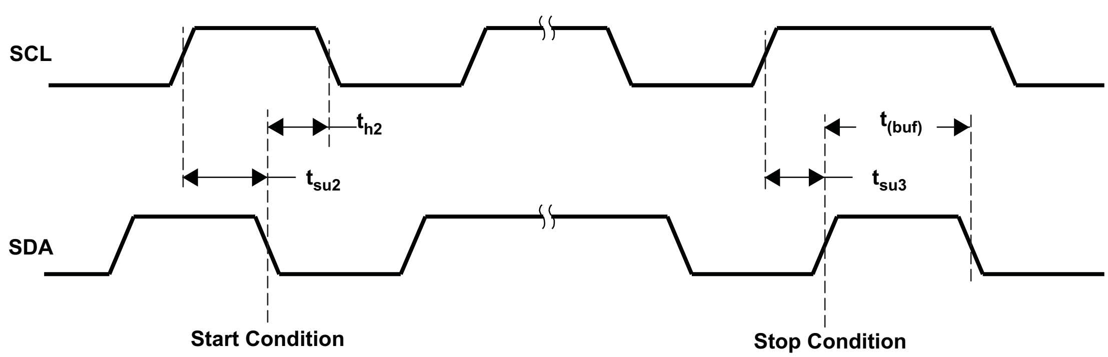


Figure 3. Start and Stop Conditions Timing

TYPICAL CHARACTERISTICS

with $C_{(DECOUPLE)}$ = 1 μF, C_I = 1 μF.

QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

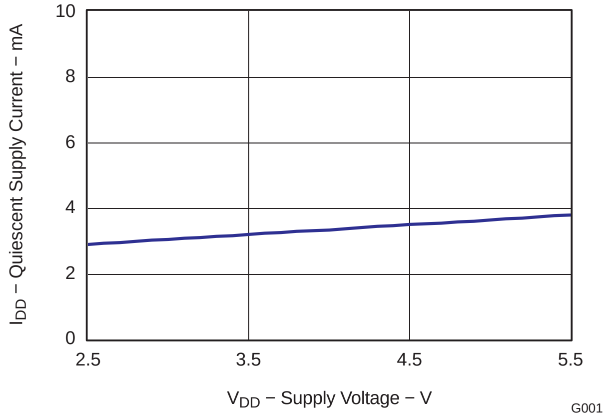


Figure 4.

SUPPLY CURRENT vs SUPPLY VOLTAGE IN SHUTDOWN

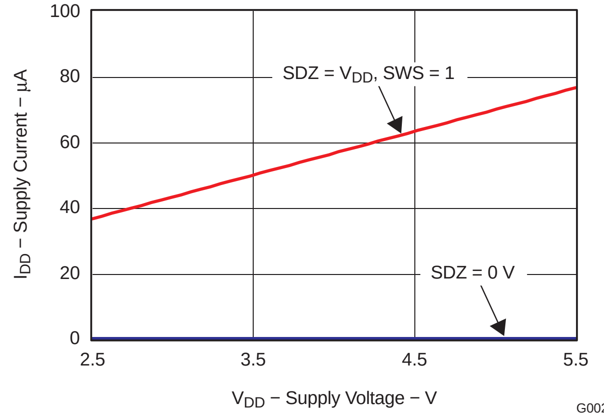


Figure 5.

OUTPUT LEVEL vs INPUT LEVEL WITH LIMITER ENABLED

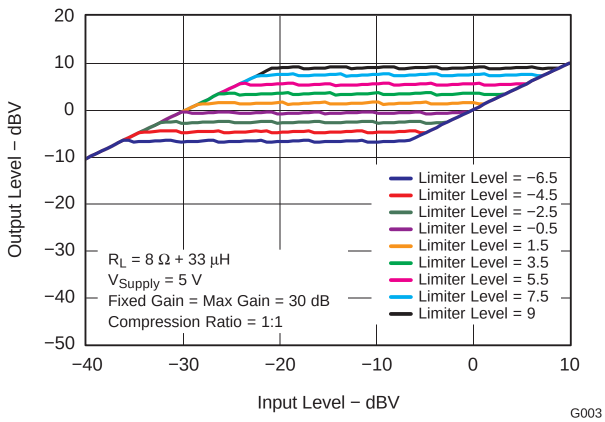


Figure 6.

OUTPUT LEVEL vs INPUT LEVEL WITH 2:1 COMPRESSION

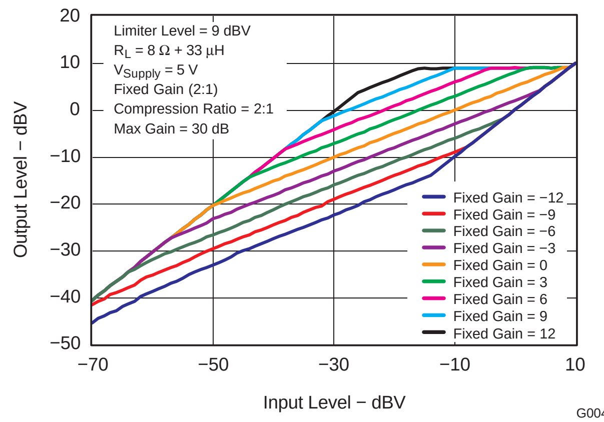


Figure 7.

TYPICAL CHARACTERISTICS (continued)

with $C_{(DECOUPLE)}$ = 1 µF, C_I = 1 µF.

OUTPUT LEVEL vs INPUT LEVEL WITH 4:1 COMPRESSION

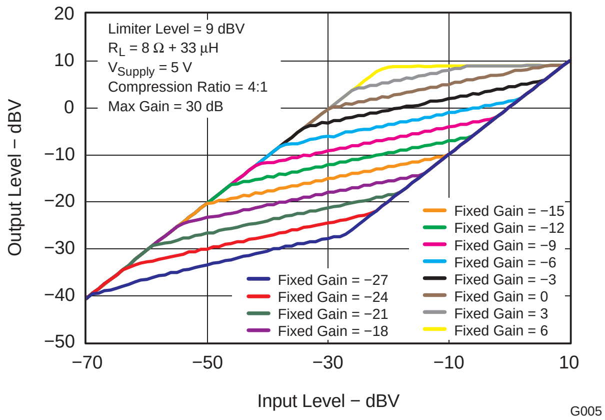


Figure 8.

OUTPUT LEVEL vs INPUT LEVEL WITH 8:1 COMPRESSION

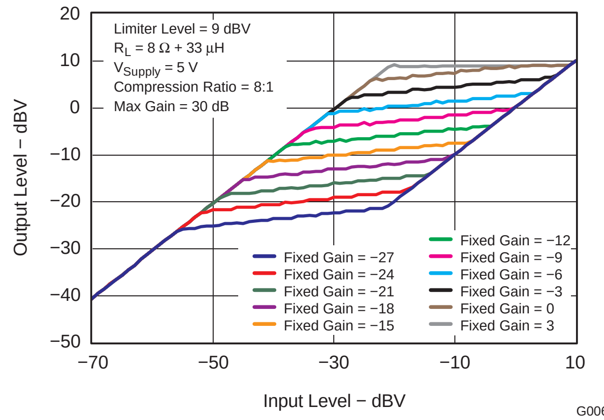


Figure 9.

OUTPUT LEVEL vs INPUT LEVEL

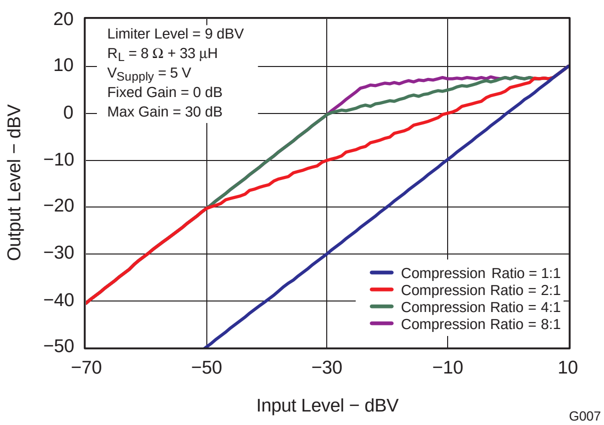


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

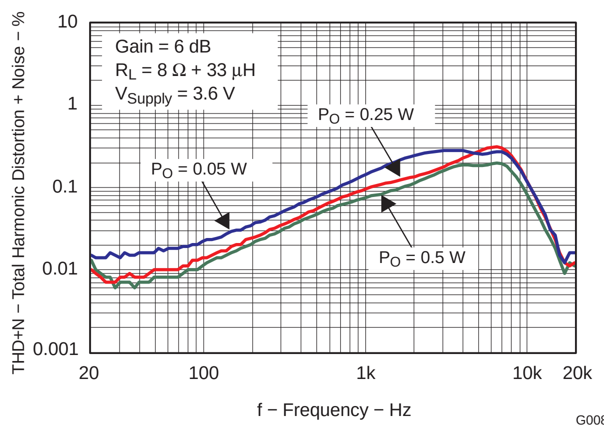


Figure 11.

TYPICAL CHARACTERISTICS (continued)

with $C_{(DECOUPLE)}$ = 1 µF, C_I = 1 µF.

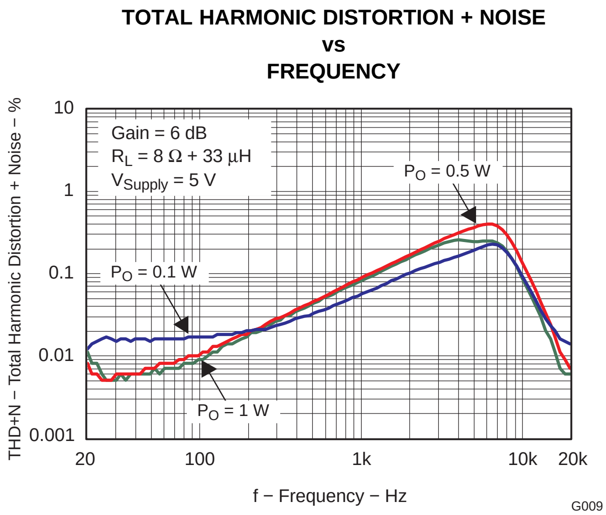


Figure 12.

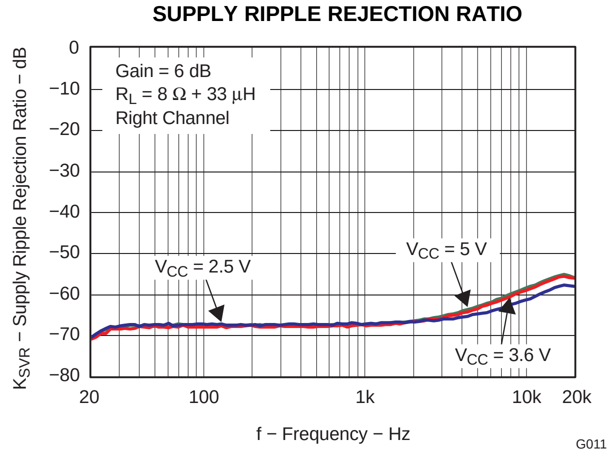


Figure 13.

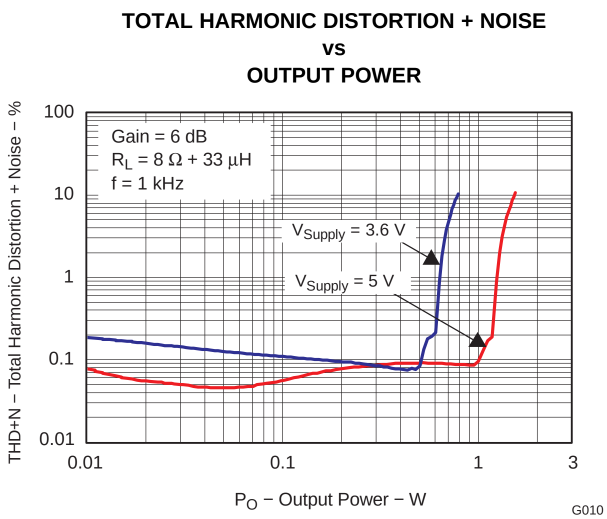


Figure 14.

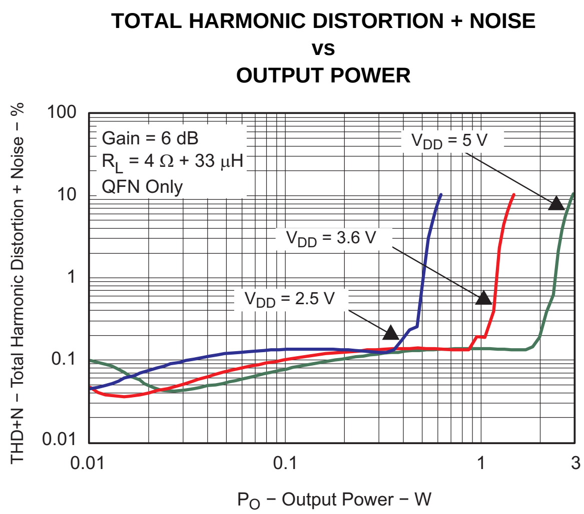


Figure 15.

TYPICAL CHARACTERISTICS (continued)

with $C_{(DECOUPLE)}$ = 1 µF, C_I = 1 µF.

EFFICIENCY vs OUTPUT POWER (PER CHANNEL)

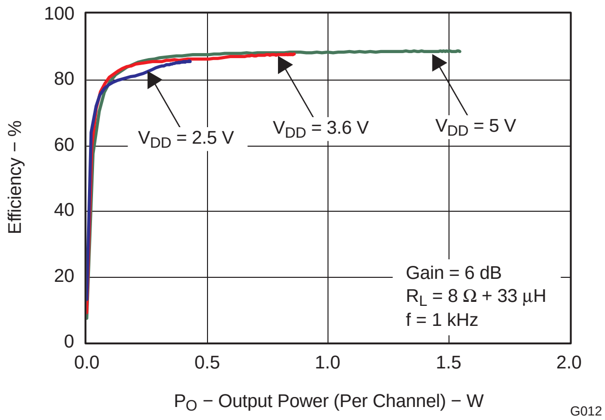


Figure 16.

EFFICIENCY vs OUTPUT POWER (PER CHANNEL)

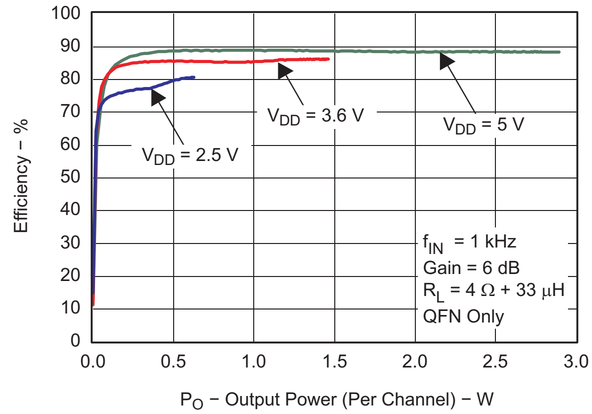


Figure 17.

TOTAL POWER DISSIPATION vs TOTAL OUTPUT POWER

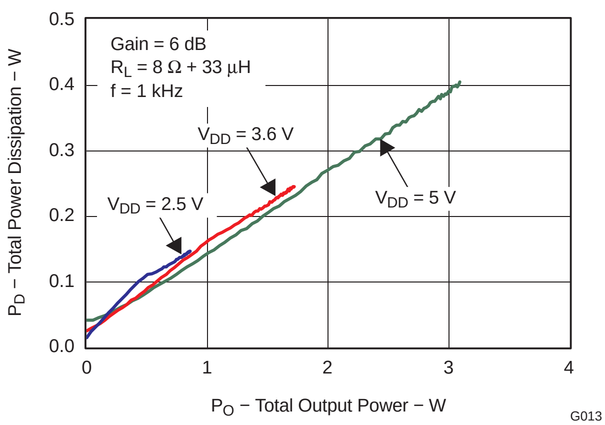


Figure 18.

TOTAL POWER DISSIPATION vs TOTAL OUTPUT POWER

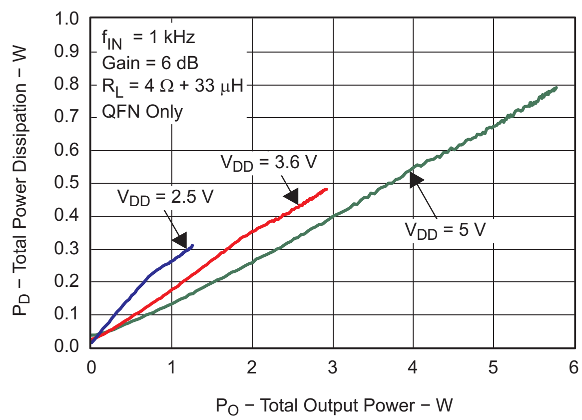


Figure 19.

TYPICAL CHARACTERISTICS (continued)

with $C_{(DECOUPLE)}$ = 1 µF, C_I = 1 µF.

TOTAL SUPPLY CURRENT vs TOTAL OUTPUT POWER

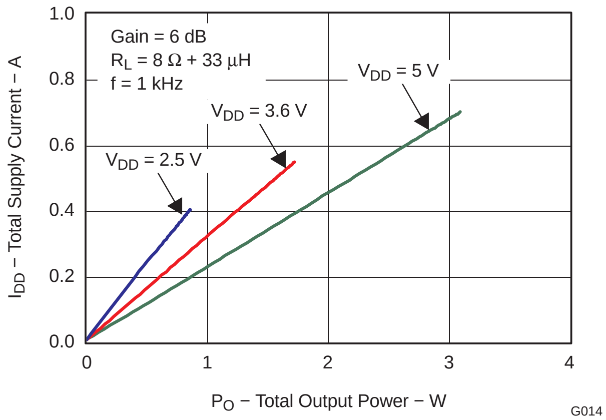


Figure 20.

TOTAL SUPPLY CURRENT vs TOTAL OUTPUT POWER

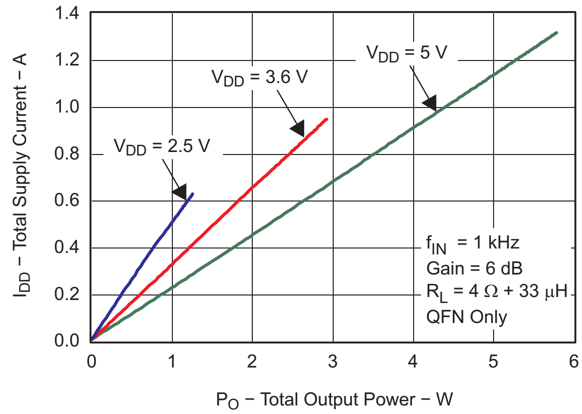


Figure 21.

OUTPUT POWER vs SUPPLY VOLTAGE

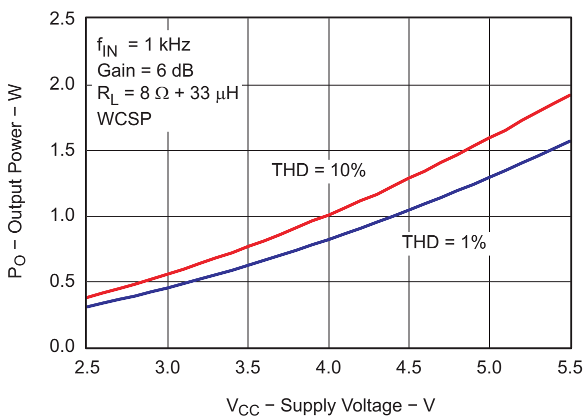


Figure 22.

OUTPUT POWER vs SUPPLY VOLTAGE

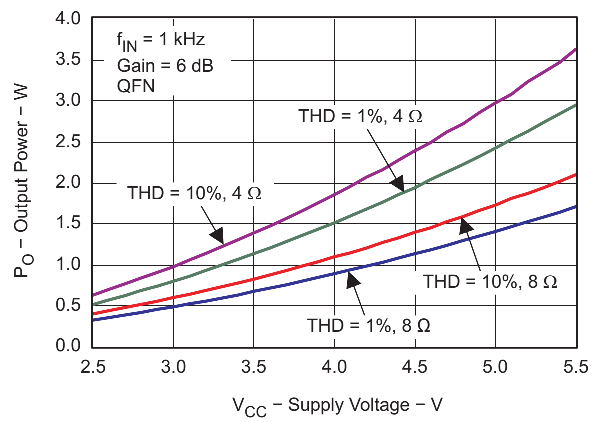


Figure 23.

APPLICATION INFORMATION

AUTOMATIC GAIN CONTROL

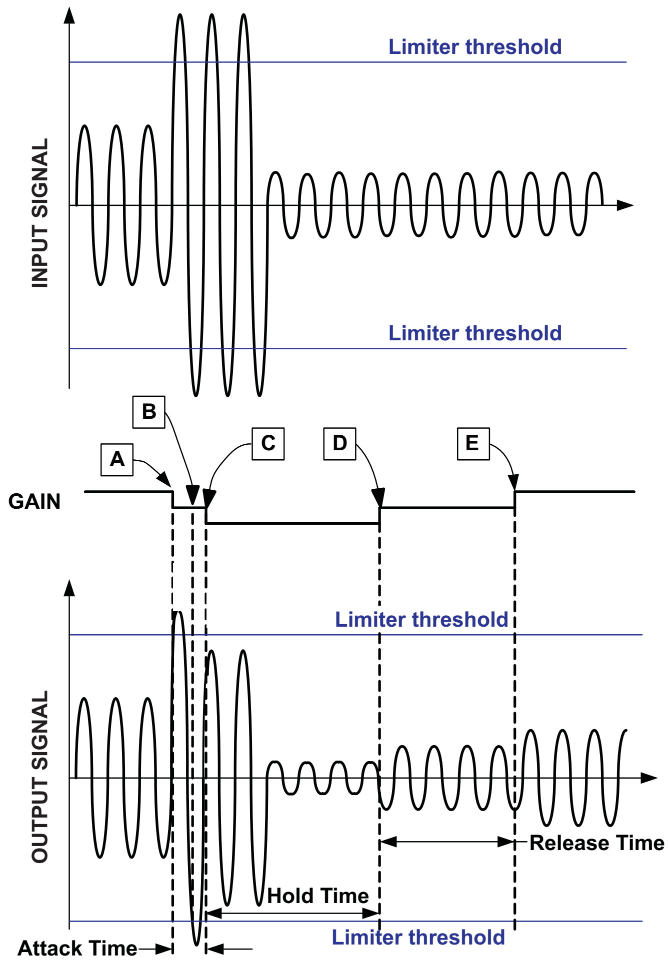
The Automatic Gain Control (AGC) feature provides continuous automatic gain adjustment to the amplifier through an internal PGA. This feature enhances the perceived audio loudness and at the same time prevents speaker damage from occurring (Limiter function).

The AGC function attempts to maintain the audio signal gain as selected by the user through the Fixed Gain, Limiter Level, and Compression Ratio variables. Other advanced features included are Maximum Gain and Noise Gate Threshold. Table 1 describes the function of each variable in the AGC function.

Table 1. TPA2016D2 AGC Variable Descriptions

VARIABLE	DESCRIPTION
Maximum Gain	The gain at the lower end of the compression region.
Fixed Gain	The normal gain of the device when the AGC is inactive. The fixed gain is also the initial gain when the device comes out of shutdown mode or when the AGC is disabled.
Limiter Level	The value that sets the maximum allowed output amplitude.
Compression Ratio	The relation between input and output voltage.
Noise Gate Threshold	Below this value, the AGC holds the gain to prevent breathing effects.
Attack Time	The minimum time between two gain decrements.
Release Time	The minimum time between two gain increments.
Hold Time	The time it takes for the very first gain increment after the input signal amplitude decreases.

The AGC works by detecting the audio input envelope. The gain changes depending on the amplitude, the limiter level, the compression ratio, and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases to create the compression effect. The gain step size for the AGC is 0.5 dB. If the audio signal has near-constant amplitude, the gain does not change. Figure 26 shows how the AGC works.



A. Gain decreases with no delay; attack time is reset. Release time and hold time are reset.
B. Signal amplitude above limiter level, but gain cannot change because attack time is not over.
C. Attack time ends; gain is allowed to decrease from this point forward by one step. Gain decreases because the amplitude remains above limiter threshold. All times are reset
D. Gain increases after release time finishes and signal amplitude remains below desired level. All times are reset after the gain increase.
E. Gain increases after release time is finished again because signal amplitude remains below desired level. All times are reset after the gain increase.

Figure 26. Input and Output Audio Signal vs Time

Since the number of gain steps is limited the compression region is limited as well. The following figure shows how the gain changes vs. the input signal amplitude in the compression region.

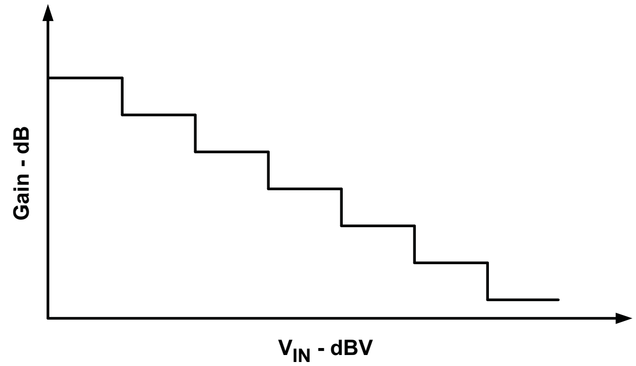


Figure 27. Input Signal Voltage vs Gain

Thus the AGC performs a mapping of the input signal vs. the output signal amplitude. This mapping can be modified according to the variables from Table 1.

The following graphs and explanations show the effect of each variable to the AGC independently and which considerations should be taken when choosing values.

Fixed Gain: The fixed gain determines the initial gain of the AGC. Set the gain using the following variables:

- Set the fixed gain to be equal to the gain when the AGC is disabled.
- Set the fixed gain to maximize SNR.
- Set the fixed gain such that it will not overdrive the speaker.

Figure 28 shows how the fixed gain influences the input signal amplitude vs. the output signal amplitude state diagram. The dotted 1:1 line is displayed for reference. The 1:1 line means that for a 1dB increase in the input signal, the output increases by 1dB.

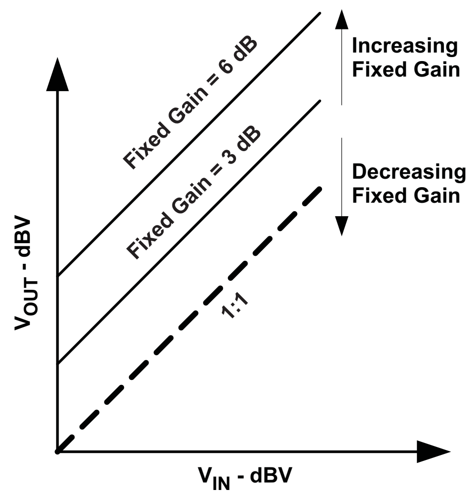


Figure 28. Output Signal vs Input Signal State Diagram Showing Different Fixed Gain Configurations

If the Compression function is enabled, the Fixed Gain is adjustable from –28dB to 30dB. If the Compression function is disabled, the Fixed gain is adjustable from 0dB to 30dB.

Limiter Level: The Limiter level sets the maximum amplitude allowed at the output of the amplifier. The limiter should be set with the following constraints in mind:

- Below or at the maximum power rating of the speaker
- Below the minimum supply voltage in order to avoid clipping

Figure 29 shows how the limiter level influences the input signal amplitude vs. the output signal amplitude state diagram.

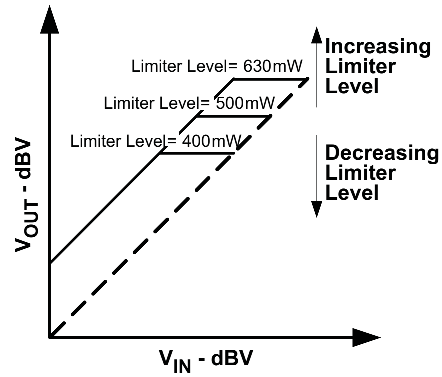


Figure 29. Output Signal vs Input Signal State Diagram Showing Different Limiter Level Configurations

The limiter level and the fixed gain influence each other. If the fixed gain is set high, the AGC has a large limiter range. The fixed gain is set low, the AGC has a short limiter range. Figure 30 illustrates the two examples:

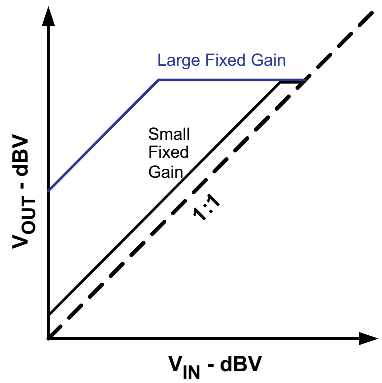


Figure 30. Output Signal vs. Input Signal State Diagram Showing Same Limiter Level Configurations with Different Fixed Gain Configurations

Compression Ratio: The compression ratio sets the relation between input and output signal outside the limiter level region. The compression ratio compresses the dynamic range of the audio. For example if the audio source has a dynamic range of 60dB and compression ratio of 2:1 is selected, then the output has a dynamic range of 30dB. Most small form factor speakers have small dynamic range. Compression ratio allows audio with large dynamic range to fit into a speaker with small dynamic range.

The compression ratio also increases the loudness of the audio without increasing the peak voltage. The higher the compression ratio, the louder the perceived audio.

For example:

- A compression ratio of 4:1 is selected (meaning that a 4dB change in the input signal results in a 1dB signal change at the output)
- A fixed gain of 0dB is selected and the maximum audio level is at 0dBV.

When the input signal decreases to –32dBV, the amplifier increases the gain to 24dB in order to achieve an output of –8dBV. The output signal amplitude equation is:

$$\text{Output signal amplitude} = \frac{\text{Input signal initial amplitude - |Current input signal amplitude|}}{\text{Compression ratio}} \tag{1}$$

In this example:

$$-8\text{dBV} = \frac{0\text{dBV} - |-32\text{ dBV}|}{4} \tag{2}$$

The gain change equation is:

$$\text{Gain change} = \left(1 - \frac{1}{\text{Compression ratio}}\right) \times \text{Input signal change} \tag{3}$$

$$24\ \text{dB} = \left(1 - \frac{1}{4}\right) \times 32 \tag{4}$$

Consider the following when setting the compression ratio:

- Dynamic range of the speaker
- Fixed gain level
- Limiter Level
- Audio Loudness vs Output Dynamic Range.

Figure 31 shows different settings for dynamic range and different fixed gain selected but no limiter level.

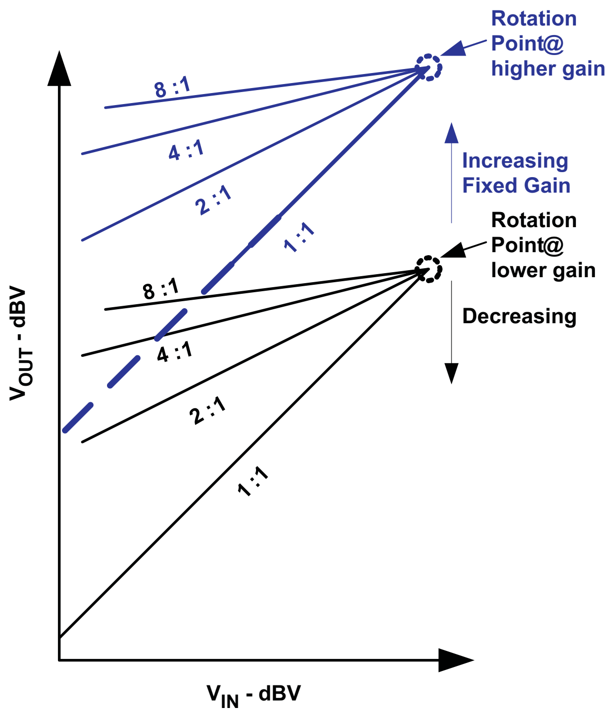


Figure 31. Output Signal vs Input Signal State Diagram Showing Different Compression Ratio Configurations with Different Fixed Gain Configurations

The rotation point is always at Vin = 10dBV. The rotation point is not located at the intersection of the limiter region and the compression region. By changing the fixed gain the rotation point will move in the y-axis direction only, as shown in the previous graph.

Interaction between compression ratio and limiter range: The compression ratio can be limited by the limiter range. Note that the limiter range is selected by the limiter level and the fixed gain.

For a setting with large limiter range, the amount of gain steps in the AGC remaining to perform compression are limited. Figure 32 shows two examples, where the fixed gain was changed.

1. Small limiter range yielding a large compression region (small fixed gain).
2. Large limiter range yielding a small compression region (large fixed gain).

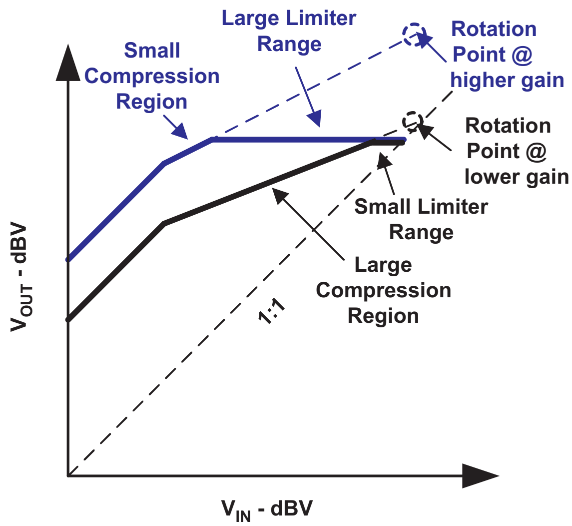


Figure 32. Output Signal vs Input Signal State Diagram Showing the Effects of the Limiter Range to the Compression Region

Noise Gate Threshold: The noise gate threshold prevents the AGC from changing the gain when there is no audio at the input of the amplifier. The noise gate threshold stops gain changes until the input signal is above the noise gate threshold. Select the noise gate threshold to be above the noise but below the minimum audio at the input of the amplifier signal. A filter is needed between delta-sigma CODEC/DAC and TPA2016D2 for effectiveness of the noise gate function. The filter eliminates the out-of-band noise from delta-sigma modulation and keeps the CODEC/DAC output noise lower than the noise gate threshold.

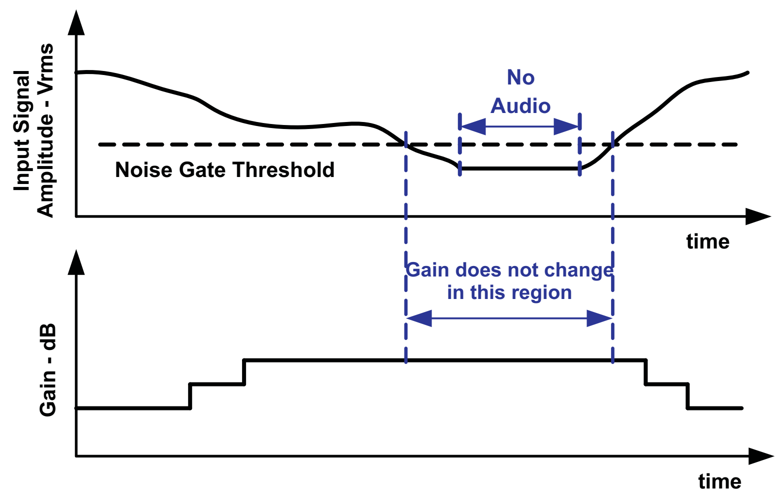


Figure 33. Time Diagram Showing the Relationship Between Input Signal Amplitude, Noise Gate Threshold and Gain Versus Time

Maximum Gain: This variable limits the number of gain steps in the AGC. This feature is useful in order to accomplish a more advanced output signal vs. input signal transfer characteristic.

For example, to prevent the gain from going above a certain value, reduce the maximum gain.

However, this variable will affect the limiter range and the compression region. If the maximum gain is decreased, the limiter range and/or compression region is reduced. Figure 34 illustrates the effects.

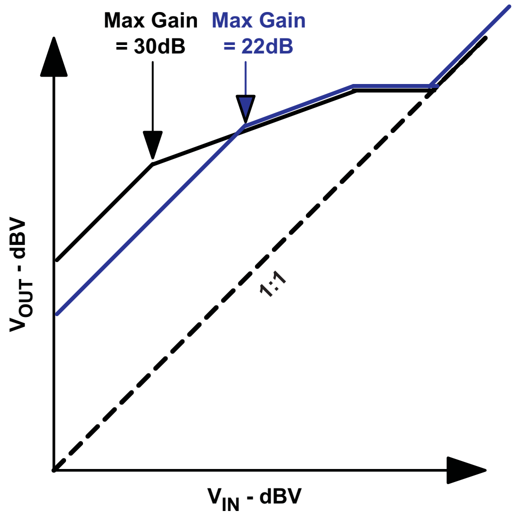


Figure 34. Output Signal vs. Input Signal State Diagram Showing Different Maximum Gains

A particular application requiring maximum gain of 22dB, for example. Thus, set the maximum gain at 22dB. The amplifier gain will never have a gain higher than 22dB; however, this will reduce the limiter range.

Attack, Release, and Hold time:

- The attack time is the minimum time between gain decreases.
- The release time is the minimum time between gain increases.
- The hold time is the minimum time between a gain decrease (attack) and a gain increase (release). The hold time can be deactivated. Hold time is only valid if greater than release time.

Successive gain decreases are never faster than the attack time. Successive gain increases are never faster than the release time.

All time variables (attack, release and hold) start counting after each gain change performed by the AGC. The AGC is allowed to decrease the gain (attack) only after the attack time finishes. The AGC is allowed to increase the gain (release) only after the release time finishes counting. However, if the preceding gain change was an attack (gain increase) and the hold time is enabled and longer than the release time, then the gain is only increased after the hold time.

The hold time is only enabled after a gain decrease (attack). The hold time replaces the release time after a gain decrease (attack). If the gain needs to be increased further, then the release time is used. The release time is used instead of the hold time if the hold time is disabled.

The attack time should be at least 100 times shorter than the release and hold time. The hold time should be the same or greater than the release time. It is important to select reasonable values for those variables in order to prevent the gain from changing too often or too slow.

Figure 35 illustrates the relationship between the three time variables.

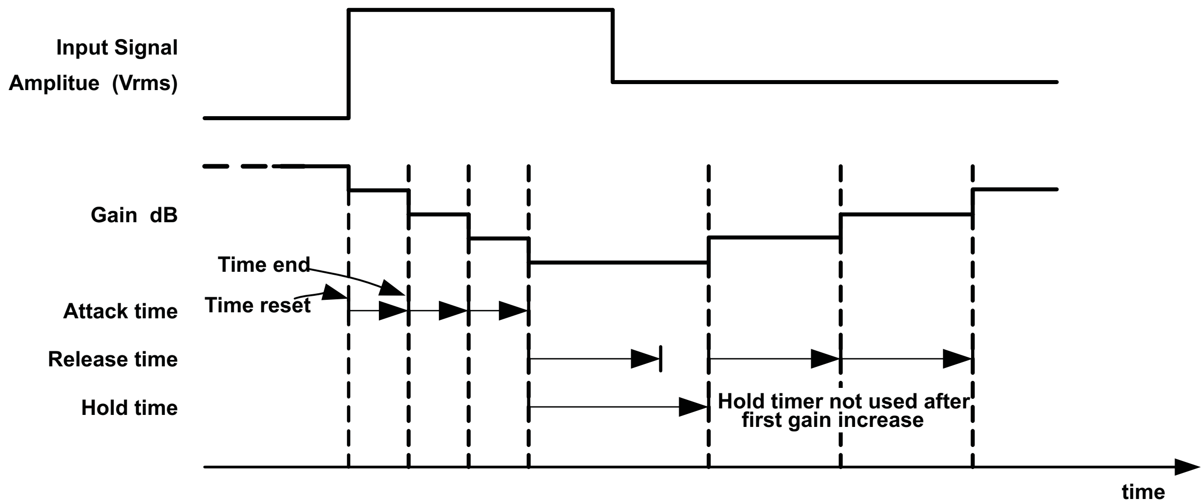


Figure 35. Time Diagram Showing the Relation Between the Attack, Release, and Hold Time vs Input Signal Amplitude and Gain

Figure 36 shows a state diagram of the input signal amplitude vs. the output signal amplitude and a summary of how the variables from table 1 described in the preceding pages affect them.

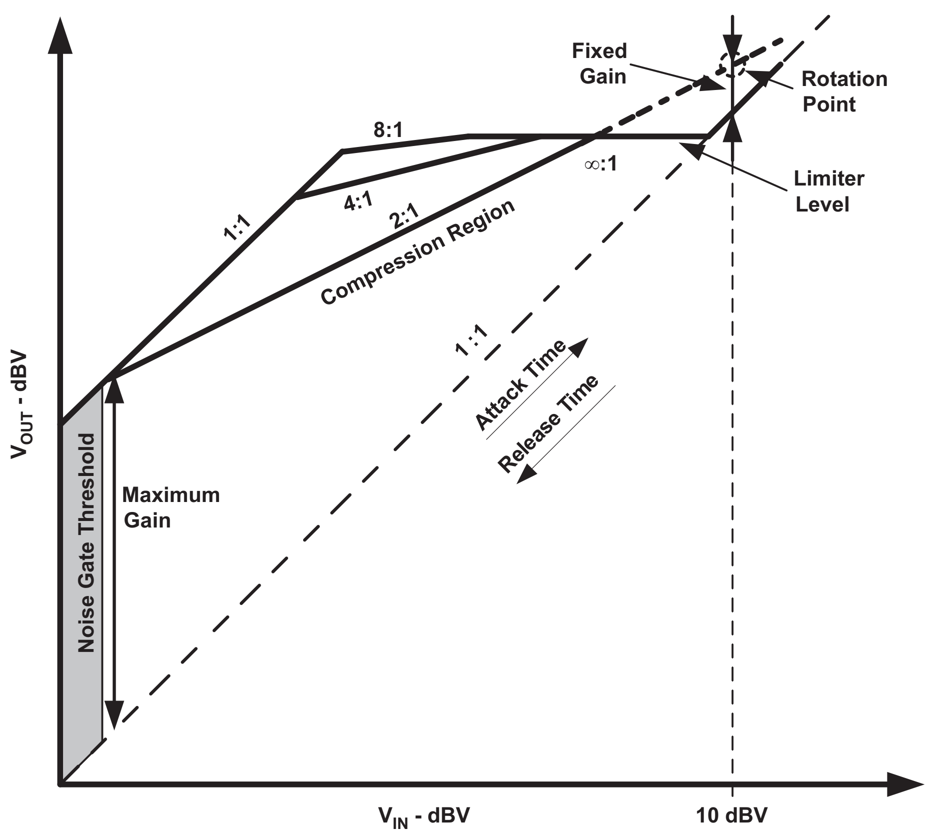


Figure 36. Output Signal vs. Input Signal State Diagram

TPA2016D2 AGC OPERATION

The TPA2016D2 is controlled by the I^2C interface. The correct start-up sequence is:

1. Apply the supply voltage to the AV_{DD} and PV_{DD} (L, R)pins.
2. Apply a voltage above V_{IH} to the SDZ pin. The TPA2016D2 powers up the I^2C interface and the control logic. By default, the device is in active mode (SWS = 0). After a few milliseconds the amplifier will enable the class-D output stage and become fully operational.
3. The amplifier starts at a gain of 0 dB and the AGC starts ramping the gain after the input signal exceeds the noise gate threshold.

CAUTION

Do not interrupt the start-up sequence after changing SDZ from V_{IL} to V_{IH}.

Do not interrupt the start-up sequence after changing SWS from 1 to 0.

The default conditions of TPA2016D2 allows audio playback without I2C control. Refer to Table 4 for entire default conditions.

There are several options to disable the amplifier:

- Write SPK_EN_R = 0 and SPK_EN_L = 0 to the register (0x01, 6 and 0x01, 7). This write disables each speaker amplifier, but leaves all other circuits operating.
- Write SWS = 1 to the register (0x01, 5). This action disables most of the amplifier functions.
- Apply V_{IL} to SDZ. This action shuts down all the circuits and has very low quiescent current consumption. This action resets the registers to its default values.

CAUTION

Do not interrupt the shutdown sequence after changing SDZ from V_{IH} to V_{IL}.

Do not interrupt the shutdown sequence after changing SWS from 0 to 1.

TPA2016D2 AGC RECOMMENDED SETTINGS

Table 2. Recommended AGC Settings for Different Types of Audio Source (V_{DD} = 3.6V)

AUDIO SOURCE	COMPRESSION RATIO	ATTACK TIME (ms/6 dB)	RELEASE TIME (ms/6 dB)	HOLD TIME (ms)	FIXED GAIN (dB)	LIMITER LEVEL (dBV)
Pop Music	4:1	1.28 to 3.84	986 to 1640	137	6	7.5
Classical	2:1	2.56	1150	137	6	8
Jazz	2:1	5.12 to 10.2	3288	—	6	8
Rap/ Hip Hop	4:1	1.28 to 3.84	1640	—	6	7.5
Rock	2:1	3.84	4110	—	6	8
Voice/ News	4:1	2.56	1640	—	6	8.5

GENERAL I^2C OPERATION

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially one bit at a time. The address and data 8-bit bytes are transferred most significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an *acknowledge* bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 37 shows a typical sequence. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device, and then waits for an acknowledge condition. The TPA2016D2 holds SDA low during the acknowledge clock period to indicate acknowledgment. When this acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

An external pull-up resistor must be used for the SDA and SCL signals to set the logic high level for the bus. When the bus level is 5 V, use pull-up resistors between 1 kΩ and 2 kΩ.

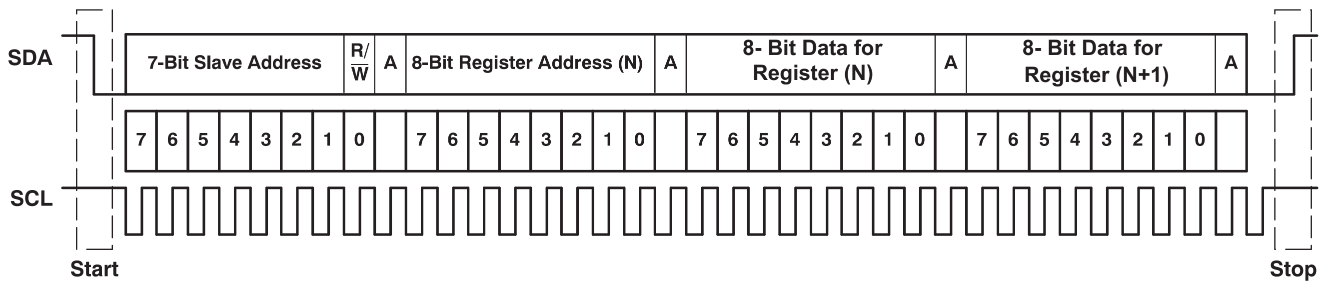


Figure 37. Typical I^{2}C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 37.

SINGLE-AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multi-byte read/write operations for all registers.

During multiple-byte read operations, the TPA2016D2 responds with data, one byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledgments.

The TPA2016D2 supports sequential I^{2}C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I^{2}C write transaction has occurred. For I^{2}C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines the number of registers written.

SINGLE-BYTE WRITE

As Figure 38 shows, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to '0'. After receiving the correct I^{2}C device address and the read/write bit, the TPA2016D2 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA2016D2 internal memory address being accessed. After receiving the register byte, the TPA2016D2 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the register byte, the TPA2016D2 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

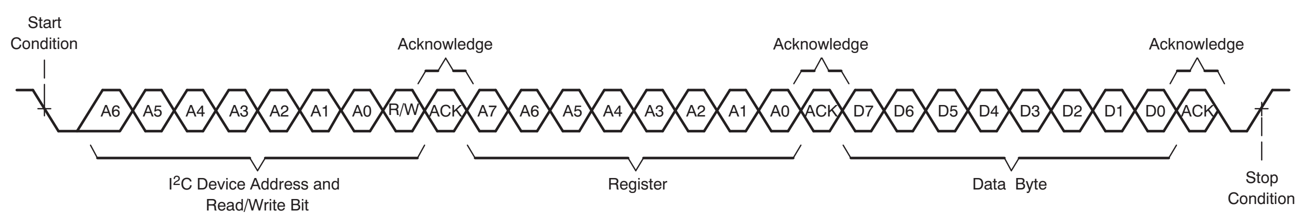


Figure 38. Single-Byte Write Transfer

MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TPA2016D2 as shown in Figure 39. After receiving each data byte, the TPA2016D2 responds with an acknowledge bit.

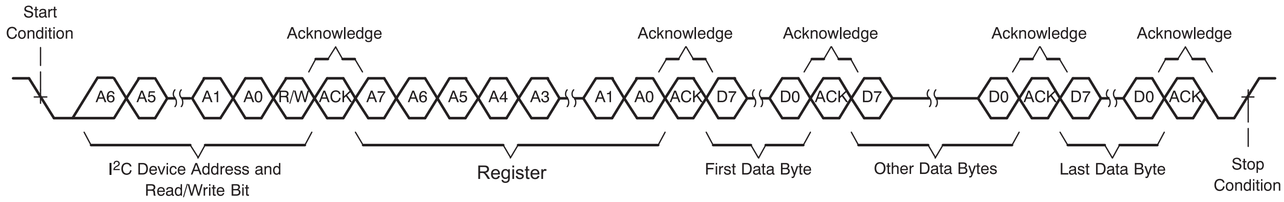


Figure 39. Multiple-Byte Write Transfer

SINGLE-BYTE READ

As Figure 40 shows, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually executed. Initially, a write is executed to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a '0'.

After receiving the TPA2016D2 address and the read/write bit, the TPA2016D2 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA2016D2 issues an acknowledge bit. The master device transmits another start condition followed by the TPA2016D2 address and the read/write bit again. This time the read/write bit is set to '1', indicating a read transfer. Next, the TPA2016D2 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a *not-acknowledge* followed by a stop condition to complete the single-byte data read transfer.

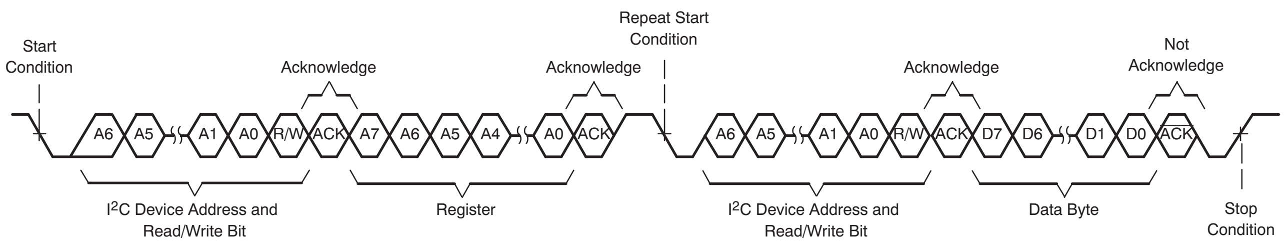


Figure 40. Single-Byte Read Transfer

MULTIPLE-BYTE READ

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TPA2016D2 to the master device as shown in Figure 41. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

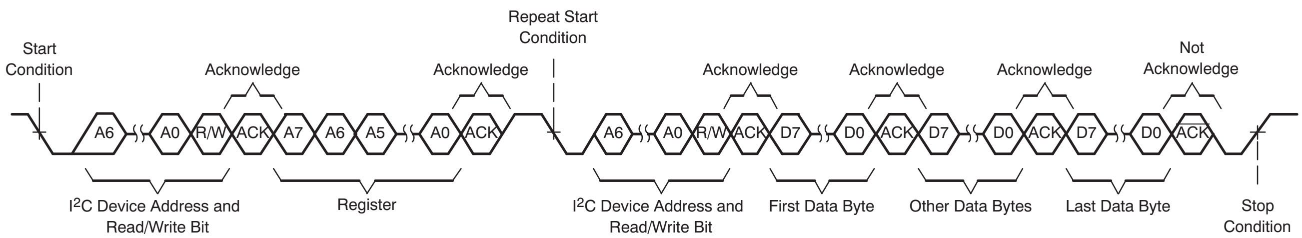


Figure 41. Multiple-Byte Read Transfer

Register Map

Table 3. TPA2016D2 Register Map

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	SPK_EN_R	SPL_EN_L	SWS	FAULT_R	FAULT_L	Thermal	1	NG_EN
2	0	0	ATK_time [5]	ATK_time [4]	ATK_time [3]	ATK_time [2]	ATK_time [1]	ATK_time [0]
3	0	0	REL_time [5]	REL_time [4]	REL_time [3]	REL_time [2]	REL_time [1]	REL_time [0]
4	0	0	Hold_time [5]	Hold_time [4]	Hold_tme [3]	Hold_time [2]	Hold_time [1]	Hold_time [0]
5	0	0	FixedGain [5]	FixedGain [4]	FixedGain [3]	FixedGain [2]	FixedGain [1]	FixedGain [0]
6	Output Limiter Disable	NoiseGate Threshold [1]	NoiseGate Threshold [2]	Output Limiter Level [4]	Output Limiter Level [3]	Output Limiter Level [2]	Output Limiter Level [1]	Output Limiter Level [0]
7	Max Gain [3]	Max Gain [2]	Max Gain [1]	Max Gain [0]	0	0	Compression Ratio [1]	Compression Ratio [0]

The default register map values are given in Table 4.

Table 4. TPA2016D2 Default Register Values Table

Register	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Default	C3h	05h	0Bh	00h	06h	3Ah	C2h

Any register above address 0x08 is reserved for testing and should not be written to because it may change the function of the device. If read, these bits may assume any value.

Some of the default values can be reprogrammed through the I^{2}C interface and written to the EEPROM. This function is useful to speed up the turn-on time of the device and minimizes the number of I^{2}C writes. If this is required, contact your local TI representative.

The TPA2016D2 I^{2}C address is 0xB0 (binary 10110000) for writing and 0xB1 (binary 10110001) for reading. If a different I^{2}C address is required, please contact your local TI representative. See the General I2C operation section for more detail.

The following tables show the details of the registers, the default values, and the values that can be programmed through the I^{2}C interface.

IC FUNCTION CONTROL (Address: 1)

REGISTER ADDRESS	I2C BIT	LABEL	DEFAULT	DESCRIPTION
01 (01_H) – IC Function Control	7	SPK_EN_R	1 (enabled)	Enables right amplifier
	6	SPK_EN_L	1 (enabled)	Enables left amplifier
	5	SWS	0 (enabled)	Shutdown IC when bit = 1
	4	FAULT_R	0	Changes to a 1 when there is a short on the right channel. Reset by writing a 0.
	3	FAULT_L	0	Changes to a 1 when there is a short on the left channel. Reset by writing a 0
	2	Thermal	0	Changes to a 1 when die temperature is above 150°C
	1	UNUSED	1	
	0	NG_EN	1 (enabled)	Enables Noise Gate function

SPK_EN_R: Enable bit for the right-channel amplifier. Amplifier is active when bit is high. This function is gated by thermal and returns once the IC is below the threshold temperature.

SPK_EN_L: Enable bit for the left-channel amplifier. Amplifier is active when bit is high. This function is gated by thermal and returns once the IC is below the threshold temperature

SWS: Software shutdown control. The device is in software shutdown when the bit is '1' (control, bias and oscillator are inactive). When the bit is '0' the control, bias and oscillator are enabled.

Fault_L: This bit indicates that an over-current event has occurred on the left channel with a '1'. This bit is cleared by writing a '0' to it.

Fault_R: This bit indicates that an over-current event has occurred on the right channel with a '1'. This bit is cleared by writing a '0' to it.

Thermal: This bit indicates a thermal shutdown that was initiated by the hardware with a '1'. This bit is deglitched and latched, and can be cleared by writing a '0' to it.

NG_EN: Enable bit for the Noise Gate function. This function is enabled when this bit is high. This function can only be enabled when the Compression ratio is not 1:1.

AGC ATTACK CONTROL (Address: 2)

REGISTER ADDRESS	I^2C BIT	LABEL	DEFAULT	DESCRIPTION			
02 (02_H) – AGC Control	7:6	Unused	00				
	5:0	ATK_time	000101 (6.4 ms/6 dB)	AGC Attack time (gain ramp down)			
					Per Step	Per 6 dB	90% Range
				000001	0.1067 ms	1.28 ms	5.76 ms
				000010	0.2134 ms	2.56 ms	11.52 ms
				000011	0.3201 ms	3.84 ms	17.19 ms
				000100	0.4268 ms	5.12 ms	23.04 ms
				(time increases by 0.1067 ms with every step)			
				111111	6.722 ms	80.66 ms	362.99 ms

ATK_time These bits set the attack time for the AGC function. The attack time is the minimum time between gain decreases.

AGC RELEASE CONTROL (Address: 3)

REGISTER ADDRESS	I²C BIT	LABEL	DEFAULT	DESCRIPTION			
03 (03H) – AGC Release Control	7:6	Unused	00				
	5:0	REL_time	001011 (1.81 sec/6 dB)	AGC Release time (gain ramp down)			
					Per Step	Per 6 dB	90% Range
				000001	0.0137 s	0.1644 s	0.7398 s
				000010	0.0274 s	0.3288 s	1.4796 s
				000011	0.0411 s	0.4932 s	2.2194 s
				000100	0.0548 s	0.6576 s	2.9592 s
				(time increases by 0.0137 s with every step)			
				111111	0.8631 s	10.36 s	46.6 s

REL_time These bits set the release time for the AGC function. The release time is the minimum time between gain increases.

Table 5. AGC HOLD TIME CONTROL (Address: 4)

REGISTER ADDRESS	I²C BIT	LABEL	DEFAULT	DESCRIPTION		
04 (04H) – AGC Hold Time Control	7:6	Unused	00			
	5:0	Hold_time	000000 (Disabled)	AGC Hold time		
						Per Step
					000000	Hold Time Disable
					000001	0.0137 s
					000010	0.0274 s
					000011	0.0411 s
					000100	0.0548 s
					(time increases by 0.0137 s with every step)	
					111111	0.8631 s

Hold_time These bits set the hold time for the AGC function. The hold time is the minimum time between a gain decrease (attack) and a gain increase (release). The hold time can be deactivated.

AGC FIXED GAIN CONTROL (Address: 5)

REGISTER ADDRESS	I^2C BIT	LABEL	DEFAULT	DESCRIPTION		
05 (05_H) – AGC Fixed Gain Control	7:6	Unused	00			
	5:0	Fixed Gain	00110 (6dB)	Sets the fixed gain of the amplifier: two's compliment		
						Gain
					100100	–28 dB
					100101	–27 dB
					100110	–26 dB
				(gain increases by 1 dB with every step)		
					111101	–3 dB
					111110	–2 dB
					111111	–1 dB
					000000	0 dB
					000001	1 dB
					000010	2 dB
					000011	3 dB
				(gain increases by 1dB with every step)		
					011100	28 dB
					011101	29 dB
					011110	30 dB

Fixed Gain These bits are used to select the fixed gain of the amplifier. If the Compression is enabled, fixed gain is adjustable from –28dB to 30dB. If the Compression is disabled, fixed gain is adjustable from 0dB to 30dB.

AGC CONTROL (Address: 6)

REGISTER ADDRESS	I^2C BIT	LABEL	DEFAULT	DESCRIPTION			
06 (06_H) – AGC Control	7	Output Limiter Disable	0 (enable)	Disables the output limiter function. Can only be disabled when the AGC compression ratio is 1:1 (off)			
	6:5	NoiseGate Threshold	01 (4mV$_{rms}$)	Select the threshold of the noise gate			
							Threshold
						00	1 mV$_{rms}$
						01	4 mV$_{rms}$
						10	10 mV$_{rms}$
						11	20 mV$_{rms}$
	4:0	Output Limiter Level	11010 (6.5dBV)	Selects the output limiter level			
					Output Power (Wrms)	Peak Output Voltage (Vp)	dBV
				00000	0.03	0.67	–6.5
				00001	0.03	0.71	–6
				00010	0.04	0.75	–5.5
				(Limiter level increases by 0.5dB with every step)			
				11101	0.79	3.55	8
				11110	0.88	3.76	8.5
				11111	0.99	3.99	9

Output Limiter Disable This bit disables the output limiter function when set to 1. Can only be disabled when the AGC compression ratio is 1:1

NoiseGate Threshold These bits set the threshold level of the noise gate. NoiseGate Threshold is only functional when the compression ratio is not 1:1

Output Limiter Level These bits select the output limiter level. Output Power numbers are for 8Ω load.

AGC CONTROL (Address: 7)

REGISTER ADDRESS	I^2C BIT	LABEL	DEFAULT	DESCRIPTION		
07 (07_H) – AGC Control	7:4	Max Gain	1100 (30 dB)	Selects the maximum gain the AGC can achieve		
						Gain
					0000	18 dB
					0001	19 dB
					0010	20 dB
				(gain increases by 1 dB with every step)		
					1100	30 dB
	3:2	Unused	00			
	1:0	Compression Ratio	10 (4:1)	Selects the compression ratio of the AGC		
						Ratio
					00	1:1 (off)
					01	2:1
					10	4:1
					11	8:1

Compression Ratio These bits select the compression ratio. Output Limiter is enabled by default when the compression ratio is not 1:1.

Max Gain These bits select the maximum gain of the amplifier. In order to maximize the use of the AGC, set the Max Gain to 30dB

DECOUPLING CAPACITOR �$_S$)

The TPA2016D2 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) 1-μF ceramic capacitor (typically) placed as close as possible to the device PVDD (L, R) lead works best. Placing this decoupling capacitor close to the TPA2016D2 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7 μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

INPUT CAPACITORS �$_I$)

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_C, determined in Equation 5.

$$f_C = \frac{1}{(2\pi \times R_I \times C_I)} \quad (5)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset. Equation 6 is used to solve for the input coupling capacitance. If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

$$C_I = \frac{1}{(2\pi \times R_I \times f_C)} \quad (6)$$

BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use non solder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 42 and Table 6 shows the appropriate diameters for a WCSP layout. The TPA2016D2 evaluation module (EVM) layout is shown in the next section as a layout example.

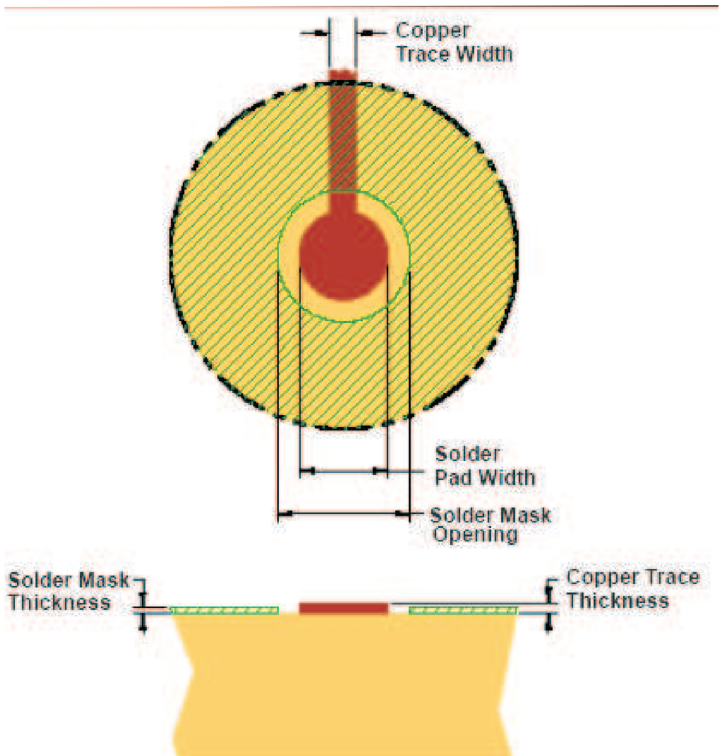


Figure 42. Land Pattern Dimensions

Table 6. Land Pattern Dimensions(1) (2) (3) (4)

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK(5) OPENING	COPPER THICKNESS	STENCIL(6) (7) OPENING	STENCIL THICKNESS
Non solder mask defined (NSMD)	275 µm (+0.0, –25 µm)	375 µm (+0.0, –25 µm)	1 oz max (32 µm)	275 µm × 275 µm Sq. (rounded corners)	125 µm thick

(1) Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern
(6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
(7) Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

COMPONENT LOCATION

Place all the external components very close to the TPA2016D2. Placing the decoupling capacitor, C_S, close to the TPA2016D2 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

TRACE WIDTH

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces. For high current pins (PVDD (L, R), PGND, and audio output pins) of the TPA2016D2, use 100-µm trace widths at the solder balls and at least 500-µm PCB traces to ensure proper performance and output power for the device. For the remaining signals of the TPA2016D2, use 75-µm to 100-µm trace widths at the solder balls. The audio input pins (INR± and INL±) must run side-by-side to maximize common-mode noise cancellation

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the packages are shown in the dissipation rating table. Converting this to θ_{JA} for the WCSP package:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.01} = 100°C/W \tag{7}$$

Given θ_{JA} of 100°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.4 W (0.2 W per channel) for 1.5 W per channel, 8-Ω load, 5-V supply, from Figure 16, the maximum ambient temperature can be calculated with the following equation.

$$T_A Max = T_J Max - \theta_{JA} P_{DMAX} = 150 - 100\ (0.4) = 110°C \tag{8}$$

Equation 8 shows that the calculated maximum ambient temperature is 110°C at maximum power dissipation with a 5-V supply and 8-Ω a load. The TPA2016D2 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 8-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

OPERATION WITH DACS AND CODECS

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance. See the functional block diagram.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker. Figure 43 shows typical ferrite bead and LC output filters.

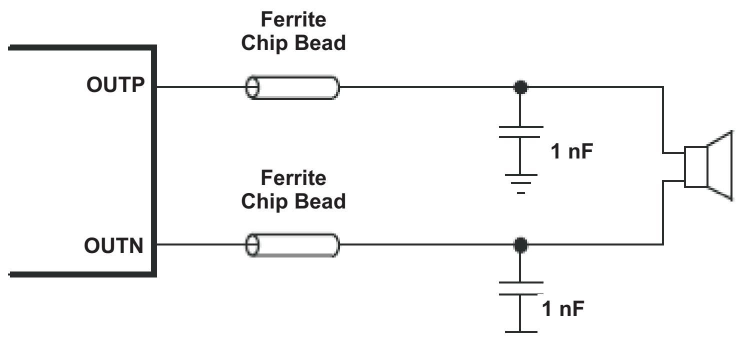


Figure 43. Typical Ferrite Bead Filter (Chip bead example: TDK: MPZ1608S221A)

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA2016D2RTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 2016D2	Samples
TPA2016D2RTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 2016D2	Samples
TPA2016D2YZHR	ACTIVE	DSBGA	YZH	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CCJ	Samples
TPA2016D2YZHT	ACTIVE	DSBGA	YZH	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CCJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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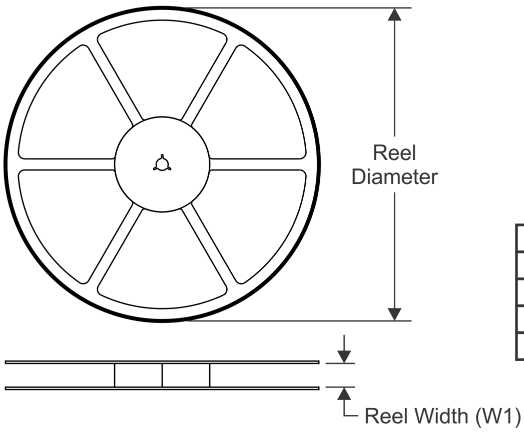
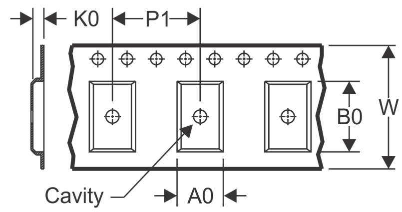
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

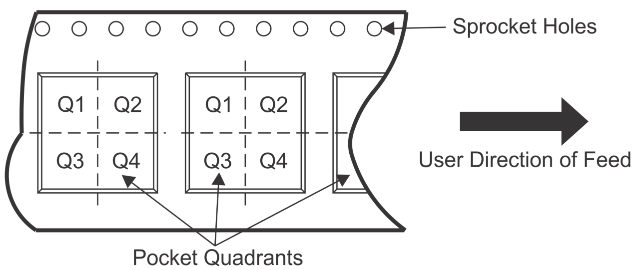
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

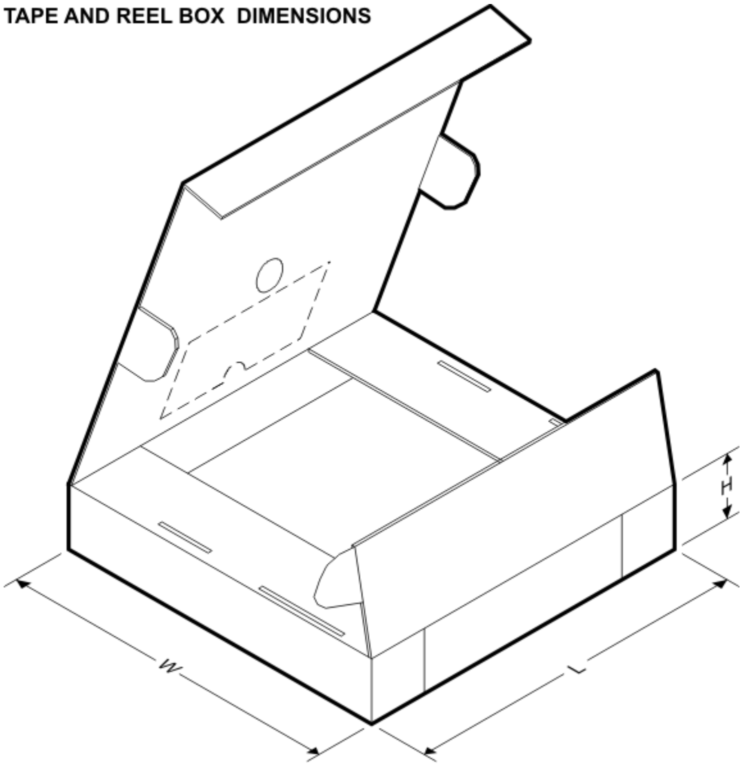
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

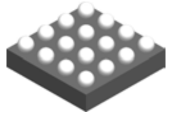
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2016D2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPA2016D2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2016D2RTJT	QFN	RTJ	20	250	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
TPA2016D2RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2016D2YZHR	DSBGA	YZH	16	3000	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
TPA2016D2YZHT	DSBGA	YZH	16	250	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

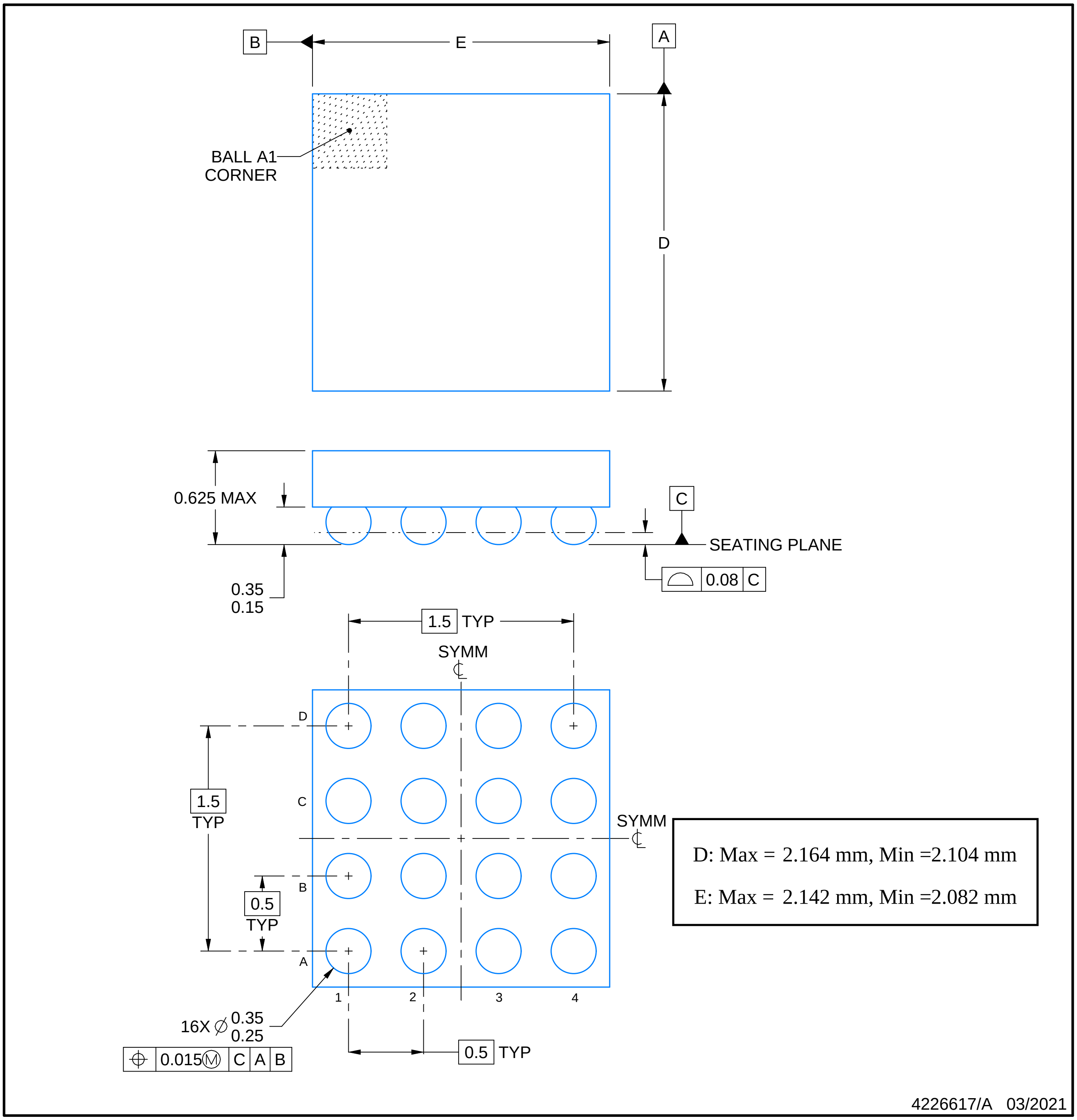


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2016D2RTJR	QFN	RTJ	20	3000	370.0	355.0	55.0
TPA2016D2RTJR	QFN	RTJ	20	3000	853.0	449.0	35.0
TPA2016D2RTJT	QFN	RTJ	20	250	195.0	200.0	45.0
TPA2016D2RTJT	QFN	RTJ	20	250	210.0	185.0	35.0
TPA2016D2YZHR	DSBGA	YZH	16	3000	182.0	182.0	20.0
TPA2016D2YZHT	DSBGA	YZH	16	250	182.0	182.0	20.0

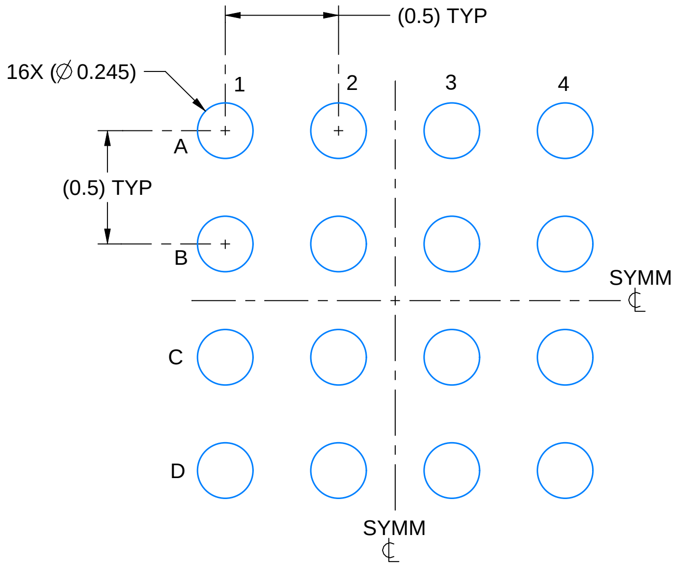


DIE SIZE BALL GRID ARRAY

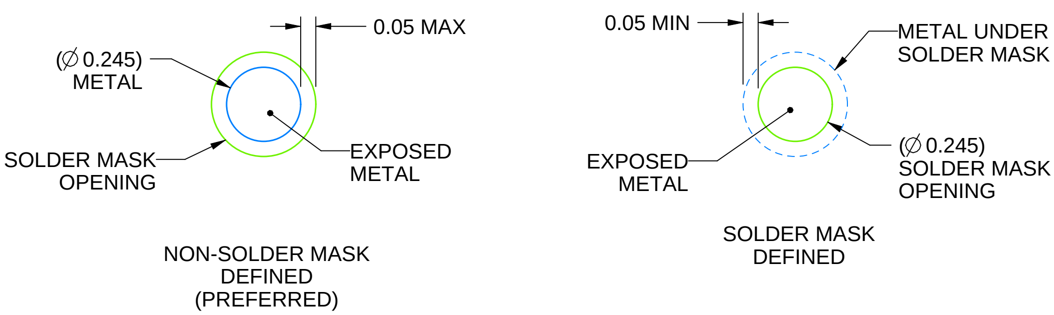


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

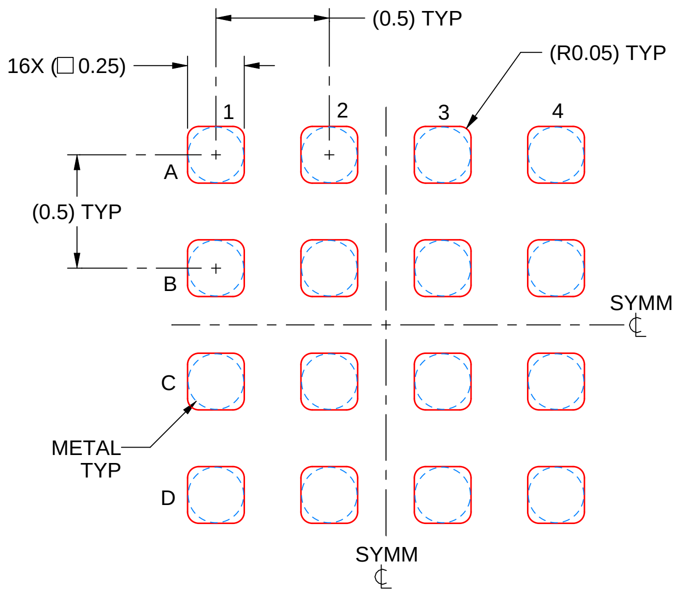


SOLDER MASK DETAILS
NOT TO SCALE

4226617/A 03/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



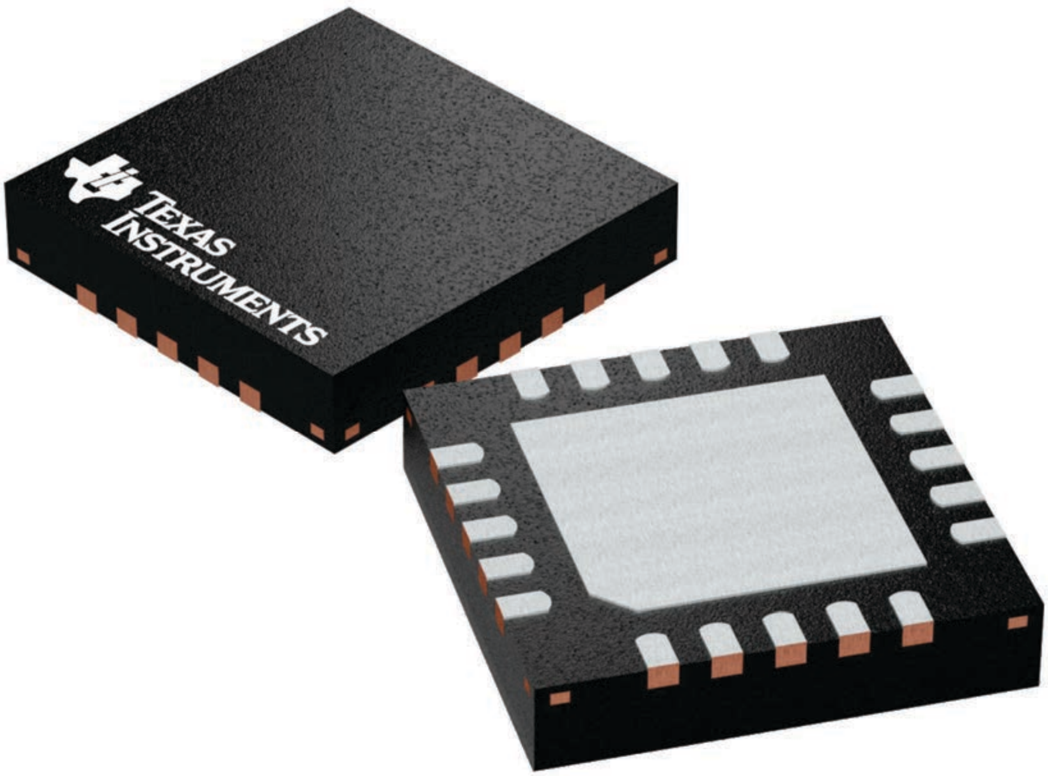
SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4226617/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016	
DESIGNER: H. DENG	DATE: 09/12/2016	
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016	
ENGINEER: T. TANG	DATE: 09/12/2016	
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016	
RELEASED: WDM	DATE: 10/24/2016	
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	

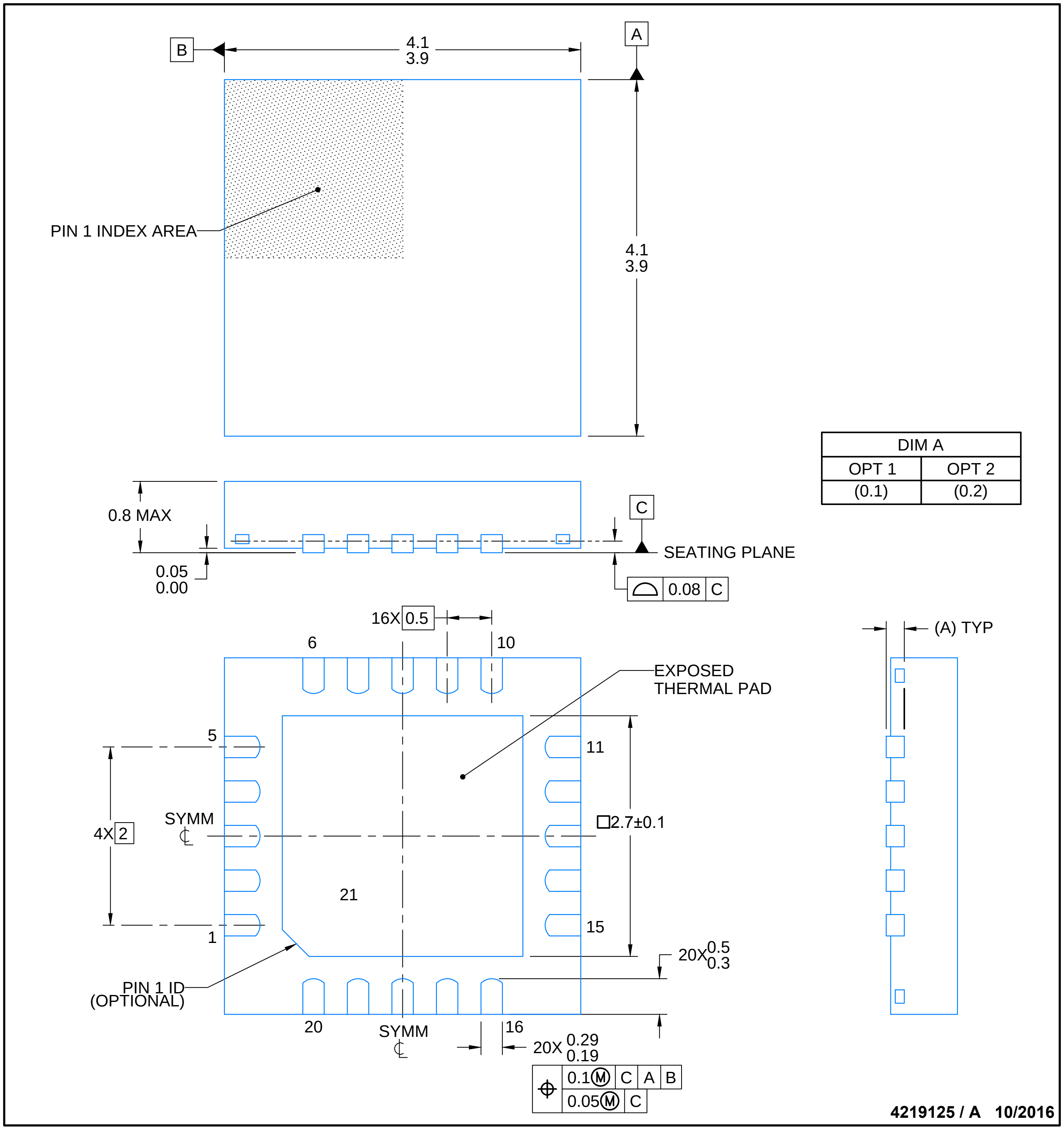
DIMENSIONS IN MILLIMETERS

TEXAS INSTRUMENTS
SEMICONDUCTOR OPERATIONS

CODE IDENTITY NUMBER 01295

ePOD, RTJ0020D / WQFN,
20 PIN, 0.5 MM PITCH

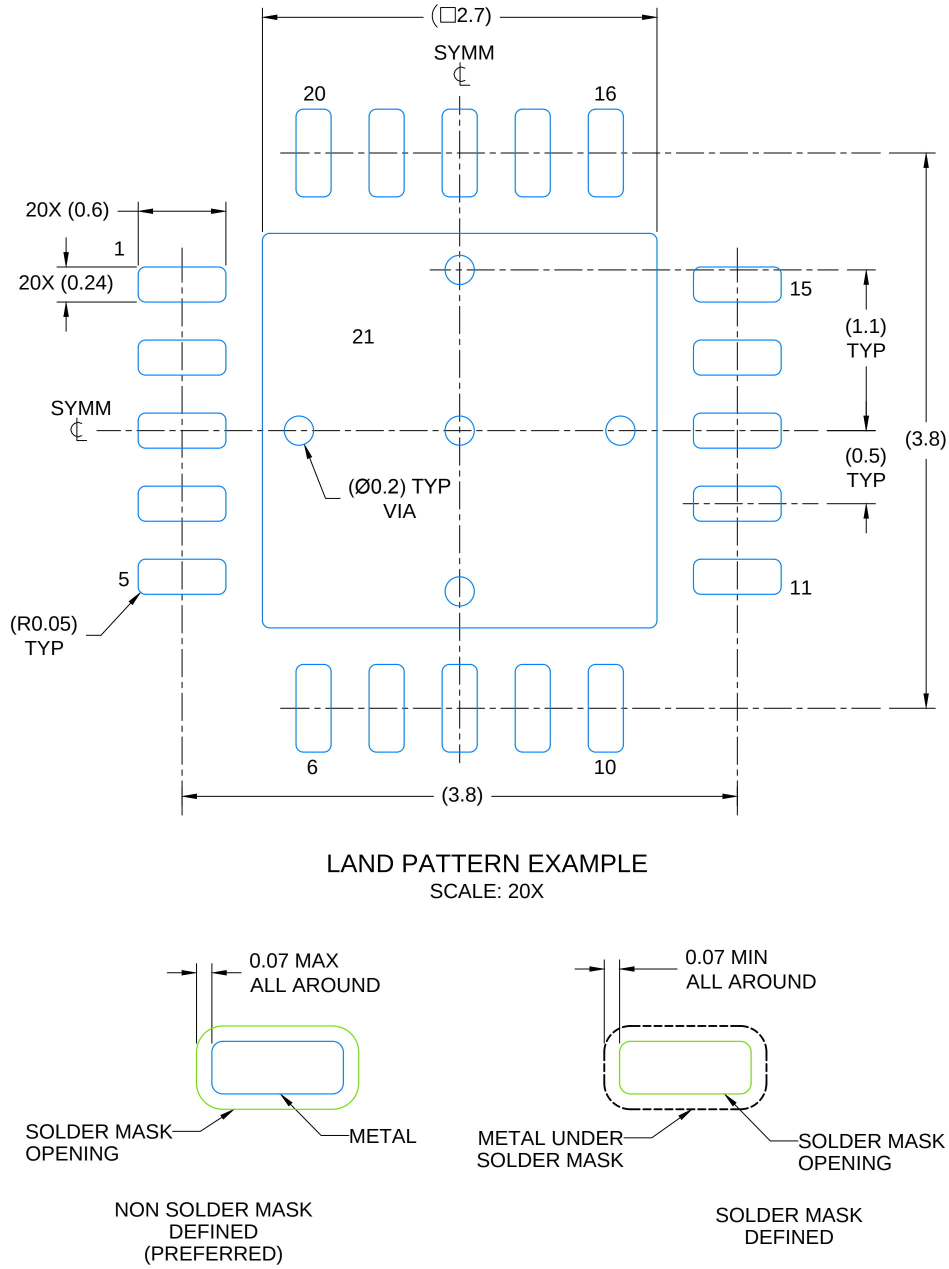
SCALE	SIZE		REV	PAGE
15X	A	4219125	A	1 OF 5



4219125 / A 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



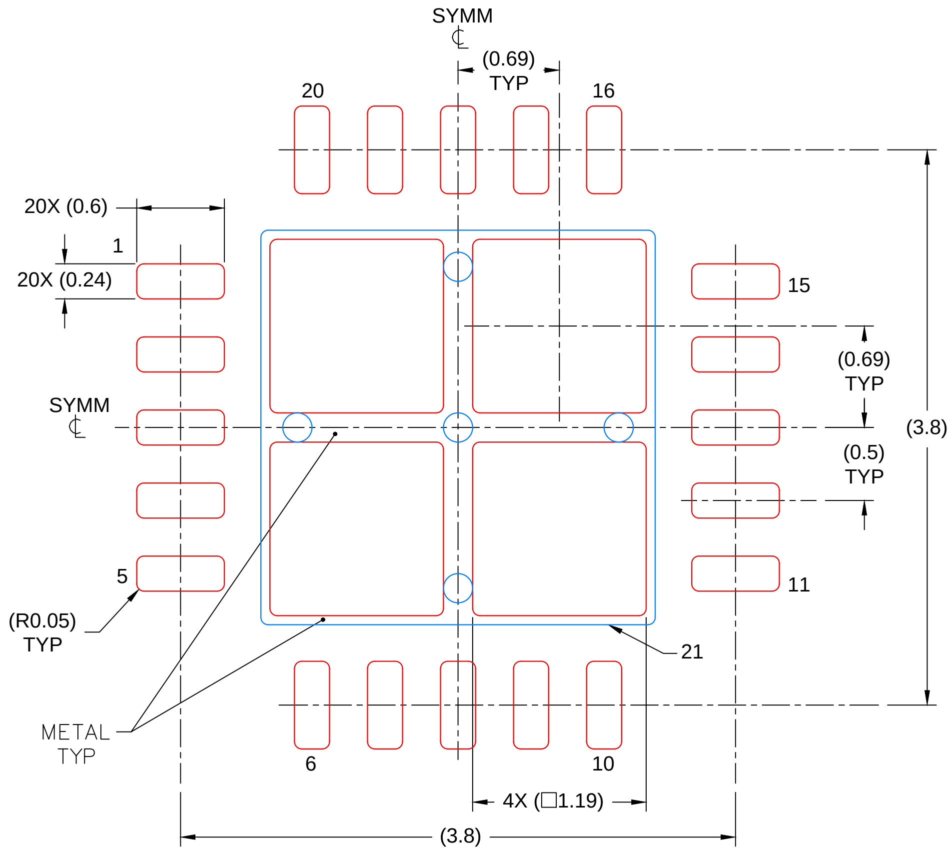
LAND PATTERN EXAMPLE
SCALE: 20X

SOLDER MASK DETAILS

4219125 / A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

重要声明和免责声明

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