LM2903-Q1 汽车类双路差动比较器

1 特性

- 符合汽车应用 标准
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 0 级：–40°C 至 150° 的环境运行温度范围 (LM2903E-Q1)
  - 器件温度 1 级：–40°C 至 125°C 的环境运行温度范围 (LM2903-Q1)
  - 器件 HBM ESD 分类等级 H1C
  - 器件 CDM ESD 分类等级 C4B
- ESD 保护超过 1000V（根据 MIL-STD-883 方法 3015）；超过 100V（使用机器放电模型，C = 200pF，R = 0Ω）
- 单电源或双电源
- 独立于电源电压的低漏极电源电流：每个比较器 0.4mA（典型值）
- 低输入偏置电流：25nA（典型值）
- 低输入失调电流：5nA（典型值）
- 低输入失调电压：2mV（典型值）
- 共模输入电压范围包括接地
- 差动输入电压范围等于最大额定电源电压 ±36V
- 低输出饱和电压
- 输出与 TTL、MOS 和 CMOS 兼容

2 应用

- 汽车
  - HEV/EV 和动力传动
  - 信息娱乐系统与仪表组
  - 车身控制模块
- 工业
- 电源监控
- 振荡器
- 峰值检测器
- 逻辑电压转换

3 说明

该器件包含两个独立的电压比较器，这些比较器可在宽电压范围内由单电源供电运行。如果两个电源之间的电压差在 2V 至 36V 的范围之内且 VCC 比输入共模电压至少高 +1.5V 以上，那么它们也可以由双电源供电运行。漏极电流不受电源电压的影响。可将输出连接到其它集电极开路输出，以实现有线 AND 关联。

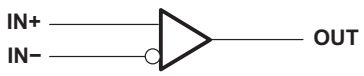
LM2903-Q1 符合 AEC-Q100 1 级温度范围（–40°C 至 +125°C）标准。LM2903E-Q1 符合 AEC-Q100 0 级温度范围（–40°C 至 +150°C）标准。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM2903-Q1	VSSOP (8)	3.00mm x 3.00mm
	SOIC (8)	4.90mm × 3.91mm
	TSSOP (8)	3.00mm × 4.40mm
LM2903E-Q1	TSSOP (8)	3.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



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4 修订历史记录

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- 已更改 previous Q1 graphs to match new format ... 6
- 已添加 LM2903E-Q1 specific graphs ... 6

Changes from Revision E (June 2014) to Revision F — **Page**

- Added Pin Functions table. ... 3
- Changed Thermal Information Table ... 4

Changes from Revision D (April 2008) to Revision E — **Page**

- 在 特性中添加了 AEC-Q100 信息。 ... 1
- 已添加 应用中添加了 AEC-Q100 信息。 ... 1
- 已添加 器件信息表。 ... 1
- Added Handling Ratings table. ... 4
- Added T_J and ESD ratings to Abs Max table. ... 4
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- Added Thermal Information table. ... 4
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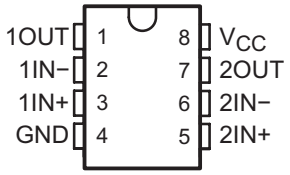
5 Pin Configuration and Functions

D, DGK OR PW PACKAGE
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1OUT	1	Output	Comparator 1's output pin
1IN-	2	Input	Comparator 1's negative input pin
1IN+	3	Input	Comparator 1's positive input pin
GND	4	Input	Ground
2IN+	5	Input	Comparator 2's positive input pin
2IN-	6	Input	Comparator 2's negative input pin
2OUT	7	Output	Comparator 2's output pin
V_{CC}	8	Input	Supply Pin

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		36	V
V_{CC}	Supply voltage, LM2903E-Q1 Only(2)		32	V
V_{ID}	Differential input voltage(3)	–36	36	V
V_I	Input voltage range (either input)	−0.3	36	V
V_O	Output voltage		36	V
I_O	Output current		20	mA
	Duration of output short-circuit to ground		Unlimited	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Differential voltages are at IN+ with respect to IN−.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range		LM2903-Q1 Only	–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		0	1000	V
		Charged device model (CDM), per AEC Q100-011	All pins	0	750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions, LM2903-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC} (non-V devices)		2		30	V
V_{CC} (V devices)		2		32	V
T_J	Junction Temperature	-40		125	°C

6.4 Recommended Operating Conditions, LM2903E-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}		2		30	V
T_J	Junction Temperature	-40		150	°C

6.5 Thermal Information

THERMAL METRIC (1)		LM2903E-Q1 PW 8 PINS	LM2903-Q1 DGK 8 PINS	LM2903-Q1 PW 8 PINS	LM2903-Q1 D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	178.9	199.4	186.6	126.0	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	70.7	120.8	79.6	74.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	108.9	90.2	116.5	66.4	
ψ_{JT}	Junction-to-top characterization parameter	11.9	21.5	17.7	25.4	
ψ_{JB}	Junction-to-board characterization parameter	107.3	119.1	114.9	65.9	

(1) 有关传统和新热指标的更多信息，请参见应用报告《*半导体和 IC 封装热指标*》（文献编号：SPRA953）。

6.6 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, $V_{IC} = V_{IC(min)}$, V_{CC} = 5 V to MAX (2)	Non-A devices	25°C		2	7	mV
				Full range			15	
			A-suffix devices	25°C		1	2	
				Full range			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−250	nA
				Full range			−500	
V_{ICR}	Common-mode input voltage range (3)			25°C	0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		25°C	25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V	V_{ID} = 1 V	25°C		0.1	50	nA
		$V_{OH} = V_{CC}$ MAX (2)		Full range			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V	25°C		150	400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = −1 V	25°C	6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5 V	25°C		0.8	1	mA
			V_{CC} = MAX (2)	Full range			2.5	

(1) Full range (MIN or MAX) for LM2903-Q1 is −40°C to 125°C and −40°C to 150°C for the LM2903E-Q1 . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) V_{CC} MAX = 30 V for non-V devices and 32 V for V-suffix devices.
(3) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is VCC+ − 1.5 V for the inverting input (−), and the non-inverting input (+) can exceed the VCC level; the comparator provides a proper output state. Either or both inputs can go to 30 V (32V for V-suffix devices) without damage.

6.7 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive	1.3	µs
	C_L = 15 pF (1) (2)	TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.8 Typical Characteristics

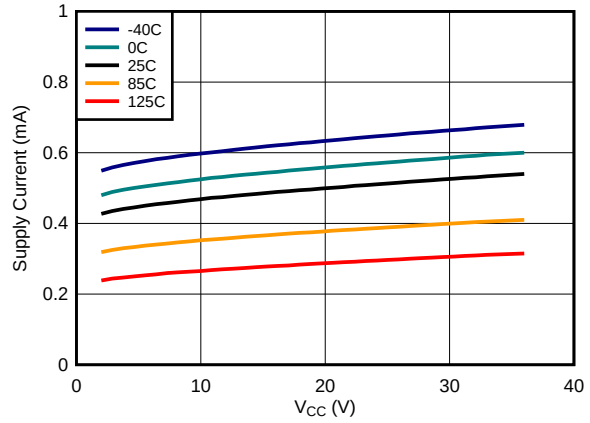


图 1. Supply Current vs. Supply Voltage

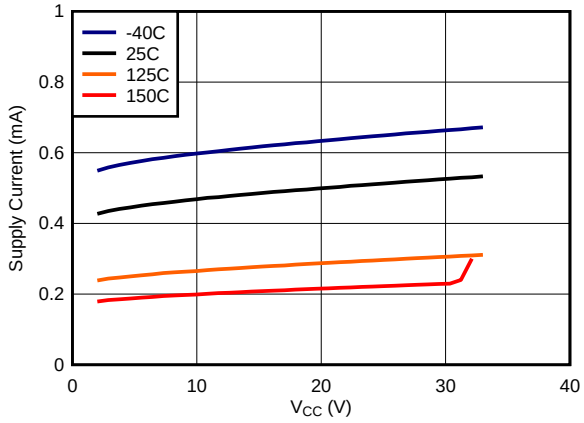


图 2. Supply Current vs. Supply Voltage
LM2903E-Q1 Only

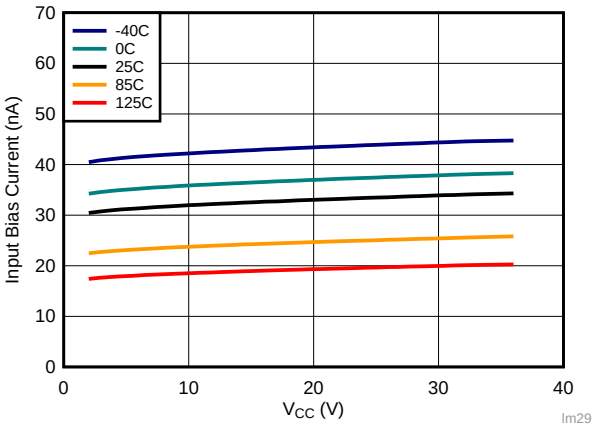


图 3. Input Bias Current vs. Supply Voltage

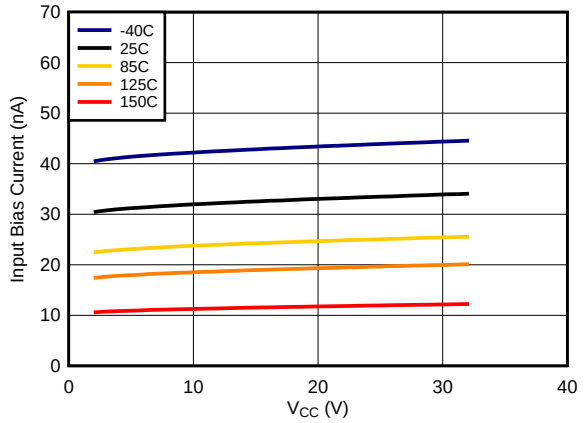


图 4. Input Bias Current vs. Supply Voltage
LM2903E-Q1 Only

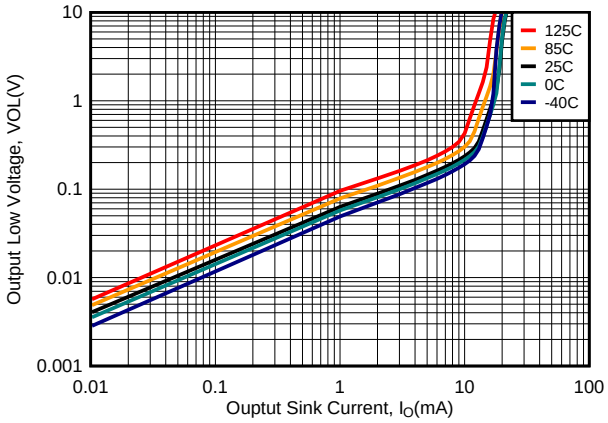


图 5. Output Low Voltage vs. Output Current

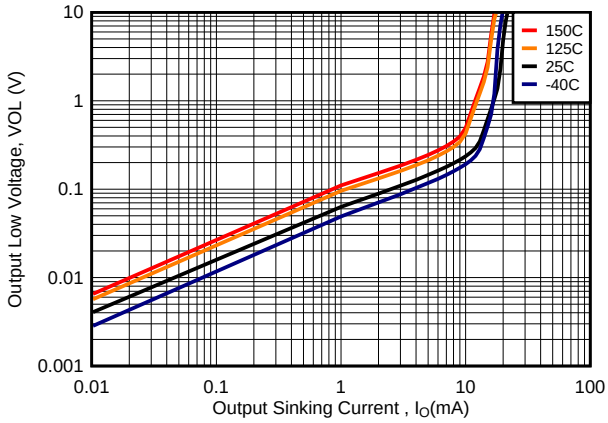


图 6. Output Low Voltage vs. Output Current
LM2903E-Q1 Only

7 Detailed Description

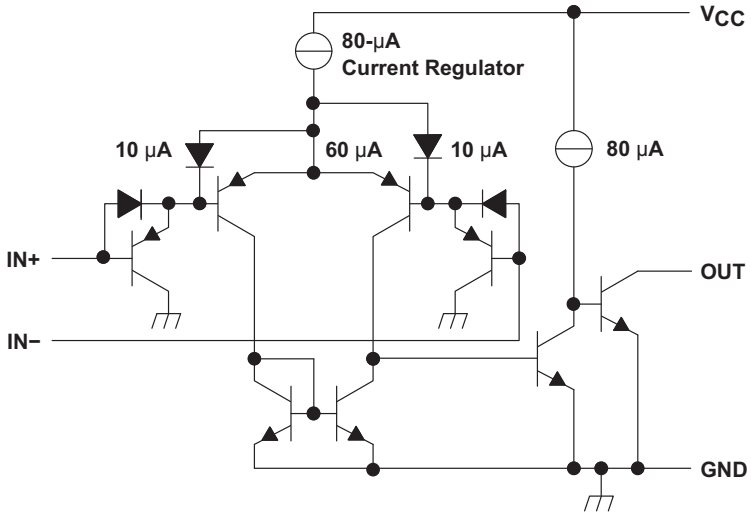
7.1 Overview

The LM2903-Q1 family is a dual comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's very wide supply voltages range (2 V to 36 V), low Iq and fast response.

This device is AEC-Q100 qualified and can operate over a wide temperature range of –40°C to 125°C (LM2903-Q1) or –40°C to 150°C (LM2903E-Q1).

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	2
Transistors	30

图 7. Schematic (Each Comparator)

7.3 Feature Description

LM2903-Q1 family consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing LM2903-Q1 to accurately function from ground to V_{CC}–1.5V differential input. This is enables much head room for modern day supplies of 3.3 V and 5.0 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the positive input voltage is higher than the negative input voltage and the offset voltage. The VOL is resistive and will scale with the output current. Please see 图 3 in the *Typical Characteristics* section for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The LM2903-Q1 family operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

8 Application and Implementation

8.1 Application Information

LM2903-Q1 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM2903Q1 optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

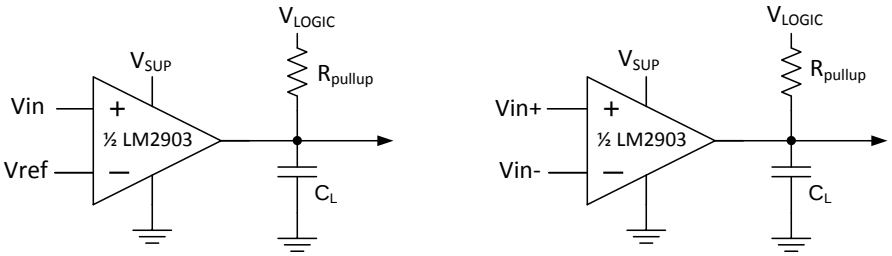


图 8. Single-ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the input parameters.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-1.5 V
Supply Voltage	2 V to 36 V
Logic Supply Voltage	2 V to 36 V
Output Current (R_{PULLUP})	1 µA to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using LM2903-Q1 family in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC}– 2.0 V. This limits the input voltage range to as high as V_{CC}– 2.0 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting

2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 图 9 and 图 10 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use 图 5 to determine V_{OL} based on the output current.

The output current can also effect the transient response. More will be explained in the next section.

8.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (τ_p) is approximately $\tau_P \sim R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N \sim R_{CE} \times C_L$
  - R_{CE} can be determine by taking the slope of 图 5 in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

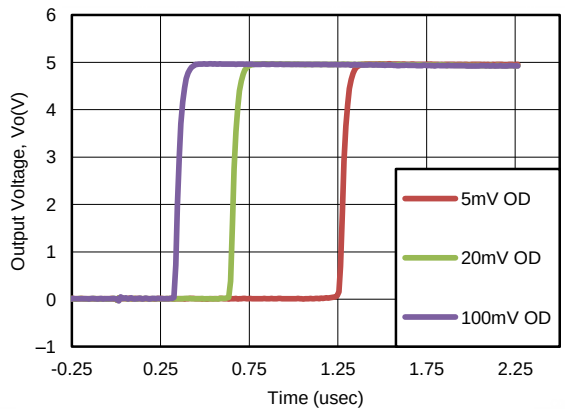


图 9. Response Time for Various Overdrives (Positive Transition)

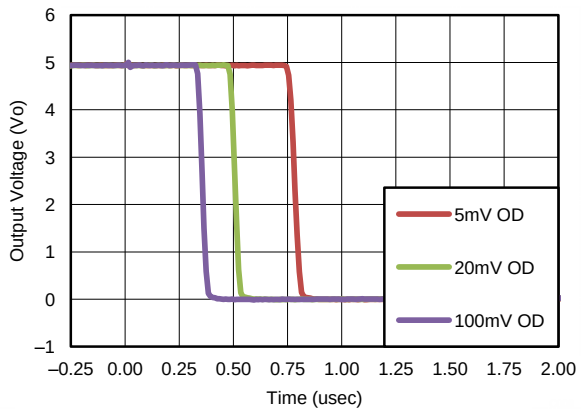


图 10. Response Time for Various Overdrives (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

10.2 Layout Example

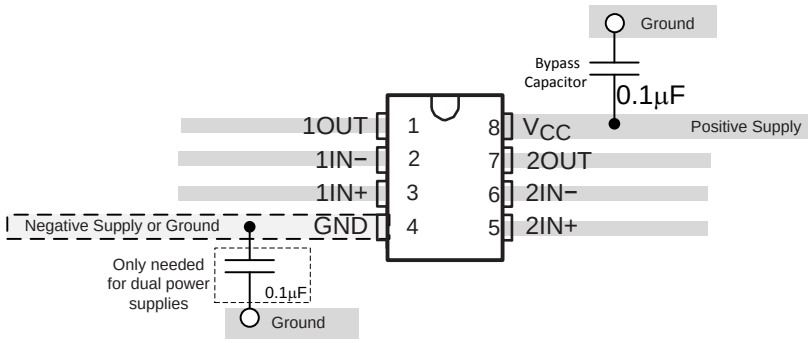


图 11. LM2903Q1 Layout Example

11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
LM2903-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM2903E-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
LM2903-Q1 符合 AEC-Q100 1 级温度范围（–40°C 至 +125°C）标准。LM2903E-Q1 符合 AEC-Q100 0 级温度范围（–40°C 至 +150°C）标准。 is a trademark of others.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903AVQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903AVQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903AVQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903AVQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903EPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	2903Q0	Samples
LM2903QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	KACQ	Samples
LM2903QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903VQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1	Samples
LM2903VQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1	Samples
LM2903VQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ	Samples
LM2903VQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

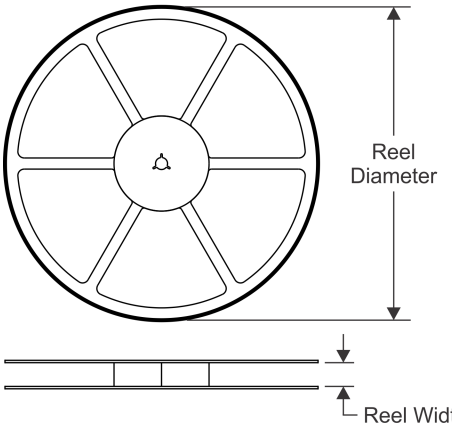
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

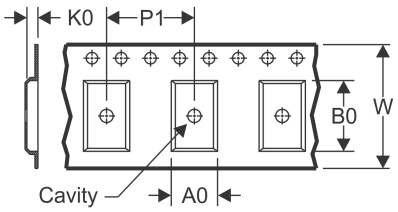
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

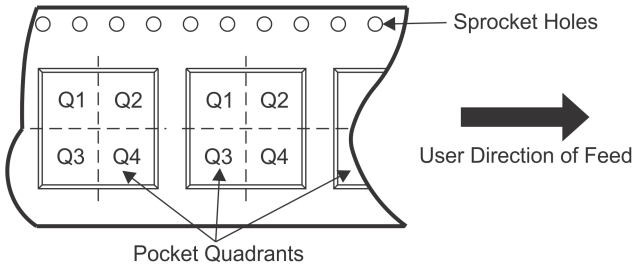


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

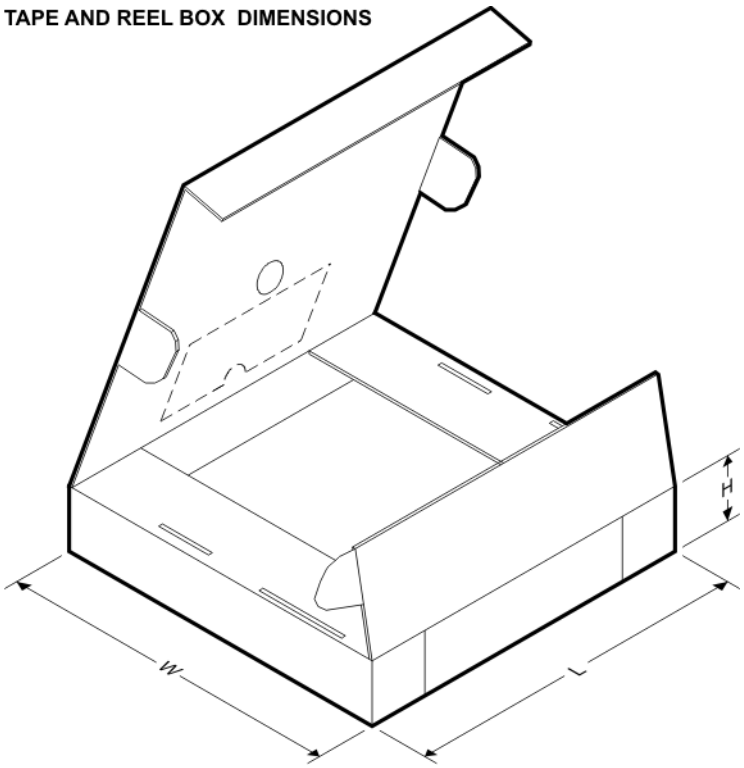
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

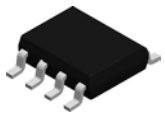
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903AVQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903EPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903AVQDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903AVQPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2903EPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2903QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903QPWRG4Q1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2903QPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903VQPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0

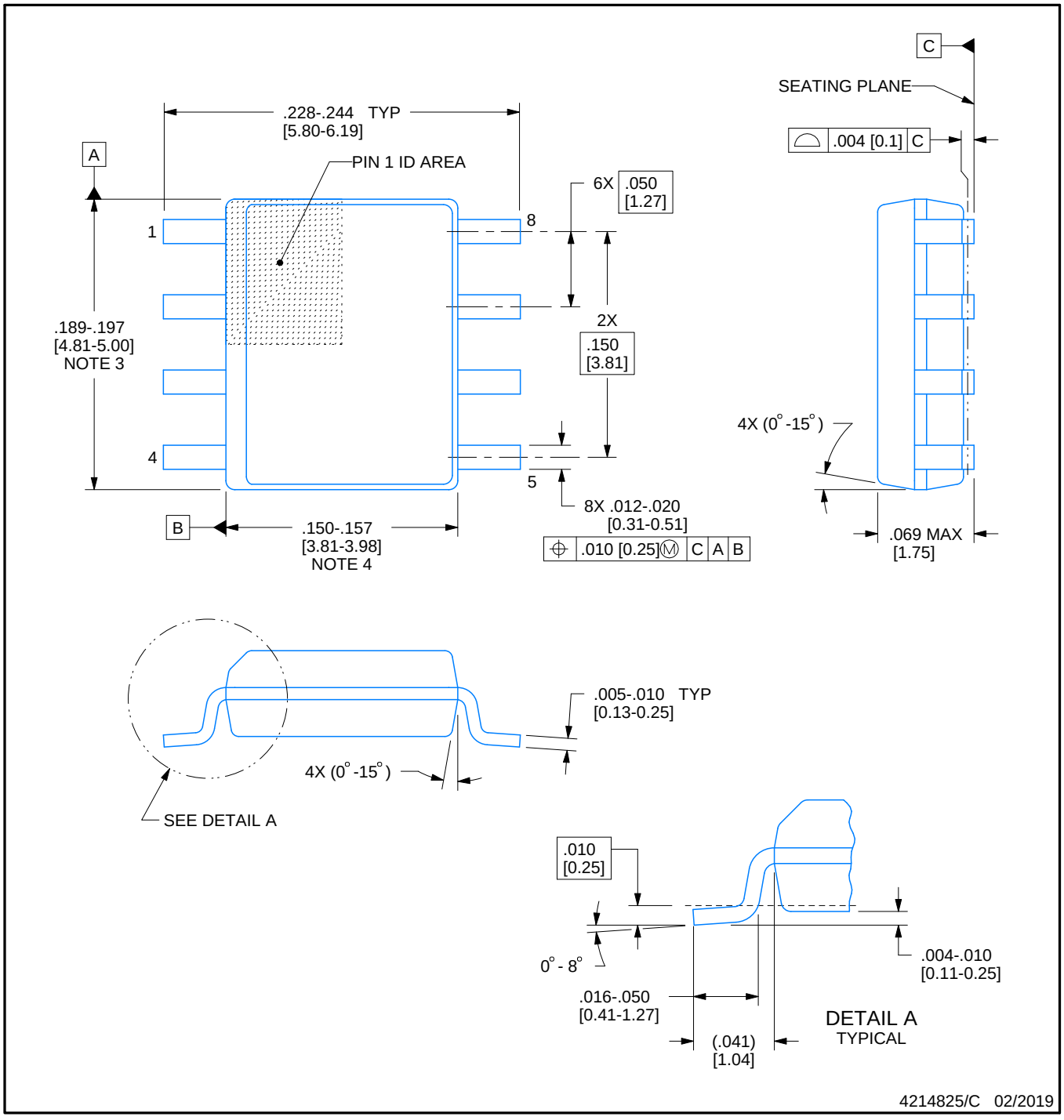


PACKAGE OUTLINE

D0008A

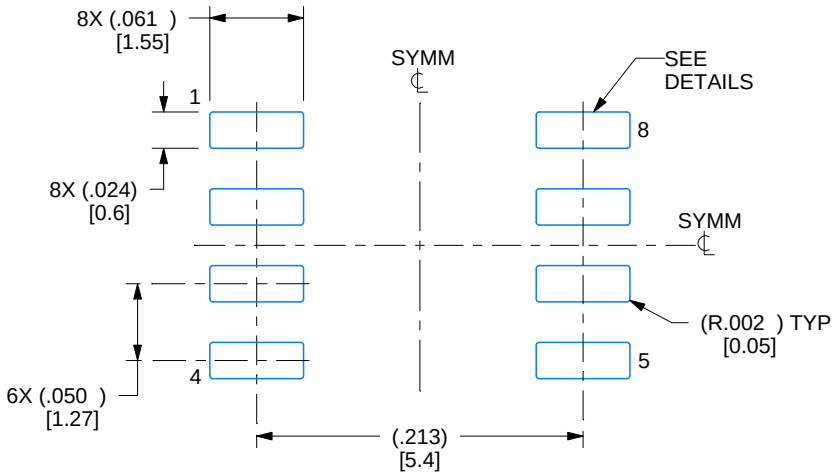
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

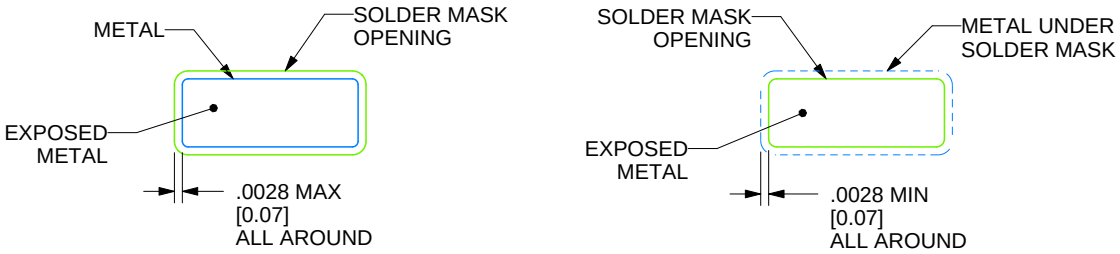


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

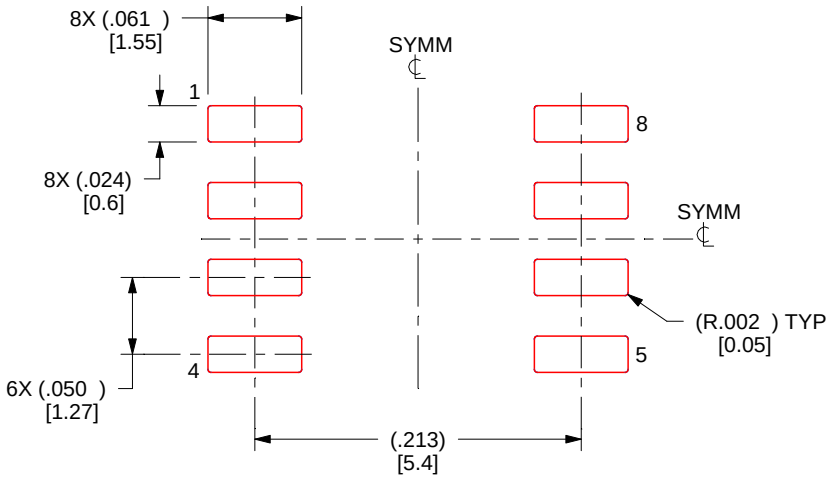
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



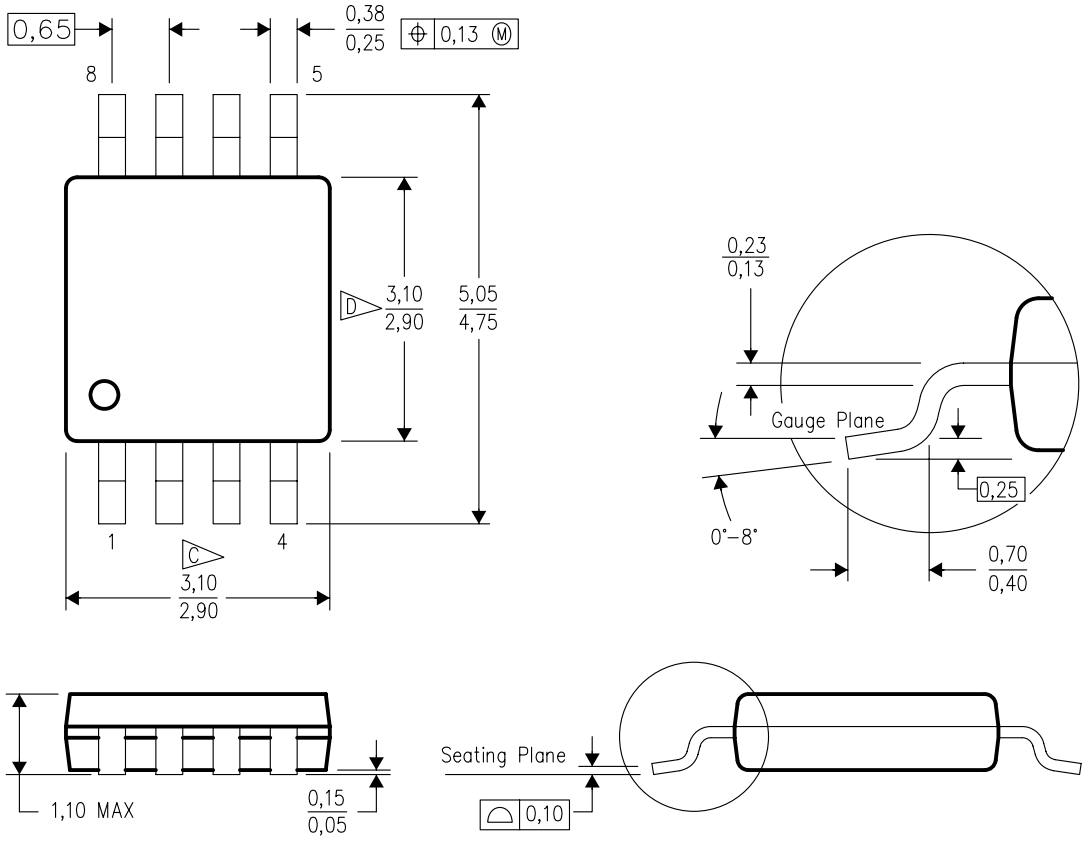
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

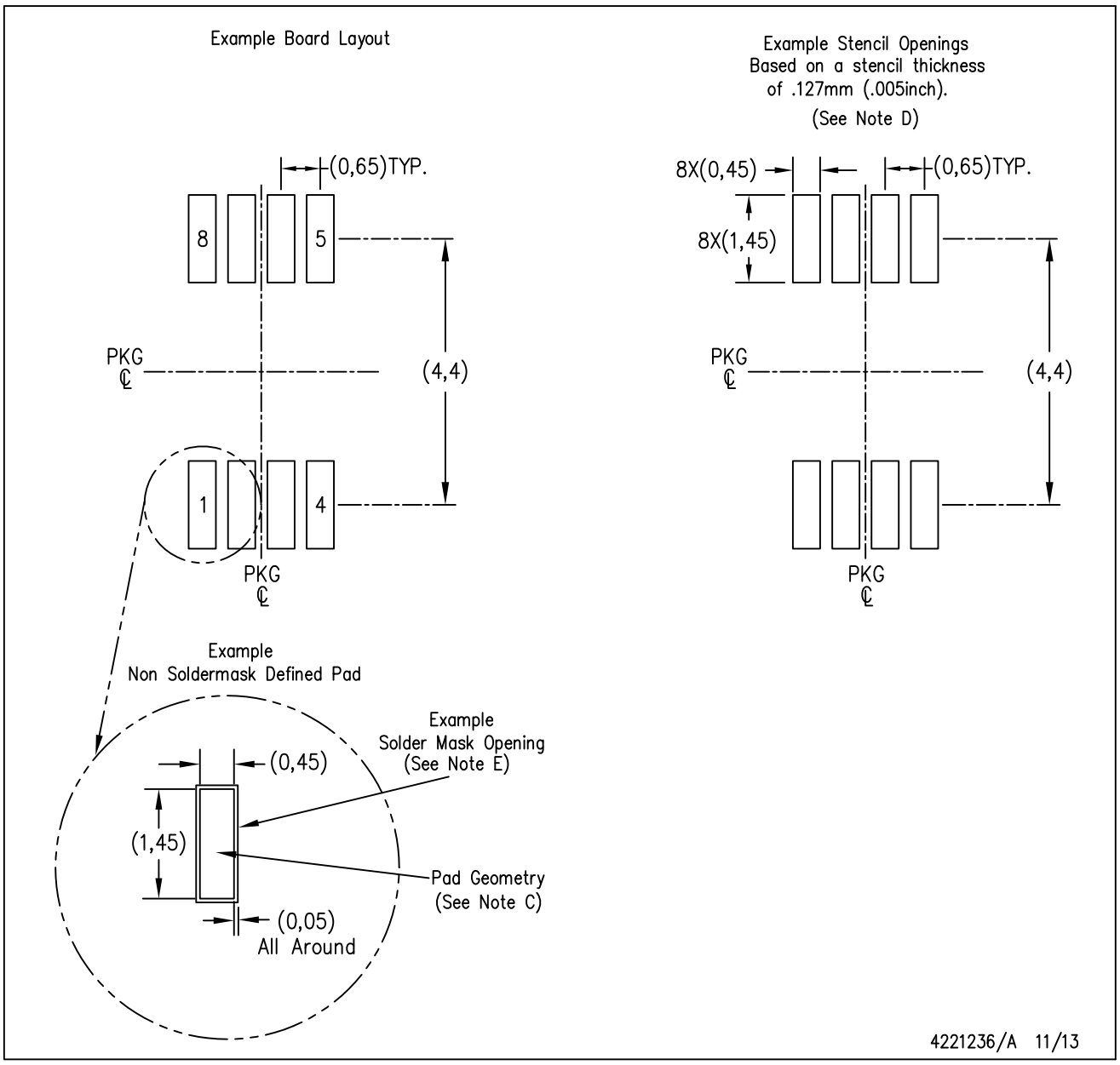
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



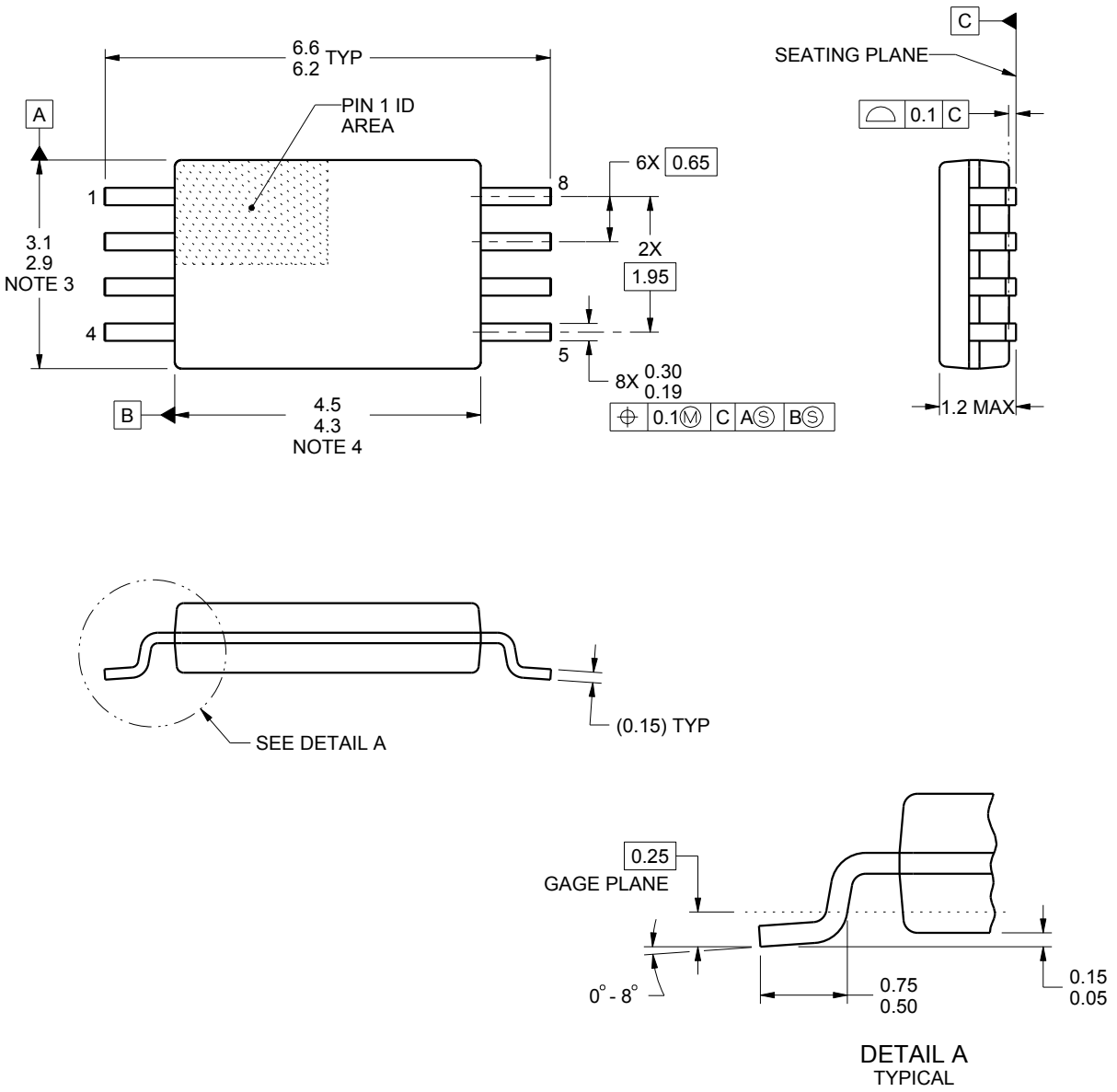
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

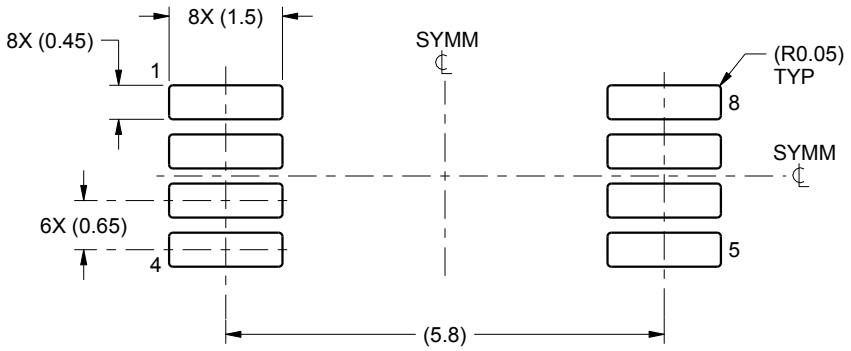
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

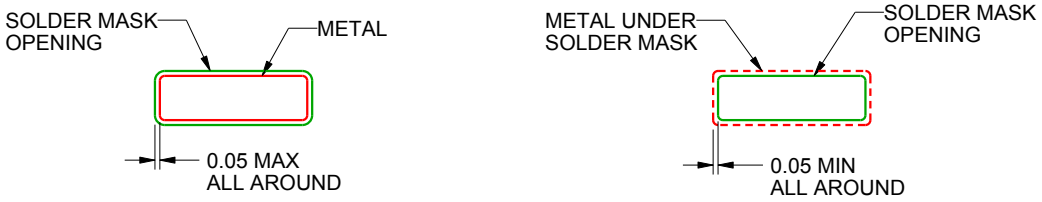


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

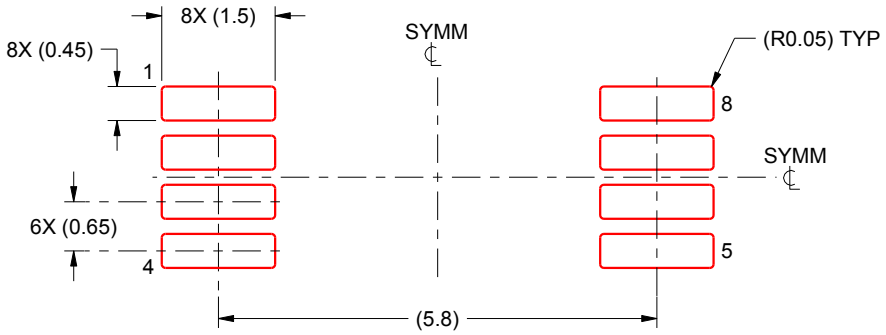


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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