

具有开漏和推挽输出的 LMV7235 和 LMV7239 75ns、超低功耗、低压、轨至轨输入比较器

1 特性

- $V_S = 5V$, $T_A = 25^\circ C$ (典型值, 除非另有说明)
- 传播延迟: 75ns
- 低电源电流: 65 μA
- 轨至轨输入
- 开漏和推挽输出
- 非常适合 2.7V 和 5V 单电源应用
- 采用节省空间的封装:
 - 5 引脚 SOT-23
 - 5 引脚 SC70

2 应用

- 便携式和电池供电类系统
- 机顶盒
- 高速差分线路接收器
- 窗口比较器
- 过零检测器
- 高速采样电路

3 说明

LMV7235 和 LMV7239 是 75ns 超低功耗低压比较器。这些器件可在 2.7V 至 5.5V 的完整电源电压范围内正常运行。这些器件可实现 75ns 的传播延迟, 而在 5V 电压下仅消耗 65 μA 的电源电流。

LMV7235 和 LMV7239 具有更大的轨至轨共模电压范围。输入共模电压范围可基于地电压向下扩展 200mV 并基于电源电压向上扩展 200mV, 从而允许接地感应和电源感应。

LMV7235 具有开漏输出。通过连接一个外部电阻器, 该比较器的输出可以用作电平转换器。

LMV7239 具有推挽式输出级。凭借此特性, 器件无需外部上拉电阻器即可运行。

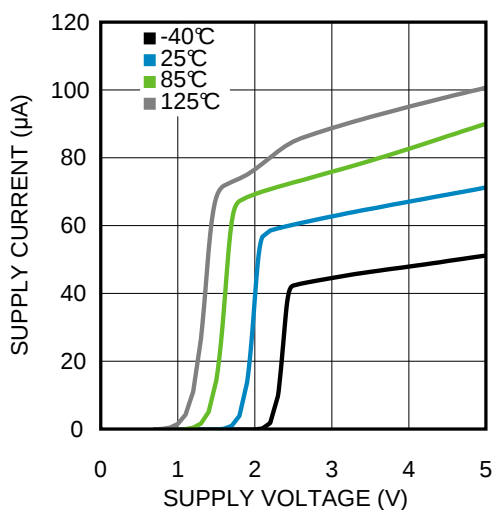
LMV7235 和 LMV7239 采用 5 引脚 SC70 和 5 引脚 SOT-23 封装, 因此非常适合需要小尺寸和低功耗特性的系统。

器件信息⁽¹⁾

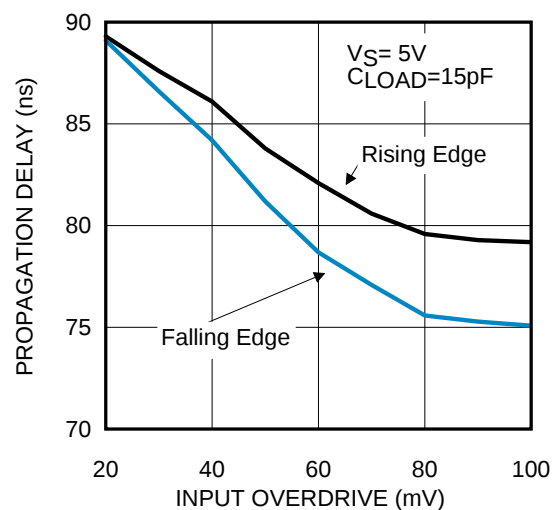
器件型号	封装	封装尺寸 (标称值)
LMV7235、LMV7239	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

电源电流与电源电压间的关系



传播延迟与过驱动



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4 修订历史记录

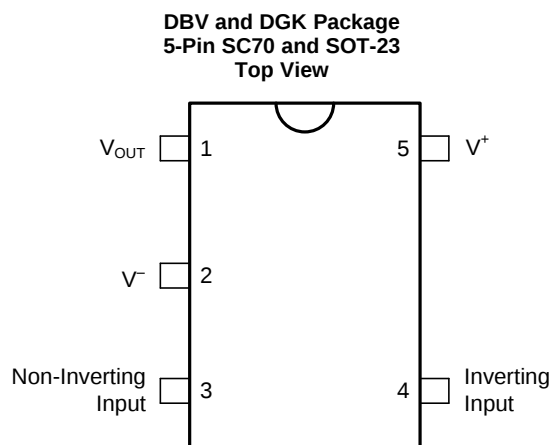
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision N (April 2015) to Revision O	Page
• 将 LMV7239-Q1 汽车器件移到单独的数据表 (SNOSD85) 中	1
• Added minimum values for the input offset voltage in the <i>Electrical Characteristics, 2.7 V</i> table	5
• Changed the input offset voltage typical value at room temperature from 0.8 to ± 0.8 in the <i>Electrical Characteristics, 2.7 V</i> table	5
• Added minimum values for the input offset voltage in the <i>Electrical Characteristics, 5 V</i> table	6
• Changed the input offset voltage typical value at room temperature from 1 to ± 1 in the <i>Electrical Characteristics, 5 V</i> table	6

Changes from Revision M (February 2013) to Revision N	Page
• 添加、更新或重命名以下部分：器件信息表、引脚配置和功能、规格。详细 说明布局、器件和文档支持、机械、封装和订购信息	1

Changes from Revision L (February 2013) to Revision M	Page
• 将美国国家半导体数据表的版面布局更改为 TI 格式	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{OUT}	O	Output
2	V^-	P	Negative Supply
3	IN+	I	Noninverting Input
4	IN-	I	Inverting Input
5	V^+	P	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Differential Input Voltage		± Supply Voltage	V
Output Short Circuit Duration		See ⁽²⁾	
Supply Voltage ($V^+ - V^-$)		6	V
SOLDERING INFORMATION			
Infrared or Convection (20 sec)		235	°C
Wave Soldering (10 sec)		260 (lead temp)	°C
Voltage at Input/Output Pins		(V^+) +0.3, (V^-) -0.3	V
Current at Input Pin ⁽³⁾		±10	mA
Storage Temperature, T_{stg}	-65	150	°C
Junction Temperature, T_j		150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
- (3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
	Machine model (MM)	±100

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltages ($V^+ - V^-$)	2.7	5.5	V
Temperature Range ⁽¹⁾	-40	85	°C

- (1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMV7235, LMV7239		UNIT
	DGK (SC70)	DBV (SOT-23)	
	5 PINS	5 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	478	265	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics, 2.7 V

Unless otherwise specified, all limits ensured for $T_A = 25^\circ\text{C}$, $V_{CM} = V^+/2$, $V^+ = 2.7\text{ V}$, $V^- = 0\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
V_{OS}	Input Offset Voltage		–6	±0.8	+6	mV
		At temp extremes	–8		+8	
I_B	Input Bias Current			30	400	nA
		At temp extremes			600	
I_{OS}	Input Offset Current			5	200	nA
		At temp extremes			400	
CMRR	Common-Mode Rejection Ratio	$0\text{ V} < V_{CM} < 2.7\text{ V}^{(3)}$	52	62		dB
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{ V}$ to 5 V	65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50 dB	$V^- - 0.1$	–0.2 to 2.9	$V^+ + 0.1$	V
		At temp extremes	V^-		V^+	
V_O	Output Swing High (LMV7239 only)	$I_L = 4\text{ mA}$, $V_{ID} = 500\text{ mV}$	$V^+ - 0.35$	$V^+ - 0.26$		V
		$I_L = 0.4\text{ mA}$, $V_{ID} = 500\text{ mV}$		$V^+ - 0.02$		V
	Output Swing Low	$I_L = -4\text{ mA}$, $V_{ID} = -500\text{ mV}$		230	350	mV
		At temp extremes			450	
		$I_L = -0.4\text{ mA}$, $V_{ID} = -500\text{ mV}$		15		mV
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0\text{ V}$ (LMV7239 only)		15		mA
		Sinking, $V_O = 2.7\text{ V}$ (LMV7235, $R_L = 10\text{ k}$)		20		mA
I_S	Supply Current	No load		52	85	μA
		At temp extremes			100	
t_{PD}	Propagation Delay	Overdrive = 20 mV $C_{LOAD} = 15\text{ pF}^{(4)}$		96		ns
		Overdrive = 50 mV $C_{LOAD} = 15\text{ pF}^{(4)}$		87		ns
		Overdrive = 100 mV $C_{LOAD} = 15\text{ pF}^{(4)}$		85		ns
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	Overdrive = 20 mV ⁽⁵⁾		2		ns
t_r	Output Rise Time	LMV7239/LMV7239Q 10% to 90%		1.7		ns
		LMV7235 10% to 90% ⁽⁴⁾		112		ns
t_f	Output Fall Time	90% to 10%		1.7		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)			3		nA

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(3) CMRR is not linear over the common mode range. Limits are guaranteed over the worst case from 0 to $V_{CC}/2$ or $V_{CC}/2$ to V_{CC} .

(4) A 10k pullup resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.

(5) Propagation Delay Skew is defined as the absolute value of the difference between t_{PDLH} and t_{PDHL} .

LMV7235, LMV7239

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6.6 Electrical Characteristics, 5 V

 Unless otherwise specified, all limits ensured for $T_A = 25^\circ\text{C}$, $V_{CM} = V^+/2$, $V^+ = 5\text{ V}$, $V^- = 0\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
V_{OS}	Input Offset Voltage		–6	±1	+6	mV
		At temp extremes	–8		+8	
I_B	Input Bias Current			30	400	nA
		At temp extremes			600	
I_{OS}	Input Offset Current			5	200	nA
		At temp extremes			400	
CMRR	Common-Mode Rejection Ratio	$0\text{ V} < V_{CM} < 5\text{ V}$	52	67		dB
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{ V}$ to 5 V	65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB	$V^- - 0.1$	–0.2 to 5.2	$V^+ + 0.1$	V
		At temp extremes	V^-		V^+	
V_O	Output Swing High (LMV7239 only)	$I_L = 4\text{ mA}$, $V_{ID} = 500\text{ mV}$	$V^+ - 0.25$	$V^+ - 0.15$		V
		$I_L = 0.4\text{ mA}$, $V_{ID} = 500\text{ mV}$		$V^+ - 0.01$		V
	Output Swing Low	$I_L = -4\text{ mA}$, $V_{ID} = -500\text{ mV}$		230	350	mV
		At temp extremes			450	
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0\text{ V}$ (LMV7239 only)	25	55		mA
		At temp extremes	15			
	Sinking, $V_O = 5\text{ V}$ (LMV7235, $R_L = 10\text{ k}$)		30	60		mA
		At temp extremes	20			
I_S	Supply Current	No load		65	95	μA
		At temp extremes			110	
t_{PD}	Propagation Delay	Overdrive = 20 mV $C_{LOAD} = 15\text{ pF}$ ⁽³⁾		89		ns
		Overdrive = 50 mV $C_{LOAD} = 15\text{ pF}$ ⁽³⁾		82		ns
		Overdrive = 100 mV $C_{LOAD} = 15\text{ pF}$ ⁽³⁾		75		ns
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	Overdrive = 20 mV ⁽⁴⁾		1		ns
t_r	Output Rise Time	LMV7239 10% to 90%		1.2		ns
		LMV7235 10% to 90%		100		ns
t_f	Output Fall Time	90% to 10%		1.2		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)			3		nA

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(3) A 10k pullup resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.

 (4) Propagation Delay Skew is defined as the absolute value of the difference between t_{PDLH} and t_{PDHL} .

6.7 Typical Characteristics

(Unless otherwise specified, $V_S = 5V$, $C_L = 10pF$, $T_A = 25^\circ C$).

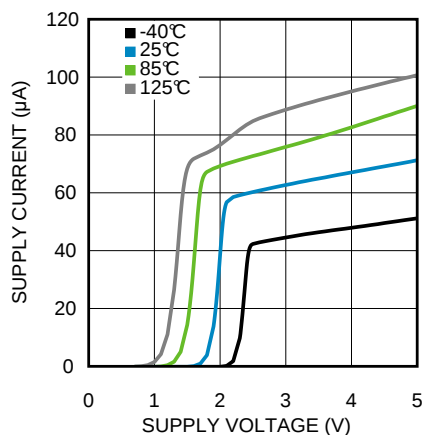


Figure 1. Supply Current vs. Supply Voltage

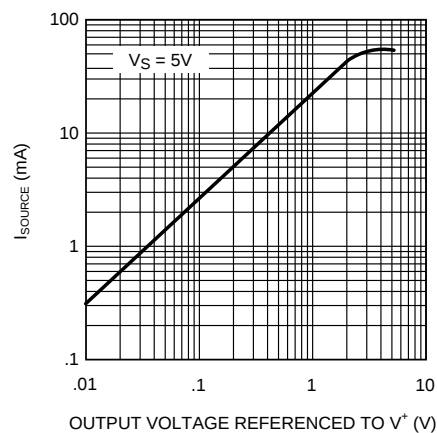


Figure 2. Sourcing Current vs. Output Voltage

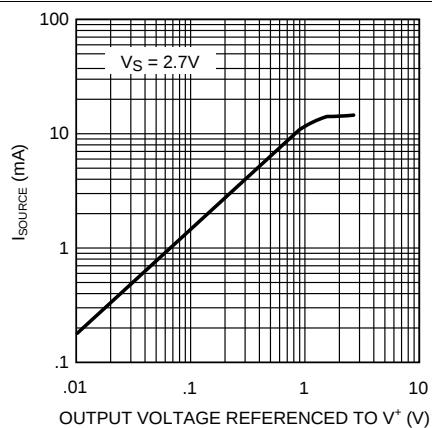


Figure 3. Sourcing Current vs. Output Voltage

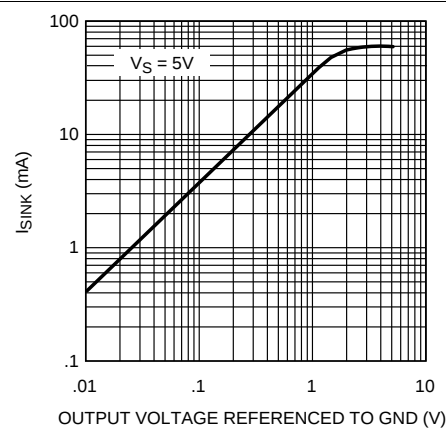


Figure 4. Sinking Current vs. Output Voltage

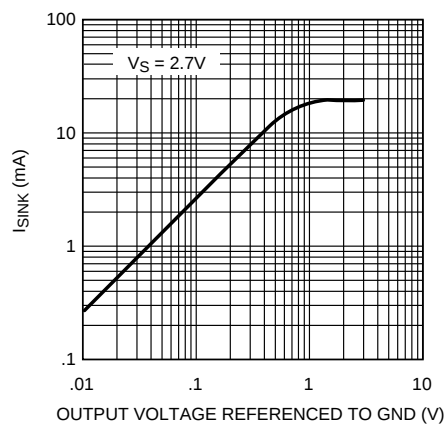


Figure 5. Sinking Current vs. Output Voltage

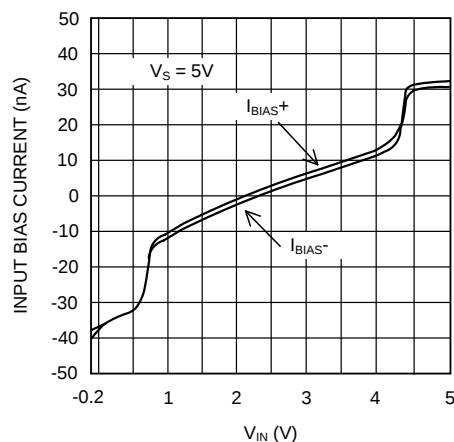


Figure 6. Input Bias Current vs. Input Voltage

Typical Characteristics (continued)

(Unless otherwise specified, $V_S = 5V$, $C_L = 10pF$, $T_A = 25^\circ C$).

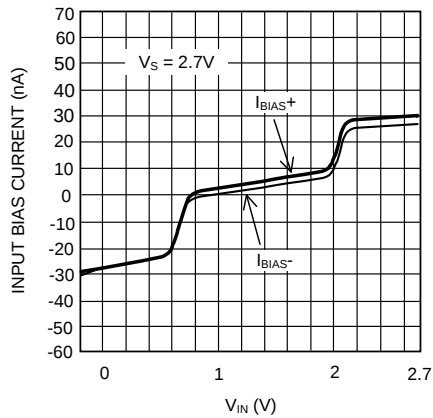


Figure 7. Input Bias Current vs. Input Voltage

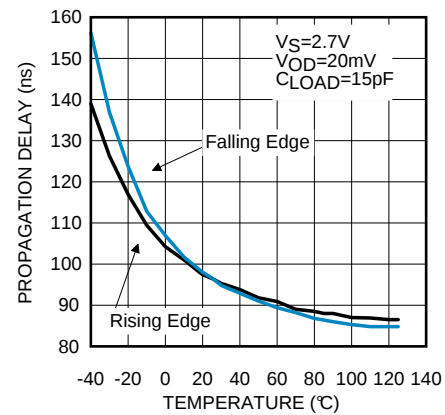


Figure 8. Propagation Delay vs. Temperature

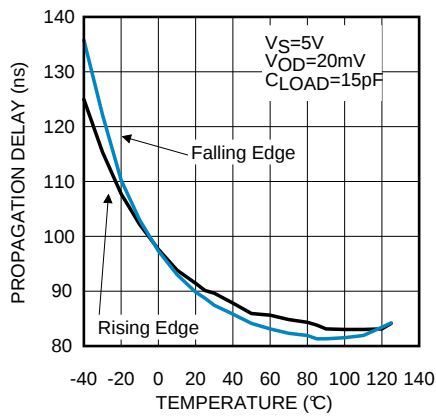


Figure 9. Propagation Delay vs. Temperature

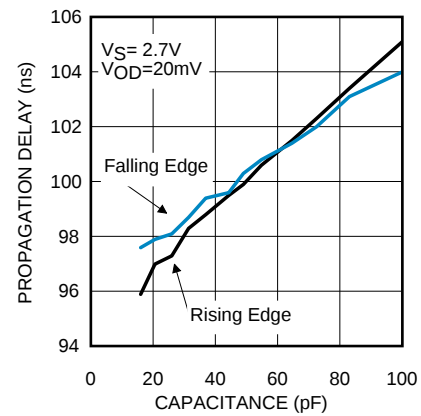


Figure 10. Propagation Delay vs. Capacitive Load

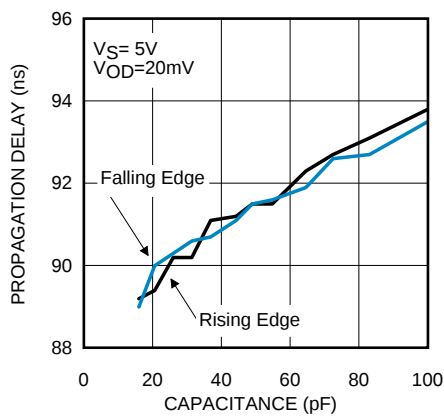


Figure 11. Propagation Delay vs. Capacitive Load

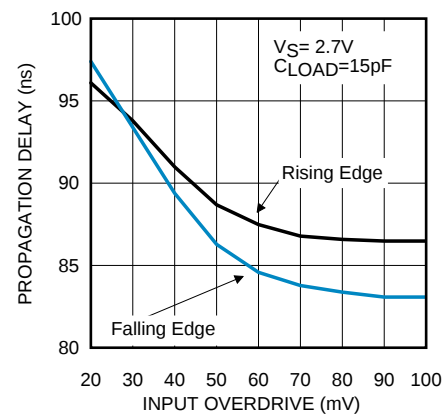


Figure 12. Propagation Delay vs. Input Overdrive

Typical Characteristics (continued)

(Unless otherwise specified, $V_S = 5V$, $C_L = 10pF$, $T_A = 25^\circ C$).

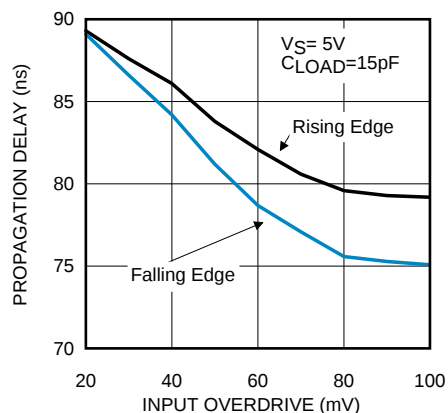


Figure 13. Propagation Delay vs. Input Overdrive

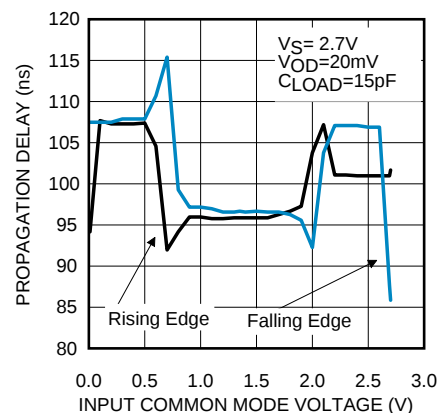


Figure 14. Propagation Delay vs. Common-Mode Voltage

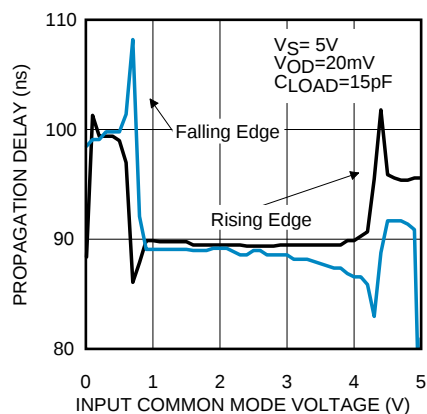


Figure 15. Propagation Delay vs. Common-Mode Voltage

7 Detailed Description

7.1 Overview

The LMV7235 and LMV7239 are ultra low power, low voltage, 75-ns comparators. They are ensured to operate over the full supply voltage range of 2.7 V to 5.5 V. These devices achieve a 75-ns propagation delay while consuming only 65 μ A of supply current at 5 V.

The LMV7235 and LMV7239 have a greater than rail-to-rail common-mode voltage range. The input common-mode voltage range extends 200 mV below ground and 200 mV above supply, allowing both ground and supply sensing.

7.2 Functional Block Diagram

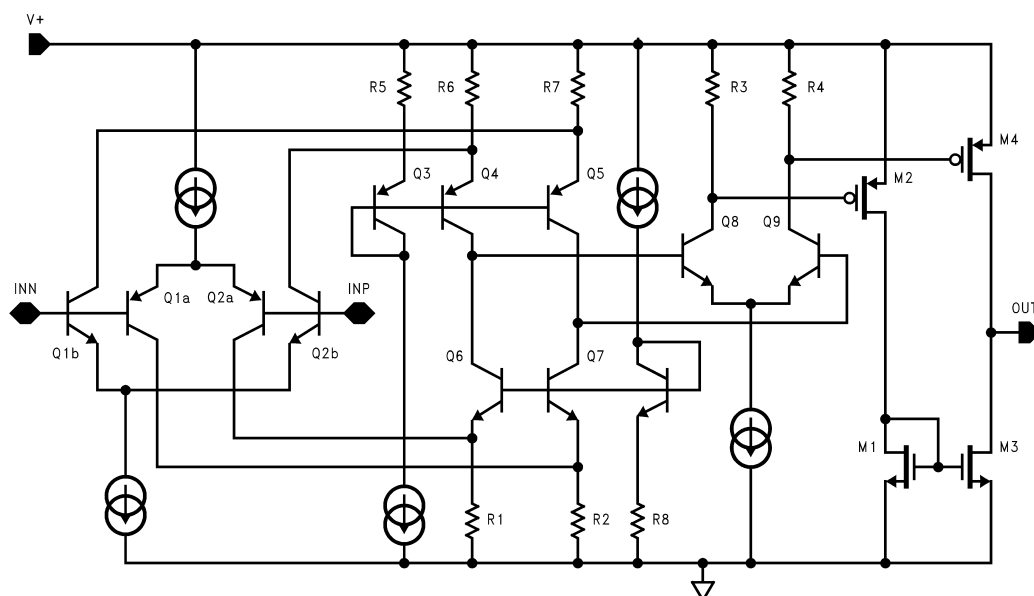


Figure 16. Simplified Schematic of LMV7239

7.3 Feature Description

7.3.1 Input Stage

The LMV7235 and LMV7239 are rail-to-rail input and output. The typical input common-mode voltage range of -0.2 V below the ground to 0.2 V above the supply. The LMV7235 and LMV7239 use a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^- and the NPN stage senses common-mode voltage near V^+ . If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on resulting in an increase of input bias current.

If one of the inputs goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common-mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

7.3.2 Output Stage: LMV7239

The LMV7239 has a push-pull output. When the output switches, there is a low resistance path between V_{CC} and ground, causing high output sinking or sourcing current during the transition.

Feature Description (continued)

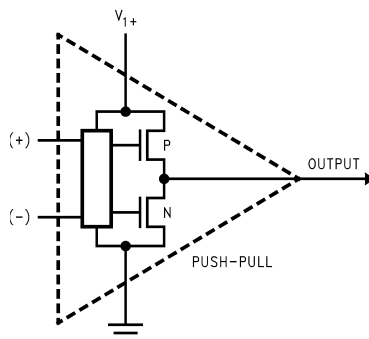


Figure 17. LMV7239 Push-Pull Output Stage

7.3.3 Output Stage: LMV7235

The LMV7235 has an open drain that requires a pull-up resistor to a positive supply voltage for the output to switch properly. The internal circuitry is identical to the LMV7239 except that the upper P channel output device M4 is absent in the [Functional Block Diagram](#) above. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage by the external pull-up resistor. This allows the output to be OR'ed with other open drain outputs on the same bus. The output pull-up resistor can be connected to any voltage level between V- and V+ for level shifting applications.

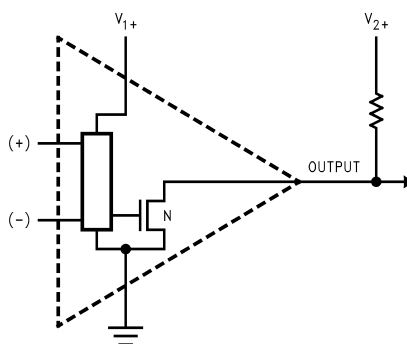


Figure 18. LMV7235 Open Drain Output

7.4 Device Functional Modes

7.4.1 Capacitive and Resistive Loads

The propagation delay on the rising edge of the LMV7235 depends on the load resistance and capacitance values.

7.4.2 Noise

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero. The high gain of this comparator eliminates this problem. Less than 1 μ V of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See [Hysteresis](#).)

7.4.3 Hysteresis

To improve propagation delay when low overdrive is needed hysteresis can be added.

Device Functional Modes (continued)

7.4.3.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V^+ of the comparator as shown in Figure 19. When V_{IN} at the inverting input is less than V_A , the voltage at the noninverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V^+). The three network resistors can be represented as $R_1 // R_3$ in series with R_2 .

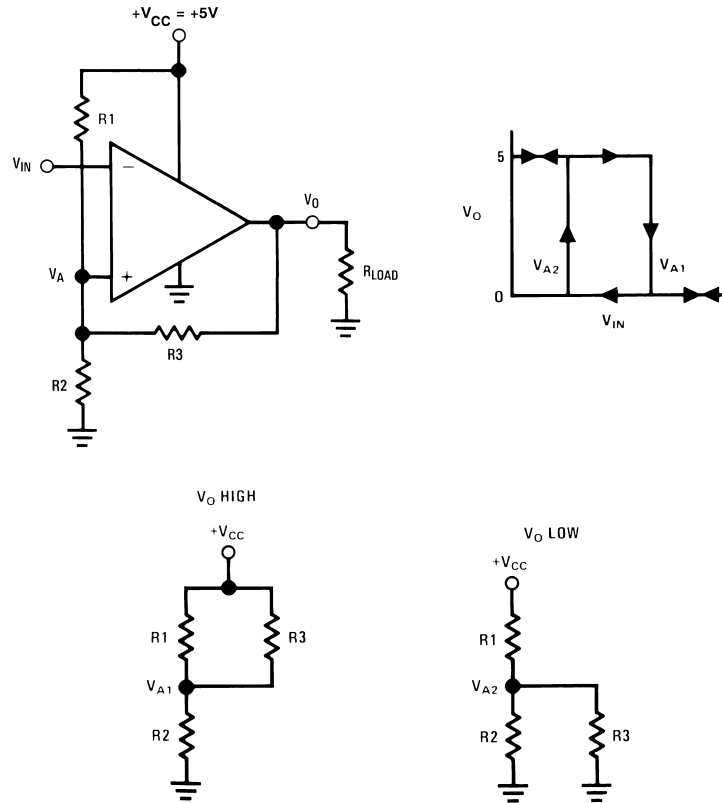


Figure 19. Inverting Comparator With Hysteresis

The lower input trip voltage V_{A1} is defined as:

$$V_{A1} = V_{CC} R_2 / [(R_1 // R_3) + R_2] \quad (1)$$

When V_{IN} is greater than V_{A1} , the output voltage is low or very close to ground. In this case the three network resistors can be presented as $R_2 // R_3$ in series with R_1 .

The upper trip voltage V_{A2} is defined as:

$$V_{A2} = V_{CC} (R_2 // R_3) / [(R_1) + (R_2 // R_3)] \quad (2)$$

The total hysteresis provided by the network is defined as $\Delta V_A = V_{A1} - V_{A2}$.

$$\Delta V_A = \frac{+V_{CC} R_1 R_2}{R_1 R_2 + R_1 R_3 + R_2 R_3} \quad (3)$$

7.4.3.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by:

$$\Delta V_{IN1} = \frac{V_{REF} (R_1 + R_2)}{R_2} \quad (4)$$

As soon as V_O switches to V_{CC} , V_A steps to a value greater than V_{REF} which is given by:

Device Functional Modes (continued)

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN1})R_1}{R_1 + R_2} \quad (5)$$

To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF} . V_{IN2} can be calculated by:

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC}R_1}{R_2} \quad (6)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2} .

$$\Delta V_{IN} = V_{CC}R_1 / R_2 \quad (7)$$

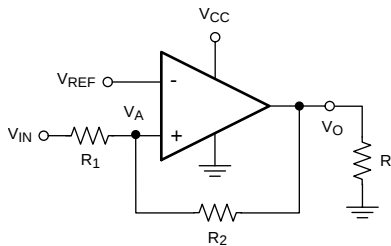


Figure 20. Noninverting Comparator With Hysteresis

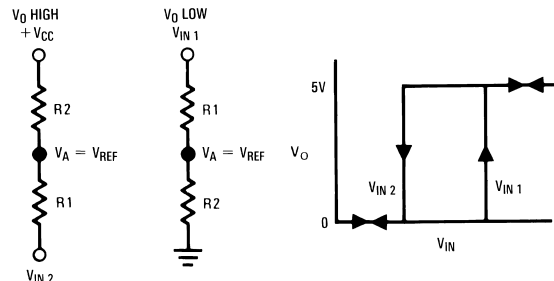


Figure 21. Noninverting Comparator Thresholds

7.4.4 Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the noninverting input is connected to a 100 mV_{PP} AC signal. As the signal at the noninverting input crosses 0V, the comparator's output changes state.

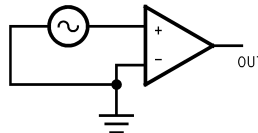


Figure 22. Simple Zero Crossing Detector

7.4.4.1 Zero Crossing Detector With Hysteresis

To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider R_4 and R_5 establishes a reference voltage, V_1 , at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5 , the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$.

The positive feedback resistor, R_6 , is made very large with respect to $R_5 \parallel R_6 = 2000 R_5$. The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions.

Device Functional Modes (continued)

Diode D_1 is used to ensure that the inverting input terminal of the comparator never goes below approximately -100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately -700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1 .

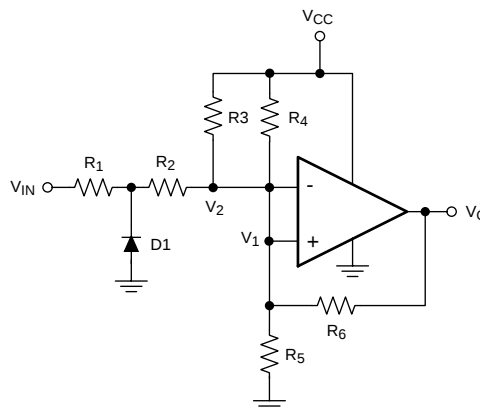


Figure 23. Zero Crossing Detector With Hysteresis

7.4.5 Threshold Detector

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. As the input on the noninverting input passes the V_{REF} threshold, the comparator's output changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

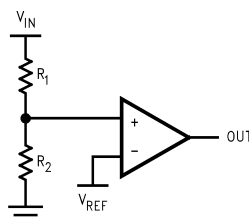


Figure 24. Threshold Detector

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV7235 and LMV7239 are single supply comparators with 75 ns of propagation delay and only 65 μ A of supply current.

8.2 Typical Applications

8.2.1 Square Wave Oscillator

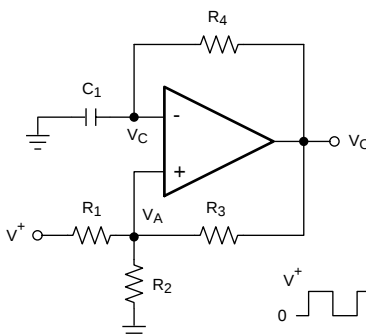


Figure 25. Square Wave Oscillator

8.2.1.1 Design Requirements

A typical application for a comparator is as a square wave oscillator. The circuit in [Figure 25](#) generates a square wave whose period is set by the RC time constant of the capacitor C_1 and resistor R_4 .

8.2.1.2 Detailed Design Procedure

The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.

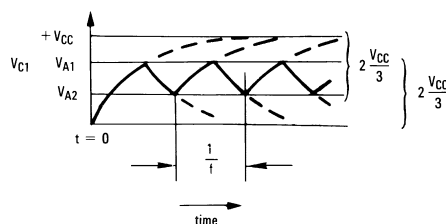


Figure 26. Square Wave Oscillator Timing Thresholds

Consider the output of [Figure 25](#) to be high to analyze the circuit. That implies that the inverted input (V_C) is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4 , and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at this point is:

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \parallel R_3} \quad (8)$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2/3 V_{CC}$

Typical Applications (continued)

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is:

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)} \quad (9)$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$.

The capacitor C_1 now discharges through R_4 , and the voltage V_C decreases until it is equal to V_{A2} , at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4 C_1 \ln 2$. Hence the formula for the frequency is:

$$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2) \quad (10)$$

The LMV7239 should be used for a symmetrical output. The LMV7235 will require a pullup resistor on the output to function, and will have a slightly asymmetrical output due to the reduced sourcing current.

8.2.1.3 Application Curves

Figure 27 shows the simulated results of an oscillator using the following values:

1. $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
2. $C_1 = 100 \text{ pF}$, $C_L = 20 \text{ pF}$
3. $V_+ = 5 \text{ V}$, $V_- = \text{GND}$
4. C_{STRAY} (not shown) from V_A to $\text{GND} = 10 \text{ pF}$

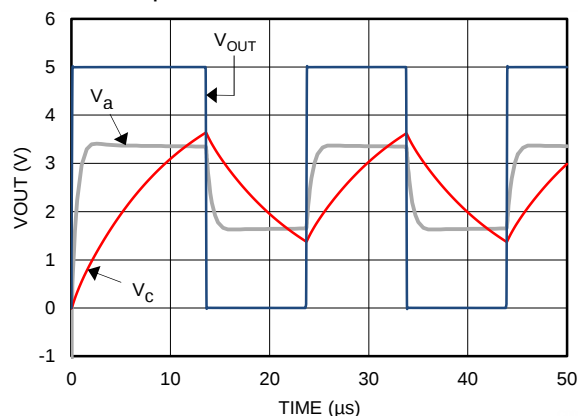


Figure 27. Square Wave Oscillator Output Waveform

8.2.2 Crystal Oscillator

A simple crystal oscillator using the LMV7235 or LMV7239 is shown in Figure 28. Resistors R_1 and R_2 set the bias point at the comparator's noninverting input. Resistors, R_3 and R_4 and capacitor C_1 set the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator

Typical Applications (continued)

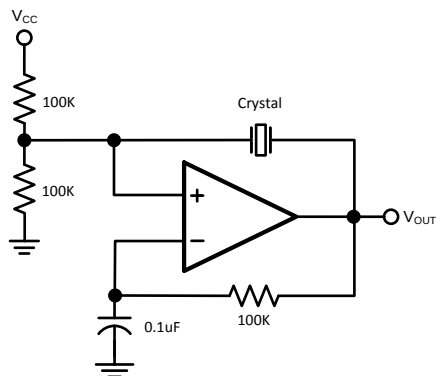


Figure 28. Crystal Oscillator

8.2.3 Infrared (IR) Receiver

The LMV7235 and LMV7239 can also be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D . When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions.

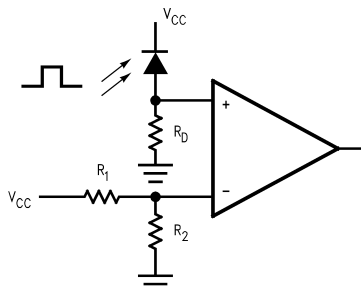


Figure 29. IR Receiver

8.2.4 Window Detector

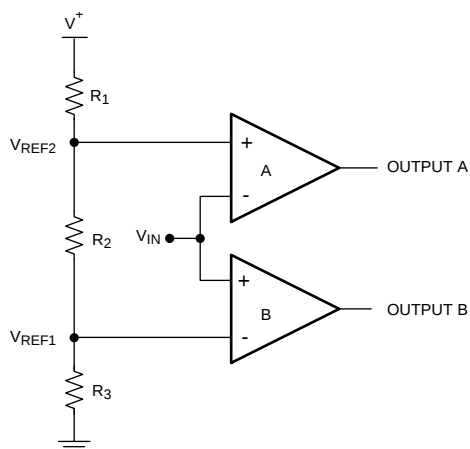


Figure 30. Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when $V_{REF1} < V_{IN} < V_{REF2}$

Typical Applications (continued)

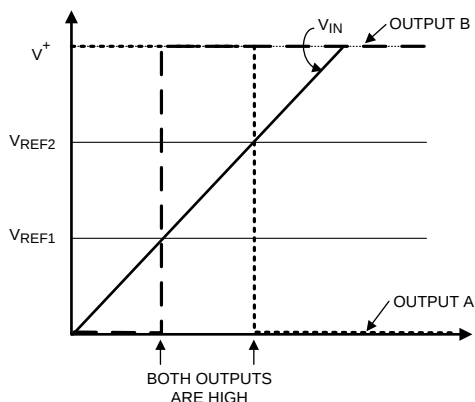


Figure 31. Window Detector Output Signal

The comparator outputs A and B are high only when $V_{REF1} < V_{IN} < V_{REF2}$, or "within the window", where these are defined as:

$$V_{REF1} = R_3 / (R_1 + R_2 + R_3) \times V_+ \quad (11)$$

$$V_{REF2} = (R_2 + R_3) / (R_1 + R_2 + R_3) \times V_+ \quad (12)$$

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

The LMV7235 with an open drain output should be used if the outputs are to be tied together for a common logic output.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.

9 Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01-μF ceramic capacitor in parallel with a 10-μF capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to "ring" due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV7235 and LMV72391 as high-speed devices. Keep the ground paths short and place small (low ESR ceramic) bypass capacitors directly between the V+ and V– pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

Proper grounding and the use of a ground plane will help to ensure the specified performance of the LMV7235 and LMV72391. Minimizing trace lengths, reducing unwanted parasitic capacitance and using surface-mount components will also help. Comparators are very sensitive to input noise.

The LMV7235 and LMV72391 require a high-speed layout. Follow these layout guidelines:

1. Use printed-circuit board with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1- μ F, ceramic surface-mount capacitor) as close as possible to V_{CC} pin.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from output.
4. Solder the device directly to the printed-circuit board rather than using a socket.
5. For slow moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to t_{PD} when the source impedance is low.
6. The top-side ground plane runs between the output and inputs.
7. Ground trace from the ground pin runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

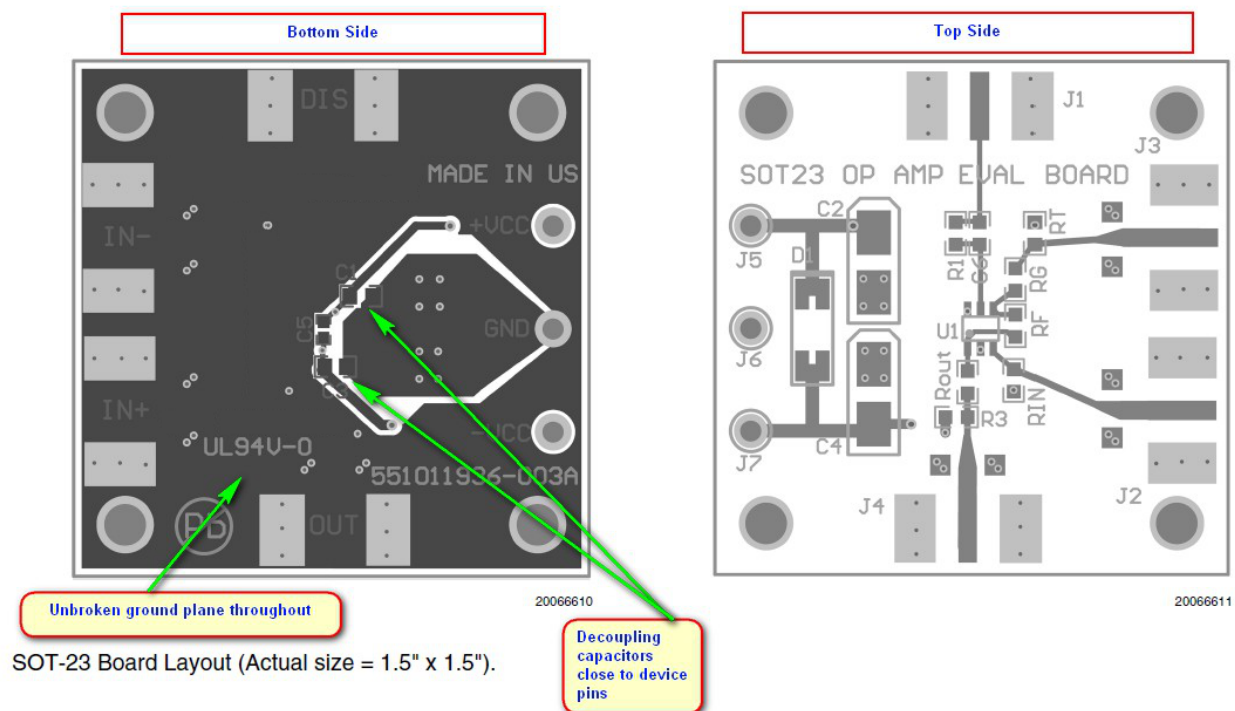


Figure 32. SOT-23 Board Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

LMV7239 TINA SPICE 模型, [SNOM392](#)

TINA-TI 基于 SPICE 的模拟仿真程序, <http://www.ti.com.cn/tool/cn/tina-ti>

DIP 适配器评估模块, <http://www.ti.com.cn/tool/cn/dip-adapter-evm>

TI 通用运行放大器评估模块, <http://www.ti.com.cn/tool/cn/opampevm>

11.2 文档支持

11.2.1 相关文档

《四个独立运行的比较器》(SNOA654)

11.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
LMV7235	单击此处	单击此处	单击此处	单击此处	单击此处
LMV7239	单击此处	单击此处	单击此处	单击此处	单击此处

11.4 接收文档更新通知

要接收文档更新通知, 请导航至 [Ti.com.cn](http://www.ti.com.cn) 上的器件产品文件夹。单击右上角的通知我 进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点; 请参阅 TI 的 《使用条款》。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.6 商标

E2E is a trademark of Texas Instruments.

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序, 可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7235M5	ACTIVE	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 85	C21A	Samples
LMV7235M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C21A	Samples
LMV7235M5X	ACTIVE	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Call TI	-40 to 85	C21A	Samples
LMV7235M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C21A	Samples
LMV7235M7	ACTIVE	SC70	DCK	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 85	C21	Samples
LMV7235M7/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C21	Samples
LMV7235M7X/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C21	Samples
LMV7239M5	NRND	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 85	C20A	
LMV7239M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C20A	Samples
LMV7239M5X	NRND	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Call TI	-40 to 85	C20A	
LMV7239M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C20A	Samples
LMV7239M7	NRND	SC70	DCK	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 85	C20	
LMV7239M7/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C20	Samples
LMV7239M7X	NRND	SC70	DCK	5	3000	Non-RoHS & Green	Call TI	Call TI	-40 to 85	C20	
LMV7239M7X/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C20	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7235M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7235M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7235M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

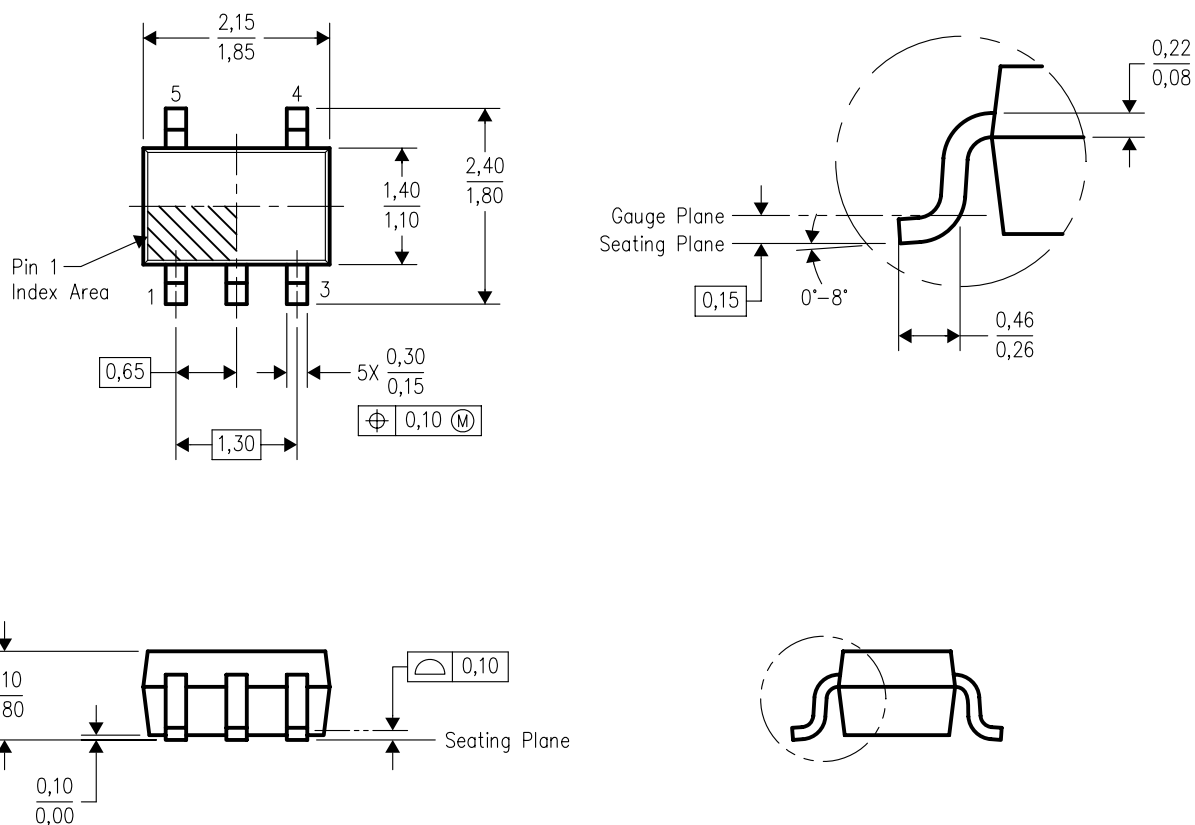


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7235M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7235M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7235M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7235M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7235M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7235M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7235M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7239M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7239M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239M7X	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

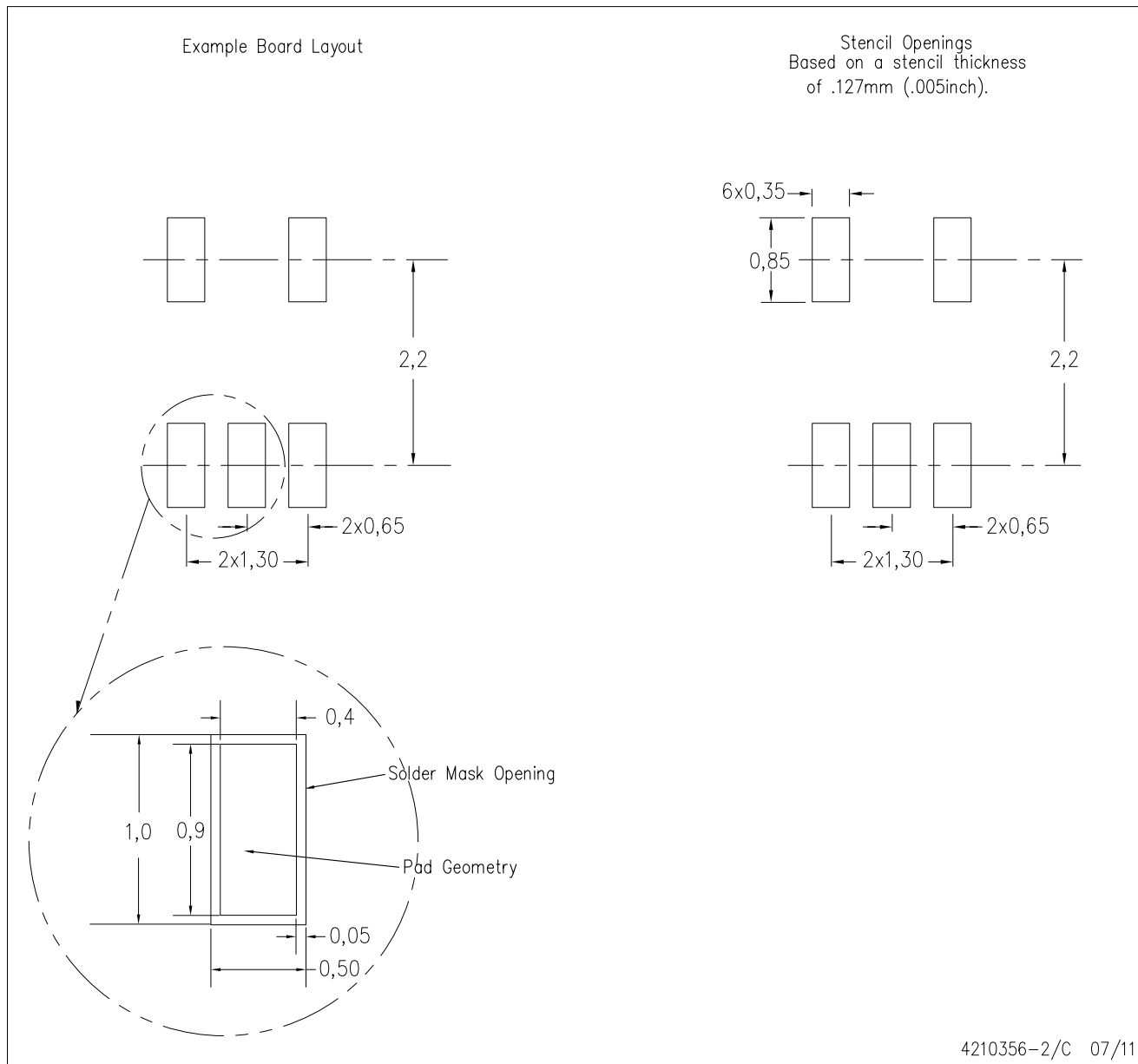


4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

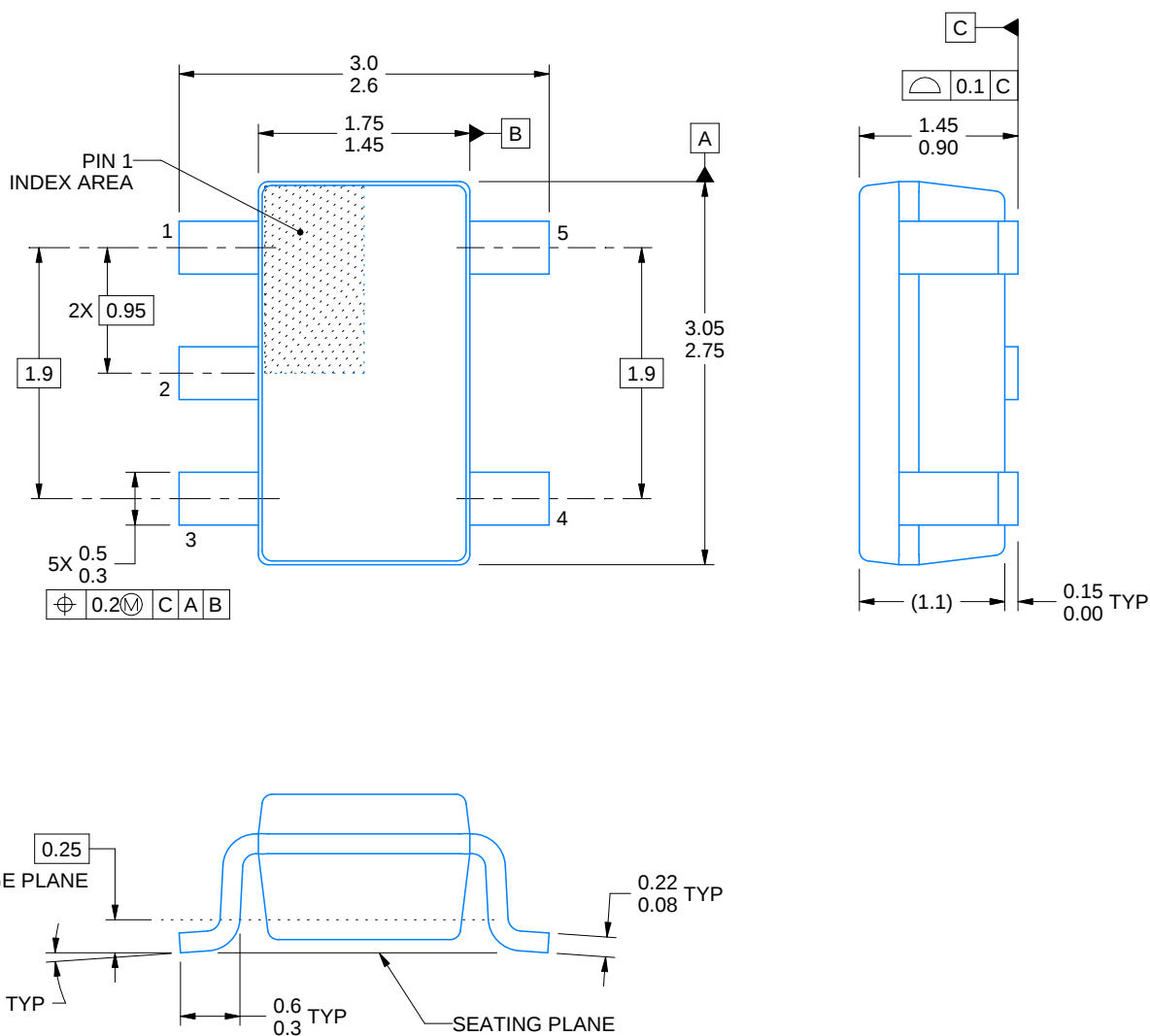


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

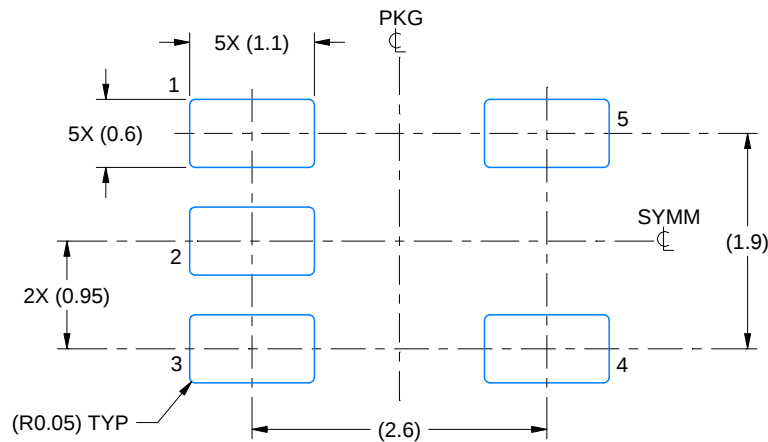
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

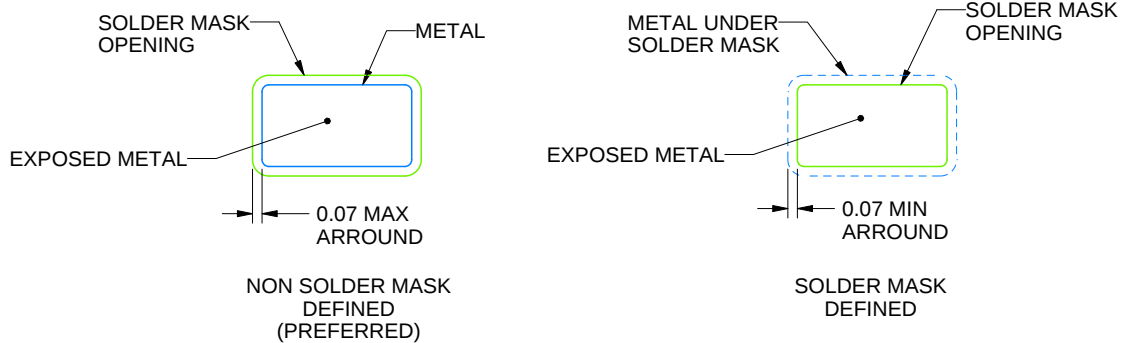
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

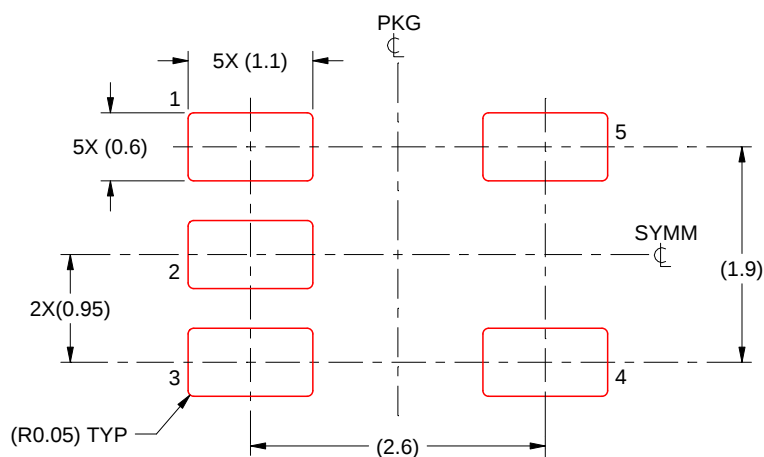
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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