INA191 低功耗、零漂移、宽动态范围、精密电流检测放大器

1 特性

- 低功耗：
  - 低电源电压 V_S：1.7V 至 5.5V
  - 低关断电流：100nA（最大值）
  - 低静态电流：25°C 下为 43µA（典型值）
- 低输入偏置电流：100pA（典型值）（支持微安级电流测量）
- 精度：
  - ±0.25% 的最大增益误差（A2 至 A5 器件）
  - 7ppm/°C 的增益漂移（最大值）
  - ±12µV（最大值）的失调电压
  - 0.13µV/°C 的失调电压温漂（最大值）
- 宽共模电压范围：–0.2V 至 +40V
- 增益选项：
  - INA191A1：25V/V
  - INA191A2：50V/V
  - INA191A3：100V/V
  - INA191A4：200V/V
  - INA191A5：500V/V
- 封装：0.895mm^2 DSBGA

2 应用

- 笔记本电脑
- 手机
- 电池供电设备
- 电信设备
- 电源管理
- 电池充电器

3 说明

INA191 是一款低功耗、电压输出、电流分流监控器（也称为电流检测放大器），常用于过流保护和精密电流测量（用于实现系统优化），此外它还可用于闭环反馈电路中。该器件可在独立于电源电压之外的 –0.2V 至 +40V 共模电压下检测分流器上的压降。INA191 的低输入偏置电流允许使用更大的电流检测电阻器，从而能够提供微安级的精确电流测量。提供了五个固定增益：25V/V、50V/V、100V/V、200V/V 或 500V/V。零漂移架构的低失调电压扩展了电流测量的动态范围，并允许使用具有更低功率损耗的更小检测电阻器，同时仍提供精确的电流测量。

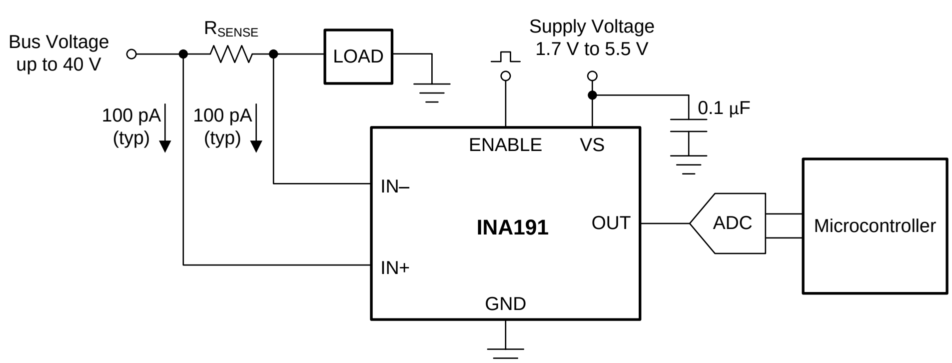
INA191 由 1.7V 至 5.5V 单电源供电，在启用时消耗的最大电源电流为 65µA，在禁用时仅为 100nA。该器件的额定工作温度范围为 –40°C 至 +125°C，并且采用 DSBGA-6 封装。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
INA191	DSBGA (6)	1.17mm × 0.765mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

简化原理图



目录

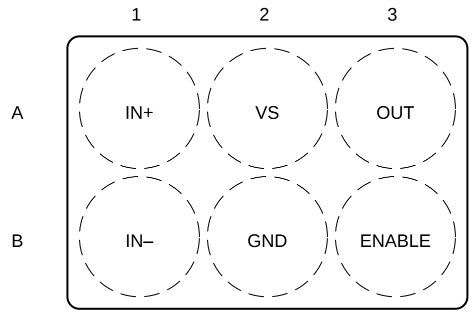
4 修订历史记录

Changes from Original (February 2019) to Revision A — **Page**

- 已更改 将器件从预告信息改为生产数据（正在供货） ... 1

5 Pin Configuration and Functions

YFD Package
6-Pin DSBGA
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ENABLE	B3	Digital input	Enable pin. When this pin is driven to V_S, the device is on and functions as a current sense amplifier. When this pin is driven to GND, the device is off, the supply current is reduced, and the output is placed in a high-impedance state. This pin must be driven externally, or connected to V_S if not used.
GND	B2	Analog	Ground
IN+	A1	Analog input	Current-shunt monitor positive input. For high-side applications, connect this pin to the bus voltage side of the sense resistor. For low-side applications, connect this pin to the load side of the sense resistor.
IN–	B1	Analog input	Current-shunt monitor negative input. For high-side applications, connect this pin to the load side of the sense resistor. For low-side applications, connect this pin to the ground side of the sense resistor.
OUT	A3	Analog output	This pin provides an analog voltage output that is the amplified voltage difference from the IN+ to the IN– pins.
VS	A2	Analog	Power supply, 1.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage			6	V
	Analog inputs, V_{IN+}, $V_{IN–}$[2]	Differential (V_{IN+}) – ($V_{IN–}$)	–42	42	V
		Common-mode, V_{CM}[3]	GND – 0.3	42	
V_{ENABLE}	ENABLE pin voltage		GND – 0.3	6	V
V_{OUT}	OUT pin Voltage[3]		GND – 0.3	(V_S) + 0.3	V
	Input current into any pin[3]			5	mA
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	–0.2		40	V
V_{IN+},V_{IN-}	Input pin voltage range	–0.2		40	V
V_S	Operating supply voltage	1.7		5.5	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA191	UNIT
		DSBGA	
		6 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	141.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	1.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	45.7	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.4	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	45.3	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report*.

6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, and V_{ENABLE} = V_S (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
CMRR	Common-mode rejection ratio, RTI (1)	V_{IN+} = –0.1 V to 40 V, T_A = –40°C to +125°C		132	150		dB
V_{OS}	Offset voltage, RTI	V_S = 1.8 V			–2.5	±12	µV
dV_{OS}/dT	Offset drift, RTI	T_A = –40°C to +125°C			10	130	nV/°C
PSRR	Power-supply rejection ratio, RTI	V_S = 1.7 V to 5.5 V			–1	±5	µV/V
I_{IB}	Input bias current	V_{SENSE} = 0 mV			0.1	3	nA
I_{IO}	Input offset current	V_{SENSE} = 0 mV			±0.07		nA
OUTPUT							
G	Gain	A1 devices			25		V/V
		A2 devices			50		
		A3 devices			100		
		A4 devices			200		
		A5 devices			500		
E_G	Gain error	V_{OUT} = 0.1 V to V_S – 0.1 V	A1 device		–0.17%	±0.35%	
			A2, A3, A4, A5 devices		–0.04%	±0.25%	
	Gain error drift	V_{OUT} = 0.1 V to V_S – 0.1 V, T_A = –40°C to +125°C			2	7	ppm/°C
	Nonlinearity error	V_{OUT} = 0.1 V to V_S – 0.1 V			±0.01%		
	Maximum capacitive load	No sustained oscillation			1		nF
VOLTAGE OUTPUT							
V_{SP}	Swing to V_S power-supply rail	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C, V_{SENSE} overdrive = 10 mV			(V_S) – 23	(V_S) – 40	mV
V_{SN}	Swing to GND	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C, V_{SENSE} = –10 mV			(V_{GND}) + 0.05	(V_{GND}) + 1	mV
V_{ZL}	Zero current output voltage	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C, V_{SENSE} = 0 mV	A1, A2, A3 devices		(V_{GND}) + 1	(V_{GND}) + 3	mV
			A4 device		(V_{GND}) + 2	(V_{GND}) + 4	
			A5 device		(V_{GND}) + 3	(V_{GND}) + 7	
FREQUENCY RESPONSE							
BW	Bandwidth	C_{LOAD} = 10 pF	A1 device		45		kHz
			A2 device		37		
			A3 device		35		
			A4 device		33		
			A5 device		27		
SR	Slew rate	V_S = 5.0 V, V_{OUT} = 0.5 V to 4.5 V			0.3		V/µs
t_S	Settling time	From current step to within 1% of final value			30		µs
NOISE, RTI (1)							
	Voltage noise density				75		nV/√Hz
ENABLE							
I_{EN}	Leakage input current	0 V ≤ V_{ENABLE} ≤ V_S			1	100	nA
V_{IH}	High-level input voltage	T_A = –40°C to +125°C		1.35		5.5	V
V_{IL}	Low-level input voltage	T_A = –40°C to +125°C		0		0.4	V
V_{HYS}	Hysteresis				100		mV
I_{ODIS}	Disabled output leakage	V_S = 1.8 V, V_{OUT} = 0 V to 1.8 V, V_{ENABLE} = 0 V			1	5	µA
POWER SUPPLY							
I_Q	Quiescent current	V_{SENSE} = 0 mV, V_S = 1.8 V			43	65	µA
		V_{SENSE} = 0 mV, V_S = 1.8 V, T_A = –40°C to +125°C				85	
I_{QDIS}	Quiescent current disabled	V_{ENABLE} < 0.4, V_{SENSE} = 0 mV			10	100	nA

(1) RTI = referred-to-input.

6.6 Typical Characteristics

at T_A = 25°C, V_S = 1.8 V, V_{IN+} = 12 V, V_{ENABLE} = V_S, and all gain options (unless otherwise noted)

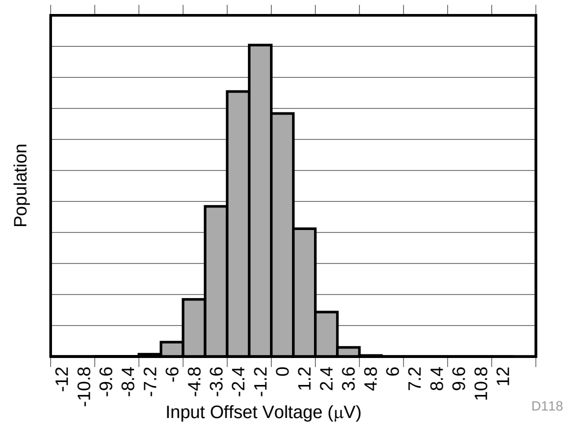


图 1. Input Offset Voltage Production Distribution

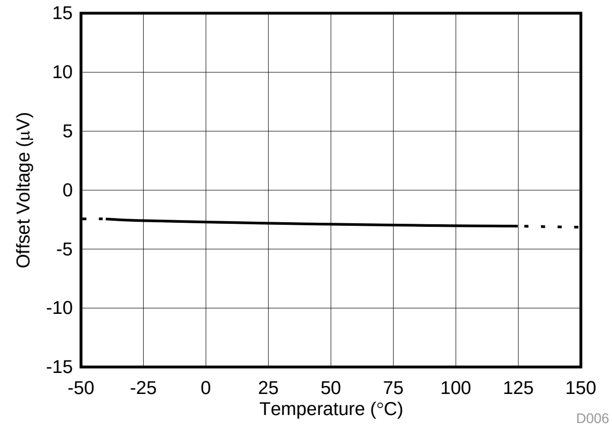


图 2. Offset Voltage vs Temperature

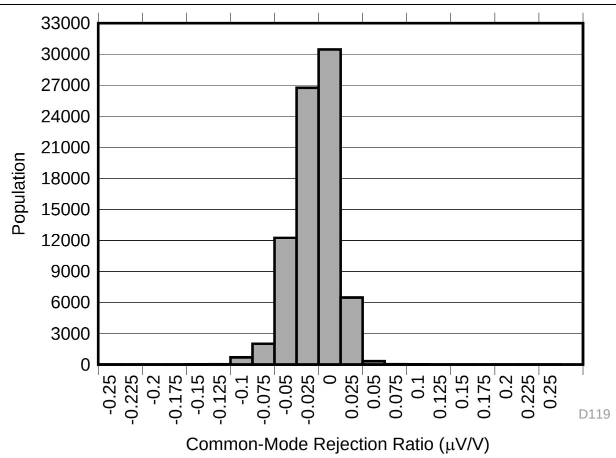


图 3. Common-Mode Rejection Production Distribution

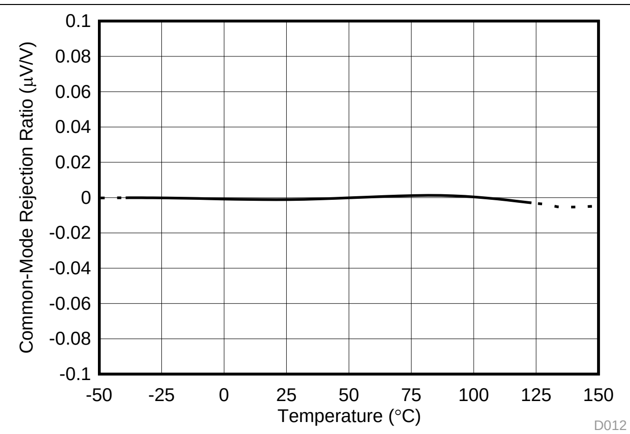
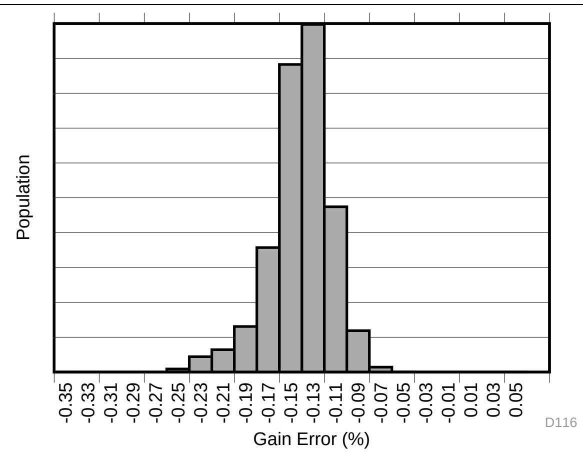
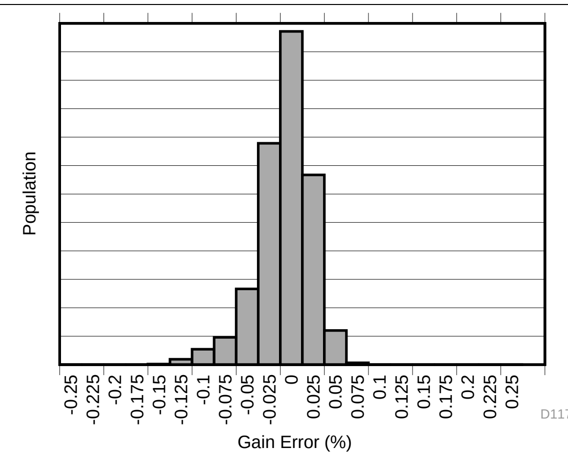


图 4. Common-Mode Rejection Ratio vs Temperature



A1 devices

图 5. Gain Error Production Distribution



A2, A3, A4, A5 devices

图 6. Gain Error Production Distribution

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 1.8 V, V_{IN+} = 12 V, V_{ENABLE} = V_S, and all gain options (unless otherwise noted)

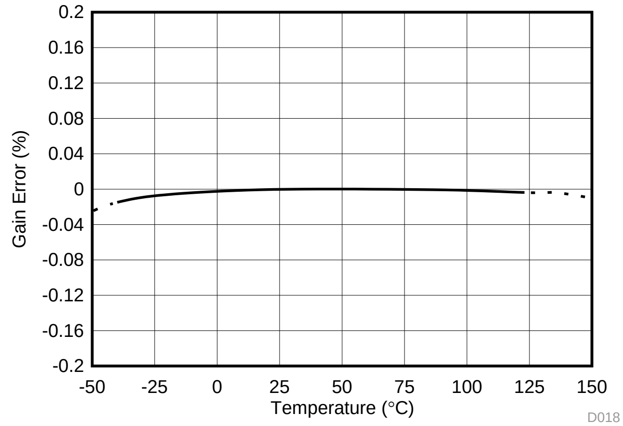
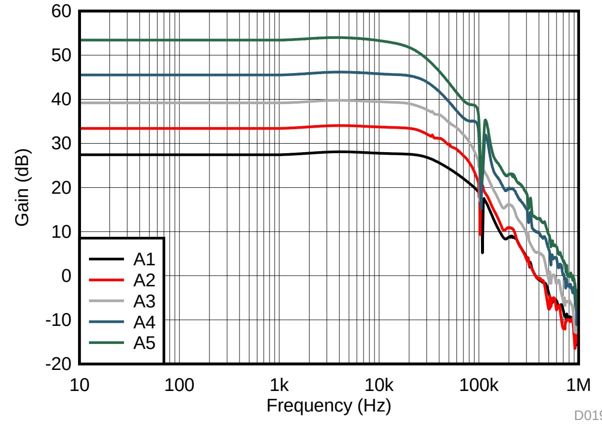
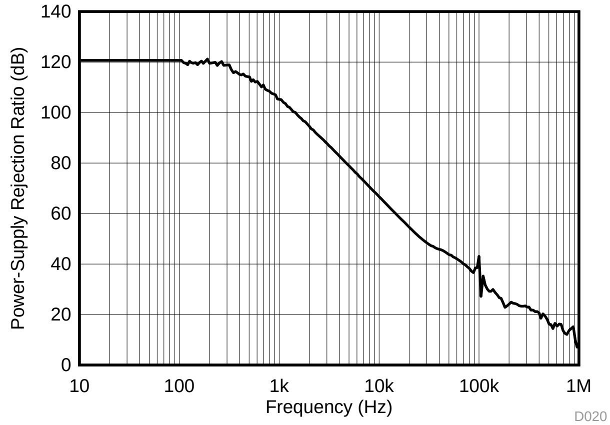


图 7. Gain Error vs Temperature



V_S = 5 V

图 8. Gain vs Frequency



V_S = 5 V

图 9. Power-Supply Rejection Ratio vs Frequency

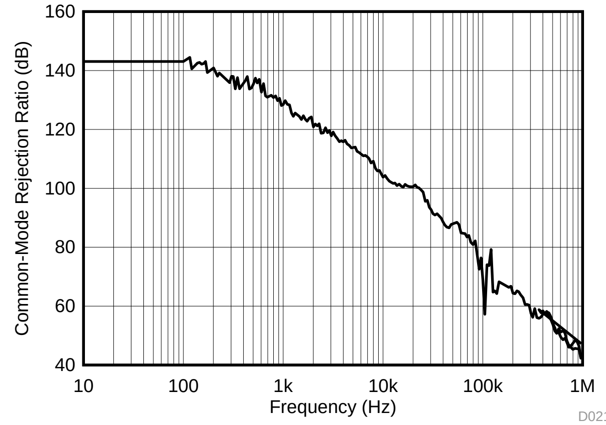
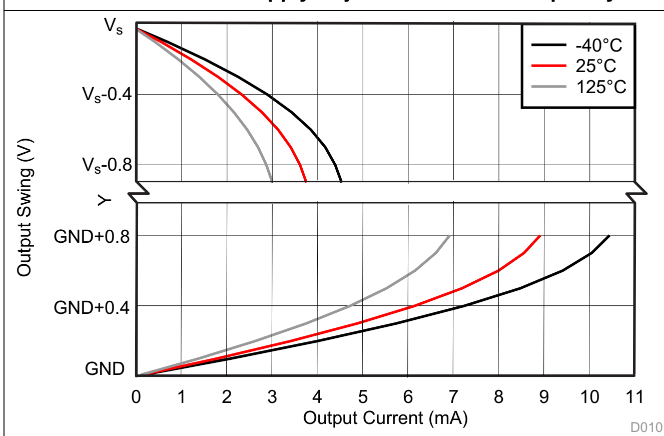
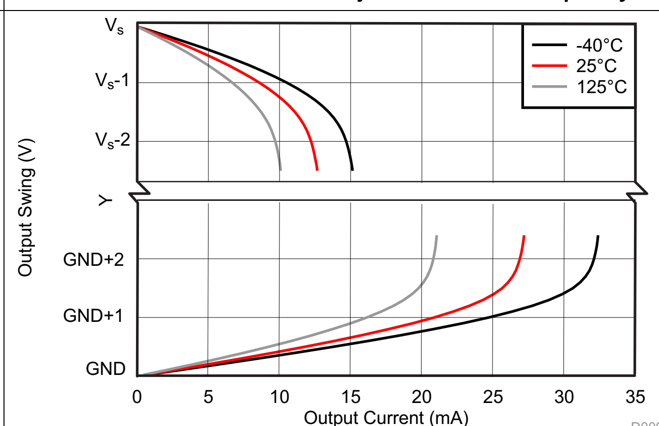


图 10. Common-Mode Rejection Ratio vs Frequency



V_S = 1.8 V

图 11. Output Voltage Swing vs Output Current

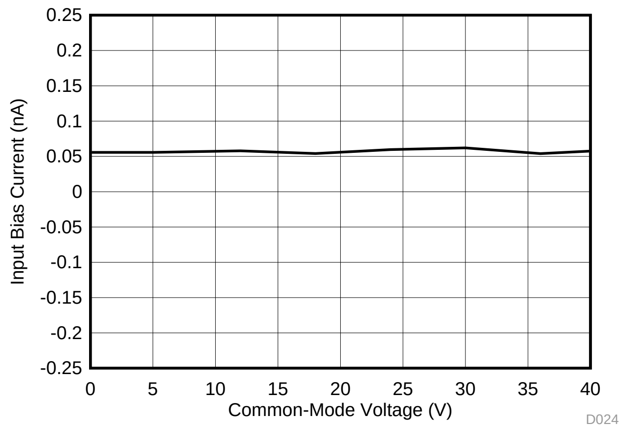


V_S = 5.0 V

图 12. Output Voltage Swing vs Output Current

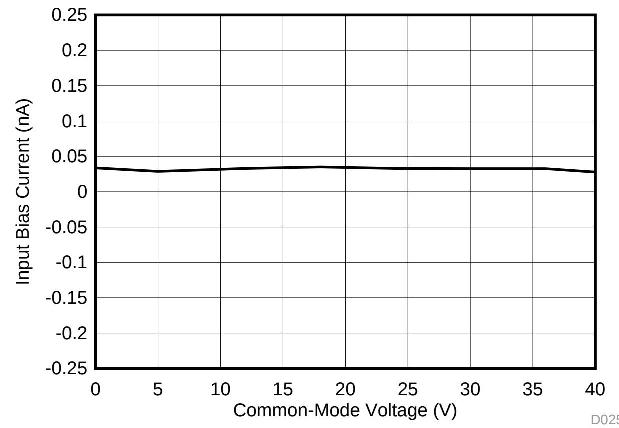
Typical Characteristics (接下页)

at T_A = 25°C, V_S = 1.8 V, V_{IN+} = 12 V, V_{ENABLE} = V_S, and all gain options (unless otherwise noted)



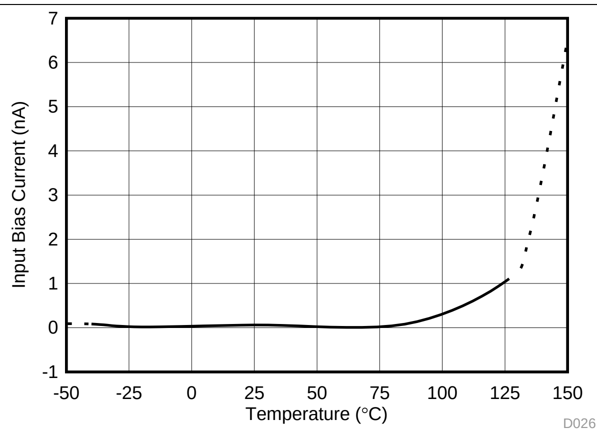
V_S = 5.0 V, V_{SENSE} = 0 V

图 13. Input Bias Current vs Common-Mode Voltage



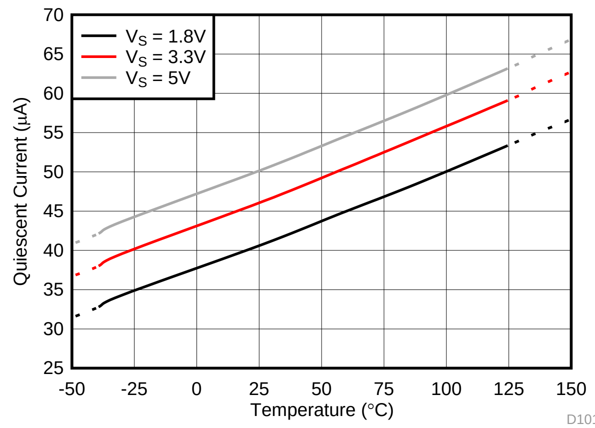
V_{ENABLE} = 0 V, V_{SENSE} = 0 V

图 14. Input Bias Current vs Common-Mode Voltage (Shutdown)



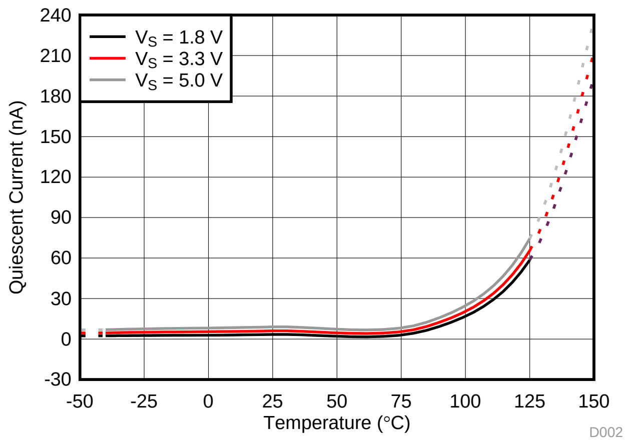
V_{SENSE} = 0 V

图 15. Input Bias Current vs Temperature



V_{ENABLE} = V_S

图 16. Quiescent Current vs Temperature (Enabled)



V_{ENABLE} = 0 V

图 17. Quiescent Current vs Temperature (Disabled)

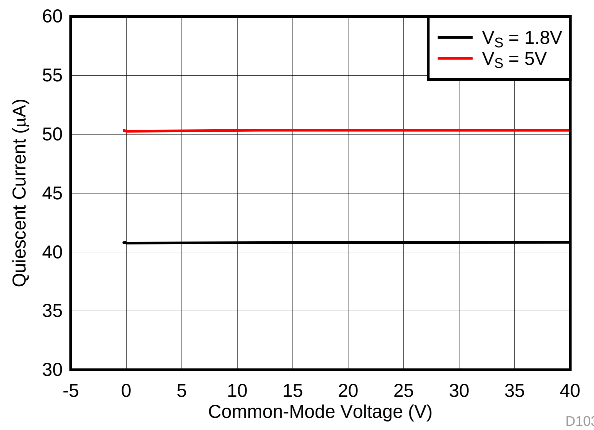


图 18. Quiescent Current vs Common Mode Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 1.8 V, V_{IN+} = 12 V, V_{ENABLE} = V_S, and all gain options (unless otherwise noted)

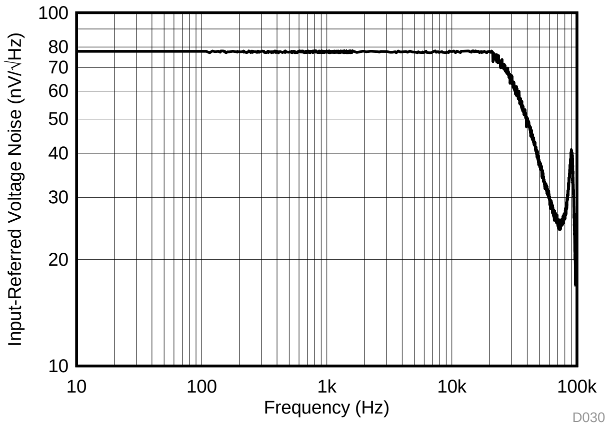


图 19. Input-Referred Voltage Noise vs Frequency

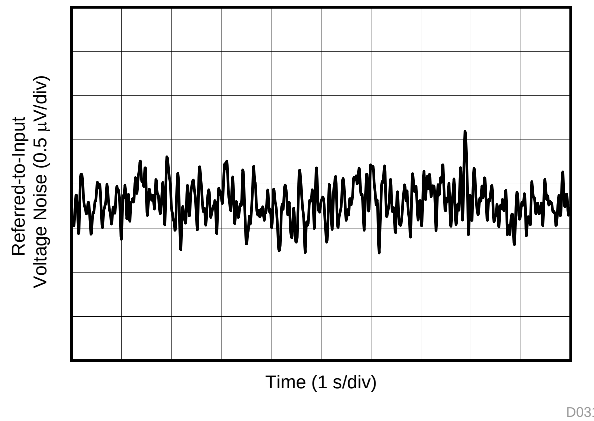
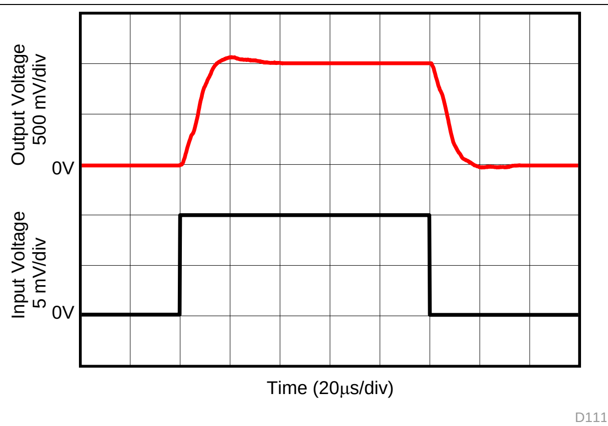


图 20. 0.1-Hz to 10-Hz Input-Referred Voltage Noise



V_S = 5.0 V, 10-mV_{PP} input step

图 21. Step Response

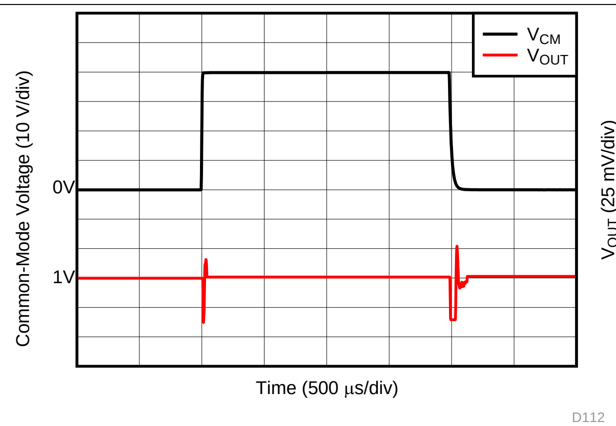


图 22. Common-Mode Voltage Transient Response

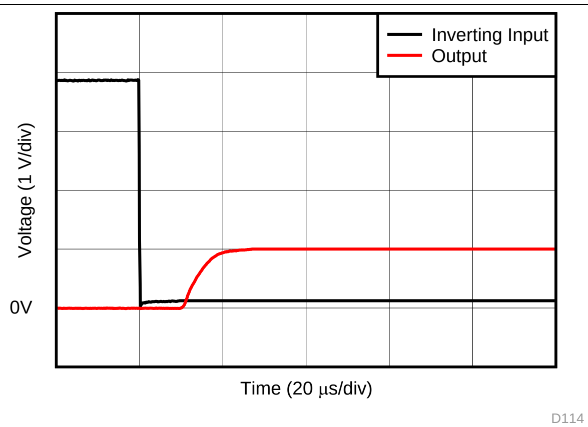
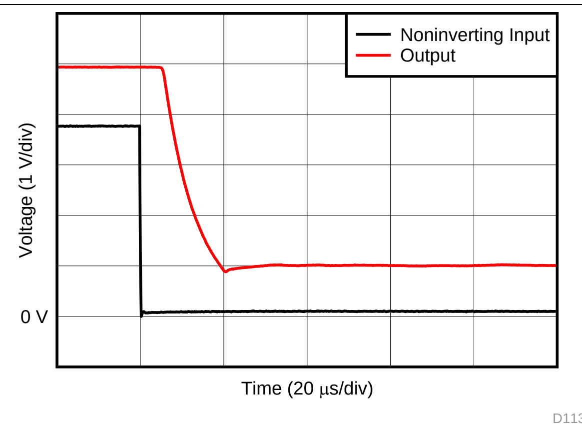


图 23. Inverting Differential Input Overload Recovery

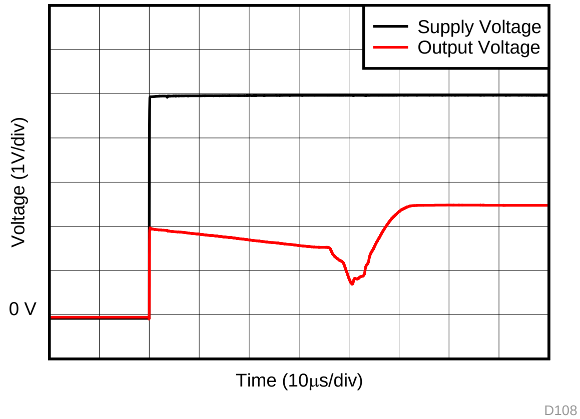


V_S = 5.0 V

图 24. Noninverting Differential Input Overload Recovery

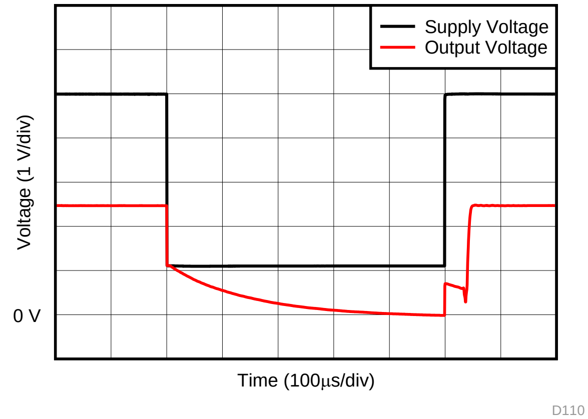
Typical Characteristics (接下页)

at T_A = 25°C, V_S = 1.8 V, V_{IN+} = 12 V, V_{ENABLE} = V_S, and all gain options (unless otherwise noted)



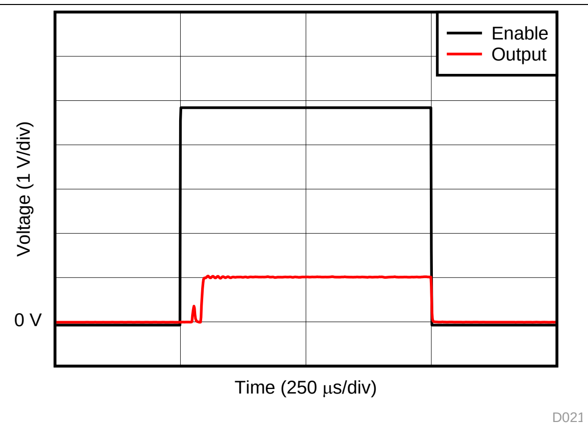
V_S = 5.0 V, A2 device

图 25. Start-Up Response



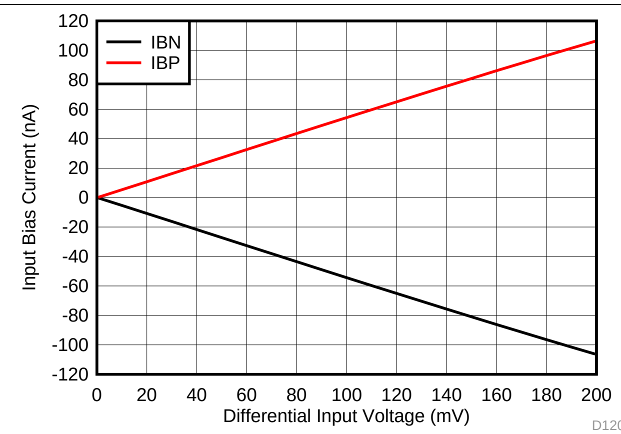
V_S = 5.0 V, A3 device

图 26. Brownout Recovery



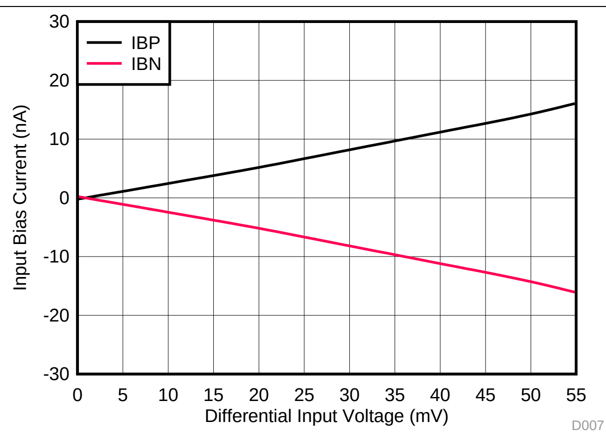
V_S = 5.0 V, A3 device

图 27. Enable and Disable Response



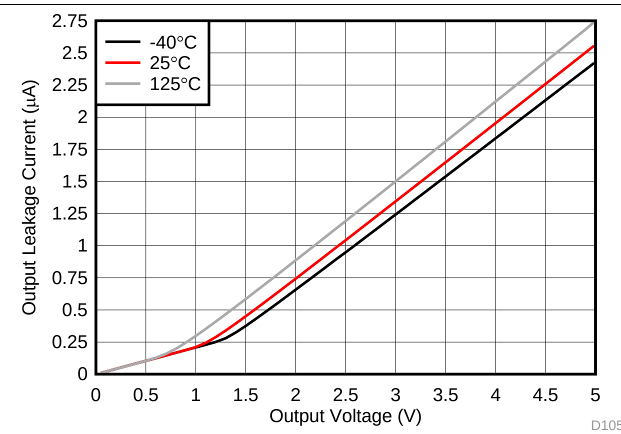
V_S = 5.0 V, A1 device

图 28. IB+ and IB– vs Differential Input Voltage



V_S = 5.0 V, A2, A3, A4, A5 devices

图 29. IB+ and IB– vs Differential Input Voltage

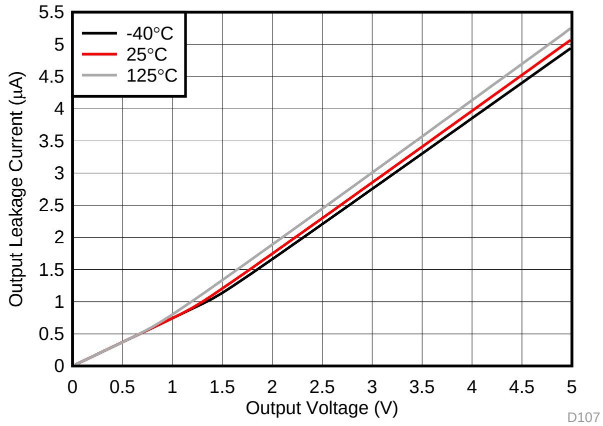


V_S = 5.0 V, V_{ENABLE} = 0 V, A1, A2, A3 devices

图 30. Output Leakage vs Output Voltage

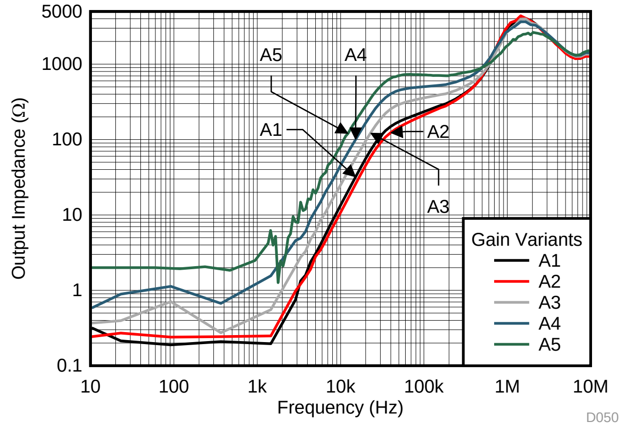
Typical Characteristics (接下页)

at T_A = 25°C, V_S = 1.8 V, V_{IN+} = 12 V, V_{ENABLE} = V_S, and all gain options (unless otherwise noted)



V_S = 5.0 V, V_{ENABLE} = 0 V, A4, A5 devices

图 31. Output Leakage vs Output Voltage



V_S = 5.0 V, V_{CM} = 0 V

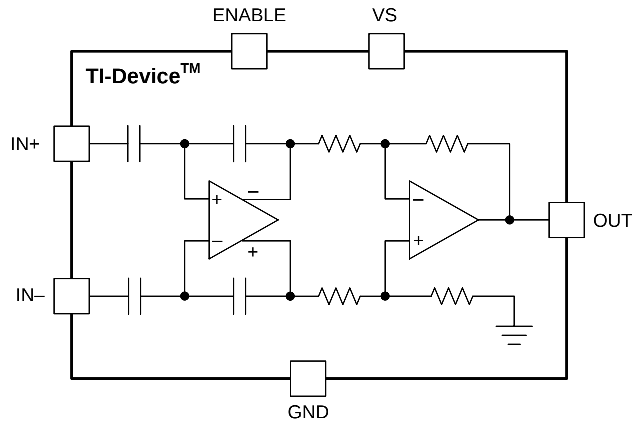
图 32. Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The INA191 is a low bias current, 40-V common-mode, current-sensing amplifier with an enable pin. When disabled, the output goes to a high-impedance state, and the supply current draw is reduced to less than 0.1 µA. The INA191 is intended for use in either low-side and high-side current-sensing configurations where high accuracy and low current consumption are required. The INA191 is a specially designed, current-sensing amplifier that accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage. Current can be measured on input voltage rails as high as 40 V, with a supply voltage as low as 1.7 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Precision Current Measurement

The INA191 provides accurate current measurements over a wide dynamic range. The high accuracy of the device is attributable to the low gain error and offset specifications. The offset voltage of the INA191 is less than 12 µV. In this case, the low offset improves the accuracy at light loads when V_{IN+} approaches V_{IN-}.

Another advantage of low offset is the ability to use a lower-value shunt resistor that reduces the power loss in the current-sense circuit, and improves the power efficiency of the end application.

The maximum gain error of the INA191 is specified to be within 0.25% for most gain options. As the sensed voltage becomes much larger than the offset voltage, the gain error becomes the dominant source of error in the current-sense measurement. When the device monitors currents near the full-scale output range, the total measurement error approaches the value of the gain error.

7.3.2 Low Input Bias Current

The INA191 is different from many current-sense amplifiers because this device offers very low input bias current. The low input bias current of the INA191 has three primary benefits.

The first benefit is the reduction of the current consumed by the device in both the enabled and disabled states. Classical current-sense amplifier topologies typically consume tens of microamps of current at the inputs. For these amplifiers, the input current is the result of the resistor network that sets the gain and additional current to bias the input amplifier. To reduce the bias current to near zero, the INA191 uses a capacitively coupled amplifier on the input stage, followed by a difference amplifier on the output stage.

The second benefit of low bias current is the ability to use input filters to reject high-frequency noise before the signal is amplified. In a traditional current-sense amplifier, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias currents, input filters have little effect on the measurement accuracy of the INA191.

The third benefit of low bias current is the ability to use a larger current-sense resistor. This ability allows the device to accurately monitor currents as low as 1 µA.

7.3.3 Low Quiescent Current With Output Enable

The device features low quiescent current (I_Q), while still providing sufficient small-signal bandwidth to be usable in most applications. The quiescent current of the INA191 is only 43 µA (typ), while providing a small-signal bandwidth of 35 kHz in a gain of 100. The low I_Q and good bandwidth allow the device to be used in many portable electronic systems without excessive drain on the battery. Because many applications only need to periodically monitor current, the INA191 features an enable pin that turns off the device until needed. When in the disabled state, the INA191 typically draws 10 nA of total supply current.

Feature Description (接下页)

7.3.4 High-Side and Low-Side Current Sensing

The INA191 supports input common-mode voltages from –0.2 V to +40 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S). The ability to operate with common-mode voltages greater or less than V_S allows the INA191 to be used in high-side and low-side current-sensing applications, as shown in 图 33.

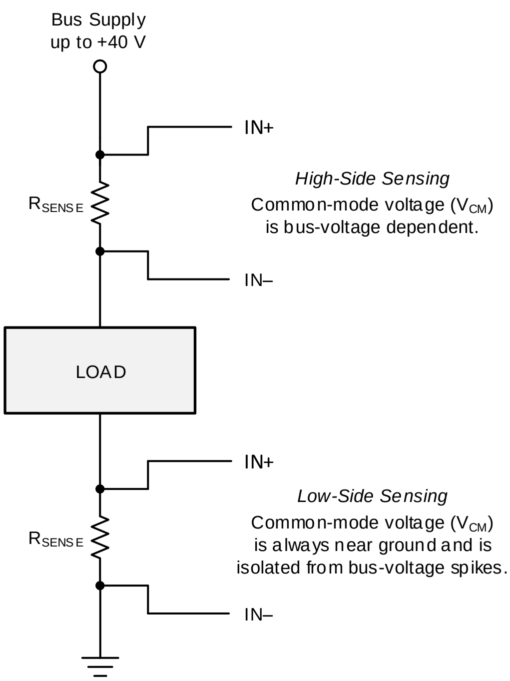


图 33. High-Side and Low-Side Sensing Connections

7.3.5 High Common-Mode Rejection

The INA191 uses a capacitively coupled amplifier on the front end. Therefore, dc common-mode voltages are blocked from downstream circuits, resulting in very high common-mode rejection. Typically, the common-mode rejection of the INA191 is approximately 150 dB. The ability to reject changes in the dc common-mode voltage allows the INA191 to monitor both high- and low-voltage rail currents with very little change in the offset voltage.

7.3.6 Rail-to-Rail Output Swing

The INA191 supports linear current-sensing operation with the output close to the supply rail and ground. The maximum specified output swing to the positive rail is V_S – 40 mV, and the maximum specified output swing to GND is only GND + 1 mV with –10 mV of differential overdrive. For cases where the sense current is zero, the swing to ground is determined by the zero current output specification. The value of the zero current output voltage can differ from the specified value depending on the common mode voltage, supply voltage, and output load. The close-to-rail output swing maximizes the usable output range, particularly when operating the device from a 1.8-V supply.

7.4 Device Functional Modes

7.4.1 Normal Operation

The INA191 is in normal operation when the following conditions are met:

- The power-supply voltage (V_S) is between 1.7 V and 5.5 V.
- The common-mode voltage (V_{CM}) is within the specified range of –0.2 V to +40 V.
- The maximum differential input signal times the gain is less than V_S minus the output voltage swing to V_S.
- The ENABLE pin is driven or connected to V_S.
- The minimum differential input signal times the gain is greater than the swing to GND (see the *Rail-to-Rail Output Swing* section).

During normal operation, this device produces an output voltage that is the *amplified* representation of the difference voltage from IN+ to IN–.

7.4.2 Input Differential Overload

If the differential input voltage ($V_{IN+} – V_{IN–}$) times gain exceeds the voltage swing specification, the INA191 drives the output as close as possible to the positive supply or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INA191 returns to the expected value approximately 40 µs after the fault condition is removed. When the differential voltage exceeds approximately 300 mV, the differential input impedance reduces to 3.3 kΩ, and results in a rapid increase in bias currents as the differential voltage increases. A 3.3-kΩ resistance exists between IN+ and IN– during a differential overload condition; therefore, currents flowing into the IN+ pin flow out of the IN– pin. An increase in bias currents during a input differential overload occurs even with the device is powered down. Input differential overloads less than the absolute maximum voltage rating do not damage the device or result in an output inversion.

7.4.3 Shutdown

The INA191 features an active-high ENABLE pin that shuts down the device when pulled to ground. When the device is shut down, the quiescent current is reduced to 10 nA (typ), the input bias currents are further reduced, and the output goes to a high-impedance state. When disabled, the low quiescent and input currents extend the battery lifetime when the current measurement is not needed. When the ENABLE pin is driven to the supply voltage, the device turns back on. When enabled, the typical output settling time is 130 µs.

The output of the INA191 goes to a high-impedance state when disabled; therefore, it is possible to connect multiple outputs of the INA191 together to a single ADC or measurement device, as shown in 图 34. When connected in this way, enable only one INA191 at a time, and make sure both devices have the same supply voltage.

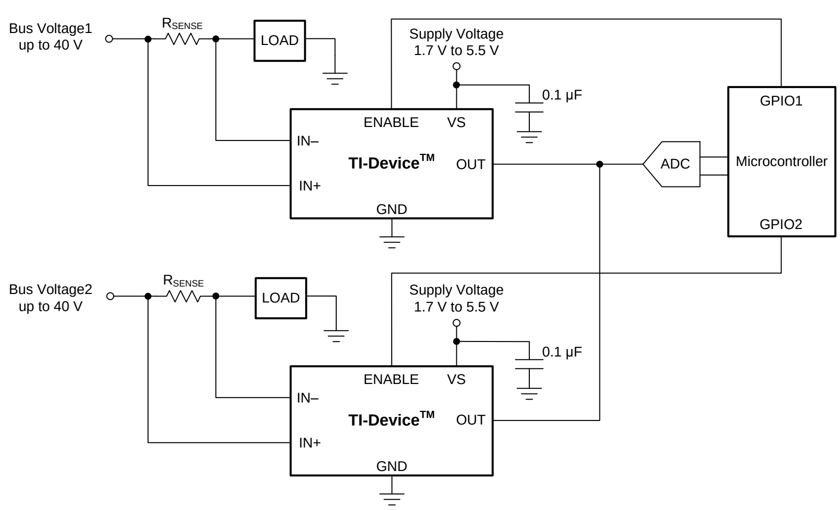


图 34. Multiplexing Multiple Devices With the ENABLE Pin

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA191 amplifies the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground.

8.1.1 Basic Connections

图 35 shows the basic connections of the INA191. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor. The ENABLE pin must be controlled externally or connected to VS if not used.

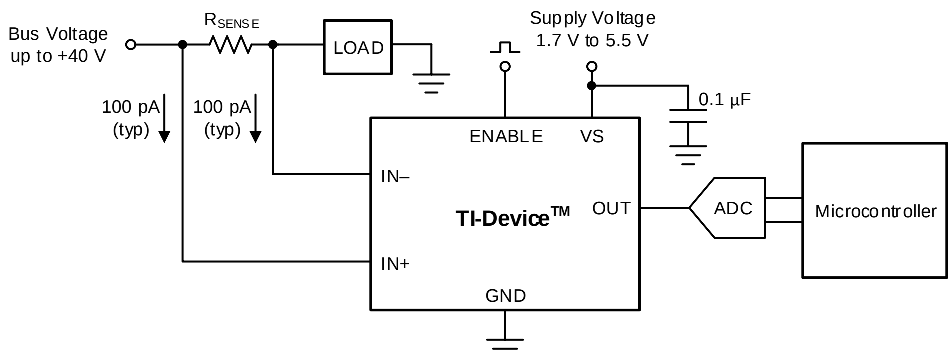


图 35. Basic Connections for the INA191

A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

Application Information (接下页)

8.1.2 R_{SENSE} and Device Gain Selection

The accuracy of any current-sense amplifier is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application because of the resistor size and maximum allowable power dissipation. 公式 1 gives the maximum value for the current-sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (1)$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current that flows through R_{SENSE}.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, V_S, and device swing-to-rail limitations. In order to make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. 公式 2 provides the maximum values of R_{SENSE} and GAIN to keep the device from hitting the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} \quad (2)$$

where:

- I_{MAX} is the maximum current that flows through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.

To avoid positive output swing limitations when selecting the value of R_{SENSE}, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device in order to avoid positive swing limitations.

The zero current output voltage places a limit on how small of a sense resistor can be used in a given application. 公式 3 provides the limit on the minimum size of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{ZL} \quad (3)$$

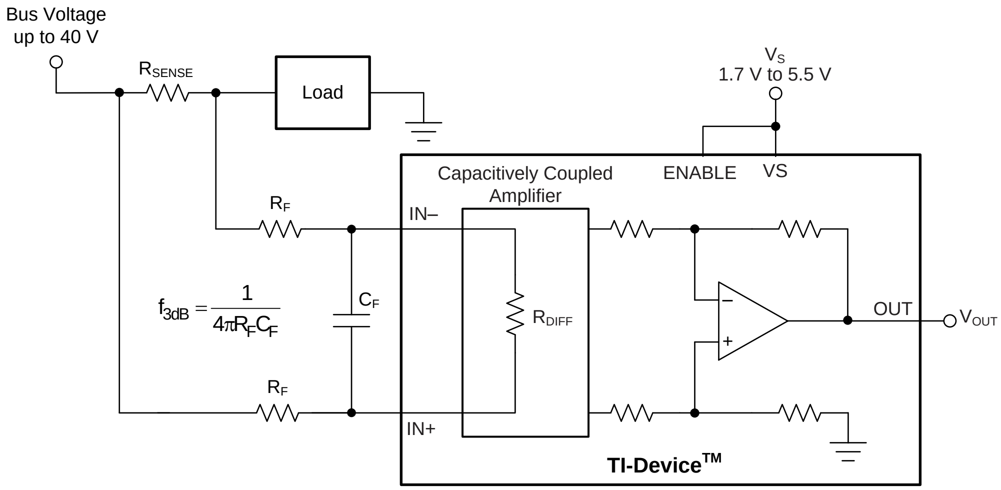
where:

- I_{MIN} is the minimum current flows through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{ZL} is the zero current output voltage of the device (see the *Rail-to-Rail Output Swing* section for more information).

Application Information (接下页)

8.1.3 Signal Conditioning

When performing accurate current measurements in noisy environments, the current-sensing signal is often filtered. The INA191 features low input bias currents. Therefore, it is possible to add a differential mode filter to the input without sacrificing the current-sense accuracy. Filtering at the input is advantageous because this action attenuates differential noise before the signal is amplified. 图 36 provides an example of how to use a filter on the input pins of the device.



$$f_{3dB} = \frac{1}{4\pi R_F C_F}$$

图 36. Filter at the Input Pins

The differential input impedance (R_{DIFF}) shown in 图 36 limits the maximum value for R_F. The value of R_{DIFF} is a function of the device temperature and gain option, as shown in 图 37.

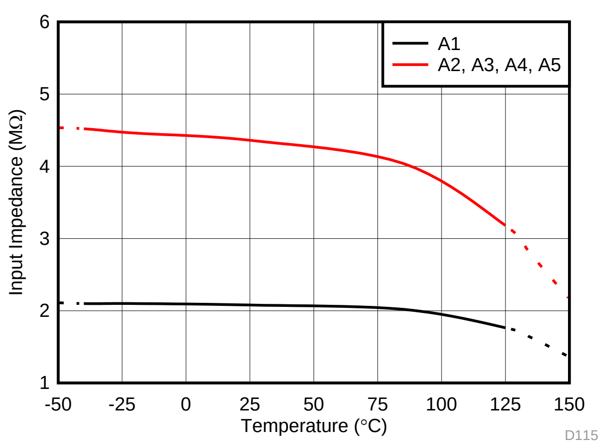


图 37. Differential Input Impedance vs Temperature

Application Information (接下页)

As the voltage drop across the sense resistor (V_{SENSE}) increases, the amount of voltage dropped across the input filter resistors (R_F) also increases. The increased voltage drop results in additional gain error. The error caused by these resistors is calculated by the resistor divider equation shown in 公式 4.

$$\text{Error}(\%) = \left(1 - \frac{R_{DIFF}}{R_{SENSE} + R_{DIFF} + (2 \times R_F)}\right) \times 100 \tag{4}$$

where:

- R_{SENSE} is the current sense resistor, as defined in 公式 1.
- R_{DIFF} is the differential input impedance.
- R_F is the added value of the series filter resistance.

The input stage of the INA191 uses a capacitive feedback amplifier topology in order to achieve high dc precision. As a result, periodic high-frequency shunt voltage (or current) transients of significant amplitude (10 mV or greater) and duration (hundreds of nanoseconds or greater) may be amplified by the INA191, even though the transients are greater than the device bandwidth. Use a differential input filter in these applications to minimize disturbances at the INA191 output.

The high input impedance and low bias current of the INA191 provides flexibility in the input filter design without impacting the accuracy of current measurement. For example, set R_F = 100 Ω and C_F = 22 nF to achieve a low-pass filter corner frequency of 36.2 kHz. These filter values significantly attenuate most unwanted high-frequency signals at the input without severely impacting the current-sensing bandwidth or precision. If a lower corner frequency is desired, increase the value of C_F.

Filtering the input filters out differential noise across the sense resistor. If high-frequency, common-mode noise is a concern, add an RC filter from the OUT pin to ground. The RC filter helps filter out both differential and common mode noise, as well as internally generated noise from the device. The value for the resistance of the RC filter is limited by the impedance of the load. Any current drawn by the load manifests as an external voltage drop from the INA191 OUT pin to the load input. To select the optimal values for the output filter, use 图 32 and see the *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT Application Report*

Application Information (接下页)

8.1.4 Common-Mode Voltage Transients

With a small amount of additional circuitry, the INA191 can be used in circuits subject to transients that exceed the absolute maximum voltage ratings. The most simple way to protect the inputs from negative transients is to add resistors in series to the IN– and IN+ pins. Use resistors that are 1 kΩ or less, and limit the current in the ESD structures to less than 5 mA. For example, using 1-kΩ resistors in series with the INA191 allows voltages as low as –5 V, while limiting the ESD current to less than 5 mA. If protection from high-voltage or more-negative, common-voltage transients is needed, use the circuits shown in 图 38 and 图 39. When implementing these circuits, use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode, as shown in 图 38. Keep these resistors as small as possible; most often, use around 100 Ω. Larger values can be used with an effect on gain that is discussed in the *Signal Conditioning* section. This circuit limits only short-term transients; therefore, many applications are satisfied with a 100-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

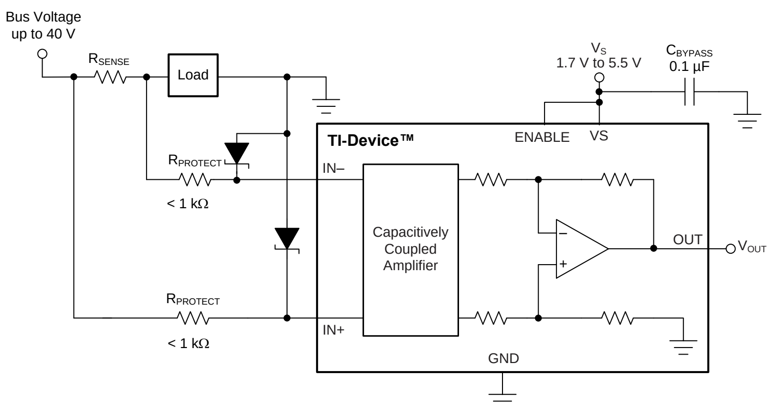


图 38. Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in 图 39. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in 图 38 and 图 39, the total board area required by the INA191 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an VSSOP-8 package.

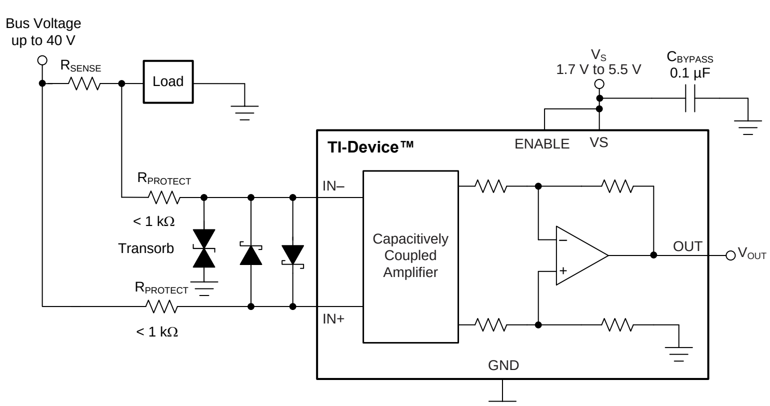


图 39. Transient Protection Using a Single Transzorb and Input Clamps

For more information, see *Current Shunt Monitor With Transient Robustness Reference Design*.

8.2 Typical Applications

8.2.1 Microamp Current Measurement

The low input bias current of the INA191 provides accurate monitoring of small-value currents. To accurately monitor currents in the microamp range, increase the value of the sense resistor to increase the sense voltage so that the error introduced by the offset voltage is small. The circuit configuration to monitor low-value currents is shown in 图 40. As a result of the differential input impedance of the INA191, limit the value of R_{SENSE} to 1 kΩ or less for best accuracy.

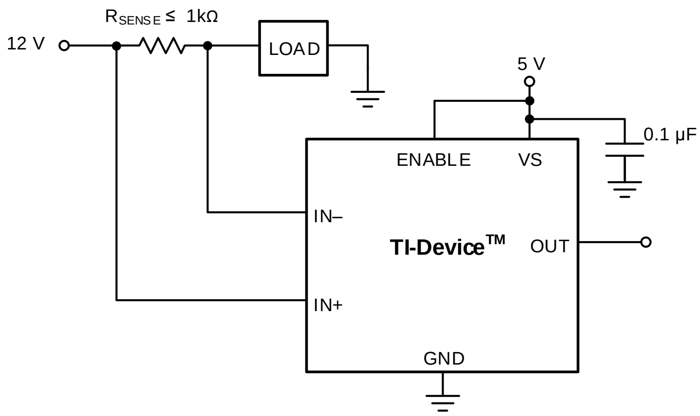


图 40. Measuring Microamp Currents

8.2.1.1 Design Requirements

The design requirements for the circuit shown in 图 40, are listed in 表 1

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	5 V
Bus supply rail (V_{CM})	12 V
Minimum sense current (I_{MIN})	1 µA
Maximum sense current (I_{MAX})	150 µA
Device gain (GAIN)	25 V/V

8.2.1.2 Detailed Design Procedure

The maximum value of the current-sense resistor is calculated based choice of gain, value of the maximum current the be sensed (I_{MAX}), and the power supply voltage (V_S). When operating at the maximum current, the output voltage must not exceed the positive output swing specification, V_{SP}. Using 公式 5, for the given design parameters the maximum value for R_{SENSE} is calculated to be 1.321 kΩ.

$$R_{SENSE} < \frac{V_{SP}}{I_{MAX} \times GAIN} \tag{5}$$

However, because this value exceeds the maximum recommended value for R_{SENSE}, a resistance value of 1 kΩ must be used. When operating at the minimum current value, I_{MIN} the output voltage must be greater than the swing to GND (V_{SN}), specification. For this example, the output voltage at the minimum current is calculated using 公式 6 to be 25 mV, which is greater than the value for V_{SN}.

$$V_{OUTMIN} = I_{MIN} \times R_{SENSE} \times GAIN \tag{6}$$

8.2.1.3 Application Curve

图 41 shows the output of the device when disabled and enabled while measuring a 40-µA load current. When disabled, the current draw from the device supply and inputs is less than 106 nA.

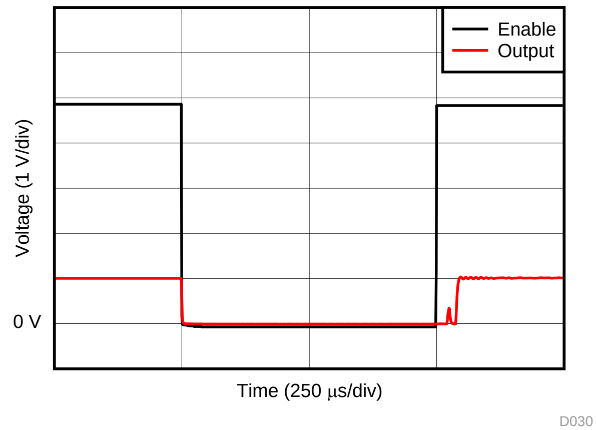


图 41. Output Disable and Enable Response

9 Power Supply Recommendations

The input circuitry of the INA191 accurately measures beyond the power-supply voltage, V_S. For example, V_S can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 40 V. However, the output voltage range of the OUT pin is limited by the voltage on the VS pin. The INA191 also withstands the full differential input signal range up to 40 V at the IN+ and IN– input pins, regardless of whether or not the device has power applied at the VS pin. There is no sequencing requirement for V_S and V_{IN+} or $V_{IN–}$.

10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. To compensate for noisy or high-impedance power supplies, add more decoupling capacitance.
- When routing the connections from the current-sense resistor to the device, keep the trace lengths as short as possible. Place input filter capacitor C_F as close as possible to the input pins of the device.

10.2 Layout Example

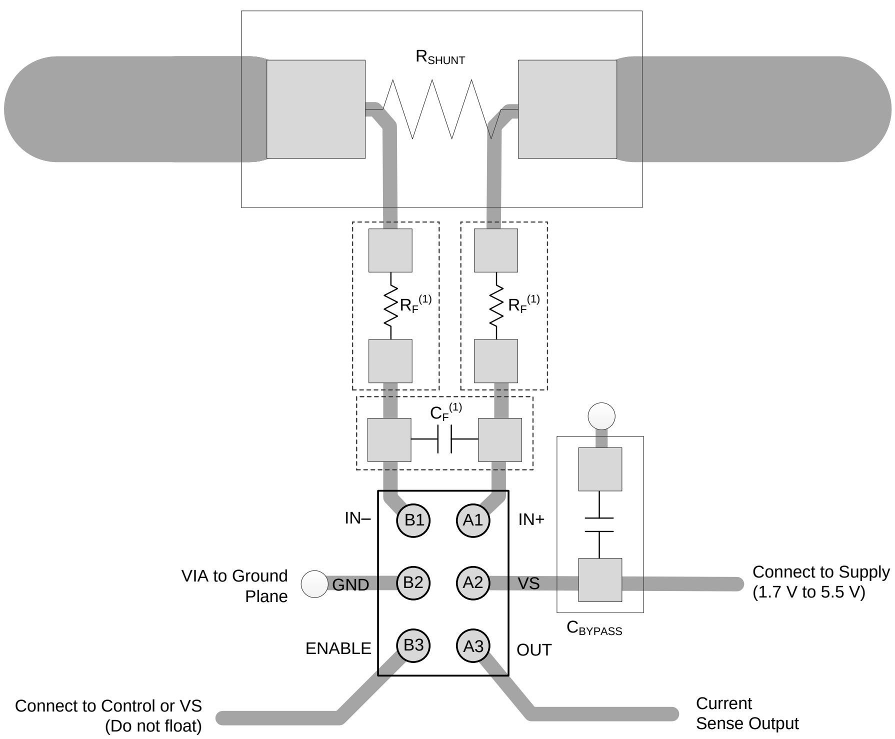


图 42. Recommended Layout DSBGA (YFD) Package

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

德州仪器 (TI)，《*INA191EVM* 用户指南》

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

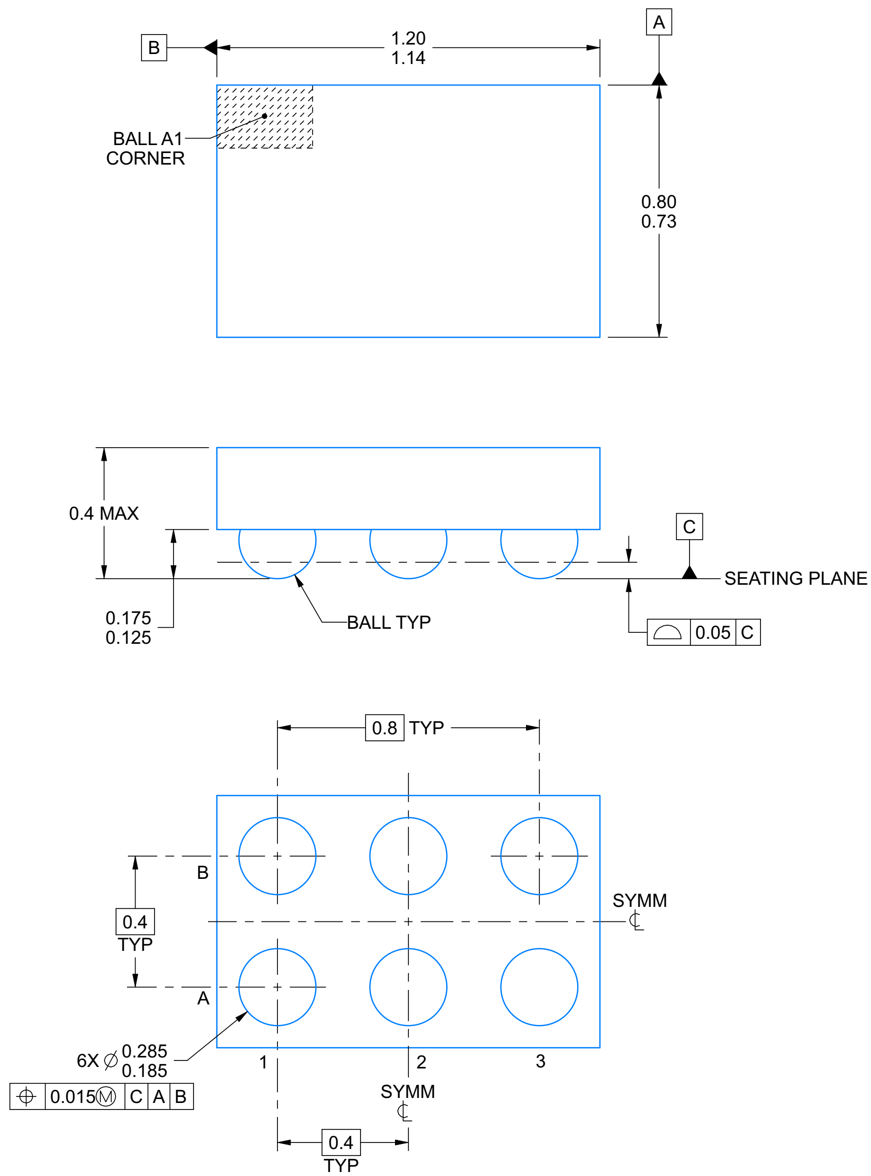
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

INA191AxIYFD
YFD0006-C02

PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

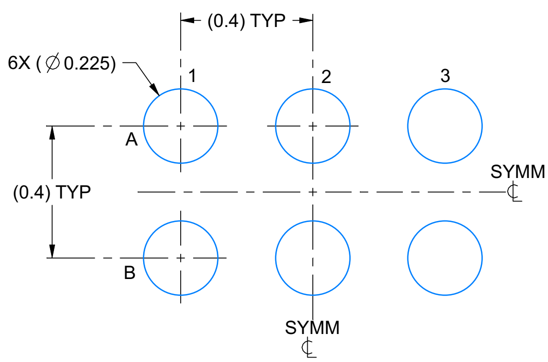
INA191AxIYFD

YFD0006-C02

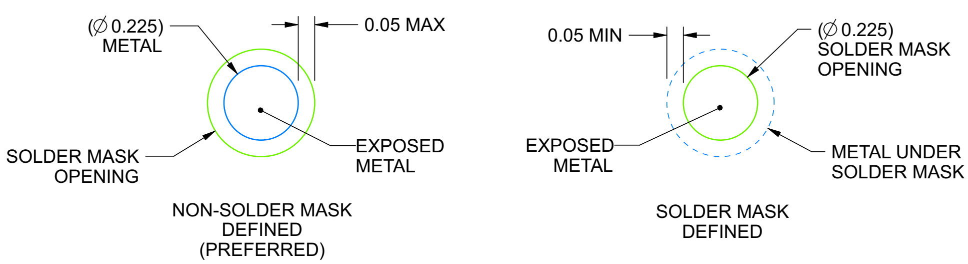
EXAMPLE BOARD LAYOUT

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4224626/B 02/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

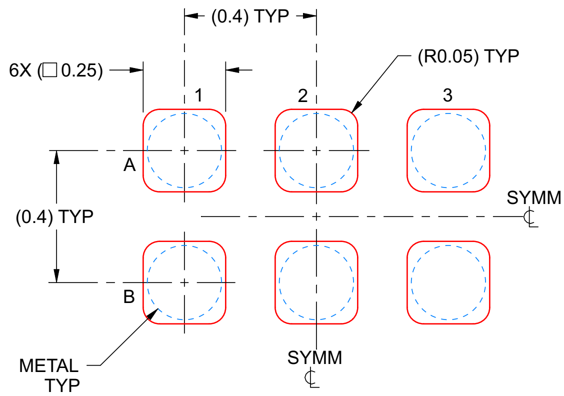
www.ti.com

INA191AxIYFD
YFD0006-C02

EXAMPLE STENCIL DESIGN

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4224626/B 02/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA191A1IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1E3	Samples
INA191A2IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1E2	Samples
INA191A3IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1E4	Samples
INA191A4IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1E5	Samples
INA191A5IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1E6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

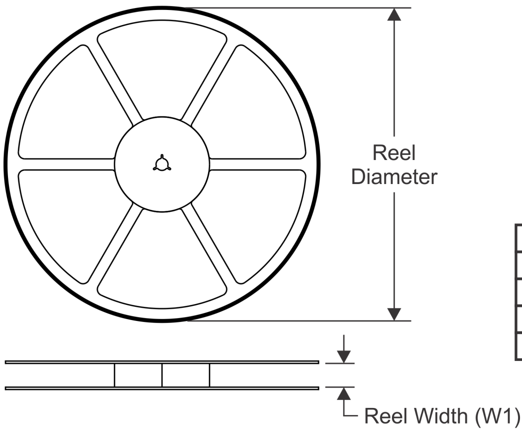
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

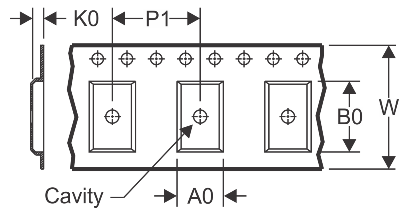
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

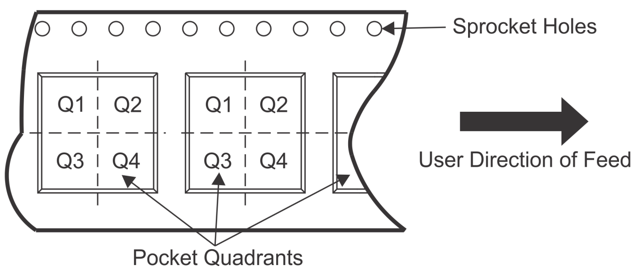


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

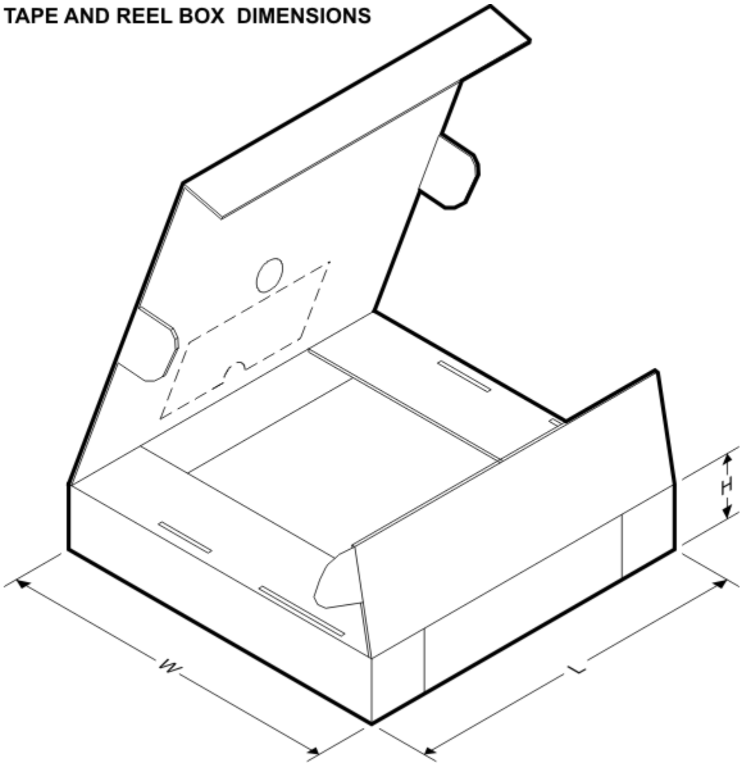
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA191A1IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA191A1IYFDR	DSBGA	YFD	6	3000	180.0	8.4	0.86	1.26	0.56	4.0	8.0	Q2
INA191A2IYFDR	DSBGA	YFD	6	3000	180.0	8.4	0.86	1.26	0.56	4.0	8.0	Q2
INA191A2IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA191A3IYFDR	DSBGA	YFD	6	3000	180.0	8.4	0.86	1.26	0.56	4.0	8.0	Q2
INA191A4IYFDR	DSBGA	YFD	6	3000	180.0	8.4	0.86	1.26	0.56	4.0	8.0	Q2
INA191A5IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA191A5IYFDR	DSBGA	YFD	6	3000	180.0	8.4	0.86	1.26	0.56	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA191A1IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA191A1IYFDR	DSBGA	YFD	6	3000	182.0	182.0	20.0
INA191A2IYFDR	DSBGA	YFD	6	3000	182.0	182.0	20.0
INA191A2IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA191A3IYFDR	DSBGA	YFD	6	3000	182.0	182.0	20.0
INA191A4IYFDR	DSBGA	YFD	6	3000	182.0	182.0	20.0
INA191A5IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA191A5IYFDR	DSBGA	YFD	6	3000	182.0	182.0	20.0

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122