

LMP860x、LMP860x-Q1 60V、双向、低侧或高侧、电压输出 电流感测放大器

1 特性

- 增益 = 20x (LMP8601 和 LMP8601-Q1)
- 增益 = 50x (LMP8602 和 LMP8602-Q1)
- 增益 = 100x (LMP8603 和 LMP8603-Q1)
- TCV_{OS} : 10 μ V/ $^{\circ}$ C (最大值)
- 共模抑制比 (CMRR): 90dB (最小值)
- 输入偏移电压: 1mV (典型值)
- $V_S = 3.3V$ 时的共模电压范围 (CMVR): -4V 至 27V
- $V_S = 5V$ 时的 CMVR: -22V 至 60V
- 单电源双向供电运行
- 所有最小和最大限值完全经过测试
- 符合汽车类应用的 Q1 器件
- Q1 器件具有符合 ACE-Q100 标准的下列结果:
 - 器件温度等级 1: 环境运行温度范围为 -40 $^{\circ}$ C 至 125 $^{\circ}$ C
 - 器件温度等级 0: -40 $^{\circ}$ C 至 150 $^{\circ}$ C (仅限 LMP8601EDRQ1)
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 2 (输入电流为 3A)
 - 器件带电器件模型 (CDM) ESD 分类等级 C6
 - 器件机器模型 (MM) ESD 分类等级 M2

2 应用

- 高侧和低侧驱动器配置电流感测
- 双向电流测量
- 电压转换的电流循环
- 汽车喷油控制
- 传动控制
- 电动助力转向
- 电池管理系统

3 说明

LMP8601、LMP8602、LMP8603 (LMP860x) 和 LMP8601-Q1、LMP8602-Q1、LMP8603-Q1 (LMP860x-Q1) 器件均为增益固定的精密电流感测放大器 (也称分流监测计)。当由 5V 或 3.3V 单电源供电时, 输入共模电压范围分别为 -22V 至 +60V 和 -4V 至 +27V。LMP860x 和 LMP860x-Q1 是单向和双向电流感测应用的理想元件。

此类器件的精密增益分别为 20x (LMP8601 和 LMP8601-Q1)、50x (LMP8602 和 LMP8602-Q1) 和 100x (LMP8603 和 LMP8603-Q1), 足以满足多数目标应用将模数转换器 (ADC) 驱动至满量程值的要求。固定增益在两个独立级中实现, 包括增益为 10x 的前置放大器和增益为 2x (LMP8601 和 LMP8601-Q1)、5x (LMP8602 和 LMP8602-Q1) 或 10x (LMP8603 和 LMP8603-Q1) 的输出级缓冲放大器。连接两级的路径通过两引脚引出, 支持选择使用附加滤波器网络或修改增益。

偏移输入引脚允许此类器件执行单向或双向单电源电压电流感测。

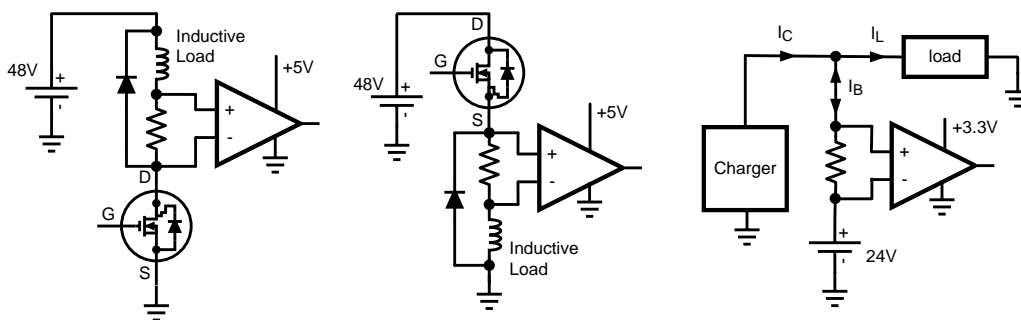
LMP860x-Q1 器件采用增强型制造与支持工艺, 适用于汽车市场, 符合 AEC-Q100 标准。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|-----------------------|-----------|-----------------|
| LMP860x | SOIC (8) | 4.90mm x 3.91mm |
| LMP860x-Q1 | | |
| LMP8602、LMP8603 | VSSOP (8) | 3.00mm x 3.00mm |
| LMP8602-Q1、LMP8603-Q1 | | |

(1) 要了解所有可用封装, 请参见数据表末尾的封装选项附录。

典型应用



目录

| | | | |
|--|-----------|---|-----------|
| 1 特性 | 1 | 7.3 Feature Description | 19 |
| 2 应用 | 1 | 7.4 Device Functional Modes | 22 |
| 3 说明 | 1 | 8 Application and Implementation | 26 |
| 4 修订历史记录 | 2 | 8.1 Application Information | 26 |
| 5 Pin Configuration and Functions | 3 | 8.2 Typical Applications | 26 |
| 6 Specifications | 4 | 9 Power Supply Recommendations | 31 |
| 6.1 Absolute Maximum Ratings | 4 | 10 Layout | 31 |
| 6.2 ESD Ratings: LMP860x | 4 | 10.1 Layout Guidelines | 31 |
| 6.3 ESD Ratings: LMP860x-Q1 | 4 | 10.2 Layout Example | 31 |
| 6.4 Recommended Operating Conditions | 4 | 11 器件和文档支持 | 32 |
| 6.5 Thermal Information | 5 | 11.1 器件支持 | 32 |
| 6.6 Electrical Characteristics: $V_S = 3.3\text{ V}$ | 5 | 11.2 相关链接 | 32 |
| 6.7 Electrical Characteristics: $V_S = 5\text{ V}$ | 7 | 11.3 社区资源 | 32 |
| 6.8 Typical Characteristics | 9 | 11.4 商标 | 32 |
| 7 Detailed Description | 18 | 11.5 静电放电警告 | 32 |
| 7.1 Overview | 18 | 11.6 Glossary | 32 |
| 7.2 Functional Block Diagram | 18 | 12 机械、封装和可订购信息 | 32 |

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Revision G (July 2015) to Revision H | Page |
|---|------|
| • 已添加新温度等级 0 型号 LMP8601-Q1 | 1 |
| • 已将 LMP8602、LMP8602-Q1、LMP8603 和 LMP8603-Q1 器件及相关信息添加至数据表 | 1 |
| • 已更改特性要点 | 1 |
| • 已更改 说明部分 | 1 |
| • Added new values to <i>Thermal Information</i> table | 5 |
| • Changed $R_{\theta JA}$ value in <i>Thermal Information</i> table | 5 |
| • Deleted previous Note 1 from <i>Electrical Characteristics</i> tables | 5 |
| • Changed all AV1 to K1 throughout data sheet for consistency | 6 |
| • Changed all AV2 to K2 throughout data sheet for consistency | 6 |
| • Deleted previous Note 1 from <i>Electrical Characteristics</i> tables | 7 |
| • 已删除相关文档部分；SNOSB36 数据表内容现与本数据表合并 | 32 |

| Changes from Revision F (January 2014) to Revision G | Page |
|---|------|
| • 已添加 ESD 额定值表以及引脚配置和功能，特性描述，器件功能模式，应用和实施，电源相关建议，布局，器件和文档支持以及机械、封装和可订购信息部分。 | 1 |

| Changes from Revision E (March 2013) to Revision F | Page |
|--|------|
| • Added four typical curves | 17 |

| Changes from Revision D (October 2009) to Revision E | Page |
|--|------|
| • Changed layout of National Data Sheet to TI format | 30 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE | DESCRIPTION |
|----------------|-----|------|---|
| NAME | NO. | | |
| A1 | 3 | O | Preamplifier output |
| A2 | 4 | I | Input from the external filter network and, or A1 |
| GND | 2 | P | Power ground |
| +IN | 8 | I | Positive input |
| -IN | 1 | I | Negative input |
| OFFSET | 7 | I | DC offset for bidirectional signals |
| OUT | 5 | O | Single-ended output |
| V _s | 6 | P | Positive supply voltage |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|---------------------------------|----------------------|-----------|------|
| Supply voltage (V _S – GND) | | –0.3 | 6 | V |
| Continuous input voltage (–IN and +IN) | | –22 | 60 | V |
| Transient (400 ms) | | –25 | 65 | V |
| Maximum voltage at A1, A2, OFFSET and OUT pins | | V _S + 0.3 | GND – 0.3 | V |
| Operating temperature, T _A | LMP8601EDRQ1 only | –40 | 150 | °C |
| | All other devices | –40 | 125 | |
| Junction temperature ⁽²⁾ | | –40 | 150 | °C |
| Mounting temperature | Infrared or convection (20 sec) | | 235 | °C |
| | Wave soldering lead (10 sec) | | 260 | |
| Storage temperature, T _{stg} | | –65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{J(MAX)}, R_{θJA}, and the ambient temperature, T_A. The maximum allowable power dissipation P_{DMAX} = (T_{J(MAX)} – T_A) / R_{θJA} or the number given in *Absolute Maximum Ratings*, whichever is lower.

6.2 ESD Ratings: LMP860x

| | | | VALUE | UNIT | |
|--------------------|-------------------------|--|-------------------------|-------|---|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | All pins except 1 and 8 | ±2000 | V |
| | | | Pins 1 and 8 | ±4000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | | ±1000 | |
| | | Machine model | | ±200 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LMP860x-Q1

| | | | VALUE | UNIT | |
|--------------------|-------------------------|---|-------------------------|-------|---|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins except 1 and 8 | ±2000 | V |
| | | | Pins 1 and 8 | ±4000 | |
| | | Charged-device model (CDM), per AEC Q100-011 | | ±1000 | |
| | | Machine model | | ±200 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--|-------------------|-----|----------------|------|
| Supply voltage (V _S – GND) | | 3 | 5.5 | V |
| OFFSET voltage (Pin 7) | | 0 | V _S | V |
| Operating temperature, T _A ⁽¹⁾ | LMP8601EDRQ1 only | –40 | 150 | °C |
| | All other devices | –40 | 125 | |

- (1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{J(MAX)}, R_{θJA}, and the ambient temperature, T_A. The maximum allowable power dissipation P_{DMAX} = (T_{J(MAX)} – T_A) / R_{θJA} or the number given in *Absolute Maximum Ratings*, whichever is lower.

6.5 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LMP860x, LMP860x-Q1 | LMP8602, LMP8602-Q1, LMP8603, LMP8603-Q1 | UNIT |
|-------------------------------|---|------------------------|---|------|
| | | D (SOIC) | DGK (VSSOP) | |
| | | 8 PINS | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽²⁾ | 113.1 | 171.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 57.3 | 64.1 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 53.5 | 91.1 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 11.1 | 9.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 53.0 | 89.7 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{J(MAX)}, R_{θJA}, and the ambient temperature, T_A. The maximum allowable power dissipation P_{DMAX} = (T_{J(MAX)} – T_A) / R_{θJA} or the number given in *Absolute Maximum Ratings*, whichever is lower.

6.6 Electrical Characteristics: V_S = 3.3 V

at T_A = 25°C, V_S = 3.3 V, GND = 0 V, –4 V ≤ V_{CM} ≤ 27 V, R_L = ∞, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT | |
|--|---|--|--------------------|--------------------|-------------------|-----|
| OVERALL PERFORMANCE (FROM -IN (PIN 1) AND +IN (PIN 8) TO OUT (PIN 5) WITH PINS A1 (PIN 3) AND A2 (PIN 4) CONNECTED) | | | | | | |
| I _S | Supply current | 1 | | | mA | |
| | Over full temperature range | 0.6 | | 1.3 | | |
| A _V | Total gain | LMP8601, LMP8601-Q1 | 19.9 | 20 | 20.1 | V/V |
| | | LMP8602, LMP8602-Q1 | 49.75 | 50 | 50.25 | |
| | | LMP8603, LMP8603-Q1 | 99.5 | 100 | 100.5 | |
| | Gain Drift ⁽³⁾ | Over full temperature range | –2.7 | ±20 | ppm/°C | |
| SR | Slew rate ⁽⁴⁾ | V _{IN} = ±0.165 V | 0.4 | 0.7 | V/μs | |
| BW | Bandwidth | | 50 | 60 | kHz | |
| V _{OS} | Input offset voltage | V _{CM} = V _S / 2 | 0.15 | ±1 | mV | |
| TCV _{OS} | Input offset voltage drift ⁽⁵⁾ | Over full temperature range | 2 | ±10 | μV/°C | |
| e _n | Input-referred voltage noise | 0.1 Hz - 10 Hz, 6 sigma | 16.4 | | μV _{P-P} | |
| | | Spectral density, 1 kHz | 830 | | nV/√Hz | |
| PSRR | Power-supply rejection ratio | 3.0 V ≤ V _S ≤ 3.6 V, DC, V _{CM} = V _S /2 | 86 | | dB | |
| | | Over full temperature range | 70 | | | |
| Midscale offset scaling accuracy | Input referred | LMP8601, LMP8601-Q1 | ±0.15% | ±0.5% | mV | |
| | | LMP8602, LMP8602-Q1 | ±0.25% | ±1% | | |
| | Input referred | LMP8601, LMP8601-Q1 | ±0.33 | | mV | |
| | | LMP8602, LMP8602-Q1 | ±0.45% | ±1.5% | | |
| Input referred | LMP8601, LMP8601-Q1 | ±0.248 | | mV | | |
| | LMP8602, LMP8602-Q1 | ±0.248 | | | | |

- (1) Data sheet min and max limits are specified by test.
- (2) Typical values represent the most likely parameter norms at T_A = 25°C, and at the *Recommended Operation Conditions* at the time of product characterization.
- (3) Both the gain of preamplifier K1 and the gain of buffer amplifier K2 are measured individually. The overall gain of both amplifiers (A_V) is also measured to assure the gain of all parts is always within the A_V limits.
- (4) Slew rate is the average of the rising and falling slew rates.
- (5) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Electrical Characteristics: $V_S = 3.3\text{ V}$ (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{ V}$, $\text{GND} = 0\text{ V}$, $-4\text{ V} \leq V_{\text{CM}} \leq 27\text{ V}$, $R_L = \infty$, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|--|---|---|-----------------------------|-----------------------------|--------------------|--------------------|-----------------------|
| PREAMPLIFIER (FROM INPUT PINS -IN, (PIN 1) AND +IN (PIN 8) TO A1 (PIN 3)) | | | | | | | |
| R_{CM} | Input impedance common mode | $-4\text{ V} \leq V_{\text{CM}} \leq 27\text{ V}$ | | | 295 | | k Ω |
| | | | Over full temperature range | 250 | 350 | | |
| R_{DM} | Input impedance differential mode | $-4\text{ V} \leq V_{\text{CM}} \leq 27\text{ V}$ | | | 590 | | k Ω |
| | | | Over full temperature range | 500 | 700 | | |
| V_{OS} | Input offset voltage | $V_{\text{CM}} = V_S / 2$ | | | ± 0.15 | ± 1 | mV |
| DC CMRR | DC common-mode rejection ratio | $-2\text{ V} \leq V_{\text{CM}} \leq 24\text{ V}$ | | | 96 | | dB |
| | | | Over full temperature range | 86 | | | |
| AC CMRR | AC common-mode rejection ratio ⁽⁶⁾ | $f = 1\text{ kHz}$ | | 80 | 94 | | dB |
| | | $f = 10\text{ kHz}$ | | | 85 | | |
| CMVR | Input common-mode voltage range | for 80-dB CMRR | Over full temperature range | -4 | | 27 | V |
| K1 | Preamplifier gain ⁽³⁾ | | | 9.95 | 10.0 | 10.05 | V/V |
| $R_{\text{F-INT}}$ | Output impedance filter resistor | | | | 100 | | k Ω |
| | | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | | 99 | | 101 | |
| | | $-40^\circ\text{C} \leq T_A \leq 150^\circ\text{C}$, LMP8601EDRQ1 only | | 97 | | 103 | |
| $\text{TCR}_{\text{F-INT}}$ | Output impedance filter resistor drift | Over full temperature range | | | ± 5 | ± 50 | ppm/ $^\circ\text{C}$ |
| A1 V_{OUT} | A1 output voltage swing | V_{OL} , $R_L = \infty$ | | | 2 | | mV |
| | | | Over full temperature range | | 10 | | |
| | | V_{OH} , $R_L = \infty$ | | | 3.25 | | V |
| | | | Over full temperature range | 3.2 | | | |
| OUTPUT BUFFER (FROM A2 (PIN 4) TO OUT (PIN 5)) | | | | | | | |
| V_{OS} | Input offset voltage | $0\text{ V} \leq V_{\text{CM}} \leq V_S$ | | -2 | ± 0.5 | 2 | mV |
| | | | Over full temperature range | -2.5 | | 2.5 | |
| K2 | Output buffer gain ⁽³⁾ | LMP8601, LMP8601-Q1 | | 1.99 | 2 | 2.01 | V/V |
| | | LMP8602, LMP8602-Q1 | | 4.975 | 5 | 5.025 | |
| | | LMP8603, LMP8603-Q1 | | 9.95 | 10 | 10.05 | |
| I_{B} | Input bias current of A2 ⁽⁷⁾ , | | | | -40 | | fA |
| | | Over full temperature range | | | | ± 20 | nA |
| A2 V_{OUT} | A2 output voltage swing ⁽⁸⁾ ⁽⁹⁾ | V_{OL} , $R_L = 100\text{ k}\Omega$ | LMP8601, LMP8601-Q1, | | 4 | | mV |
| | | | | Over full temperature range | | 20 | |
| | | | LMP8602, LMP8602-Q1 | | 10 | | |
| | | | | Over full temperature range | | 40 | |
| | | LMP8603, LMP8603-Q1 | | 10 | | | |
| | | | Over full temperature range | | 80 | | |
| V_{OH} , $R_L = 100\text{ k}\Omega$ | | | 3.29 | | V | | |
| | Over full temperature range | 3.28 | | | | | |
| I_{SC} | Output short-circuit current ⁽¹⁰⁾ | Sourcing, $V_{\text{IN}} = V_S$, $V_{\text{OUT}} = \text{GND}$ | | -25 | -38 | -60 | mA |
| | | Sinking, $V_{\text{IN}} = \text{GND}$, $V_{\text{OUT}} = V_S$ | | 30 | 46 | 65 | |

(6) AC common-mode signal is a $5\text{-}V_{\text{PP}}$ sine-wave (0 V to 5 V) at the given frequency.

(7) Positive current corresponds to current flowing into the device.

(8) For this test input is driven from A1 stage.

(9) For V_{OL} , R_L is connected to V_S and for V_{OH} , R_L is connected to GND.

(10) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

6.7 Electrical Characteristics: $V_S = 5\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22\text{ V} \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT | |
|--|---|---|--------------------|--------------------|--------------------|------------------------------|-----------|
| OVERALL PERFORMANCE (FROM -IN (PIN 1) AND +IN (PIN 8) TO OUT (PIN 5) WITH PINS A1 (PIN 3) AND A2 (PIN 4) CONNECTED) | | | | | | | |
| I_S | Supply current | | 1.1 | | | mA | |
| | | Over full temperature range | 0.7 | | 1.5 | | |
| A_V | Total gain ⁽³⁾ | LMP8601, LMP8601-Q1 | 19.9 | 20 | 20.1 | V/V | |
| | | LMP8602, LMP8602-Q1 | 49.75 | 50 | 50.25 | | |
| | | LMP8603, LMP8603-Q1 | 99.5 | 100 | 100.5 | | |
| | Gain drift | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | | -2.8 | ± 20 | ppm/ $^\circ\text{C}$ | |
| SR | Slew rate ⁽⁴⁾ | $V_{\text{IN}} = \pm 0.25\text{ V}$ | 0.6 | 0.83 | | V/ μs | |
| BW | Bandwidth | | 50 | 60 | | kHz | |
| V_{OS} | Input offset voltage | | | 0.15 | ± 1 | mV | |
| TCV_{OS} | Input offset voltage drift ⁽⁵⁾ | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | | 2 | ± 10 | $\mu\text{V}/^\circ\text{C}$ | |
| e_N | Input-referred voltage noise | 0.1 Hz - 10 Hz, 6 sigma | | 17.5 | | $\mu\text{V}_{\text{P-P}}$ | |
| | | Spectral density, 1 kHz | | 890 | | nV/ $\sqrt{\text{Hz}}$ | |
| PSRR | Power-supply rejection ratio | $4.5\text{ V} \leq V_S \leq 5.5\text{ V}$, DC | | 90 | | dB | |
| | | Over full temperature range | 70 | | | | |
| Midscale offset scaling accuracy | | LMP8601, LMP8601-Q1 | Input-referred | $\pm 0.15\%$ | $\pm 0.5\%$ | mV | |
| | | | | ± 0.625 | $\pm 0.25\%$ | | $\pm 1\%$ |
| | | LMP8602, LMP8602-Q1 | Input-referred | ± 0.50 | $\pm 0.45\%$ | $\pm 1.5\%$ | mV |
| | | | | ± 0.375 | ± 0.375 | | |

- (1) Data sheet min and max limits are specified by test.
- (2) Typical values represent the most likely parameter norms at $T_A = 25^\circ\text{C}$, and at the *Recommended Operation Conditions* at the time of product characterization.
- (3) Both the gain of preamplifier K1 and the gain of buffer amplifier K2 are measured individually. The overall gain of both amplifiers (A_V) is also measured to assure the gain of all parts is always within the A_V limits.
- (4) Slew rate is the average of the rising and falling slew rates.
- (5) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Electrical Characteristics: $V_S = 5\text{ V}$ (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22\text{ V} \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT | |
|---|---|---|-----------------------------|-----------------------------|--------------------|-----------------------|-----|
| PREAMPLIFIER (FROM INPUT PINS -IN (PIN 1) AND +IN (PIN 8) TO A1 (PIN 3)) | | | | | | | |
| R_{CM} | Input impedance, common mode | $0\text{ V} \leq V_{\text{CM}} \leq 60\text{ V}$ | | 295 | | k Ω | |
| | | | Over full temperature range | 250 | 350 | | |
| R_{DM} | Input impedance, differential mode | $-20\text{ V} \leq V_{\text{CM}} \leq 0\text{ V}$ | | 193 | | k Ω | |
| | | | Over full temperature range | 165 | 250 | | |
| R_{DM} | Input impedance, differential mode | $0\text{ V} \leq V_{\text{CM}} \leq 60\text{ V}$ | | 590 | | k Ω | |
| | | | Over full temperature range | 500 | 700 | | |
| R_{DM} | Input impedance, differential mode | $-20\text{ V} \leq V_{\text{CM}} \leq 0\text{ V}$ | | 386 | | k Ω | |
| | | | Over full temperature range | 300 | 500 | | |
| V_{OS} | Input offset voltage | $V_{\text{CM}} = V_S / 2$ | | ± 0.15 | ± 1 | mV | |
| DC CMRR | DC common-mode rejection ratio | $-20\text{ V} \leq V_{\text{CM}} \leq 60\text{ V}$ | | 105 | | dB | |
| | | | | Over full temperature range | 90 | | |
| AC CMRR | AC common-mode rejection ratio ⁽⁶⁾ | $f = 1\text{ kHz}$ $f = 10\text{ kHz}$ | | 80 | 96 | dB | |
| | | | | | 83 | | |
| CMVR | Input common-mode voltage range | for 80-dB CMRR | Over full temperature range | -22 | 60 | V | |
| K1 | Preamplifier gain ⁽³⁾ | | | 9.95 | 10 | 10.05 | V/V |
| $R_{\text{F-INT}}$ | Output impedance filter resistor | | | 100 | | k Ω | |
| | | $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, | | 99 | 101 | | |
| | | $-40^\circ\text{C} \leq T_A \leq 150^\circ\text{C}$, LMP8601EDRQ1 only | | 97 | 103 | | |
| $\text{TCR}_{\text{F-INT}}$ | Output impedance filter resistor drift | | | ± 5 | ± 50 | ppm/ $^\circ\text{C}$ | |
| A1 V_{OUT} | A1 output voltage swing | $V_{\text{OL}}, R_L = \infty$ | | 2 | | mV | |
| | | | | Over full temperature range | | | 10 |
| | | $V_{\text{OH}}, R_L = \infty$ | | 4.985 | | V | |
| | | | | Over full temperature range | 4.95 | | |
| OUTPUT BUFFER (FROM A2 (PIN 4) TO OUT (PIN 5)) | | | | | | | |
| V_{OS} | Input offset voltage | $0\text{ V} \leq V_{\text{CM}} \leq V_S$ | | -2 | ± 0.5 | 2 | mV |
| | | | | Over full temperature range | -2.5 | | |
| K2 | Output buffer gain ⁽³⁾ | LMP8601, LMP8601-Q1 | | 1.99 | 2 | 2.01 | V/V |
| | | LMP8602, LMP8602-Q1 | | 4.975 | 5 | 5.025 | |
| | | LMP8603, LMP8603-Q1 | | 9.95 | 10 | 10.05 | |
| I_{B} | Input bias current of A2 ⁽⁷⁾ | | | | -40 | | fA |
| | | Over full temperature range | | | | ± 20 | nA |
| A2 V_{OUT} | A2 output voltage swing ^{(8) (9)} | $V_{\text{OL}}, R_L = \infty$ | LMP8601, LMP8601-Q1, | Over full temperature range | 4 | 20 | mV |
| | | | | | 10 | 40 | |
| | | | LMP8602, LMP8602-Q1 | Over full temperature range | 10 | 40 | |
| | | | | | 10 | 80 | |
| | | $V_{\text{OH}}, R_L = \infty$ | Over full temperature range | | 4.99 | | V |
| | | | | | 4.98 | | |
| I_{SC} | Output short-circuit current ⁽¹⁰⁾ | Sourcing, $V_{\text{IN}} = V_S$, $V_{\text{OUT}} = \text{GND}$ | | -25 | -42 | -60 | mA |
| | | Sinking, $V_{\text{IN}} = \text{GND}$, $V_{\text{OUT}} = V_S$ | | 30 | 48 | 65 | |

(6) AC common-mode signal is a $5\text{-}V_{\text{PP}}$ sine-wave (0 V to 5 V) at the given frequency.

(7) Positive current corresponds to current flowing into the device.

(8) For this test input is driven from A1 stage.

(9) For V_{OL} , R_L is connected to V_S and for V_{OH} , R_L is connected to GND.

(10) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

6.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

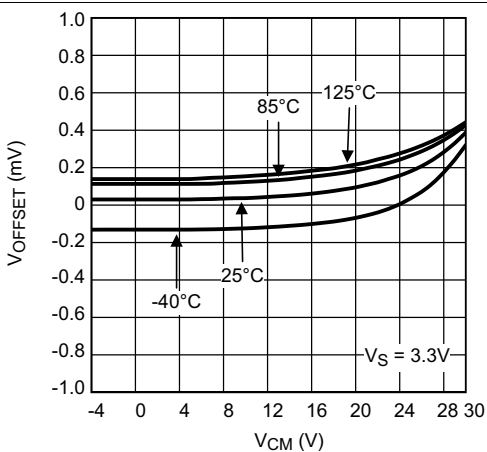


Figure 1. V_{OS} vs V_{CM} at $V_S = 3.3\text{ V}$

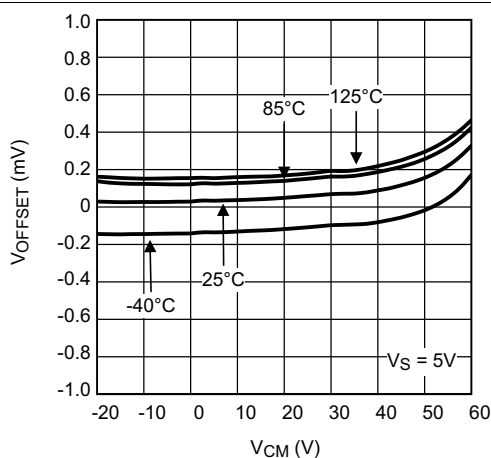


Figure 2. V_{OS} vs V_{CM} at $V_S = 5\text{ V}$

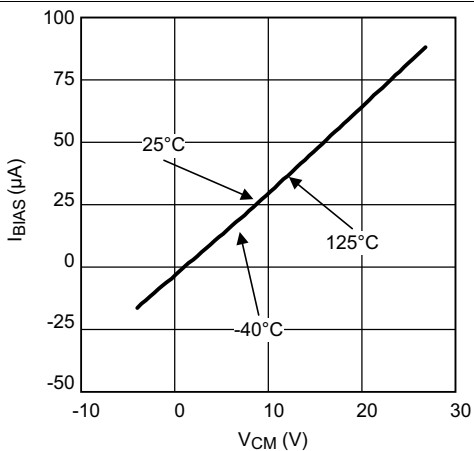


Figure 3. Input Bias Current Over Temperature (+IN and -IN pins) at $V_S = 3.3\text{ V}$

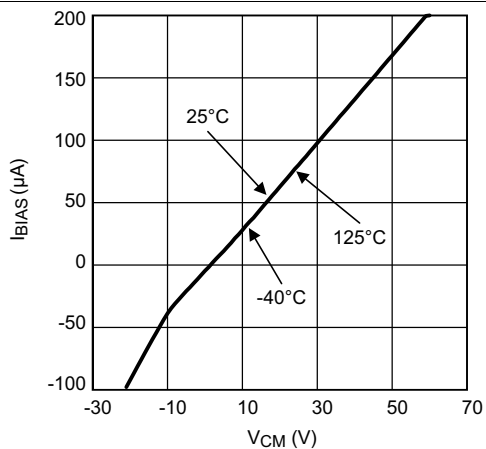


Figure 4. Input Bias Current Over Temperature (+IN and -IN pins) at $V_S = 5\text{ V}$

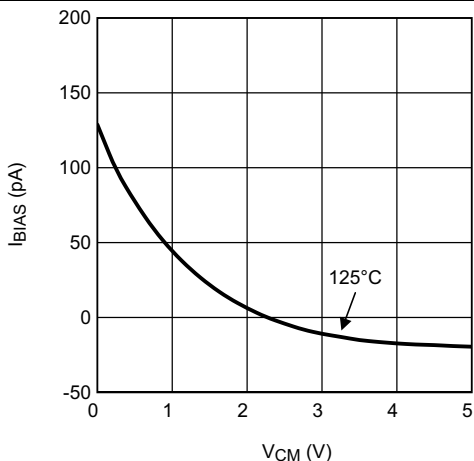


Figure 5. Input Bias Current Over Temperature (A2 pin) at $V_S = 5\text{ V}$

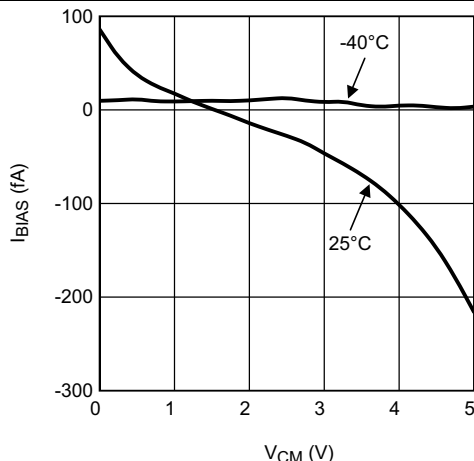


Figure 6. Input Bias Current Over Temperature (A2 pin) at $V_S = 5\text{ V}$

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

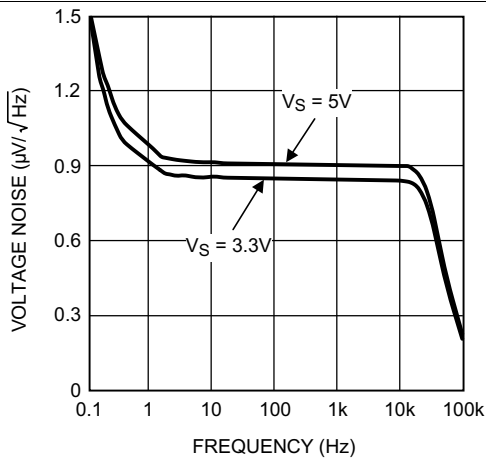


Figure 7. Input-Referred Voltage Noise vs Frequency

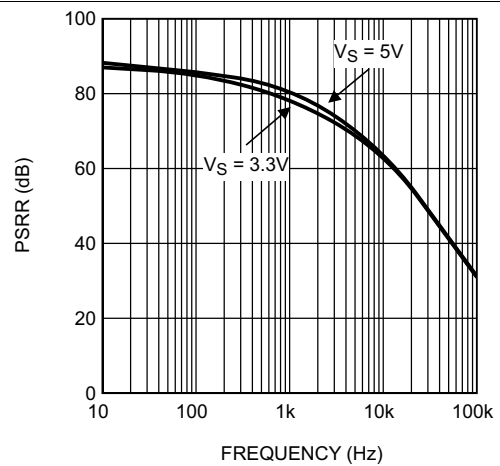


Figure 8. PSRR vs Frequency

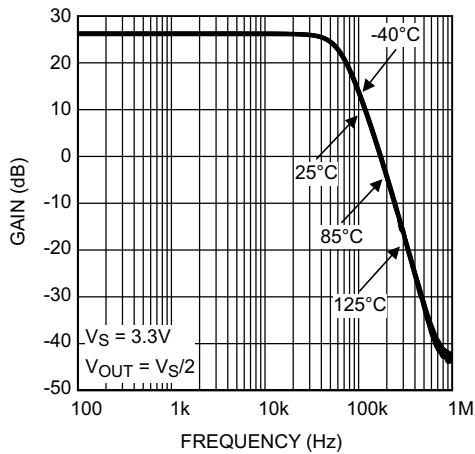


Figure 9. Gain vs Frequency at $V_S = 3.3\text{ V}$

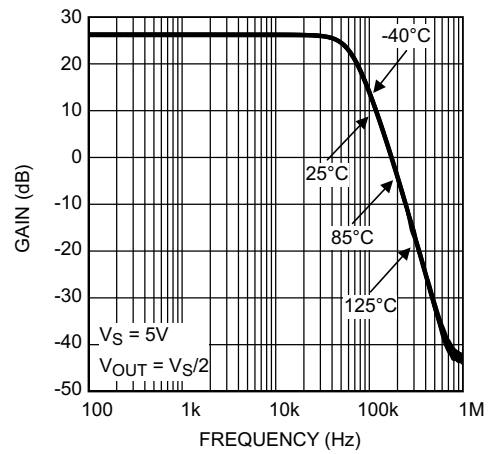


Figure 10. Gain vs Frequency at $V_S = 5\text{ V}$

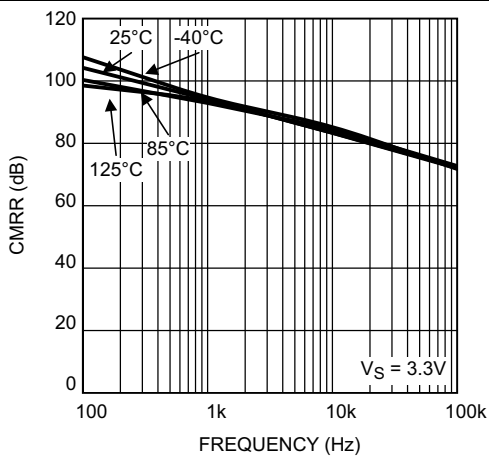


Figure 11. CMRR vs Frequency at $V_S = 3.3\text{ V}$

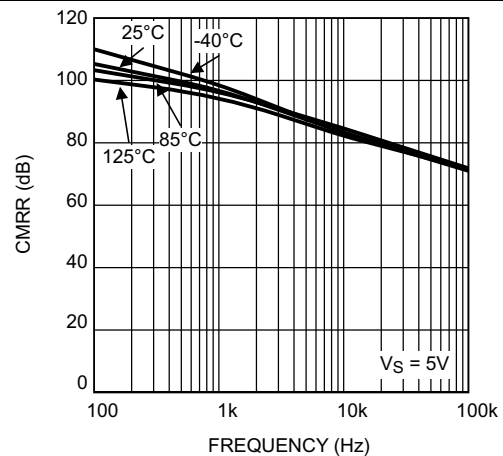


Figure 12. CMRR vs Frequency at $V_S = 5\text{ V}$

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

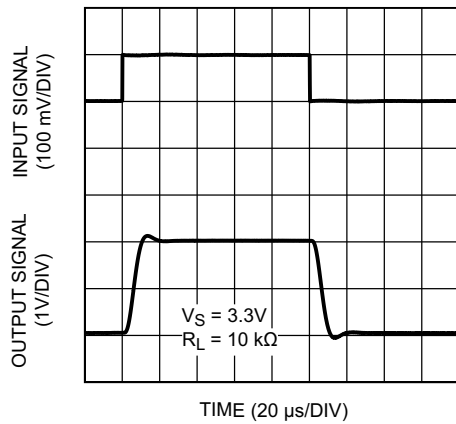


Figure 13. Step Response at $V_S = 3.3\text{ V}$
LMP8601 and LMP8601-Q1

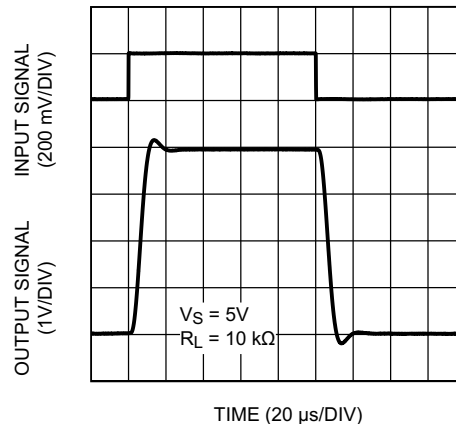


Figure 14. Step Response at $V_S = 5\text{ V}$
LMP8601 and LMP8601-Q1

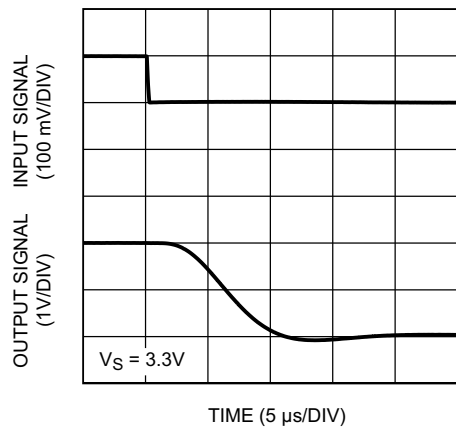


Figure 15. Settling Time (Falling Edge) at $V_S = 3.3\text{ V}$
LMP8601 and LMP8601-Q1

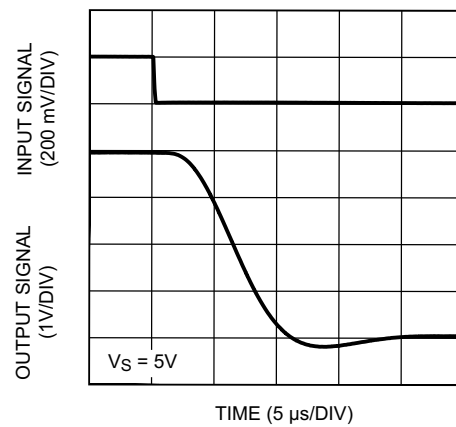


Figure 16. Settling Time (Falling Edge) at $V_S = 5\text{ V}$
LMP8601 and LMP8601-Q1

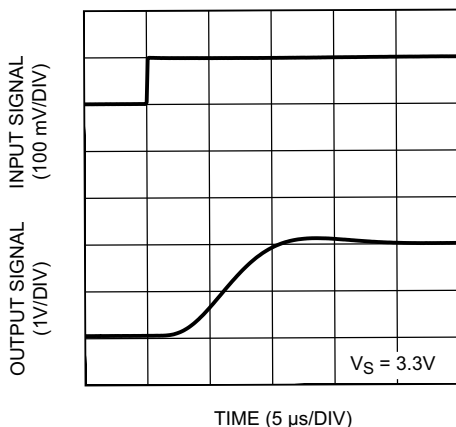


Figure 17. Settling Time (Rising Edge) at $V_S = 3.3\text{ V}$
LMP8601 and LMP8601-Q1

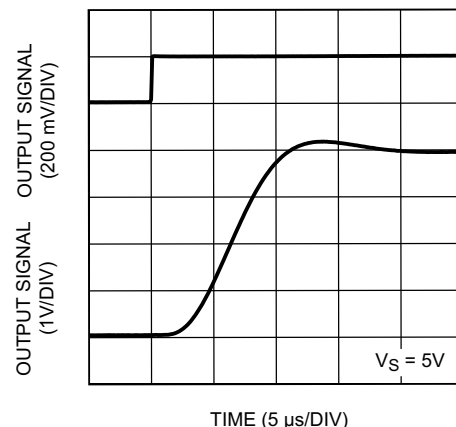


Figure 18. Settling Time (Rising Edge) at $V_S = 5\text{ V}$
LMP8601 and LMP8601-Q1

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

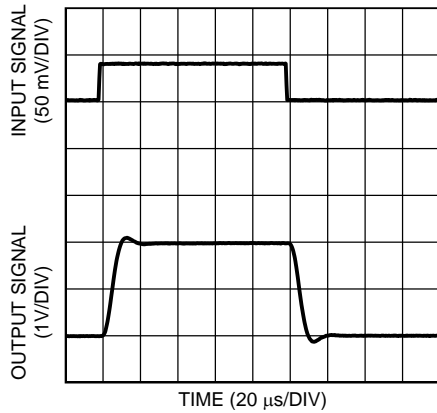


Figure 19. Step Response at $V_S = 3.3\text{ V}$, $R_L = 10\text{ k}\Omega$
 LMP8602 and LMP8602-Q1

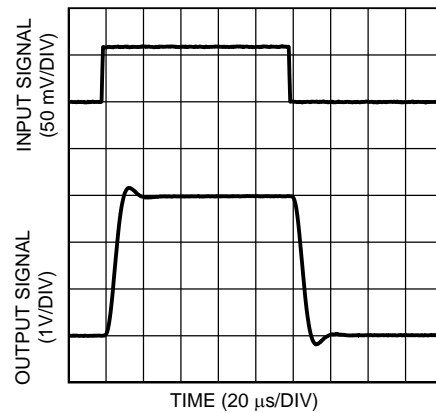


Figure 20. Step Response at $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$
 LMP8602 and LMP8602-Q1

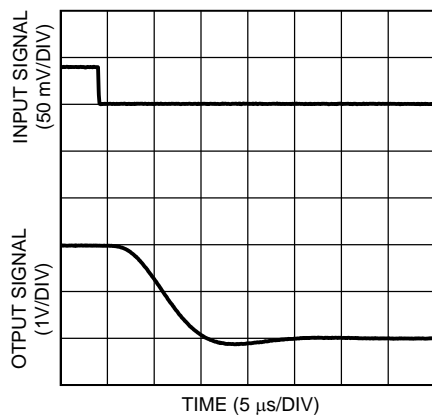


Figure 21. Settling Time (Falling Edge) at $V_S = 3.3\text{ V}$
 LMP8602 and LMP8602-Q1

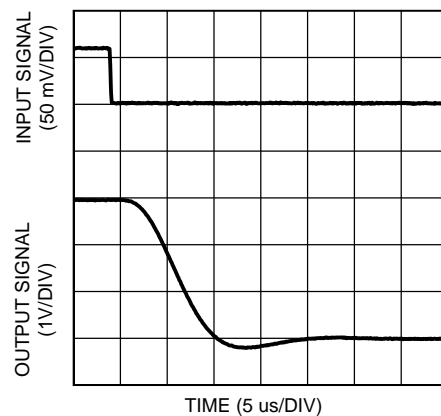


Figure 22. Settling Time (Falling Edge) at $V_S = 5\text{ V}$
 LMP8602 and LMP8602-Q1

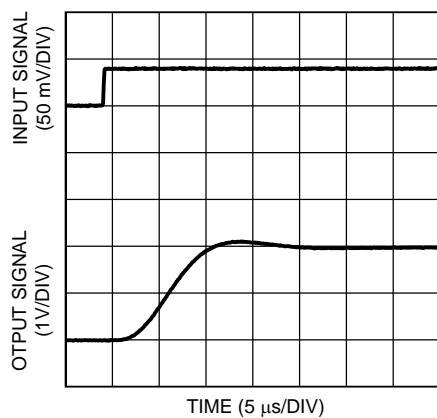


Figure 23. Settling Time (Rising Edge) at $V_S = 3.3\text{ V}$
 LMP8602 and LMP8602-Q1

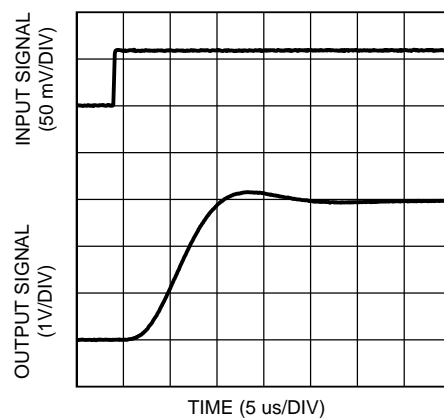


Figure 24. Settling Time (Rising Edge) at $V_S = 5\text{ V}$
 LMP8602 and LMP8602-Q1

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

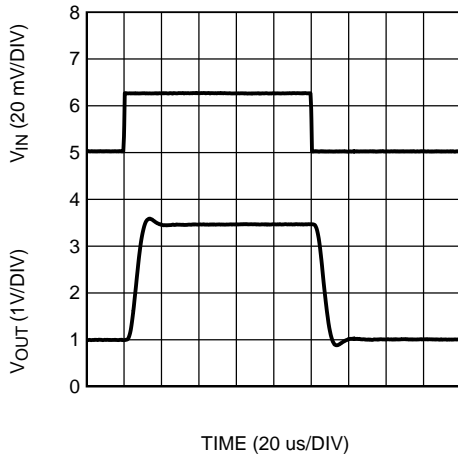


Figure 25. Step Response at $V_S = 3.3\text{ V}$, $R_L = 10\text{ k}\Omega$
LMP8603 and LMP8603-Q1

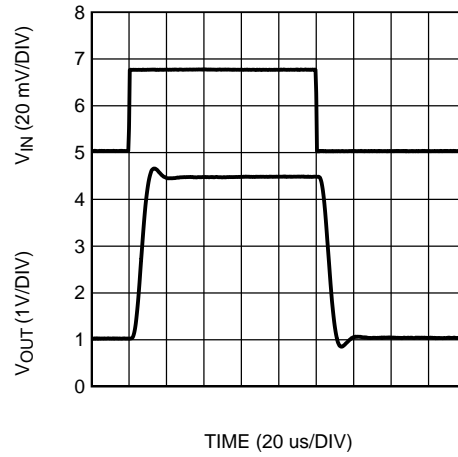


Figure 26. Step Response at $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$
LMP8603 and LMP8603-Q1

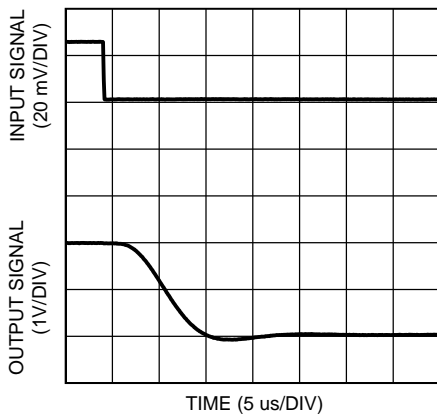


Figure 27. Settling Time (Falling Edge) at $V_S = 3.3\text{ V}$
LMP8603 and LMP8603-Q1

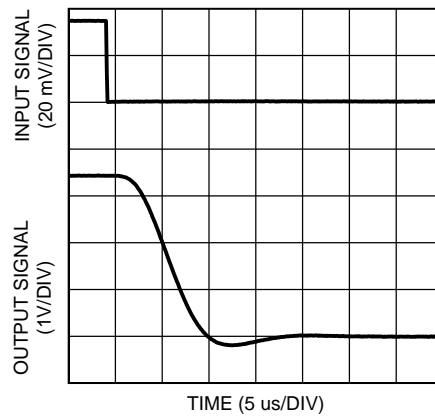


Figure 28. Settling Time (Falling Edge) at $V_S = 5\text{ V}$
LMP8603 and LMP8603-Q1

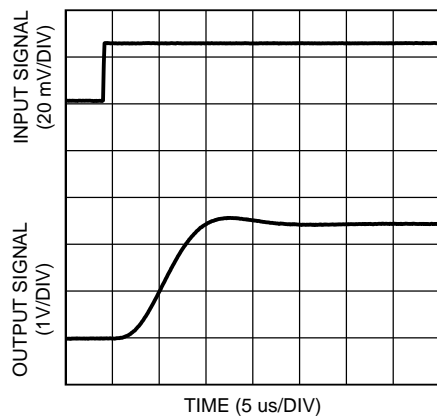


Figure 29. Settling Time (Rising Edge) at $V_S = 3.3\text{ V}$
LMP8603 and LMP8603-Q1

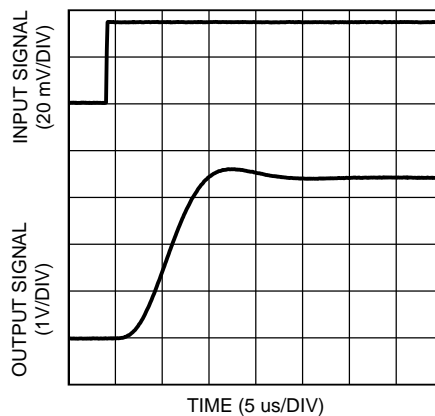


Figure 30. Settling Time (Rising Edge) at $V_S = 5\text{ V}$
LMP8603 and LMP8603-Q1

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

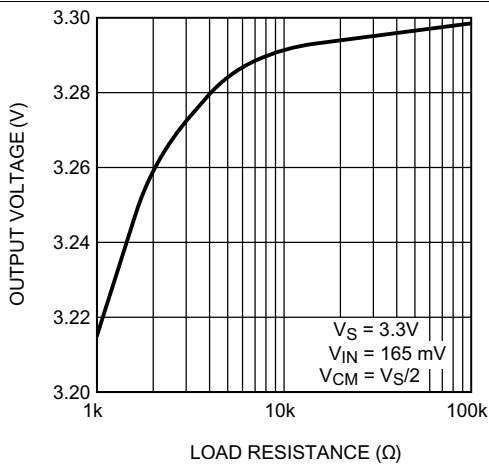


Figure 31. Positive Swing vs R_{LOAD} at $V_S = 3.3\text{ V}$

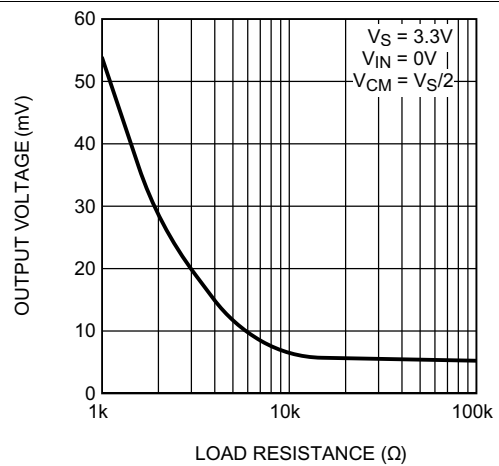


Figure 32. Negative Swing vs R_{LOAD} at $V_S = 3.3\text{ V}$

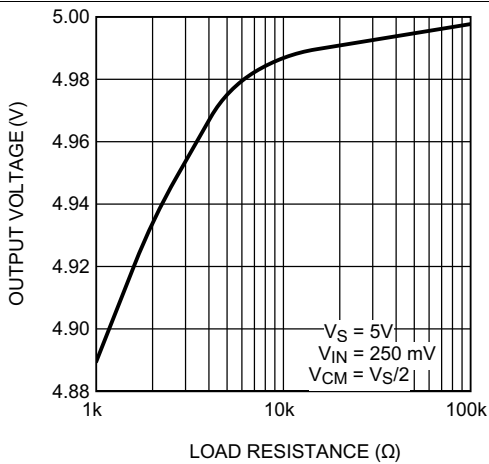


Figure 33. Positive Swing vs R_{LOAD} $V_S = 5\text{ V}$

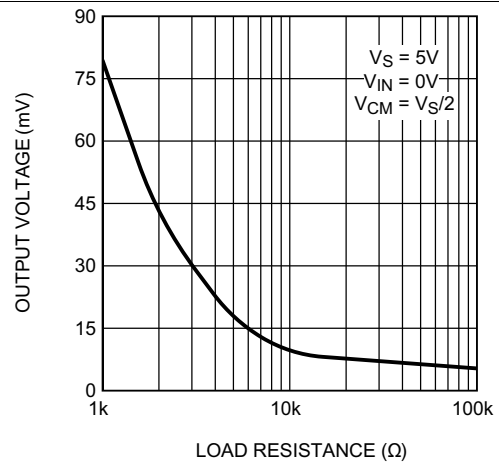


Figure 34. Negative Swing vs R_{LOAD} at $V_S = 5\text{ V}$

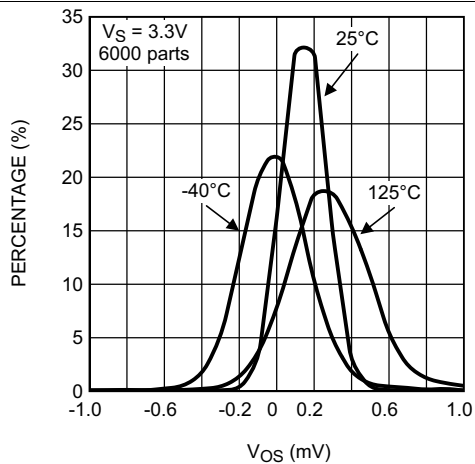


Figure 35. V_{OS} Distribution at $V_S = 3.3\text{ V}$

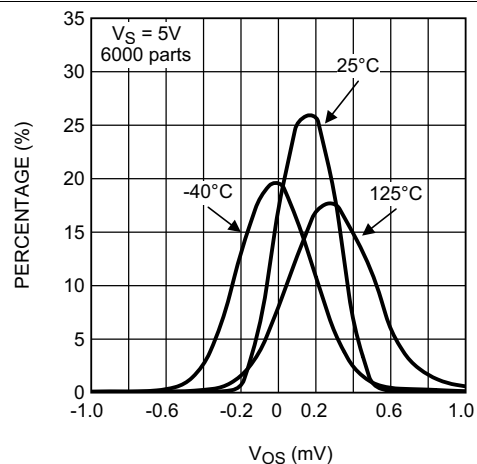


Figure 36. V_{OS} Distribution at $V_S = 5\text{ V}$

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

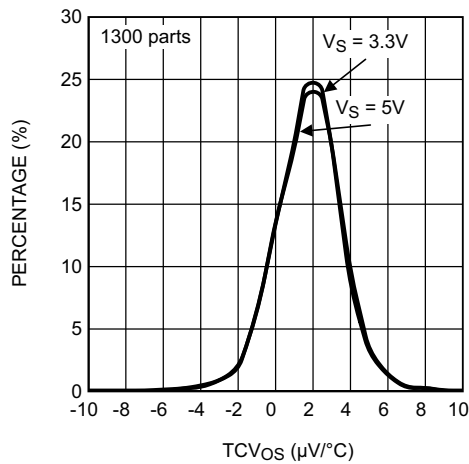


Figure 37. TCV_{OS} Distribution

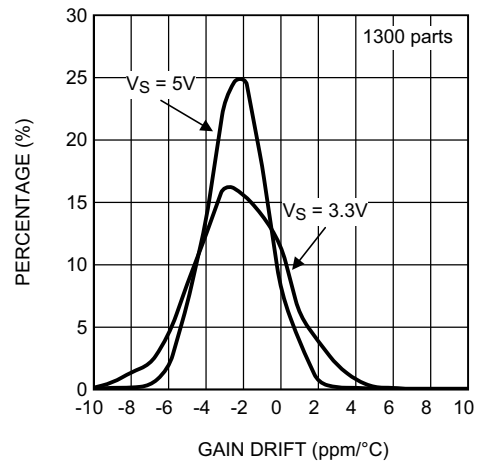


Figure 38. Gain Drift Distribution, 1300 Parts LMP8601 and LMP8601-Q1

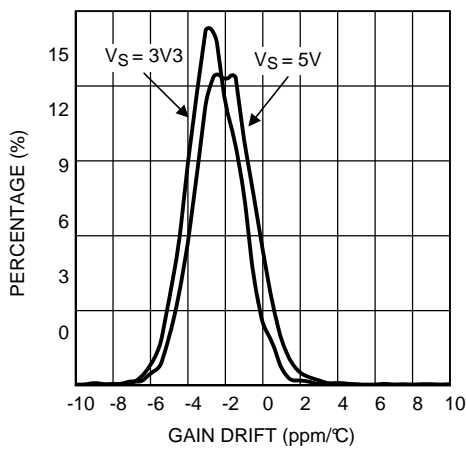


Figure 39. Gain Drift Distribution, 5000 Parts LMP8602 and LMP8602-Q1

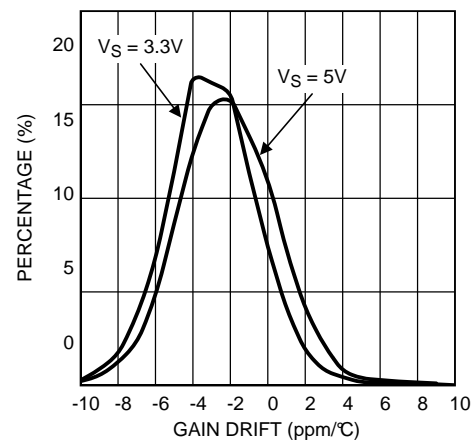


Figure 40. Gain Drift Distribution, 5000 Parts LMP8603 and LMP8603-Q1

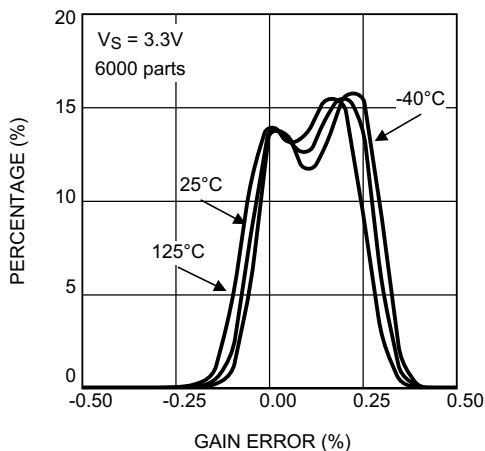


Figure 41. Gain Error Distribution at $V_S = 3.3\text{ V}$ LMP8601 and LMP8601-Q1

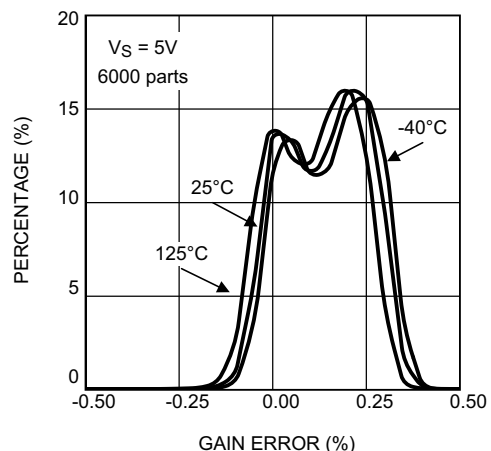


Figure 42. Gain Error Distribution at $V_S = 5\text{ V}$ LMP8601 and LMP8601-Q1

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

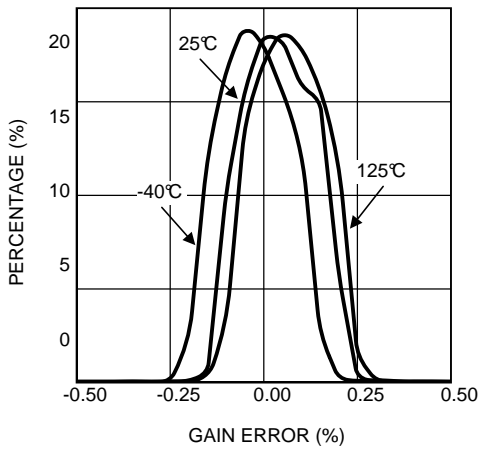


Figure 43. Gain Error Distribution at $V_S = 3.3\text{ V}$, 5000 Parts LMP8602 and LMP8602-Q1

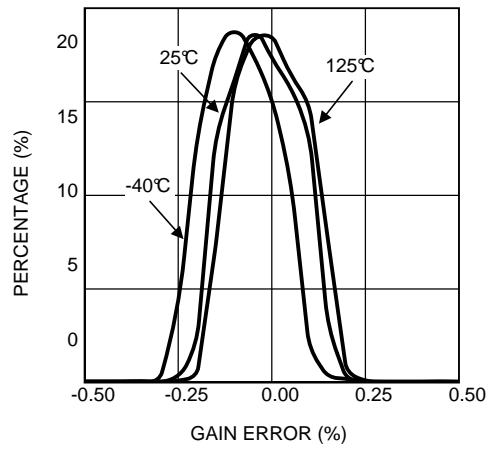


Figure 44. Gain Error Distribution at $V_S = 5\text{ V}$, 5000 Parts LMP8602 and LMP8602-Q1

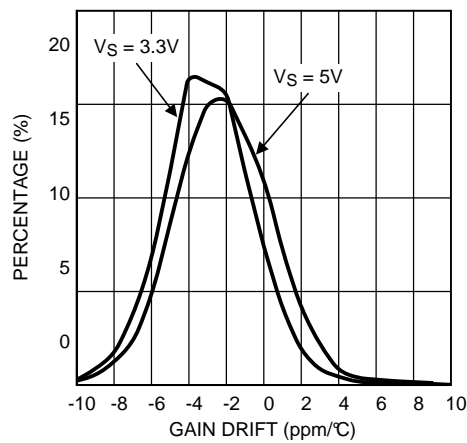


Figure 45. Gain Error Distribution at $V_S = 3.3\text{ V}$, 5000 Parts LMP8603 and LMP8603-Q1

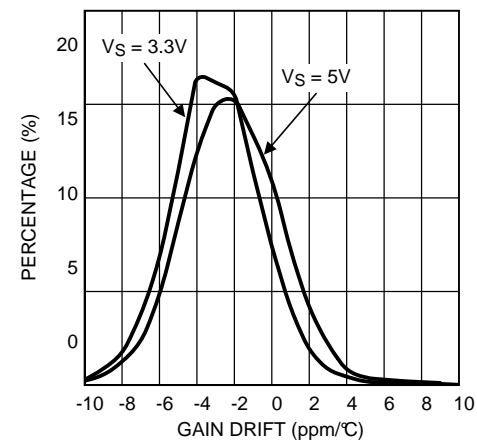


Figure 46. Gain Error Distribution at $V_S = 5\text{ V}$, 5000 Parts LMP8603 and LMP8603-Q1

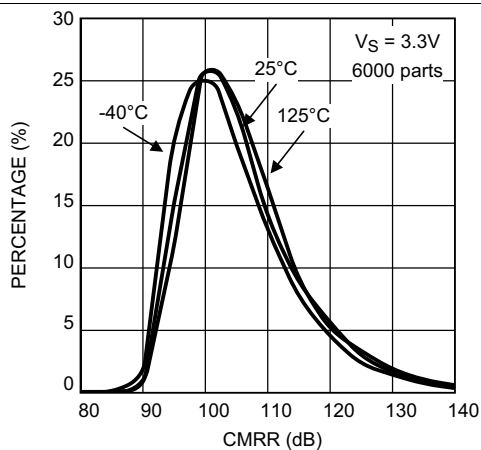


Figure 47. CMRR Distribution at $V_S = 3.3\text{ V}$, 6000 parts

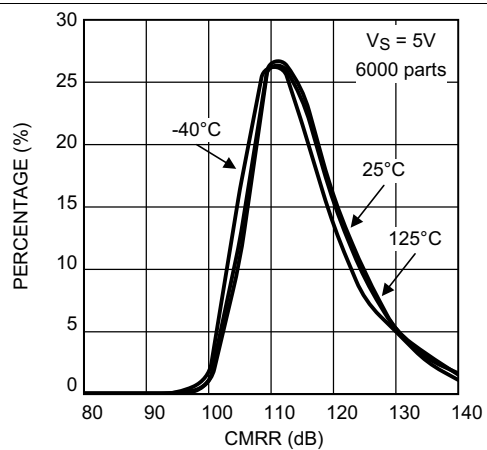


Figure 48. CMRR Distribution at $V_S = 5\text{ V}$, 6000 parts

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $-22 \leq V_{\text{CM}} \leq 60\text{ V}$, $R_L = \infty$, OFFSET (pin 7) connected to V_S , and 10 nF between V_S and GND (unless otherwise noted)

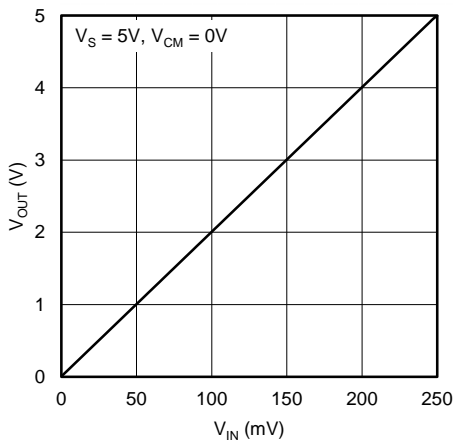


Figure 49. Output Voltage vs VIN

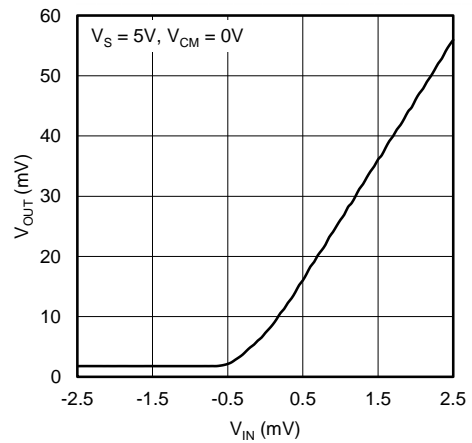


Figure 50. Output Voltage vs VIN (Enlarged Close to 0 V)

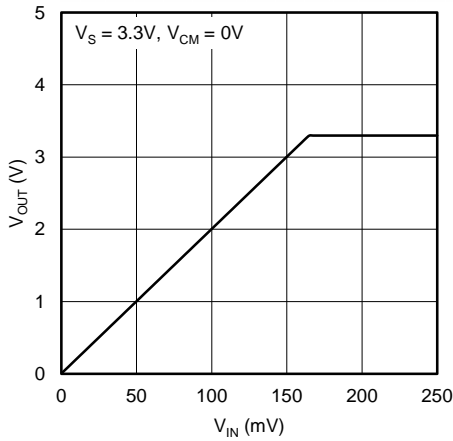


Figure 51. Output Voltage vs VIN

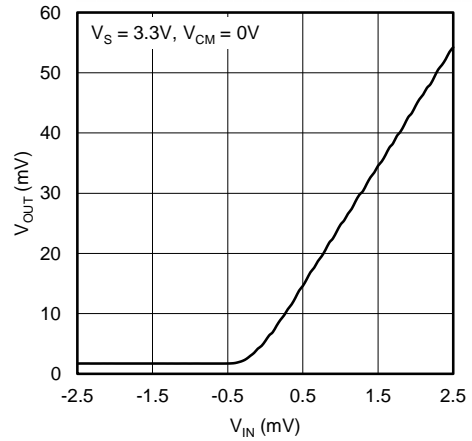


Figure 52. Output Voltage vs VIN (Enlarged Close to 0 V)

7 Detailed Description

7.1 Overview

The LMP860x and LMP860x-Q1 are fixed gain differential voltage precision amplifiers, with a -22-V to $+60\text{-V}$ input common-mode voltage range when operating from a single 5-V supply, or a -4-V to $+27\text{-V}$ input common-mode voltage range when operating from a single 3.3-V supply. The LMP8601 and LMP8601-Q1 have a gain of $20\times$, the LMP8602 and LMP8602-Q1 have a gain of $5\times$, and the LMP8603 and LMP8603-Q1 have a gain of $100\times$.

The LMP860x and LMP860x-Q1 are members of the LMP family and are ideal parts for unidirectional and bidirectional current sensing applications. Because of the proprietary chopping level-shift input stage, the LMP860x and LMP860x-Q1 achieve very low offset, very low thermal offset drift, and very high CMRR. The LMP860x and LMP860x-Q1 amplify and filter small differential signals in the presence of high common-mode voltages.

The LMP860x and LMP860x-Q1 use level shift resistors at the inputs. Because of these resistors, the LMP860x and LMP860x-Q1 can easily withstand very large differential input voltages that may exist in fault conditions where some other less protected high-performance current sense amplifiers might sustain permanent damage.

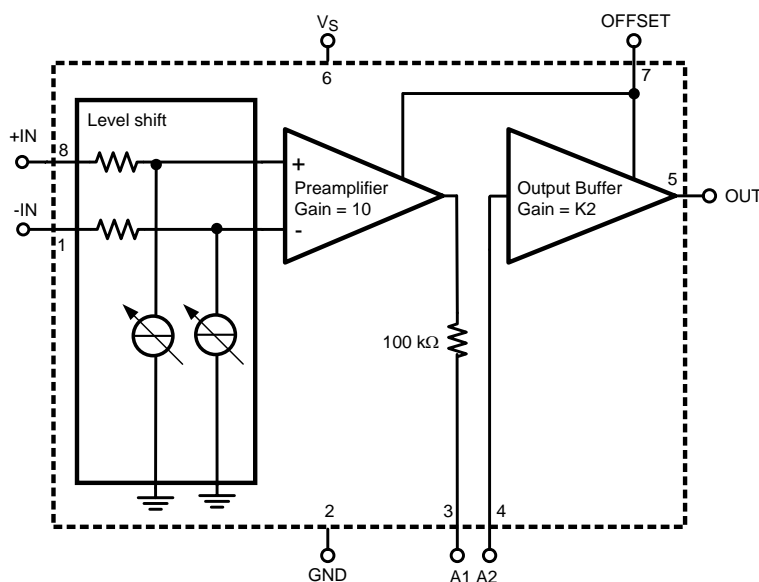
7.1.1 Theory of Operation

The schematic shown in the *Functional Block Diagram* gives a basic representation of the internal operation of the LMP860x and LMP860x-Q1.

The signal on the input pins is typically a small differential voltage developed across a current sensing shunt resistor. The input signal may also appear at a high common-mode voltage. The input signals are accessed through two input resistors that change the voltage into a current. The proprietary chopping level-shift current circuit pulls or pushes current through the input resistors to bring the common-mode voltage behind these resistors within the supply rails.

Subsequently, the signal is gained up by a factor of 10 and brought out on the A1 pin through a trimmed $100\text{-k}\Omega$ resistor. In the application, additional gain adjustment or filtering components can be added between the A1 and A2 pins as explained in subsequent sections. The signal on the A2 pin is further amplified by a factor of 2 (LMP8601 and LMP8601-Q1), 5 (LMP8602, LMP8602-Q1), or 10 (LMP8603, LMP8603-Q1), and brought out on the OUT pin.

7.2 Functional Block Diagram



NOTE: $K2 = 2$ for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

7.3 Feature Description

7.3.1 Offset Input Pin

The OFFSET pin allows the output signal to be level-shifted to enable bidirectional current sensing. The output signal is bidirectional and mid-rail referenced when the offset pin is connected to the positive supply rail. With the offset pin connected to ground, the output signal is unidirectional and ground-referenced.

The signal on the A1 and OUT pins is ground-referenced when the offset pin is connected to ground. This means that the output signal can only represent positive values of the current through the shunt resistor, so only currents flowing in one direction can be measured.

When the offset pin is tied to the positive supply rail, the signal on the A1 and OUT pins is referenced to a mid-rail voltage which allows bidirectional current sensing. The operation of the amplifier will be fully bidirectional and symmetrical around 0 V differential at the input pins. The signal at the output will follow this voltage difference multiplied by the gain and at an offset voltage at the output of half V_S .

When the offset pin is connected to an external voltage source, the output signal will be level shifted to that voltage divided by two. In principle, the output signal can be shifted to any voltage between 0 and $V_S / 2$ by applying twice that voltage to the OFFSET pin.

NOTE

The OFFSET pin must be driven from a very low-impedance source ($< 10 \Omega$). This low source impedance is required because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (for example, a resistive divider between the supply rails), accuracy decreases.

Examples:

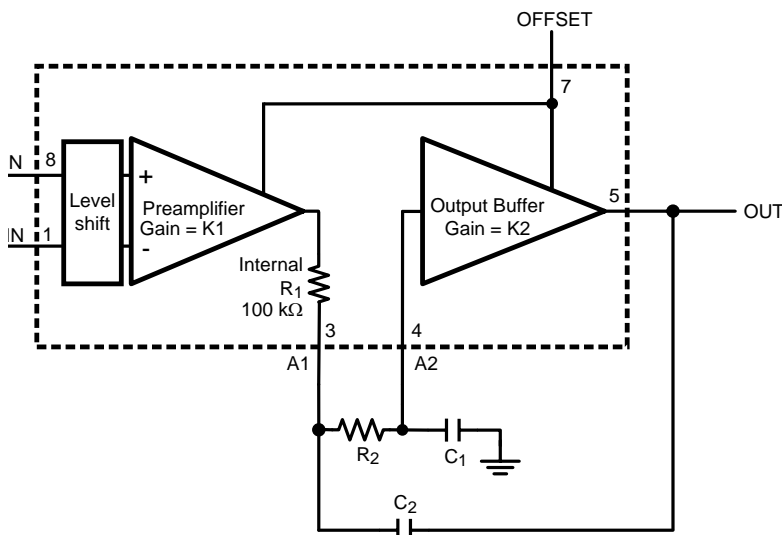
- **LMP8601, LMP8601-Q1:** A 5-V supply, a gain of 20x, OFFSET pin tied to V_S , and a differential input signal of 10 mV results in 2.7 V at the output pin. Similarly, -10 mV at the input results in 2.3 V at the output pin.
 - **LMP8602, LMP8602-Q1:** A 5-V supply, a gain of 50x, and a differential input signal of 10 mV results in 3.0 V at the output pin. Similarly, -10 mV at the input results in 2.0 V at the output pin.
 - **LMP8603, LMP8603-Q1:** A 5-V supply, a gain of 100x, and a differential input signal of 10 mV results in 3.5 V at the output pin. Similarly, -10 mV at the input results in 1.5 V at the output pin.^{(1) (1)}
- (1) The OFFSET pin must be driven from a very low-impedance source ($< 10 \Omega$) because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (for example, a resistive divider between the supply rails), accuracy decreases.

Feature Description (continued)

7.3.2 Additional Second-Order Low-Pass Filter

The LMP86x1 and LMP86x1-Q1 have a third-order Butterworth lowpass characteristic with a typical bandwidth of 60 kHz integrated in the preamplifier stage. The bandwidth of the output buffer can be reduced by adding a capacitor on the A1 pin to create a first-order low-pass filter with a time constant determined by the 100-kΩ internal resistor and the external filter capacitor.

It is also possible to create an additional second-order, Sallen-Key, low-pass filter by adding external components R_2 , C_1 and C_2 . Together with the internal 100-kΩ resistor R_1 as illustrated in Figure 53, this circuit creates a second-order, low-pass filter characteristic.



NOTE: $K_1 = 10$; $K_2 = 2$ for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 53. Second-Order Low-Pass Filter

When the corner frequency of the additional filter is much lower than 60 kHz, the transfer function of the described amplifier can be written as:

$$H(s) = \frac{K_1 * K_2 \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s * \left[\frac{1}{R_1 C_2} + \frac{1}{R_2 C_2} + \frac{(1 - K_2)}{R_2 C_1} \right] + \frac{1}{R_1 R_2 C_1 C_2}}$$

where

- K_1 equals the gain of the preamplifier and K_2 that of the buffer amplifier. (1)

Equation 1 can be written in the normalized frequency response for a second-order lowpass filter:

$$G(j\omega) = K_1 * \frac{K_2}{\frac{(j\omega)^2}{\omega_0^2} + \frac{j\omega}{Q\omega_0} + 1} \quad (2)$$

The cutoff frequency ω_0 in rad/sec (divide by 2π to get the cut-off frequency in Hz) is given by:

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \quad (3)$$

Feature Description (continued)

and the quality factor of the filter is given by:

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 + (1 - K_2) * R_1 C_2} \quad (4)$$

With $K_2 = 2x$, Equation 4 transforms results in:

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 - R_1 C_2} \quad (5)$$

For any filter gain $K > 1x$, the design procedure can be very simple if the two capacitors are chosen to in a certain ratio.

$$C_2 = \frac{C_1}{K_2 - 1} \quad (6)$$

Inserting this in Equation 4 for Q results in:

$$Q = \frac{\sqrt{R_1 R_2 \frac{C_1^2}{K_2 - 1}}}{R_1 C_1 + R_2 C_1 - \frac{(K_2 - 1) R_1 C_1}{K_2 - 1}} \quad (7)$$

Which results in:

$$Q = \frac{\sqrt{R_1 R_2 \frac{C_1^2}{K_2 - 1}}}{C_1 R_2} = \frac{\sqrt{\frac{R_1 R_2}{K_2 - 1}}}{R_2} \quad (8)$$

In this case, given the predetermined value of $R_1 = 100 \text{ k}\Omega$ (the internal resistor), the quality factor is set solely by the value of the resistor R_2 .

R_2 can be calculated based on the desired value of Q as the first step of the design procedure with the following equation:

$$R_2 = \frac{R_1}{(K - 1) Q^2} \quad (9)$$

For the gain of 2 for the LMP8601 and LMP8601-Q1, the result is:

$$R_2 = \frac{R_1}{Q^2} \quad (10)$$

For the gain of 5 for the LMP8602 and LMP8602-Q1, the result is:

$$R_2 = \frac{R_1}{4Q^2} \quad (11)$$

For the gain of 10 for the LMP8603 and LMP8603-Q1, the result is:

$$R_2 = \frac{R_1}{9Q^2} \quad (12)$$

Feature Description (continued)

For instance, the value of Q can be set to $0.5\sqrt{2}$ to create a Butterworth response, to $1/\sqrt{3}$ to create a Bessel response, or a 0.5 to create a critically damped response. After the value of R_2 has been found, the second and last step of the design procedure is to calculate the required value of C to give the desired low-pass cut-off frequency using:

$$C_1 = \frac{(K_2 - 1)Q}{R_1\omega_0} \quad (13)$$

For the gain = 2, the result is:

$$C = \frac{Q}{R_1\omega_0} \quad (14)$$

The gain = 5 results in:

$$C_1 = \frac{4Q}{R_1\omega_0} \quad (15)$$

The gain = 10 gives:

$$C_1 = \frac{9Q}{R_1\omega_0} \quad (16)$$

For C_2 the value is calculated with:

$$C_2 = \frac{C_1}{K_2 - 1} \quad (17)$$

For a gain = 2:

$$C_2 = C_1 \quad (18)$$

Or for a gain = 5:

$$C_2 = \frac{C_1}{4} \quad (19)$$

And for a gain = 10:

$$C_2 = \frac{C_1}{9} \quad (20)$$

Note that the frequency response achieved using this procedure is only accurate if the cut-off frequency of the second-order filter is much smaller than the intrinsic 60-kHz, low-pass filter. In other words, choose the frequency response of the LMP860x or LMP860x-Q1 circuit so that the internal poles do not affect the external second-order filter.

7.4 Device Functional Modes

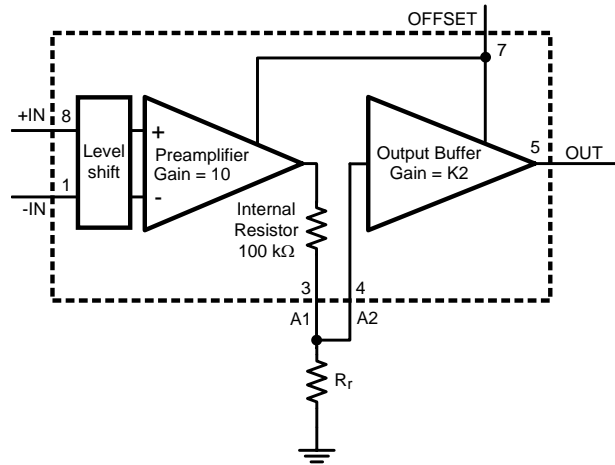
7.4.1 Gain Adjustment

The gain of the LMP860x and LMP860x-Q1 is fixed; however, the overall gain may be adjusted as the signal path between the two internal amplifiers is available on the A1 and A2 pins.

Device Functional Modes (continued)

7.4.1.1 Reducing Gain

Figure 54 shows the configuration that can be used to reduce the gain of the LMP8601 and LMP8601-Q1.



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 54. Reduce Gain

R_r creates a resistive divider together with the internal 100-k Ω resistor such that the reduced gain G_r becomes:

$$G_r = \frac{20 R_r}{R_r + 100 \text{ k}\Omega} \quad (21)$$

For the LMP8602 and LMP8602-Q1:

$$G_r = \frac{50 R_r}{R_r + 100 \text{ k}\Omega} \quad (22)$$

And for the LMP8603 and LMP8603-Q1:

$$G_r = \frac{100 R_r}{R_r + 100 \text{ k}\Omega} \quad (23)$$

Given a desired value of the reduced gain G_r , using this equation, the LMP8601 and LMP8601-Q1 required value for the R_r is calculated with:

$$R_r = 100 \text{ k}\Omega \times \frac{G_r}{20 - G_r} \quad (24)$$

For the LMP8602 and LMP8602-Q1:

$$R_r = 100 \text{ k}\Omega \times \frac{G_r}{50 - G_r} \quad (25)$$

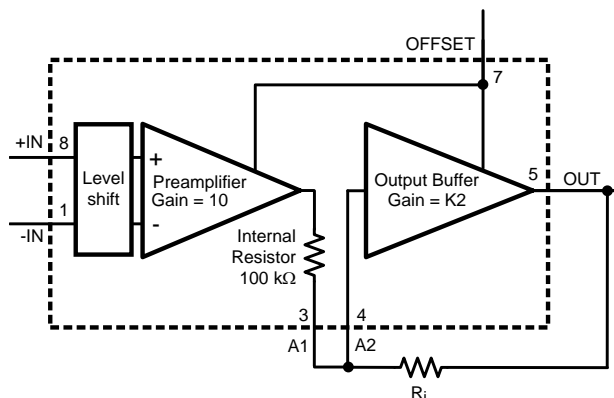
And for the LMP8603 and LMP8603-Q1:

$$R_r = 100 \text{ k}\Omega \times \frac{G_r}{100 - G_r} \quad (26)$$

7.4.1.2 Increasing Gain

Figure 55 shows the configuration that can be used to increase the gain of the LMP8601 and LMP8601-Q1.

Device Functional Modes (continued)



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 55. Increase Gain

R_i creates positive feedback from the output pin to the input of the buffer amplifier. The positive feedback increases the gain. The increased gain G_i for the LMP8601 and LMP8601-Q1 becomes:

$$G_i = \frac{20 R_i}{R_i - 100 \text{ k}\Omega} \quad (27)$$

For the LMP8602 and LMP8602-Q1:

$$G_i = \frac{50 R_i}{R_i - 400 \text{ k}\Omega} \quad (28)$$

And for the LMP8603 and LMP8603-Q1:

$$G_i = \frac{100 R_i}{R_i - 900 \text{ k}\Omega} \quad (29)$$

From this equation, for a desired value of the gain, the LMP8601 and LMP8601-Q1 required value of R_i is calculated with:

$$R_i = 100 \text{ k}\Omega \times \frac{G_i}{G_i - 20} \quad (30)$$

For the LMP8602 and LMP8602-Q1:

$$R_i = 400 \text{ k}\Omega \times \frac{G_i}{G_i - 50} \quad (31)$$

And for the LMP8603 with:

$$R_i = 900 \text{ k}\Omega \times \frac{G_i}{G_i - 100} \quad (32)$$

Note that from the equation for the gain G_i , for large gains, R_i approaches 100 kΩ. In this case, the denominator in the equation becomes close to zero. In practice, for large gains, the denominator is determined by tolerances in the value of the external resistor R_i and the internal 100-kΩ resistor. In this case, the gain becomes very inaccurate. If the denominator becomes equal to zero, the system becomes unstable. TI recommends to limit the application of this technique to gain values of 50 or smaller.

Device Functional Modes (continued)

7.4.2 Driving Switched Capacitive Loads

Some ADCs load their signal source with a sample and hold capacitor. The capacitor may be discharged prior to being connected to the signal source. If the LMP860x and LMP860x-Q1 are driving such ADCs, the sudden current that should be delivered when the sampling occurs may disturb the output signal. This effect was simulated with the circuit shown in Figure 56 where the output is to a capacitor that is driven by a rail-to-rail square wave.

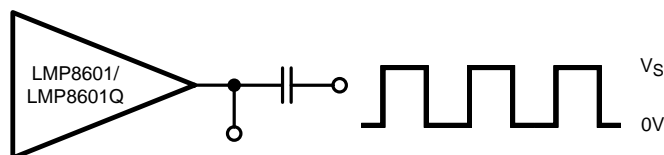


Figure 56. Driving Switched Capacitive Load

This circuit simulates the switched connection of a discharged capacitor to the LMP860x and LMP860x-Q1 output. The resulting V_{OUT} disturbance signals are shown in Figure 57 and Figure 58.

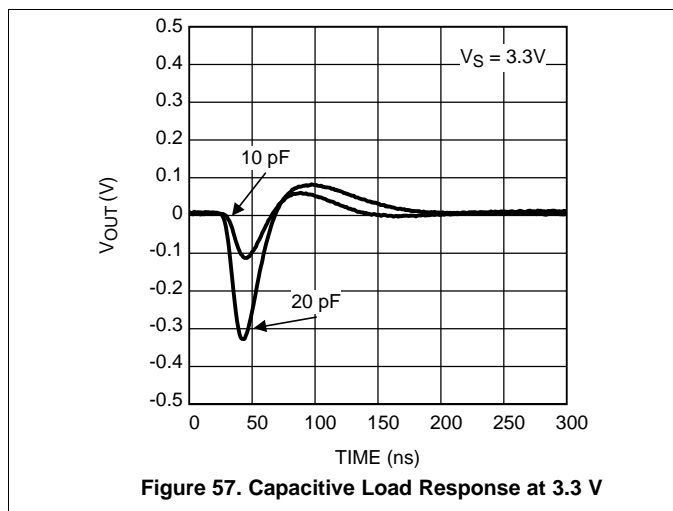


Figure 57. Capacitive Load Response at 3.3 V

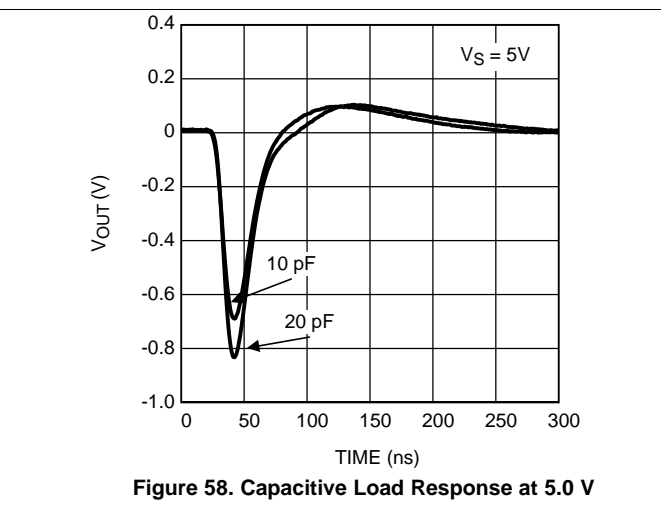


Figure 58. Capacitive Load Response at 5.0 V

These figures can be used to estimate the disturbance that will be caused when driving a switched capacitive load. To minimize the error signal introduced by the sampling that occurs on the ADC input, place an additional RC filter between the LMP860x or LMP860x-Q1 and the ADC, as illustrated in Figure 59.

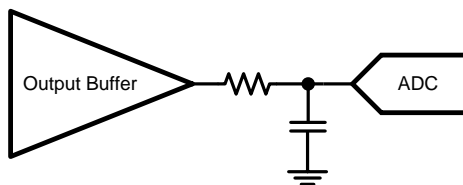


Figure 59. Reduce Error When Driving ADCs

The external capacitor absorbs the charge that flows when the ADC sampling capacitor is connected. The external capacitor should be much larger than the sample-and-hold capacitor at the input of the ADC, and the RC time constant of the external filter should be such that the speed of the system is not affected.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

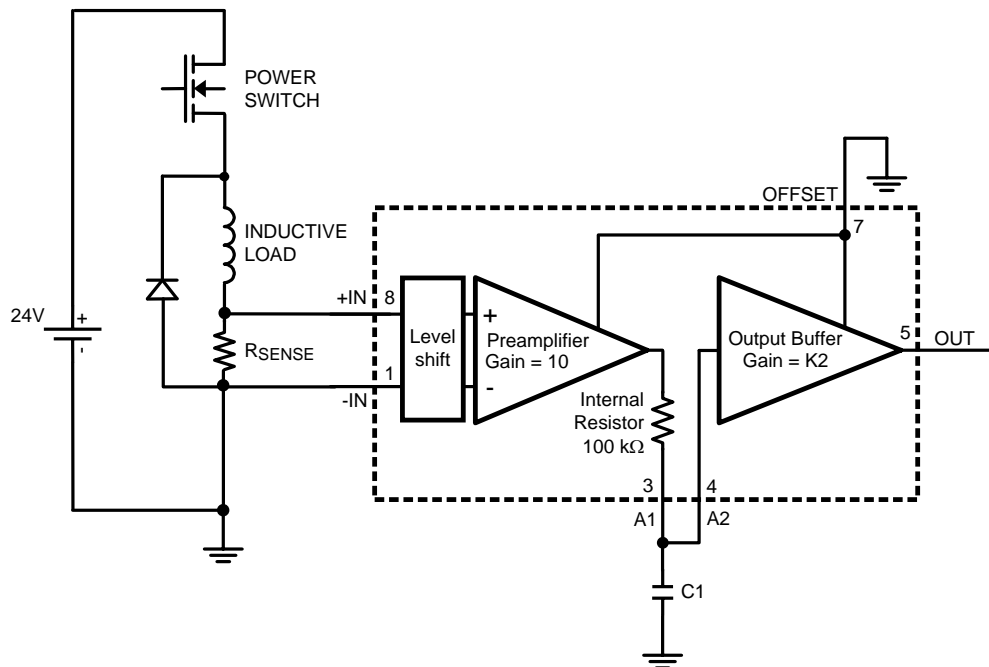
8.1.1 Specifying Performance

To specify the high performance of the LMP860x and LMP860x-Q1, all minimum and maximum values shown in the parameter tables of this data sheet are 100% tested, and all over temperature limits are also 100% tested over temperature.

8.2 Typical Applications

8.2.1 High-Side, Current-Sensing Application

Figure 60 illustrates the application of the LMP860x and LMP860x-Q1 in a high-side sensing application. This application is similar to the low-side sensing discussed below, except in this application the common-mode voltage on the shunt drops below ground when the driver is switched off. Because the common-mode voltage range of the LMP860x and LMP860x-Q1 extends below the negative rail, the LMP860x and LMP860x-Q1 are also very well suited for this application.



NOTE: For this application example, $K2 = 2$.

Figure 60. High-Side, Current-Sensing Application

Typical Applications (continued)

8.2.1.1 Design Requirements

Using the circuit in [Figure 60](#), the requirement is to measure coil current up to 10 A and drive the ADC input to a maximum of 3.3 V. The OFFSET pin is grounded, so zero current will result in a zero volt output.

8.2.1.2 Detailed Design Procedure

First, the value of R_{SENSE} must be determined. R_{SENSE} can be found by dividing the maximum desired output swing by the gain to determine the maximum input voltage. In this example, the LMP8601 is used, with a gain of 20 V/V, as shown in [Equation 33](#):

$$V_{INMAX} = \frac{V_{OUTMAX}}{\text{Gain}} = \frac{3.3 \text{ V}}{20 \text{ V/V}} = 165 \text{ mV} \quad (33)$$

Knowing 165 mV must be generated, the ideal value of the sense resistor can be determined through simple ohms law:

$$R_{SENSE} = \frac{V_{INMAX}}{I_{LOADMAX}} = \frac{165 \text{ mV}}{10 \text{ A}} = 16.5 \text{ m}\Omega \quad (34)$$

The ideal sense resistor value is 16.5 m Ω . The closest standard value is 15 m Ω , but this value may cause the output to slightly overrange at 10 V. It is recommended to reduce the expected maximum output by a few percent to allow for overloads and component tolerances. The next most popular values would be 10 m Ω , 15 m Ω , and 20 m Ω . 10 m Ω allows for a maximum output of 2 V at 10 A, but may be too low and not use the full output range. 20 m Ω provides more sensitivity, but limits the maximum current to 8.25 A. 15 m Ω is a good compromise at 11 A maximum, and allows for some component tolerance variation.

If a suitable sense resistor value is not available, it is possible to adjust the gain as detailed in the [Gain Adjustment](#) section.

The sense resistor does dissipate power, so the maximum wattage rating and appropriate power deratings must be observed. In the example above, the sense resistor dissipates $0.165 \text{ V} \times 10 \text{ A} = 1.65 \text{ W}$, so a sense resistor of at least twice the maximum expected power should be used (greater than 4 W).

8.2.1.3 Application Curve

Below is the expected output value using a 15-m Ω sense resistor.

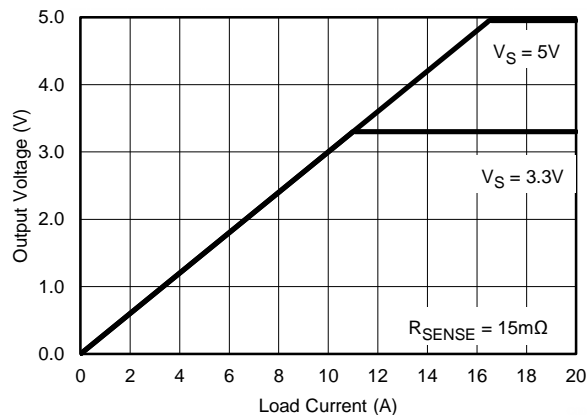


Figure 61. Expected Output Voltage vs Load Current Using 15-m Ω Sense Resistor

Typical Applications (continued)

8.2.2 Low-Side, Current-Sensing Application

Figure 62 illustrates a low-side, current-sensing application with a low-side driver. The power transistor is pulse width modulated to control the average current flowing through the inductive load which is connected to a relatively high battery voltage. The current through the load is measured across a shunt resistor R_{SENSE} in series with the load. When the power transistor is on, current flows from the battery through the inductive load, the shunt resistor and the power transistor to ground. In this case, the common-mode voltage on the shunt is close to ground. When the power transistor is off, current flows through the inductive load, through the shunt resistor and through the freewheeling diode. In this case the common-mode voltage on the shunt is at least one diode voltage drop above the battery voltage. Therefore, in this application the common-mode voltage on the shunt is varying between a large positive voltage and a relatively low voltage. Because the large ac common-mode rejection ratio, the LMP860x and LMP860x-Q1 are very well suited for this application.

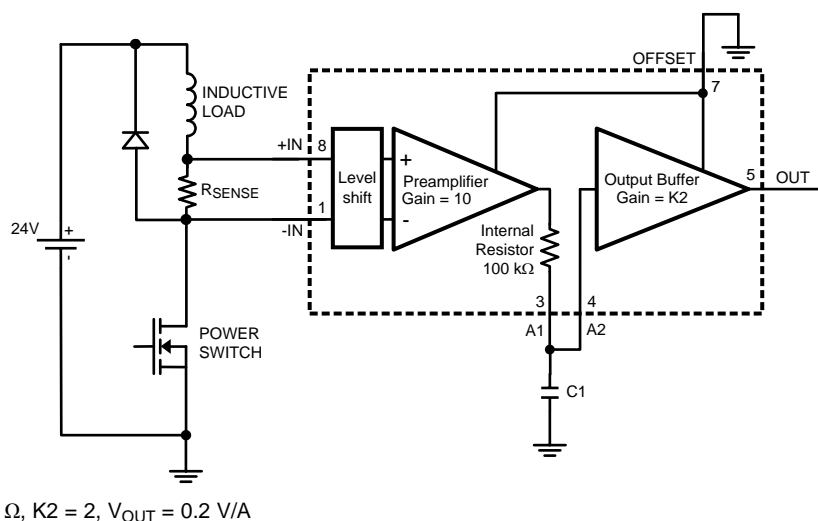


Figure 62. Low-Side Current-Sensing Application

For this application, the following example can be used for the calculation of the sense voltage (V_{SENSE}):

When using a sense resistor, R_{SENSE} , of 0.01Ω and a current, I_{LOAD} , of 1 A, the sense voltage at the input pins of the LMP860x and LMP860x-Q1 is:

$$V_{SENSE} = R_{SENSE} \times I_{LOAD} = 0.01 \Omega \times 1 \text{ A} = 0.01 \text{ V} \quad (35)$$

With the gain of 20 for the LMP8601, the result is an output of 0.2 V. Or in other words, $V_{OUT} = 0.2 \text{ V/A}$. The result is the same for the LMP8601-Q1.

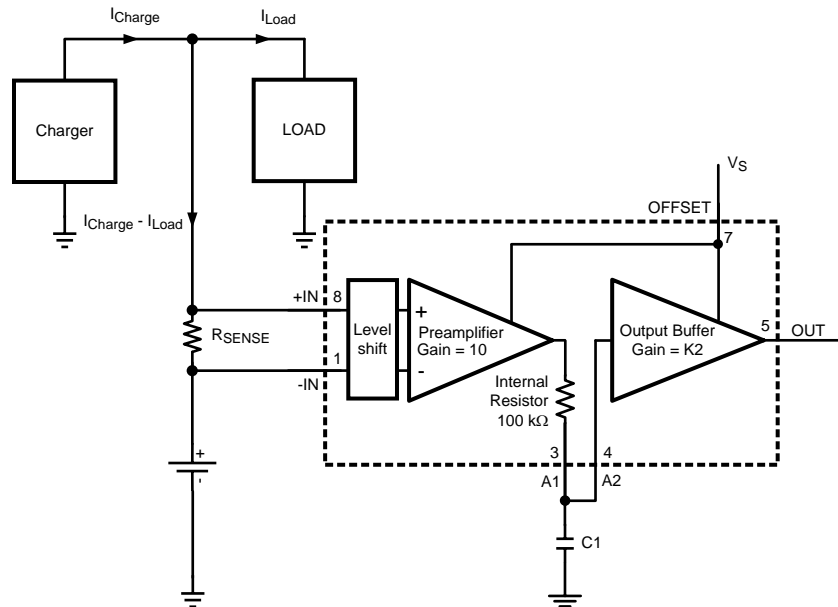
For the LMP8602 and LMP8602-Q1 with a gain of 50, the output is 0.5 V/A.

For the LMP8603 and LMP8603-Q1 with a gain of 100, the output is 1 V/A.

Typical Applications (continued)

8.2.3 Battery Current Monitor Application

This application example shows how the LMP860x and LMP860x-Q1 can be used to monitor the current flowing in and out of a battery pack. The fact that the LMP860x and LMP860x-Q1 can measure small voltages at a high offset voltage outside the parts own supply range makes this part a very good choice for such applications. If the load current of the battery is higher than the charging current, the output voltage of the LMP860x and LMP860x-Q1 will be above the *half offset voltage* for a net current flowing out of the battery. When the charging current is higher than the load current the output will be below this half offset voltage.



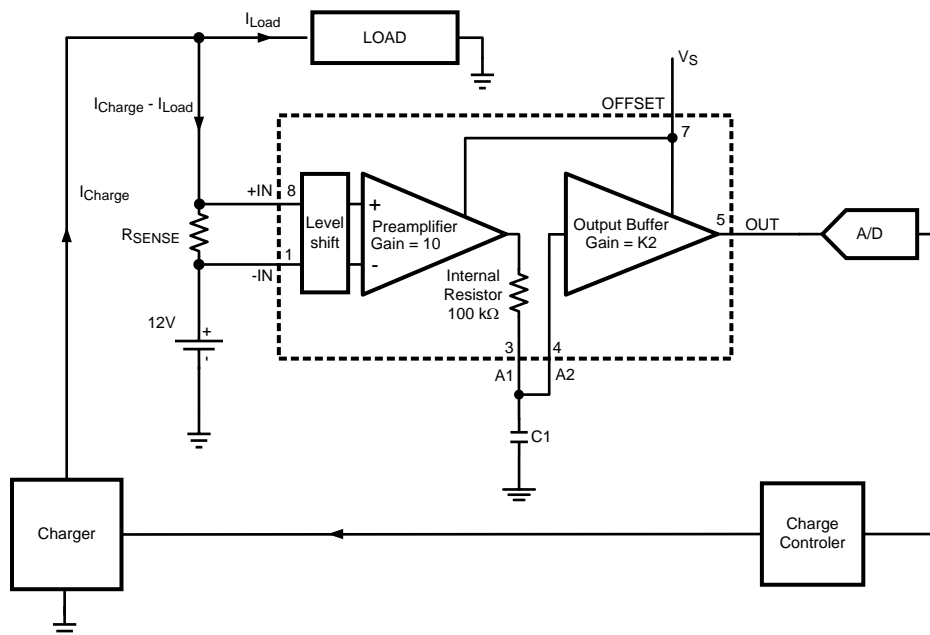
NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 63. Battery Current Monitor Application

Typical Applications (continued)

8.2.4 Advanced Battery Charger Application

Figure 63 can be used to realize an advanced battery charger that has the capability to monitor the exact net current that flows in and out the battery as show in Figure 64. The output signal of the LMP860x and LMP860x-Q1 is digitized with the ADC and used as an input for the charge controller. The Charge controller can be used to regulate the charger circuit to deliver exactly the current that is required by the load, avoiding overcharging a fully loaded battery.

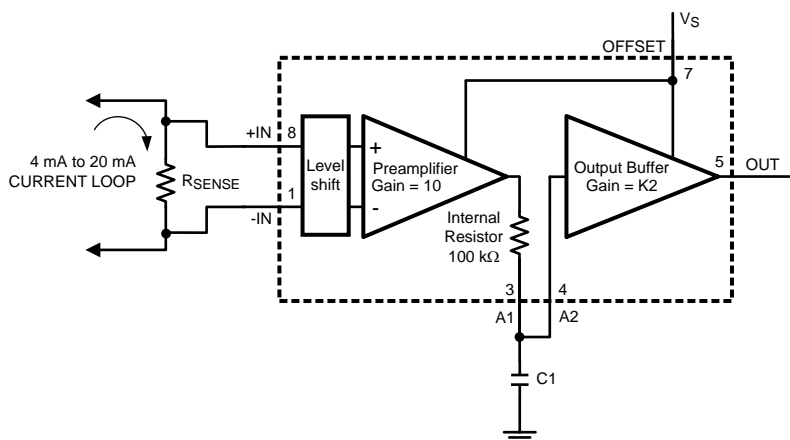


NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 64. Advanced Battery Charger Application

8.2.5 Current Loop Receiver Application

Many industrial applications use 4-mA to 20-mA transmitters to send an analog value of a sensor to a central control room. The LMP860x and LMP860x-Q1 can be used as a current loop receiver as shown in Figure 65.



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 65. Current-Loop Receiver Application

9 Power Supply Recommendations

In order to decouple the LMP860x and LMP860x-Q1 from AC noise on the power supply, place a 0.1- μ F bypass capacitor between the V_S and GND pins. Place this capacitor as close as possible to the supply pins. In some cases, an additional 10- μ F bypass capacitor may further reduce the supply noise.

10 Layout

10.1 Layout Guidelines

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors ($< 100\text{ m}\Omega$), any trace resistance shared with the load current can cause significant errors.

The amplifier inputs should be directly connected to the sense resistor pads using Kelvin or 4-wire connection techniques. The traces should be one continuous piece of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients.

To minimize noise pickup and thermal errors, the input traces should be treated as a differential signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these traces can contain high voltage, and should have the appropriate trace routing clearances.

Since the sense traces only carry the amplifier bias current, the connecting input traces can be thinner, signal level traces. Excessive Resistance in the trace should also be avoided.

The paths of the traces should be identical, including connectors and vias, so that any errors will be equal and cancel.

The sense resistor will heat up as the load increases. As the resistor heats up, the resistance generally goes up, which will cause a change in the readings. The sense resistor should have as much heatsinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting over time after turnon can usually be traced back to sense resistor heating.

10.2 Layout Example

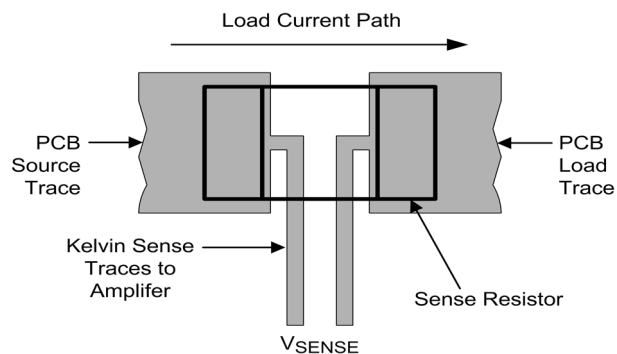


Figure 66. Kelvin or 4-wire Connection to the Sense Resistor

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

《LMP8601 TINA SPICE 模型》， [SNOM084](#)

TINA-TI 基于 SPICE 的模拟仿真程序， <http://www.ti.com.cn/tool/cn/tina-ti>

11.2 相关链接

表 1 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 1. 相关链接

| 器件 | 产品文件夹 | 样片与购买 | 技术文档 | 工具与软件 | 支持与社区 |
|------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| LMP8601 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| LMP8601-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| LMP8602 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| LMP8602-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| LMP8603 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| LMP8603-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用中所用 TI 产品的功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或使用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMP8601EDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 150 | LMP86 01EDQ1 | Samples |
| LMP8601MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 01MA | Samples |
| LMP8601MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 01MA | Samples |
| LMP8601QMA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 01QMA | Samples |
| LMP8601QMAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 01QMA | Samples |
| LMP8602MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 02MA | Samples |
| LMP8602MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 02MA | Samples |
| LMP8602MM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AN3A | Samples |
| LMP8602MME/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AN3A | Samples |
| LMP8602MMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AN3A | Samples |
| LMP8602QMA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 02QMA | Samples |
| LMP8602QMAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 02QMA | Samples |
| LMP8602QMM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AF7A | Samples |
| LMP8602QMME/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AF7A | Samples |
| LMP8602QMMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AF7A | Samples |
| LMP8603MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 03MA | Samples |
| LMP8603MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 03MA | Samples |
| LMP8603MM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AP3A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMP8603MME/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AP3A | Samples |
| LMP8603MMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AP3A | Samples |
| LMP8603QMA/NOPB | ACTIVE | SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 03QMA | Samples |
| LMP8603QMAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 03QMA | Samples |
| LMP8603QMM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AH7A | Samples |
| LMP8603QMMME/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AH7A | Samples |
| LMP8603QMMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AH7A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



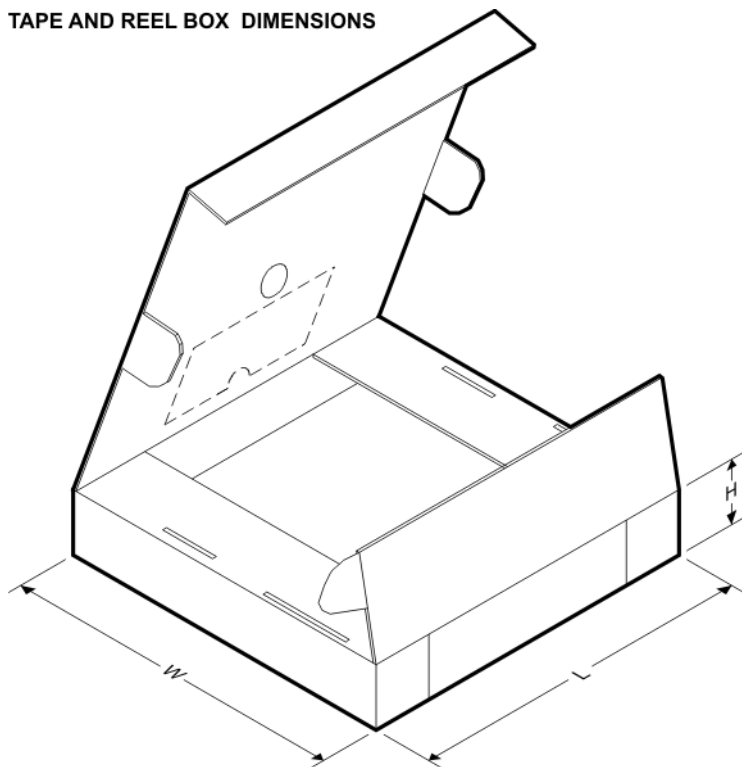
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMP8601EDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8601MAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8601QMAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8602MAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8602MM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8602MME/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8602MMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8602QMAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8602QMM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8602QMME/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8602QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8603MAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8603MM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8603MME/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8603MMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8603QMAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8603QMM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8603QMME/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMP8603QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMP8601EDRQ1 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8601MAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8601QMAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8602MAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8602MM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LMP8602MME/NOPB | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| LMP8602MMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LMP8602QMAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8602QMM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LMP8602QMME/NOPB | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| LMP8602QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LMP8603MAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8603MM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LMP8603MME/NOPB | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| LMP8603MMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LMP8603QMAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMP8603QMM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LMP8603QMME/NOPB | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| LMP8603QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI 均以“原样”提供技术性及其可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司