THP210 超低失调电压、高电压、低噪声、精密、全差分放大器

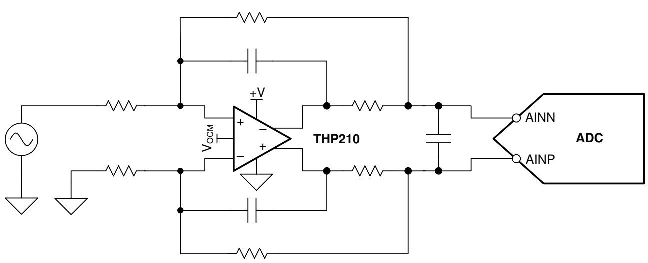
1 特性

- 输入失调电压：±40µV（最大值）
- 输入失调电压漂移：0.4µV/°C（最大值）
- 低电源电流：±18V 时为 950µA
- 低输入偏置电流：2nA（最大值）
- 低输入偏置电流漂移：15pA/°C（最大值）
- 增益带宽积：9.2MHz
- 差分输出压摆率：15V/µs
- 低输入电压噪声：1kHz 时为 3.7nV/√Hz
- 低 THD + N：10kHz 时为 –120dB
- 宽输入和输出共模范围
- 宽单电源工作电压范围：3V 至 36V
- 低电源电流断电特性：<20µA
- 放大器过载功率限制
- 电流限制
- 封装：8 引脚 VSSOP
- 温度范围：–40°C 至 +125°C

2 应用

- 数据采集 (DAQ)
- 模拟输入模块
- 变电站自动化
- 半导体测试
- 实验室和现场仪表

精密、低噪声、低功耗、全差分放大器增益模块和接口



3 说明

THP210 是一款超低失调电压、低噪声、高电压、精密、全差分放大器，可轻松过滤和驱动全差分信号链。THP210 还可用于将单端源转换为高分辨率模数转换器 (ADC) 所需的差分输出。双极性超级 ß 输入专为实现出色的失调电压、低噪声和 THD 而设计，可在极低的静态电流和输入偏置电流下产生极低的噪声系数。该器件专为要求低失调电压和功耗以及高信噪比 (SNR) 的信号调节电路而设计。

THP210 具有 高压电源功能，支持高达 ±18V 的电源电压。高压差分信号链可通过该功能提高裕量和动态范围，而无需为差分信号的每个极性添加单独的放大器。极低的电压和电流噪声使得 THP210 可用于高增益配置，而对信号保真度的影响最小。

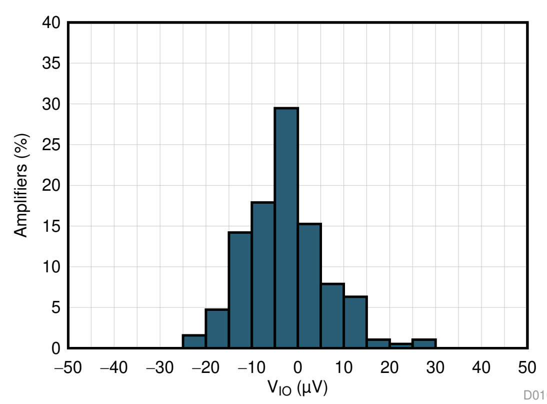
THP210 具有 –40°C 至 +125°C 的宽额定工作温度范围，并采用 8 引脚 VSSOP 封装。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
THP210	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

低输入失调电压



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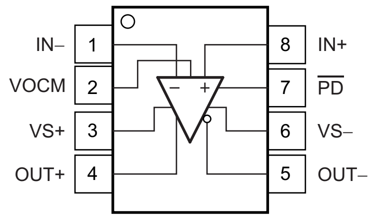
4 修订历史记录

日期	修订版本	说明
2020 年 2 月	*	初始发行版

5 Pin Configuration and Functions

**DGK Package
8-Pin VSSOP
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	1	I	Inverting (negative) amplifier input
IN+	8	I	Noninverting (positive) amplifier input
OUT–	5	O	Inverting (negative) amplifier output
OUT+	4	O	Noninverting (positive) amplifier output
$\overline{\text{PD}}$	7	I	Power down. $\overline{\text{PD}}$ = logic low = power off mode. $\overline{\text{PD}}$ = logic high = normal operation. The logic threshold is referenced to VS+. If power down is not needed, leave $\overline{\text{PD}}$ floating.
VOCM	2	I	Ouput common-mode voltage control input
VS–	6	I	Negative power-supply input
VS+	3	I	Positive power-supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply		40	V
		Dual supply		±20	V
	IN+, IN–, differential voltage[2]			±0.5	V
	IN+, IN–, VOCM, $\overline{PD}$, OUT+, OUT− voltage[3]		V_{VS-} – 0.5	V_{VS+} + 0.5	V
	IN+, IN− current		–10	10	mA
	OUT+, OUT− current		–50	50	mA
	Output short-circuit[4]			Continuous	
T_A	Operating temperature		–40	150	°C
T_J	Junction temperature		–40	175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins IN+ and IN– are connected with anti-parallel diodes in between the two terminals. Differential input signals that are greater than 0.5 V or less than –0.5 V must be current-limited to 10 mA or less.
(3) Input terminals are diode-clamped to the supply rails (VS+, VS–). Input signals that swing more than 0.5 V greater or less the supply rails must be current-limited to 10 mA or less.
(4) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	3		36	V
		Dual-supply	±1.5		±18	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		THP210 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	181.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±1.5 V to ±18 V, VOCM = 0 V, input common mode voltage (V_{ICM}) = 0 V, R_F = 2 kΩ, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input-referred offset voltage			10	±40	µV
		T_A = –40°C to 125°C			±80	µV
	Input offset voltage drift	T_A = –40°C to 125°C		0.1	±0.4	µV/°C
PSRR	Power-supply rejection ratio			0.025	0.25	µV/V
		T_A = –40°C to 125°C			0.5	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±2	nA
		T_A = –40°C to 125°C			±4	nA
	Input bias current drift	T_A = –40°C to 125°C		±2	±15	pA/°C
I_{OS}	Input offset current			±0.2	±1	nA
		T_A = –40°C to 125°C			±3	nA
	Input offset current drift	T_A = –40°C to 125°C		1	±10	pA/°C
NOISE						
e_n	Input differential voltage noise	f = 1 kHz		3.7		nV/√Hz
		f = 10 Hz		4		nV/√Hz
		f = 0.1 to 10 Hz		0.1		µVpp
e_i	Input current noise, each input	f = 1 kHz		300		fA/√Hz
		f = 10 Hz		400		fA/√Hz
		f = 0.1 to 10 Hz		13.4		pApp
INPUT VOLTAGE						
	Common-mode voltage range	T_A = –40°C to 125°C	V_{VS-} + 1		V_{VS+} – 1	V
CMRR	Common-mode rejection ratio	V_{VS-} + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V		140		dB
		V_{VS-} + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V, V_S = ±18 V	126	140		
		V_{VS-} + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V, V_S = ±18 V, T_A = –40°C to +125°C	120			
INPUT IMPEDANCE						
	Input impedance differential mode	V_{ICM} = 0 V		1 || 1		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = ±2.5 V, V_{VS-} + 0.2 V < V_O < V_{VS+} – 0.2 V	115	120		dB
		V_S = ±2.5 V, V_{VS-} + 0.3 V < V_O < V_{VS+} – 0.3 V, T_A = –40°C to +125°C	115	120		dB
		V_S = ±15 V, V_{VS-} + 0.6 V < V_O < V_{VS+} – 0.6 V	115	120		dB
		V_S = ±15 V, V_{VS-} + 0.6 V < V_O < V_{VS+} – 0.6 V, T_A = –40°C to +125°C	110	120		dB
FREQUENCY RESPONSE						
SSBW	Small-signal bandwidth	V_O = 100 mV_{PP}, G = –1 V/V		7		MHz
GBP	Gain-bandwidth product	V_O = 100 mV_{PP}, G = –10 V/V		9.2		MHz
FBP	Full-power bandwidth	V_O = –1 V_{PP}, G = –1 V/V		2.4		MHz
SR	Slew rate	G = –1, 10-V step		15		V/µs
	Settling time	To 0.1% of final value, G = –1 V/V, V_O = 10-V step		1		µs
		To 0.01% of final value, G = –1 V/V, V_O= 10-V step		2		µs

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Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±1.5 V to ±18 V, VOCM = 0 V, input common mode voltage (V_{ICM}) = 0 V, R_F = 2 kΩ, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion and Noise	Differential input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
	Total harmonic distortion and Noise	Single-ended input, f = 10 kHz, V_O = 10 V_{PP}		–115		dB
HD2	Second-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
HD3	Third-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}		–120		dB
	Overdrive recovery time	G = 5 V/V, 2x output overdrive, dc-coupled		3.3		µs
Z_O	Open-loop output impedance	f = 100 kHz (differential)		14		Ω
C_{LOAD}	Capacitive load drive	Differential capacitive load, no output isolation resistors, phase margin = 30°		50		pF
OUTPUT						
V_{OL}, V_{OH}	Output voltage range low, high	V_S = ±2.5 V		100		mV
		V_S = ±2.5 V, T_A = –40°C to 125°C		100		mV
		V_S = ±18 V		230		mV
		V_S = ±18 V, T_A = –40°C to 125°C		270		mV
I_{SC}	Short-circuit current			±31		mA
OUTPUT COMMON-MODE VOLTAGE						
	Small-signal bandwidth from VOCM pin	V_{VOCM} = 100 mV_{PP}		2		MHz
	Large-signal bandwidth from VOCM pin	V_{VOCM} = 0.6 V_{PP}		5.7		MHz
	Slew rate from VOCM pin	V_{VOCM} = 0.5-V step, rising		3.5		V/µs
		V_{VOCM} = 0.5-V step, falling		5.5		V/µs
	DC output balance	V_{VOCM} fixed midsupply (V_O = ±1 V)		78		dB
	Output balance SSBW	V_{VOCM} fixed midsupply, V_O / VOCM (–3 dB from dc)		TBD		kHz
	Output balance LSBW	V_{VOCM} fixed midsupply, V_O / VOCM with V_O = 5 V_{PP} (–3 dB from dc)		TBD		kHz
	VOCM Input Voltage Range	V_S = ±2.5 V	$V_{VS–}$ + 1		V_{VS+} – 1	
		V_S = ±18 V	$V_{VS–}$ + 2		V_{VS+} – 2	
	VOCM input impedance			2.5 || 1		MΩ || pF
	VOCM offset from mid-supply	V_{VOCM} pin floating, V_O = V_{ICM} = 0 V		±1		mV
	VOCM common-mode offset voltage	V_{VOCM} = V_{ICM}, V_O = 0 V		±1	±6	mV
		V_{VOCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C			±10	mV
	VOCM common-mode offset voltage drift	V_{VOCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C		±20	±60	µV/°C
POWER SUPPLY						
I_Q	Quiescent operating current			0.95	1.1	mA
		T_A = –40°C to +125°C			1.5	mA

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±1.5 V to ±18 V, VOCM = 0 V, input common mode voltage (V_{ICM}) = 0 V, R_F = 2 kΩ, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER DOWN						
$V_{\overline{PD}(HI)}$	Power-down enable voltage	T_A = –40°C to +125°C	V_{VS+} – 0.5			V
$V_{\overline{PD}(LOW)}$	Power-down disable voltage	T_A = –40°C to +125°C			V_{VS+} – 2.0	V
	$\overline{PD}$ bias current	$V_{\overline{PD}}$ = V_{VS+} – 2 V		1	2	µA
	Powerdown quiescent current			10	20	µA
	Turn-on time delay	Time to V_O = 90% of final value		10		µs
	Turn-off time delay	Time to V_O = 10% of original value		15		µs

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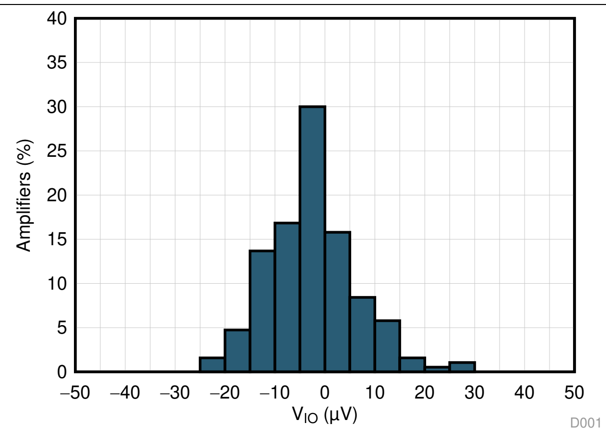
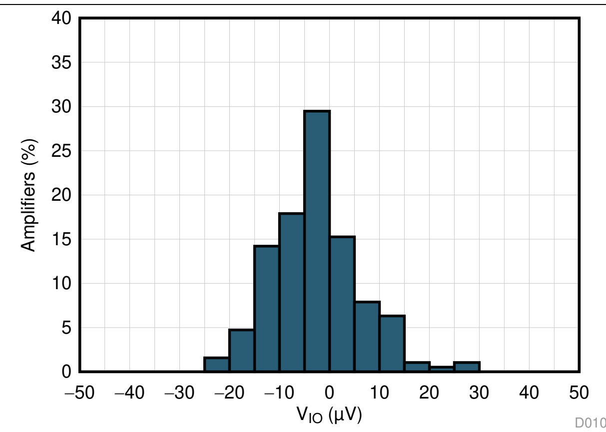
6.6 Typical Characteristics

at T_A = 25°C, V_{VOCM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, V_{OUT} = 2 V_{PP} G = 1 V/V, and $\overline{PD}$ = VS+ (unless otherwise noted)



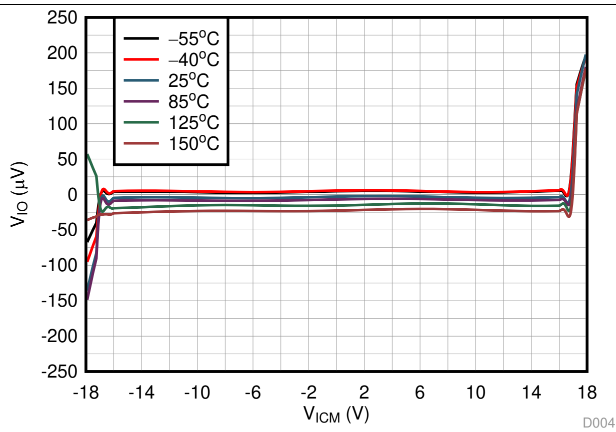
V_S = ±1.5 V

图 1. Input Offset Voltage Histogram



V_S = ±18 V

图 2. Input Offset Voltage Histogram



V_S = ±18 V

图 3. Input Offset Voltage vs Input Common Mode Voltage

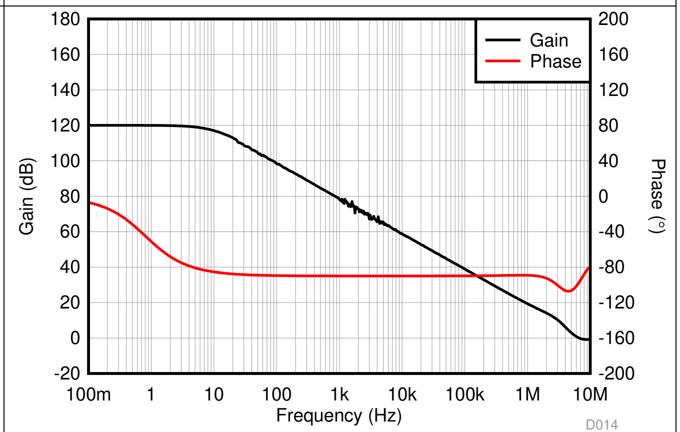


图 4. Open-Loop Gain and Phase

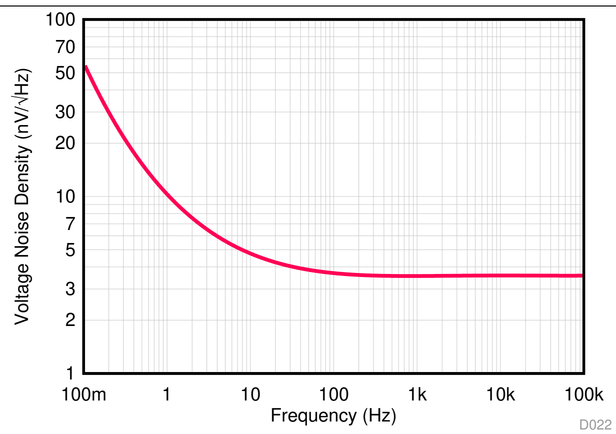


图 5. Input-Referred Voltage Noise vs Frequency

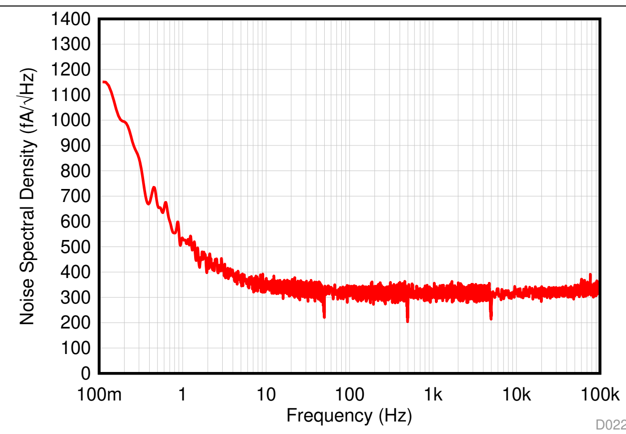


图 6. Current Noise vs Frequency

Typical Characteristics (接下页)

at T_A = 25°C, V_{VOCM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, V_{OUT} = 2 V_{PP} G = 1 V/V, and $\overline{VPD}$ = VS+ (unless otherwise noted)

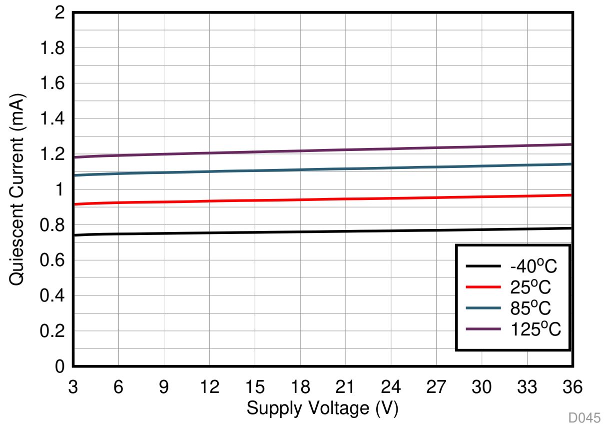


图 7. Quiescent Current vs Supply Voltage

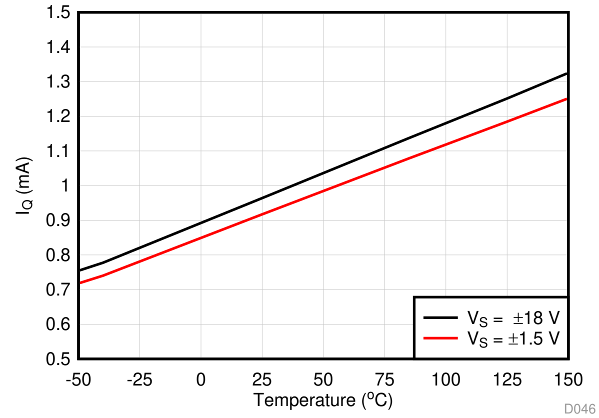


图 8. Quiescent Current vs Temperature

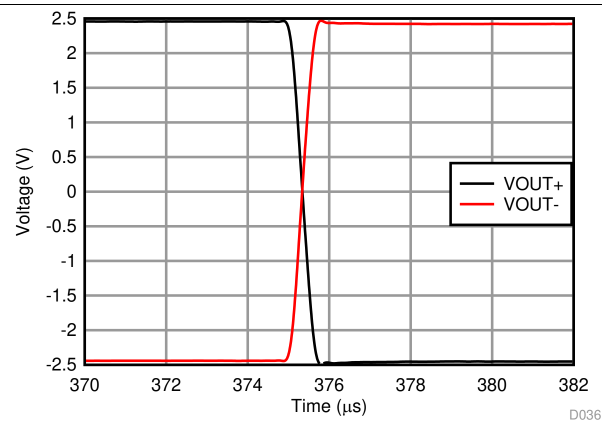


图 9. Large-Signal Step Response

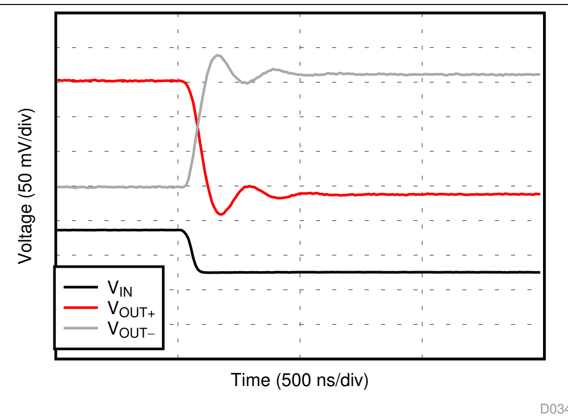
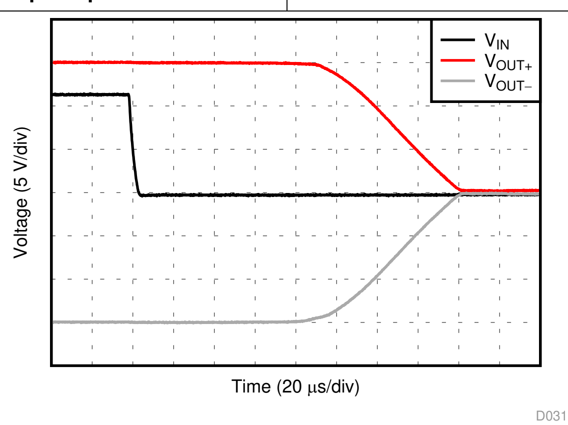


图 10. Small-Signal Step Response



V_S = ±15 V

图 11. Small-Signal Step Response

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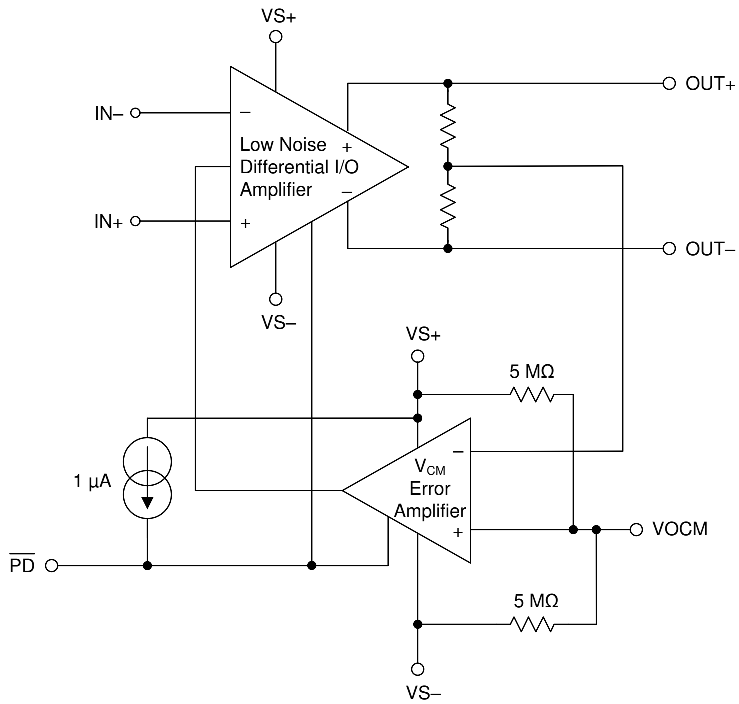
7 Detailed Description

7.1 Overview

The THP210 is a low-noise, low-distortion fully-differential amplifier (FDA) that features Texas Instrument's super-beta bipolar input devices. Super-beta input devices feature very low input bias current as compared to standard bipolar technology. The low input bias current and current noise makes the THP210 an excellent choice for high performance applications that require low-noise differential signal processing without significant current consumption. This device is also designed for analog-to-digital input circuits that require low offset and low noise in a single fully-differential amplifier. The THP210 features high-voltage capability, which allows the device to be used in ±15-V supply circuits without any additional voltage clamping or regulators. This feature enables a direct, single solution for a 24-dBm differential output drive without any additional amplification.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Super-Beta Input Bipolar Transistors

The THP210 is designed on a modern bipolar process that features TI's super-beta input transistors. Traditional bipolar transistors feature excellent voltage noise and offset drift, but suffer a tradeoff in high input bias current (I_B) and input bias current noise. Super-beta transistors offer the benefits of low voltage noise and offset drift with an order of magnitude reduction in input bias current and reduction in input bias current noise. For many filter circuits, input bias current noise can dominate in circuits where higher resistance input resistors are used. The THP210 enables a fully-differential, low-noise amplifier design without restrictions of low input resistance at a power level unmatched by traditional single-ended amplifiers.

7.3.2 Power Down

The THP210 features a power-down circuit to disable the amplifier when a low-power mode is required by the system. In the power-down state, the amplifier outputs are high-impedance, and the amplifier total quiescent current is reduced to less than 20 µA.

7.3.3 Flexible Gain Setting

The THP210 offers considerable flexibility in the configuration and selection of resistor values. Low input bias current and bias current noise allows for larger gain resistor values with minimal impact to noise or offset. The design starts with the selection of the feedback resistor value. The 2-kΩ feedback resistor value used for the characterization curves is a good compromise between power, noise, and phase margin considerations. With the feedback resistor values selected (and set equal on each side), the input resistors are set to obtain the desired gain, with input impedance also set with these input resistors. Differential I/O designs provide an input impedance that is the sum of the two input resistors. Single-ended input to differential output designs present a more complicated input impedance. Most characteristic curves implement the single-ended to differential design as the more challenging requirement over differential-to-differential I/O.

7.3.4 Amplifier Overload Power Limit

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (meaning the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The THP210 has an advanced output stage design that eliminates this problem. When the output voltage reaches the V_{VS+} or V_{VS-} voltage, there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by a large external transient voltage.

7.4 Device Functional Modes

The THP210 requires external resistors for correct signal-path operation. When setting the gain with these external resistors, the amplifier can be either on with the $\overline{PD}$ pin left floating, asserted to a voltage greater than V_{VS+} – 0.5 V, or turned off by forcing $\overline{PD}$ to a voltage lower than V_{VS+} – 2 V. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors, which provides poor signal isolation from the input to output in power-down mode.

Internal protection diodes remain present across the input pins in both operating and shutdown mode. Large input signals during disable can turn on the input differential protection diodes, thus producing a load current in the supply, even in shutdown.

The VOCM control pin sets the output average voltage. Left open, VOCM defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal V_{CM} error amplifier. If floated to obtain a default midsupply reference for VOCM, an external decoupling capacitor must be added on the VOCM pin to reduce the otherwise high output noise for the internal high-impedance bias.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Most applications for the THP210 strive to deliver the best dynamic range in a design that delivers the desired signal processing along with adequate phase margin for the amplifier itself. The following sections detail some of the design issues with analysis and guidelines for improved performance.

8.1.1 Driving Capacitive Loads

The capacitive load of an ADC or some other next-stage device is commonly required to be driven. Directly connecting a capacitive load to the output pins of a closed-loop amplifier such as the THP210 can lead to an unstable response. One typical remedy to this instability is to add two small series resistors (R_O) at the outputs of the THP210 before the capacitive load. Good practice is to leave a place for the R_O elements in a board layout (a 0-Ω value initially) for later adjustment, in case the response appears unacceptable.

8.1.2 Operating the Power-Down Feature

The power-down feature on the THP210 allows the device to be put into a low power-consumption state, in which quiescent current is minimized. To force the device into the low-power state, drive the $\overline{PD}$ pin to less than 2 V less than the positive supply voltage (V_{VS+} – 2 V). Driving the $\overline{PD}$ pin to less than 2 V forces the internal logic to disable both the differential and common-mode amplifiers. The $\overline{PD}$ pin has an internal pullup current that allows for the pin to be used in an open-drain MOSFET configuration without an additional pullup resistor, as seen in 图 12. In this configuration, the logic level can be referenced to the MOSFET, and the voltage at the $\overline{PD}$ pin is level-shifted to account for use with high supply voltages. Be sure to select an N-type MOSFET with a maximum B_{VDSS} greater than the total supply voltage.

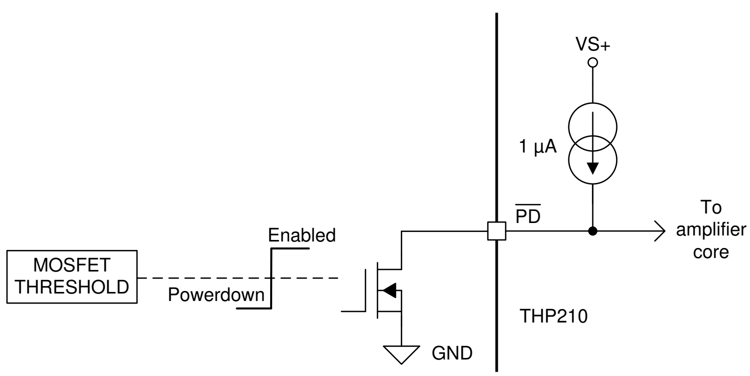

图 12. Power-Down ($\overline{PD}$) Pin Interface With Low-Voltage Logic Level Signals

For applications that do not use the power-down feature, tie the $\overline{PD}$ pin to the positive supply voltage.

When $\overline{PD}$ is low (device is in power down) the output pins will be in a high-impedance state.

Application Information (接下页)

8.1.3 Noise Performance

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground. 图 13 shows the simplest analysis circuit with the FDA and resistor noise terms to be considered.

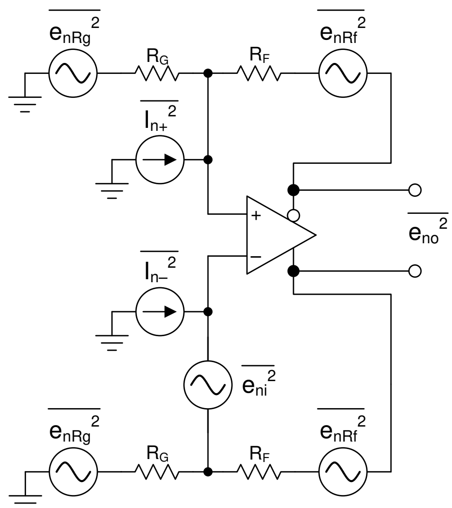

图 13. FDA Noise Analysis Circuit

The noise powers are shown in 图 13 for each term. When the R_F and R_G (or R_I) terms are matched on each side, the total differential output noise is the root sum squared (RSS) of these separate terms.

Using NG ≡ 1 + R_F / R_G, the total output noise is given by 公式 1.

Each resistor noise term is a 4kT × R power (4kT = 1.6E-20 J at 290 K).

$$e_o = \sqrt{(e_{ni}NG)^2 + 2(i_N R_F)^2 + 2(4kTR_F NG)} \quad (1)$$

The first term is simply the differential input spot noise times the noise gain, the second term is the input current noise terms times the feedback resistor (and because there are two uncorrelated current noise terms, the power is two times one of them), and the last term is the output noise resulting from both the R_F and R_G resistors, at again twice the value for the output noise power of each side added together. Running a wide sweep of gains when holding R_F to 2 kΩ gives the standard values and resulting noise listed in 表 1.

When the gain increases, the input-referred noise approaches only the gain of the FDA input voltage noise term at 3.7 nV/√Hz.

表 1. Swept Gain of the Output- and Input-Referred Spot Noise Calculations

GAIN (V/V)	R_F	R_{G1}	A_V	E_O (nV/√Hz)	E_I (nV/√Hz)
0.1	2000	20000	0.1	9.4	93.9
1	2000	2000	1	13.6	13.6
2	2000	1000	2	17.8	8.9
5	2000	402	4.98	29.5	5.9
10	2000	200	10	48.6	4.9

8.2 Typical Applications

8.2.1 An MFB Filter Driving an ADC Application

A common application use case for fully-differential amplifiers is to easily convert a single-ended signal into a differential signal to drive a differential input source, such as an ADC or class D amplifier. 图 14 shows an example of THP210 used to convert a single-ended low voltage signal source, such as a small electret microphone, and deliver a low-noise differential signal that is common-mode shifted to the center of the ADC input range. A multiple-feedback (MFB) configuration is used to provide a Butterworth filter response, giving a 40-dB/decade rolloff with a –3-dB frequency of 30 kHz.

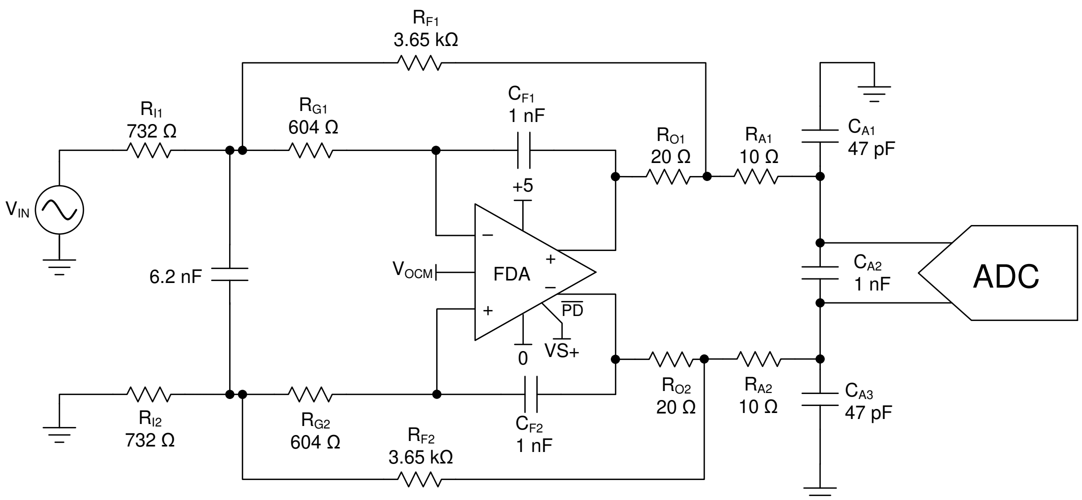

图 14. Example 30-kHz Butterworth Filter

8.2.1.1 Design Requirements

The requirements for this application are:

- Single-ended to differential conversion
- 5-V/V gain
- Active filter set to a Butterworth, 30-kHz response shape
- Output RC elements set by SAR input requirements (not part of the filter design)
- Filter element resistors and capacitors are set to limit added noise over the THP210 and noise peaking

8.2.1.2 Detailed Design Procedure

The design proceeds using the techniques and tools suggested in the *Design Methodology for MFB Filters in ADC Interface Applications* application note. The process includes:

- Scale the resistor values to not meaningfully contribute to the output noise produced by the THP210.
- Select the RC ratios to hit the filter targets when reducing the noise gain peaking within the filter design.
- Set the output resistor to 10 Ω into a 1-nF differential capacitor.
- Add 47-pF common-mode capacitors to the load capacitor to improve common noise filtering.
- Inside the loop, add 20-Ω output resistors after the filter feedback capacitor to increase the isolation to the load capacitor.

ADVANCE INFORMATION

Typical Applications (接下页)

8.2.1.3 Application Curve

The gain and phase plots are shown in 图 15. The MFB filter features a Butterworth responses feature very flat passband gain, with a 2-pole rolloff at 30 kHz to eliminate any higher-frequency noise from contaminating the signal chain and potentially alias back into the desired band.

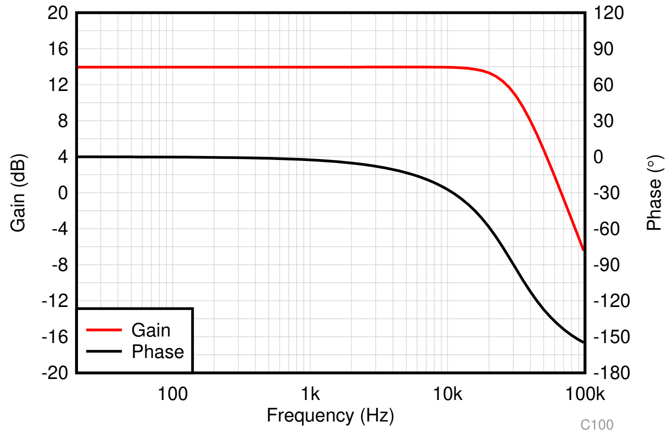

图 15. Gain and Phase Plot for a 30-kHz Butterworth Filter

ADVANCE INFORMATION

9 Power Supply Recommendations

The THP210 operates from supply voltages of 3.0 V to 36 V (±1.5 V to ±18 V, dual supply). Connect ceramic bypass capacitors from both VS+ and VS– to GND.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations

- Keep differential signals routed together to minimize parasitic impedance mismatch.
- Connect a 0.1-µF capacitor to the supply nodes through a via.
- Connect a 0.1-µF capacitor to the VOCM pin if no external voltage is used.
- Keep any high-frequency nodes that can couple through parasitic paths away from the VOCM node.
- Clean the PCB board after assembly to minimize any leakage paths from excess flux into the VOCM node.

10.2 Layout Example

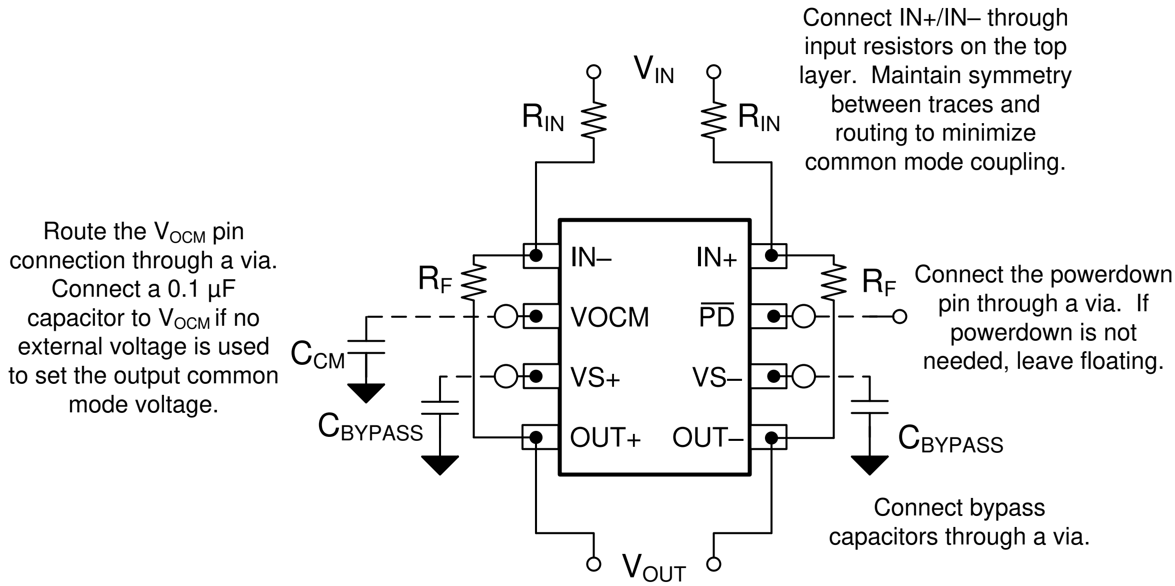

图 16. Example Layout

ADVANCE INFORMATION

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

- THP210 TINA-TI™ 模型
- *TINA-TI 增益为 0.2 的 100kHz 巴特沃斯 MFB 滤波器*
- *TINA-TI 100kHz MFB 滤波器 LG 测试*
- *TINA-TI 差分跨阻 LG 仿真*

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《INA188 高精度、零漂移、轨至轨输出、高电压仪表放大器》* 数据表
- 德州仪器 (TI)，*《具有 e-trim™ 的 OPAx192 36V 高精度、轨至轨输入/输出、低失调电压、低输入偏置电流运算放大器》* 数据表
- 德州仪器 (TI)，*《OPA161x SoundPlus™ 高性能、双极输入音频运算放大器》* 数据表
- 德州仪器 (TI)，*《ADC 接口应用中 MFB 滤波器的 应用》* 应用报告
- 德州仪器 (TI)，*《宽带差分跨阻 DAC 输出设计》* 应用报告

11.3 接收文档更新通知

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11.4 支持资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THP210DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1237	Samples
THP210DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1237	Samples
THP210DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	THP210	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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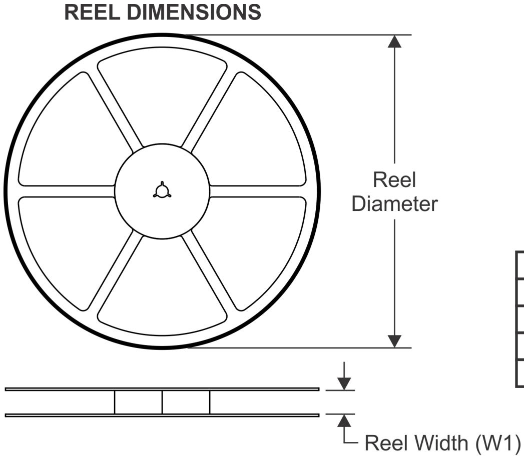
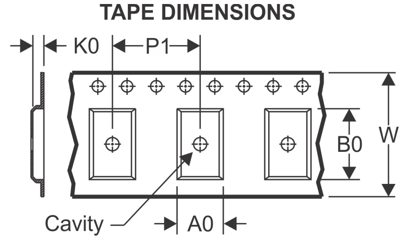
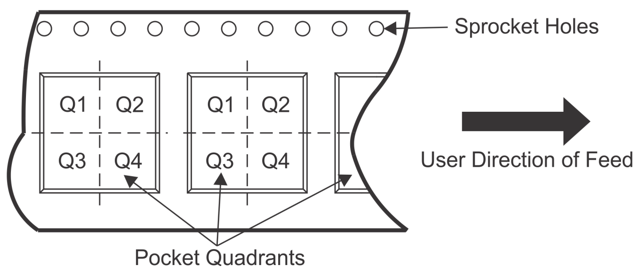
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

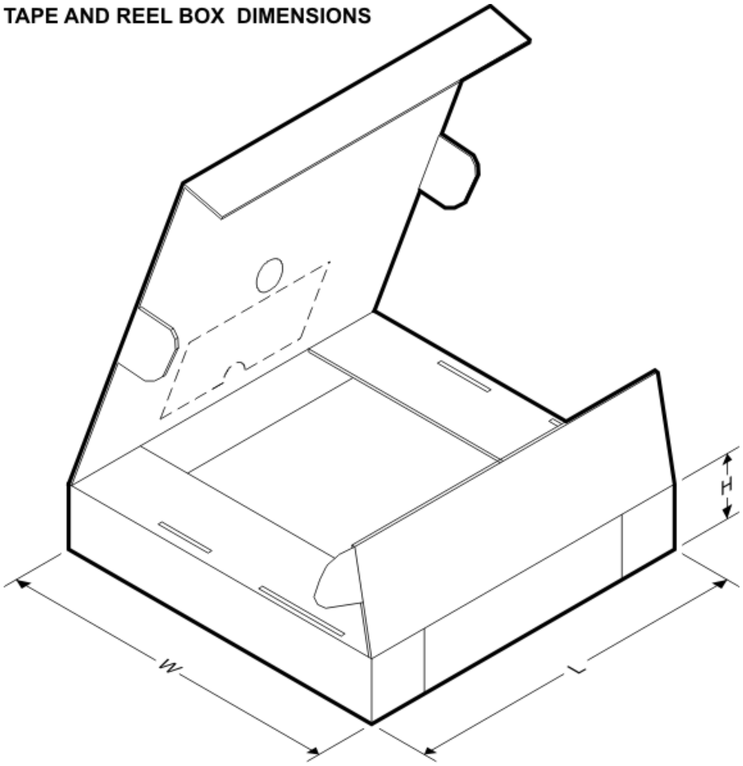
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

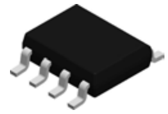
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THP210DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THP210DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THP210DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THP210DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THP210DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
THP210DR	SOIC	D	8	2500	853.0	449.0	35.0

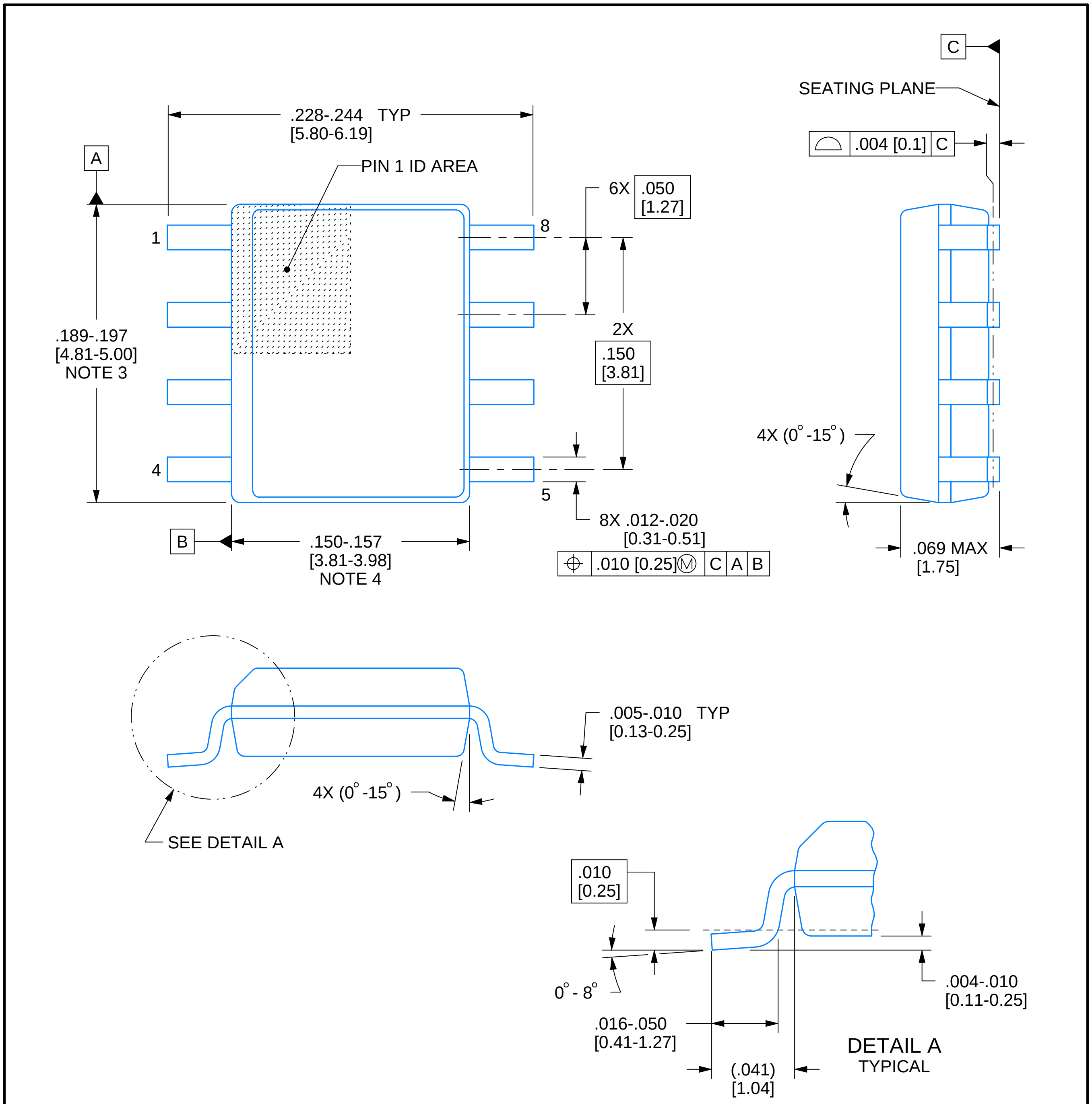


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

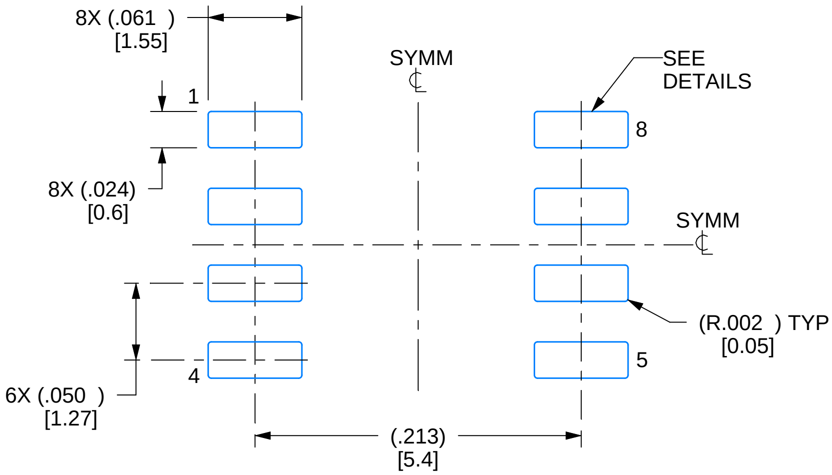
SMALL OUTLINE INTEGRATED CIRCUIT



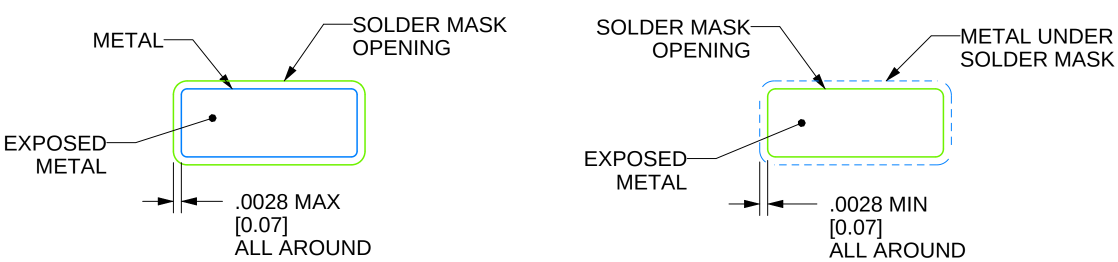
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

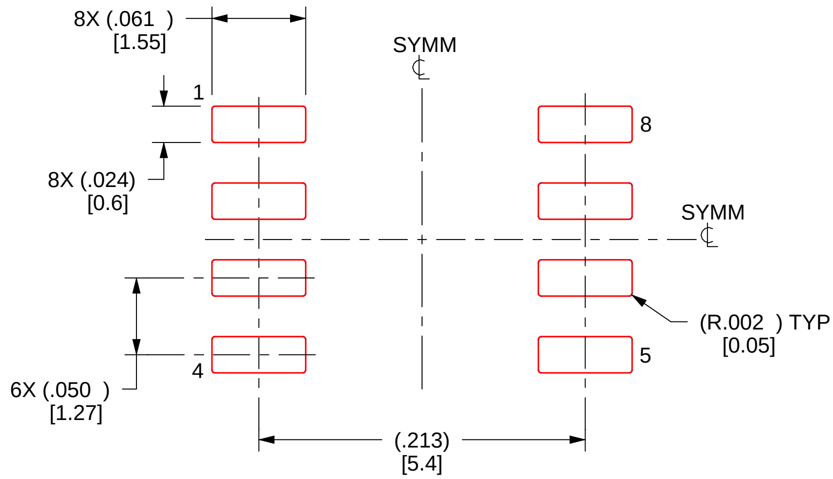
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



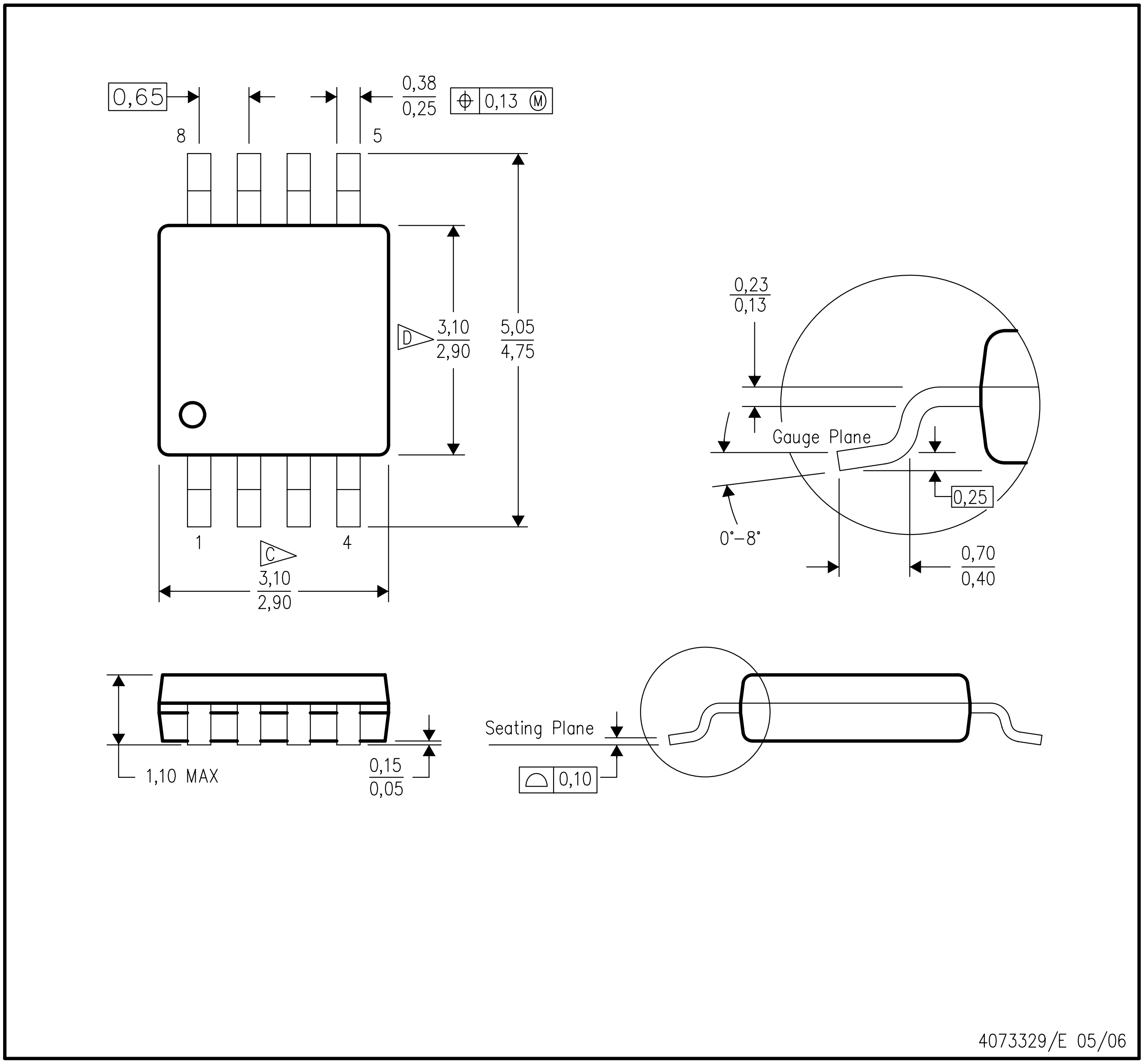
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

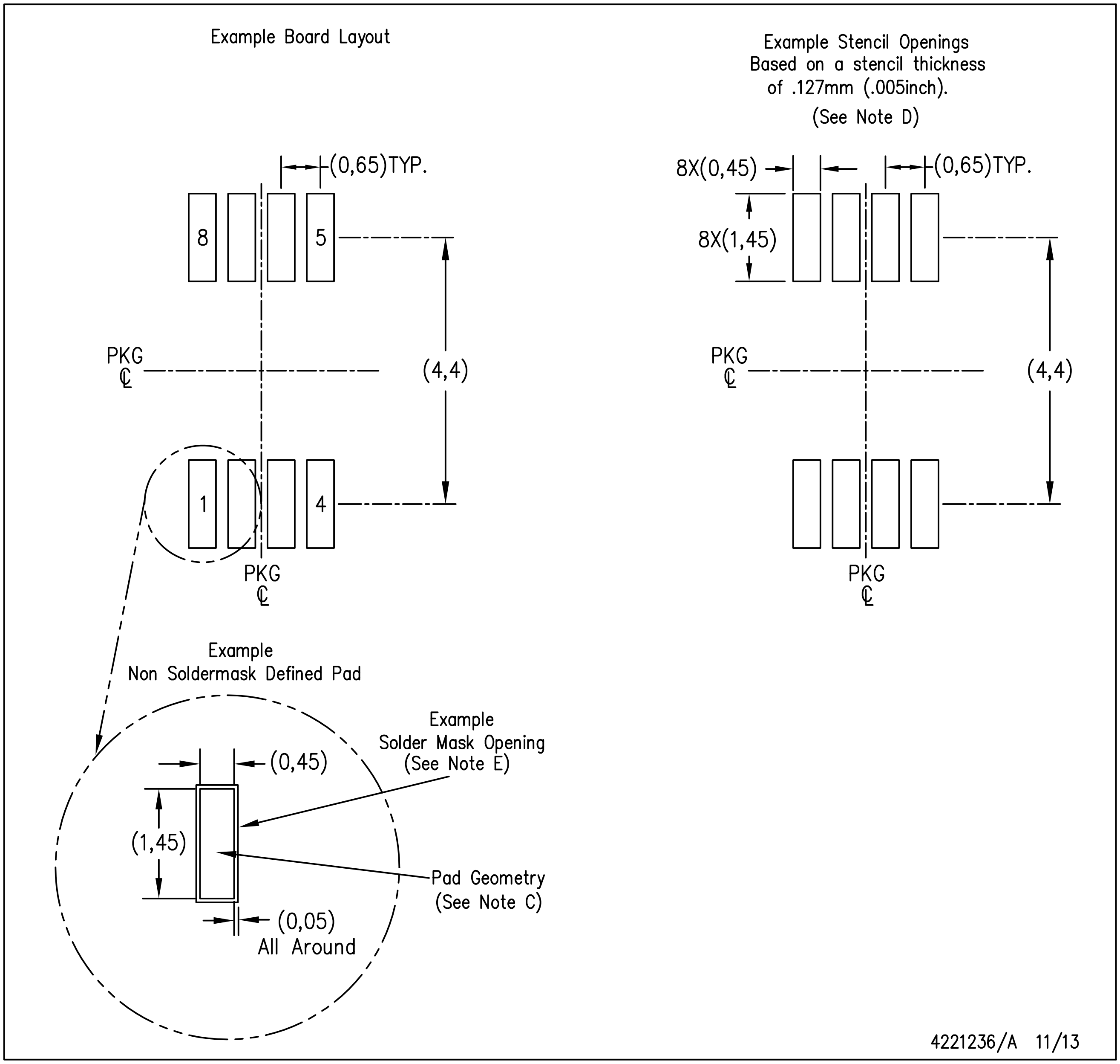
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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