TPS54122 3A QuietSupply™稳压器
（带有集成式直流/直流转换器和低噪声 LDO）

1 特性

- 输入电压范围：
  - V_{IN}：2.95V 至 6V
  - LDOIN：V_{OUT} + V_{DO} 至 5.5V
  - BIAS：2.375V 至 5.5V
- 提供高效低噪声电源轨
- 独立启用，电源正常，软启动
- 3A 高效同步降压开关：
  - 可调节输出电压低至 0.8V
  - 同步至外部时钟：300kHz 至 2MHz
  - 1% 参考精度
- 3A 低噪声低压降稳压器 (LDO)：
  - 输出噪声：17µV$_{RMS}$，10Hz 到 1MHz，直流/直流运行
  - 输出电压范围：0.8V 至 3.6V
  - 超低压降：3A 时为 100mV（典型值）
  - 1% 输出精度
  - 出色的负载和线路瞬态响应
- 小型封装：5.50mm × 3.50mm VQFN-24

2 应用

- 测试和测量
- 医疗成像设备
- 电信基础设施
- 微基站和节点基站
- 供电射频 (RF) 部件：压控振荡器 (VCO)，接收器，模数转换器 (ADC)
- 专业音频

3 说明

TPS54122 器件将高效的降压开关（直流/直流）转换器与高电源抑制 (PSR)、低噪声、低压差稳压器 (LDO) 相结合，可提供超低噪声电源，从而为噪声敏感型应用提供 QuietSupply 轨。

TPS54122 非常适合使用 5V 电源总线的系统，通过直流/直流或 LDO 输出支持 3A 连续输出电流。可在 0.8V 到 3.6V 范围内设置 LDO 输出电压，并可使用外部电阻器在 0.83V 到 5V 范围内调节直流/直流转换器电压。该器件可用于广泛的低噪声 应用， 因为其直流/直流转换器和 LDO 完全可配置。此外，TPS54122 还包括以下 特性 ，如软启动、开关频率同步和电源正常信号等。
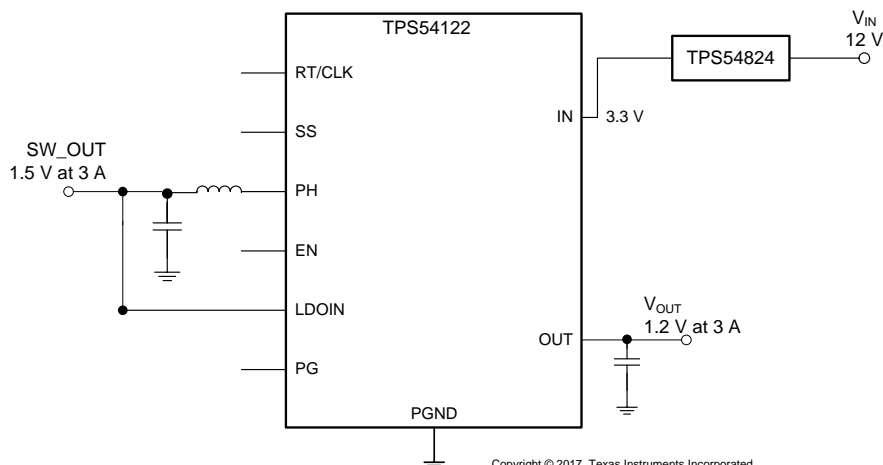
通过将直流/直流转换器的输出馈送到 LDO 的输入，TPS54122 可以提供高效、低噪声的电源，最高可达 3A。

TPS54122 可用于节省空间的 5.50mm × 3.50mm 的 VQFN 封装中，额定工作环境温度范围为 –40°C 到 +125°C。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TPS54122	VQFN (24)	5.50mm × 3.50mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路

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4 修订历史记录

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5 Pin Configuration and Functions

**RHL Package
24-Pin VQFN
Top View**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	22	—	Ground return for DC-DC control circuitry of the DC-DC converter
BIAS	11	—	Bias input supply to the LDO error amplifier and reference, and internal control circuits. An input capacitor of 1-μF or greater is recommended for optimal performance.
BOOT	5	—	A bootstrap capacitor is required between the BOOT and PH pins. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET of the DC-DC converter.
COMP	1	O	Input to the output switch current comparator and DC-DC error amplifier output. Connect the external compensation to this pin.
EN	7	I	Enable pin for DC-DC converter. This pin can be left floating to enable the device or can be used with two external resistors to set the undervoltage lockout threshold.
FB	16	I	This pin is the input to the control-loop error amplifier of the LDO and is used to set its output voltage.
GND	13	—	LDO ground
LDOEN	12	I	Enable pin for the LDO. Note that the LDOEN pin must not be left floating; connect this pin to LDOIN if not used.
LDOIN	8, 9	I	LDO input. An input capacitor of 1-μF or greater is recommended for optimal performance.
NC	14, 23	—	No internal connection, can be left floating or connected as needed.
NR	15	—	LDO noise reduction pin. Connect an external capacitor between this pin and LDO ground to reduce output noise and set the V_{OUT} ramp rate of the LDO.
OUT	17, 18	O	LDO output. A 1-μF or larger capacitor is required for stability.
PG	10	O	Open-drain, power-good fault pin of the LDO. Asserts low as a result of thermal shutdown, undervoltage, LDOEN shutdown, or during a slow start of the LDO. If not used, this pin can be left open or grounded.
PGND	21	—	Return for the DC-DC control circuitry and low-side power MOSFET of the DC-DC converter.
PH	4	O	DC-DC converter switch node; connect the inductor and boot capacitor to this pin.
PWRGD	6	O	Open-drain, power-good fault pin of the DC-DC converter. Asserts low as a result of thermal shutdown, undervoltage, overvoltage, EN pin shutdown, or during a soft-start of the DC-DC converter.
RT/CLK	2	I	In RT mode, adding an external timing resistor to this pin adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock signal.
SS	3	I	Soft-start pin. Connect an external capacitor to this pin to set the internal reference voltage rise time for the DC-DC converter. The voltage on this pin overrides the DC-DC converter internal reference.
VIN	19, 20	I	Supplies the power and control circuitry of the DC-DC converter. Use at least a 4.7-μF ceramic capacitor for decoupling.
VSENSE	24	I	Inverting input of the g_M error amplifier of the DC-DC converter.
Thermal pad		—	GND; for best noise and thermal performance, connect the thermal pad to GND and to a large printed circuit board (PCB) ground pad for thermal dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	VIN, EN, PWRGD	−0.3	7	V
	PH	−0.6	7	V
	PH (10-ns transient)	−2	10	V
	BOOT	−0.3	PH + 7	V
	BOOT − PH	0	7	V
	LDOIN, LDOEN, BIAS, PG, NR, FB, RT/CLK	−0.3	6	V
	OUT	−0.3	V_{LDOIN} + 0.3	V
	VSENSE, COMP, SS	−0.3	3	V
Current	OUT	Internally limited		A
	RT/CLK, EN, SS	−100	100	µA
	PH	Internally limited		A
	PVIN	Internally limited		A
	COMP	−100	100	µA
	PWRGD (sinking)	−0.1	10	mA
Temperature	Storage, T_{stg}	−55	150	°C
	Operating junction, T_J	−40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage range	VIN	2.95		6	V
		BIAS	2.375		5.5	V
		LDOIN	V_O + $V_{DO(LDOIN)}$		5.5	V
		EN	0		6	V
		LDOEN	0		5.5	V
$I_{(OUTDC-DC)}$	DC-DC output current		0		3	A
$V_{(OUTLDO)}$	LDO output voltage		V_{FB}		3.6	V
$I_{(OUTLDO)}$	LDO output current		0		3	A
T_A, T_J	Operating free-air temperature		−40		125	°C
C_{VIN}	DC-DC input		4.7			µF
C_{LDOIN}	LDO input capacitor		1			µF
C_{BIAS}	Bias input capacitor		1			µF
$C_{OUT(LDO)}$	LDO output capacitor		1			µF
C_{BST}	Bootstrap capacitor		0.1			nF

6.4 Thermal Information

THERMAL METRIC[1]		TPS54122	UNIT
		RHL (VQFN)	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	39.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Electrical Characteristics

at T_J = –40°C to +125°C, V_{BIAS} = V_{VIN} = 5 V, V_{LDOIN} = DC-DC_OUT[1] = 2.1 V, V_{LDOEN} = 1.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, and C_{OUT} = 10.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{VIN}	VIN pin input voltage range		2.95		6	V
	UVLO threshold			2.6	2.8	V
$I_{SD(VIN)}$	VIN pin shutdown current	V_{EN} < 0.3 V		2		µA
$I_{(OP)}$	VIN pin operating current (no switching)	V_{VSENSE} = 900 mV		360	575	µA
DC-DC BOOT (BOOT PIN)						
	(V_{BOOT} – V_{PH}) UVLO			2.2		V
	Boot charge resistance	V_{EN} = 3 V		16		Ω
DC-DC CONVERTER ENABLE (EN PIN)						
$V_{IL(EN)}$	EN pin low-level input voltage	Falling		1.18		V
$V_{IH(EN)}$	EN pin high-level input voltage	Rising		1.25		V
I_{EN}	EN pin input current	V_{EN} = 1.13 V		1.2		µA
		V_{EN} = 1.3 V		4.6		µA
DC-DC CONVERTER VOLTAGE REFERENCE						
V_{ref}	Reference voltage	2.95 V ≤ V_{VIN} ≤ 6 V	0.802	0.827	0.852	V
DC-DC MOSFET						
R_{HS}	High-side switch resistance	V_{BOOT} – V_{PH} = 5 V		45	81	mΩ
		V_{BOOT} – V_{PH} = 2.95 V		64	110	mΩ
R_{LS}	Low-side switch resistance	V_{VIN} = 5 V		42	81	mΩ
		V_{VIN} = 2.95 V		59	110	mΩ
DC-DC ERROR AMPLIFIER						
I_{IN}	Input current	V_{EN} = 3 V		7		nA
g_M	Error amplifier transconductance	–2 µA ≤ I_{COMP} ≤ 2 µA, V_{COMP} = 1 V		245		µMho
	Error amplifier transconductance during slow-start operation	–2 µA ≤ I_{COMP} ≤ 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		79		µMho
I_{COMP}	Error amplifier output current	V_{COMP} = 1 V, 100-mV input overdrive		±20		µA
	COMP pin to I_{SWITCH} g_M			18		A/V
DC-DC CURRENT LIMIT						
	High-side current limit	V_{VIN} = 3 V	4.2	6.6		A
DC-DC SOFT-START (SS PIN)						
	SS pin charge current	V_{SS} = 0.4 V		2.2		µA
	SS pin to VSENSE pin matching	V_{SS} = 0.4 V		35		mV

(1) DC-DC_OUT refers to the regulated output voltage of the switching regulator (see Figure 27).

Electrical Characteristics (continued)

at T_J = –40°C to +125°C, V_{BIAS} = V_{VIN} = 5 V, V_{LDOIN} = DC-DC_OUT[1] = 2.1 V, V_{LDOEN} = 1.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, and C_{OUT} = 10.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC POWER GOOD (PWRGD PIN)						
	VSENSE pin threshold	VSENSE falling (fault)		0.91 V_{ref}		V
		VSENSE rising (good)		0.93 V_{ref}		V
		VSENSE rising (fault)		1.07 V_{ref}		V
		VSENSE falling (good)		1.05 V_{ref}		V
	High-level output leakage current	V_{VSENSE} = V_{ref}, V_{PWRGD} = 5.5 V, V_{EN} = 3 V		2		nA
	Low-level output voltage	I_{PWRGD} = 3 mA		0.3	0.6	V
	Minimum VIN voltage for valid output	V_{PWRGD} < 0.5 V at 100 µA		1.2	1.6	V
LDO						
V_{LDOIN}	LDO input voltage range		$V_O + V_{DO}$		5.5	V
V_{BIAS}	LDO bias input voltage range		2.375		5.5	V
V_{FB}	FB pin voltage	T_A = 25°C	0.796	0.8	0.804	V
V_O	OUT pin voltage range		V_{FB}		3.6	V
	OUT pin voltage accuracy	V_O = V_{FB}, 50 mA ≤ I_O < 3 A, 2.97 V ≤ V_{BIAS} ≤ 5.25 V, V_{LDOIN} ≥ $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} ≥ $V_{OUT(nom)}$ + 1.62 V	–1.0%	±0.2%	1.0%	
$\Delta V_{O(\Delta IL)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.013		%/mA
		50 mA ≤ I_{OUT} ≤ 3 A		0.03		%/A
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 V ≤ V_{LDOIN} ≤ 5.5 V		0.0005	0.06	%/V
$V_{DO(LDOIN)}$	V_{LDOIN} dropout voltage	I_O ≤ 3.0 A, V_{BIAS} − $V_{OUT(nom)}$ ≥ 1.62 V		100	200	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage	I_O ≤ 3.0 A, V_{LDOIN} = V_{BIAS}			1.62	V
I_{LIM}	Output current limit	V_O = 0.8 × $V_{OUT(nom)}$	3.8		6.0	A
I_{BIAS}	BIAS pin current			2	4	mA
$I_{SD(LDO)}$	Shutdown current (I_{BIAS})	V_{EN} < 0.4 V		1	100	µA
I_{FB}	FB pin current		–250	95	250	nA
I_{LDOEN}	LDOEN pin input current	V_{EN} = 5 V		0.1	1	µA
$V_{IL(LDOEN)}$	LDOEN pin low-level input voltage (disable)				0.4	V
$V_{IH(LDOEN)}$	LDOEN pin high-level input voltage (enable)		1.1			V
	PG pin trip threshold	V_{FB} decreasing	0.86 V_{FB}	0.90 V_{FB}	0.94 V_{FB}	V
	PG pin trip hysteresis			0.03 V_{FB}		V
	High-level output leakage current	V_{PG} = 5.25 V		0.03	1	µA
	Low-level output voltage	I_{PG} = 1 mA			0.3	V
I_{NR}	NR pin charging current	V_{NR} = 0.4 V	0.5	0.73	1	µA
THERMAL SHUTDOWN						
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		°C
NOISE						
V_n	Output noise voltage	BW = 10 Hz to 1 MHz, C_{NR} = 10 µF, C_{FB} = 0.1 µF, I_O = 1 A , C_{OUT} = 100 µF		17		µV$_{RMS}$

6.6 Timing Requirements

at V_{BIAS} = V_{VIN} = 5 V, and T_J , T_A= –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Minimum on-time	Measured at 50% points on PH, I_O = 3 A		65		ns
		Measured at 50% points on PH, I_O = 0 A		120		ns
	Minimum off-time	Prior to skipping off pulses, V_{BOOT} − V_{PH} = 2.95 V, I_O = 3 A		60		ns
t_R	Rise time	V_{VIN} = 5 V, I_O = 3 A		2.5		V/ns
t_F	Fall time	V_{VIN} = 5 V, I_O = 3 A		2		V/ns

6.7 Switching Characteristics

at V_{BIAS} = V_{VIN} = 5 V, and T_J , T_A= –40°C to +125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching frequency range (RT mode set point and PLL mode)		300		2000	kHz
Switching frequency	R_{RT} = 400 kΩ (1%)	400	500	600	kHz
Switching frequency range in CLK mode		300		2000	kHz
RT/CLK pin high threshold				2.2	V
RT/CLK pin low threshold		0.4			V
PLL lock-in time			14		µs
RT/CLK pin falling edge to PH pin rising edge delay	Measure at 500 kHz with RT resistor in series		90		ns

6.8 Typical Characteristics

At V_{VIN} = V_{BIAS}= V_{LDOEN}= 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 27), unless otherwise noted.

NOTE: Y-axis shows a 1% V_{OUT} per division.
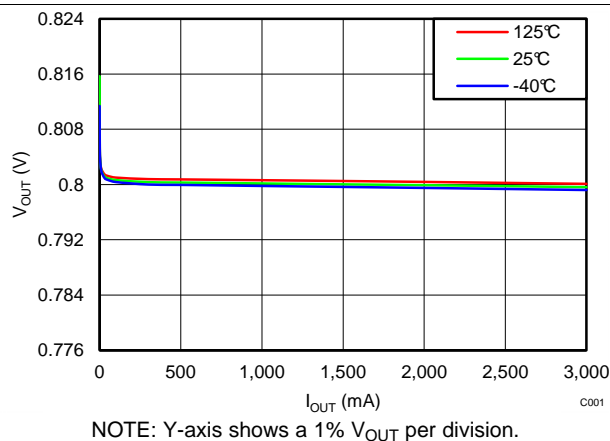
Figure 1. Load Regulation

NOTE: Y-axis shows a 1% V_{OUT} per division.
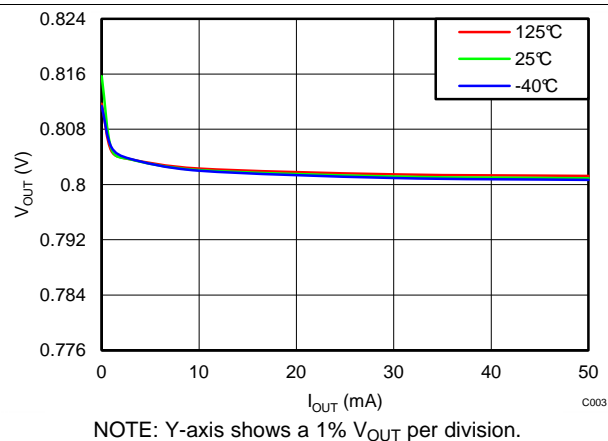
Figure 2. Load Regulation Under Light Loads

NOTE: Y-axis shows a 1% V_{OUT} per division.
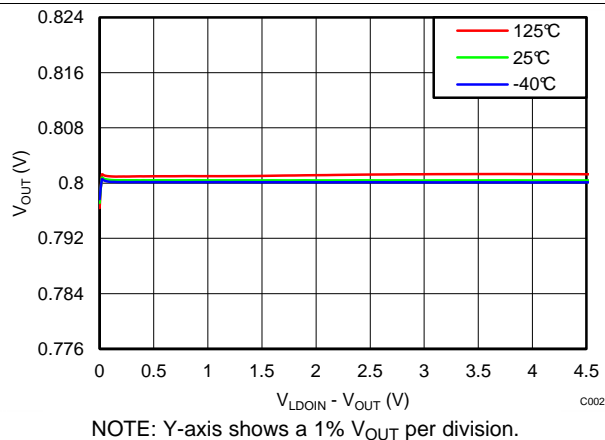
Figure 3. LDOIN Line Regulation

NOTE: Y-axis shows a 1% V_{OUT} per division.
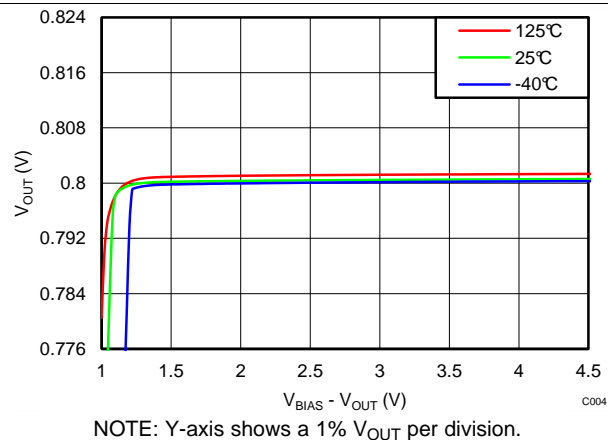
Figure 4. LDO Bias Line Regulation

I_O = 3 A
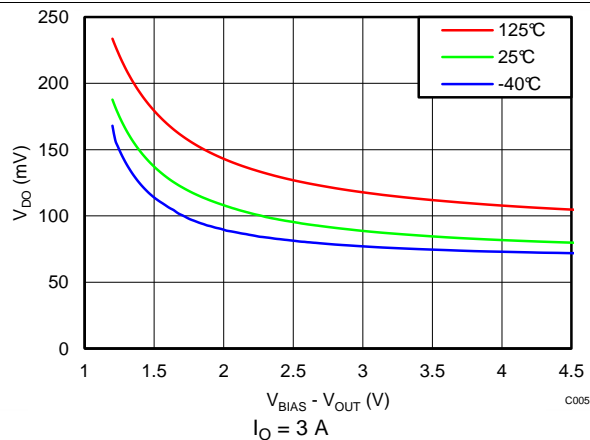
Figure 5. LDO Dropout Voltage vs LDO Bias Voltage

I_O = 500 mA

Figure 6. LDO Power-Supply Ripple Rejection vs LDO Dropout Voltage

Typical Characteristics (continued)

At V_{VIN} = V_{BIAS}= V_{LDOEN}= 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 27), unless otherwise noted.

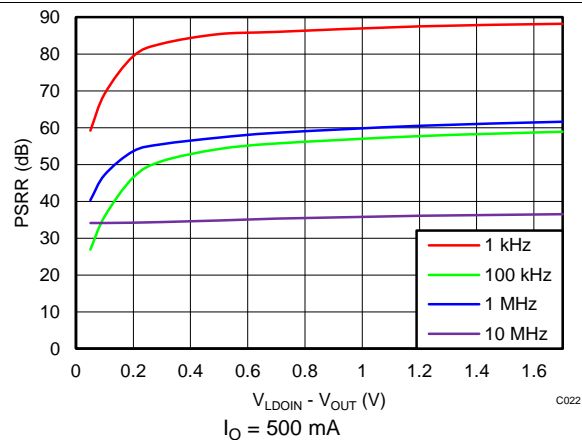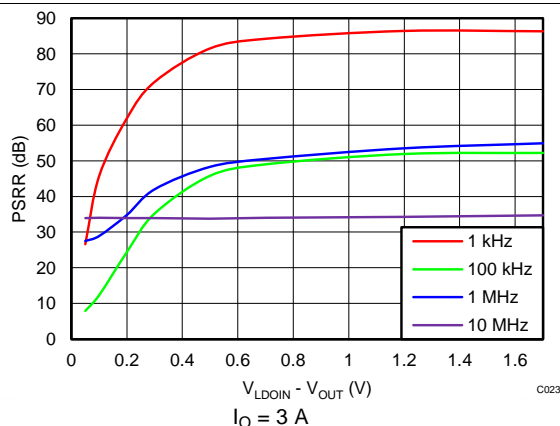**Figure 7. LDO Power-Supply Ripple Rejection vs LDO Dropout Voltage**
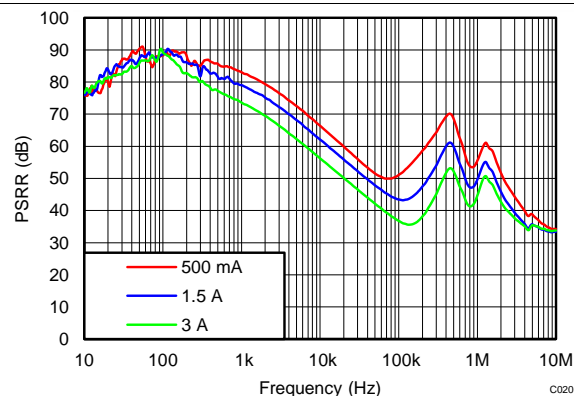
Figure 8. LDO Power-Supply Ripple Rejection vs Frequency
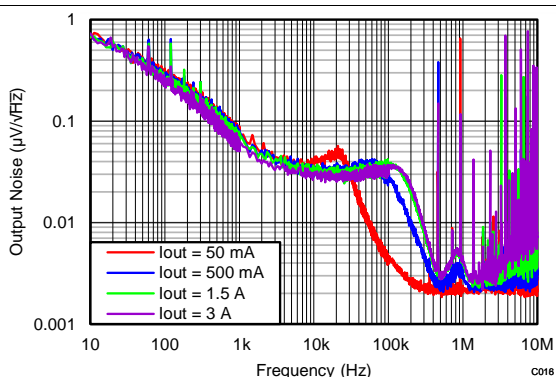
C_{OUT} = 122 µF, C_{NR} = 1 µF, RMS noise = 100 Hz to 100 kHz,
50-mA I_O = 9 μV_{RMS}, 500-mA I_O = 11 μV_{RMS}, 1.5-A I_O = 11 μV_{RMS},
3-A I_O = 10 μV_{RMS}

Figure 9. Output Spectral Noise Density vs Frequency (LDO Powered by DC-DC)
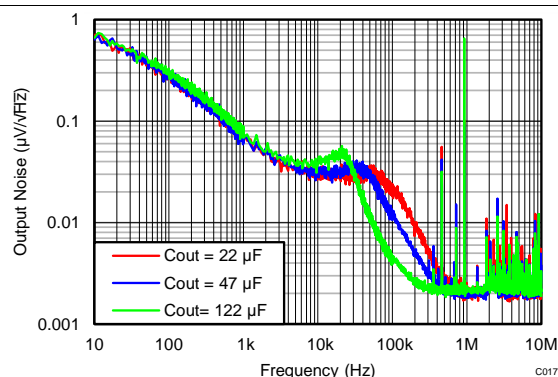
C_{NR} = 1 µF, RMS noise = 100 Hz to 100 kHz,
22-µF C_{OUT} = 10 μV_{RMS}, 47-µF C_{OUT} = 9 μV_{RMS},
122-µF C_{OUT} = 9 μV_{RMS}

Figure 10. Output Spectral Noise Density vs Frequency (LDO Powered by DC-DC)
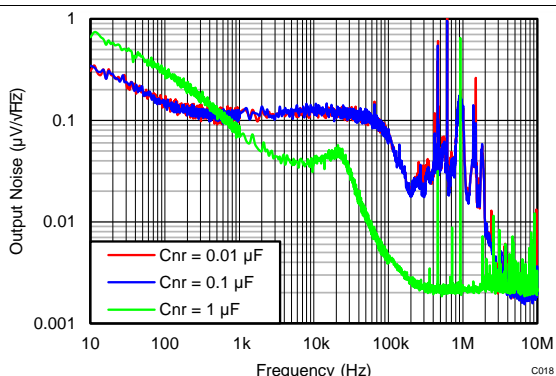
C_{OUT} = 122 µF, RMS noise = 100 Hz to 100 kHz,
0.01-µF C_{NR} = 33 μV_{RMS}, 0.1-µF C_{NR} = 33 μV_{RMS},
1-µF C_{NR} = 9 μV_{RMS}

Figure 11. Output Spectral Noise Density vs Frequency (LDO Powered by DC-DC)
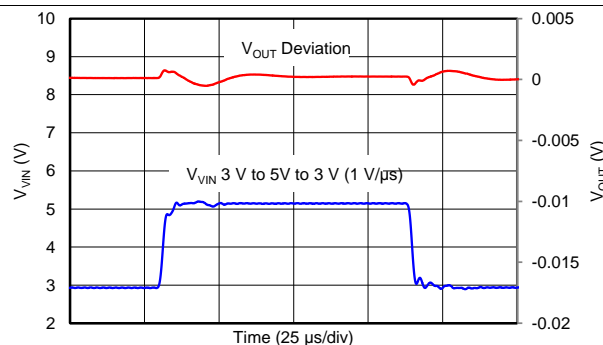
Figure 12. LDO Line Transient Response

Typical Characteristics (continued)

At V_{VIN} = V_{BIAS} = V_{LDOEN} = 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 μF, and C_{SS} = C_{NR} = 0.01 μF (see Figure 27), unless otherwise noted.
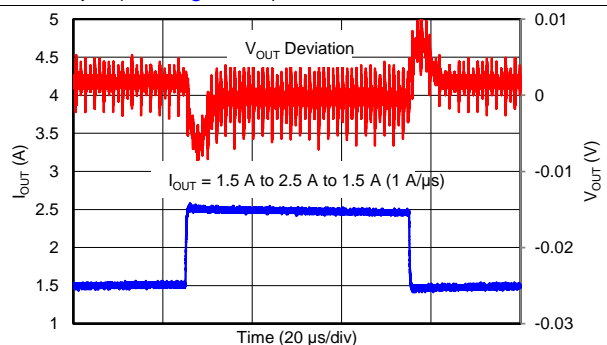
Figure 13. DC-DC Load Transient Response
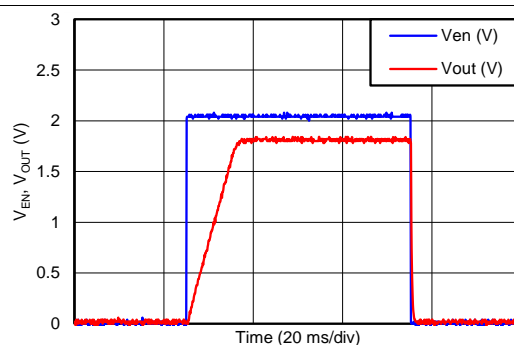
R_{LOAD} = 1.8 Ω

Figure 14. LDO Enable Pulse Response
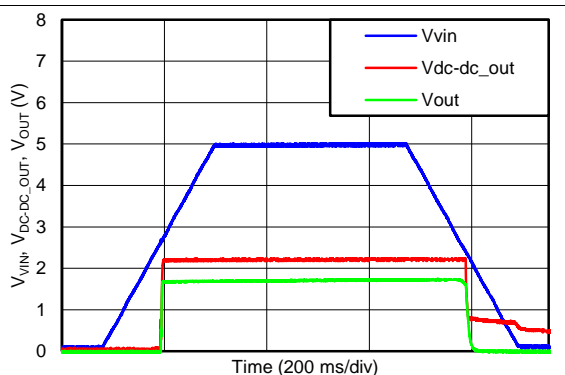
V_{EN} = V_{VIN}, V_{LDOEN} = V_{DC-DC_OUT}

**Figure 15. Power-Up and Power-Down Response
(LDO Powered by DC-DC)**
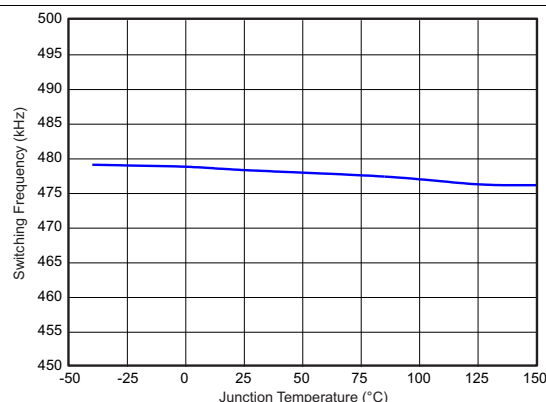
RT = 400 kΩ, V_I = 5 V

Figure 16. DC-DC Switching Frequency vs Temperature
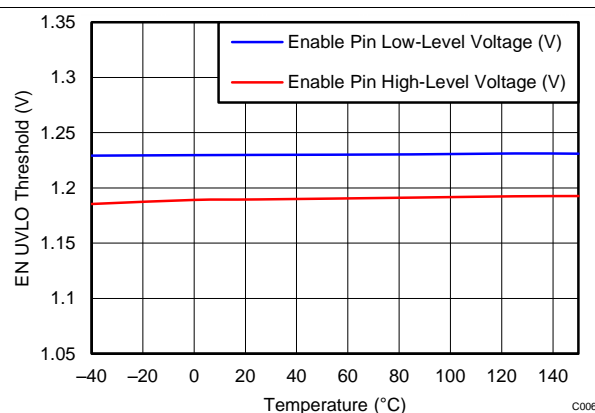
Figure 17. DC-DC EN UVLO Threshold vs Temperature
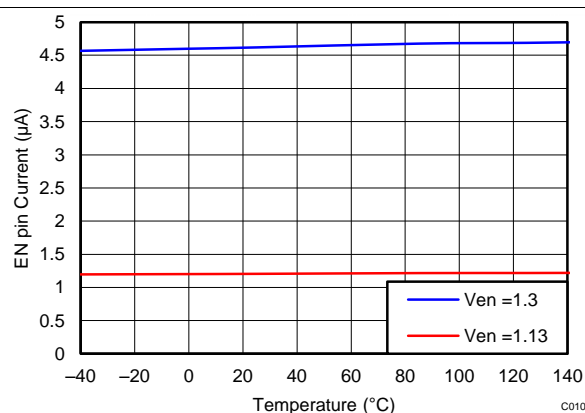
Figure 18. Enable Pin Current vs Temperature

Typical Characteristics (continued)

At V_{VIN} = V_{BIAS} = V_{LDOEN} = 5 V, V_{LDOIN} = DC-DC_OUT = 2.1 V, V_O = 1.8 V, I_O = 50 mA, V_{EN} = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 27), unless otherwise noted.
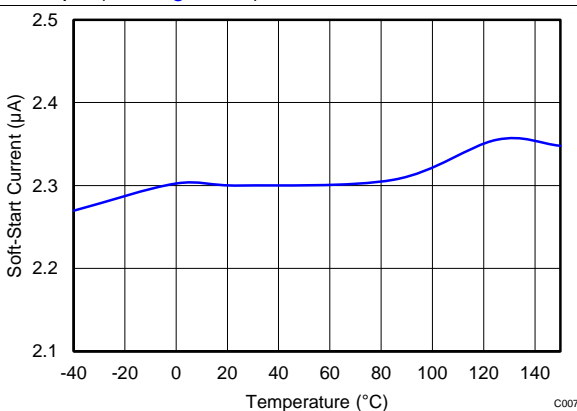
Figure 19. DC-DC Soft-Start Current vs Temperature
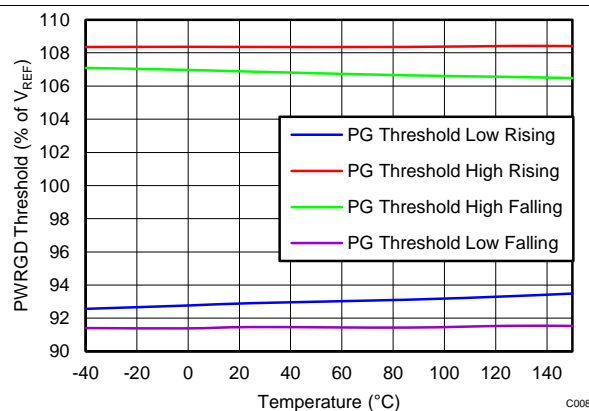
Figure 20. LDO PG Threshold vs Temperature
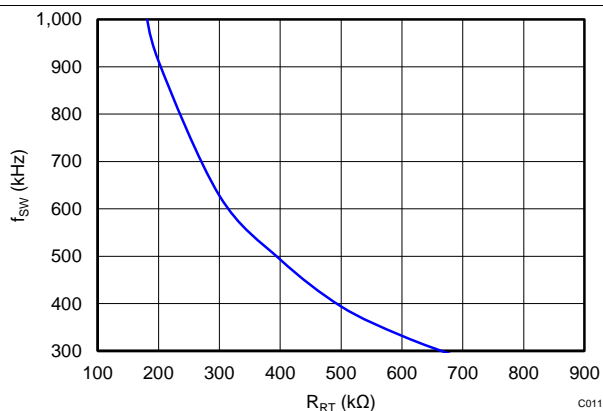
Figure 21. DC-DC Switching Frequency vs R$_{RT}$
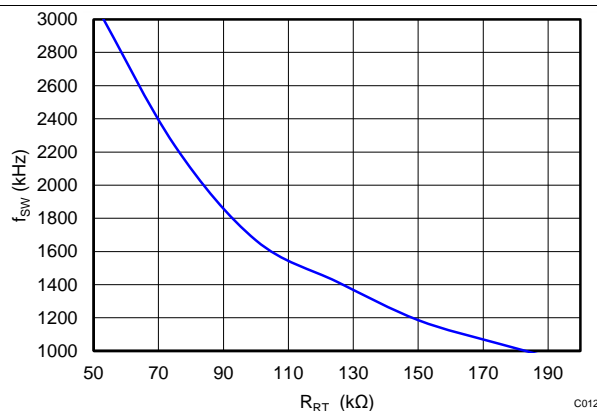
Figure 22. DC-DC Switching Frequency vs R$_{RT}$
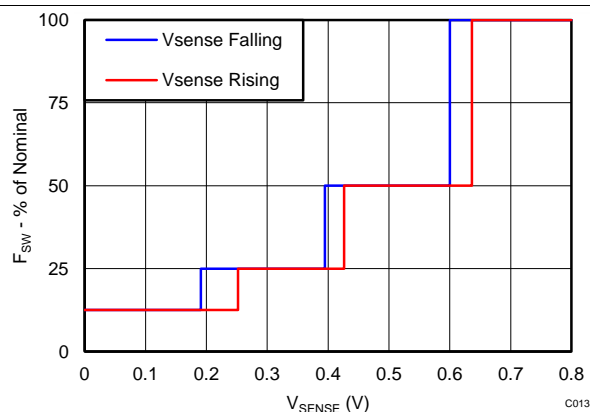
Figure 23. Switching Frequency vs V$_{SENSE}$
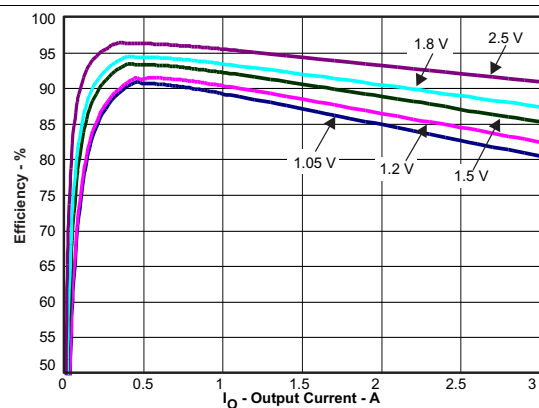
Figure 24. DC-DC Efficiency vs Output Current

7 Detailed Description

7.1 Overview

The TPS54122 device is a low-noise power supply that delivers a quiet power rail to noise-sensitive components. This device combines a current-mode-controlled, DC-DC, step-down regulator, and a low-noise, wide-bandwidth, low-dropout regulator (LDO) to create an efficient, stable, low-noise power supply. The TPS54122 device is fully characterized for noise performance, allowing for easy creation of a quiet power supply. The device includes features such as soft-start, clock synchronization, and a power-good signal, making the TPS54122 device well suited as a power supply for communication, test and measurement, and audio-equipment applications. The integrated switching regulator and LDO are fully configurable, allowing for complete design flexibility.

7.2 Functional Block Diagram
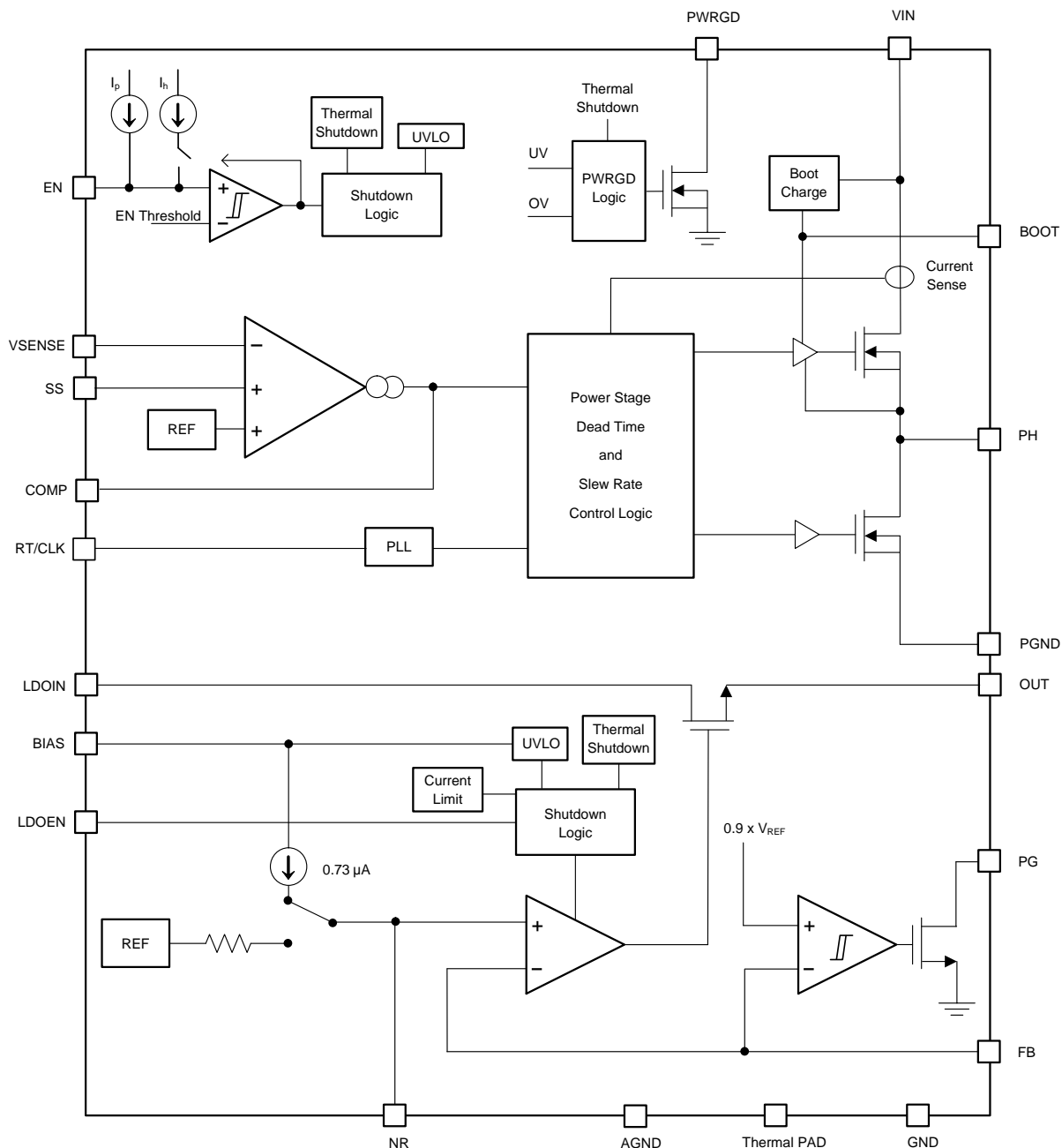
7.3 Feature Description

7.3.1 Input Voltage Range

7.3.1.1 DC-DC Input Voltage (VIN)

The TPS54122 VIN pin provides power to the DC-DC control circuitry and the DC-DC power stage. Use a voltage divider connected from the VIN pin to the EN pin to set an undervoltage lockout (UVLO) for the DC-DC regulator to provide consistent power-up behavior; see *Device Enable and Undervoltage Lockout Adjustment* for more information. Decouple the VIN pin to PGND with a 4.7-µF ceramic capacitor.

7.3.1.2 LDO Input Voltage (LDOIN)

The LDOIN pin provides power to the pass device of the LDO. The minimum input operating voltage that can be applied to the LDOIN pin of the TPS54122 device is V_{LDOIN} = [V_{OUT} + V_{DO}]. The voltage into this pin must not exceed 6.0 V. This pin is designed to be connected to the output capacitor of the integrated switcher; decouple this pin to the GND pin with a 1.0-µF ceramic capacitor.

7.3.1.3 LDO Bias Input Voltage (BIAS)

The BIAS pin provides power to the control circuitry of the LDO. The BIAS voltage requires additional voltage headroom over the LDOIN voltage to allow the control circuitry to operate the N-channel pass device. The minimum input operating voltage that can be applied to the BIAS pin is 2.375 V, or V_{OUT} + 1.62 V, whichever is greater. Therefore, when V_{OUT} = 1.5 V, LDOIN can be set as low as 1.8 V and BIAS can be set to 3.3 V, ±5%. In the majority of applications, the BIAS pin can be connected to the capacitors at the VIN pin of the TPS54122 device. High levels of noise on the bias pin can cause various problems with the device. Proper PCB layout and decoupling capacitance must be used to reduce the noise at the BIAS pin. TI recommends placing a capacitor of 1-µF or greater from this pin to ground.

7.3.2 Dual Adjustable Output Voltages

The output voltage of the switcher and the LDO are adjustable. The output voltages are set with a resistor divider from the output voltage to the feedback sensing pins (VSENSE or FB). Use 1% tolerance or better divider resistors for the best accuracy.

The LDO feedback resistor values can be calculated using Equation 1:

$$R_1 = (V_{OUT} / V_{ref} - 1) \times R_2$$

where:

- V_{ref} = 0.8 V,
- R_1 = the resistor from the output to the FB pin of the LDO, and
- R_2 = the resistor from the FB pin to ground of the LDO.   (1)

The switching regulator feedback resistor value can be calculated using Equation 2:

$$R_5 = (DC\text{-}DC\_OUT / V_{ref}) \times R_6$$

where:

- V_{ref} = 0.827 V,
- R_5 = the resistor from the switcher output at the inductor to the VSENSE pin, and
- R_6 = the resistor from the VSENSE pin to the ground-switching regulator.   (2)

To improve efficiency at light loads, consider using larger-value resistors. Larger-value resistors increase the noise sensitivity at the VSENSE and FB pins and error from the VSENSE and FB pin input currents. Using a value of 10 kΩ for R_1 and R_5 provides a good trade-off between noise and light load efficiency.

Feature Description (continued)

7.3.3 Power Conversion Efficiency versus Output Noise

The TPS54122 configuration consists of a switching regulator followed by an LDO. The ability of the LDO to reject noise created by the switching regulator (and instead of passing the noise to the LDO output) is determined by the power-supply rejection (PSR) of the LDO. The PSR of an LDO depends on the LDO input to LDO output voltage difference. The higher the voltage difference, the better the LDO ability to reject noise at the input. The LDO in the TPS54122 device is designed to provide high, wide-bandwidth PSR with a minimum of input-to-output voltage differential. At 3 A for the highest PSR performance, set the input-to-output voltage differential to 0.5 V or greater.

The LDO input-to-output voltage differential is a primary contributor to the overall power loss in the TPS54122 device. The contribution of the LDO input and output voltage differentials to the power loss is defined as the output current multiplied by the input-to-output voltage differential, as shown in Equation 3:

$$\text{Power Loss from the LDO} = I_{OUT} \times [V_{LDOIN} - V_{OUT}] \tag{3}$$

Therefore, for a 0.5-V drop at 1.5 A, this loss is 0.75 W. Reduce the impact of the power loss by lowering $V_{LDOIN} - V_{OUT}$. In the *Typical Characteristics* section, Figure 6 and Figure 7 illustrate the trade-off between PSR and $V_{LDOIN} - V_O$ for various output current levels and frequencies. For currents less than 1 A, a $V_{LDOIN} - V_O$ of 0.3 V does not have significant impact on PSR performance and provides a substantial improvement to the power loss from the $V_{LDOIN} - V_O$.

7.3.4 DC-DC Output Overvoltage Transient Protection (OVTP)

The TPS54122 device has an overvoltage transient protection (OVTP) circuit on the DC-DC switcher output to minimize overshoots on the DC-DC switcher output. This circuit protects the input of the LDO from experiencing overshoot above the rated values.

CAUTION
Any voltage above the absolute maximum rated input voltage into the LDOIN pin can damage the device.

The OVTP feature minimizes overshoot by comparing the V_{SENSE} pin voltage to the OVTP threshold (107% of the DC-DC V_{ref}). If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops below the OVTP threshold, the high-side MOSFET is enabled at the next clock cycle.

7.3.5 Overcurrent Protection

The TPS54122 device provides multiple forms of overcurrent protection, as discussed in this section.

7.3.5.1 Switcher Overcurrent Protection

The integrated switcher of the TPS54122 is protected from overcurrent conditions by using a cycle-by-cycle current limit. During each switching cycle, the high-side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current crosses the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current until the error amplifier output reaches the internally clamped voltage, which then functions as the switch current limit.

7.3.5.1.1 Frequency Division

In addition to a current limit on the high-side switch, the TPS54122 device implements a switching-frequency division technique to allow the low-side MOSFET to be turned off long enough to reduce the current in the inductor to prevent current runaway. During an overcurrent condition, the frequency division reduces the frequency from 100% to 50%, then to 25%, and finally to 12.5%. The overcurrent condition is detected by the decreasing voltage on the V_{SENSE} pin. Figure 23 illustrates the frequency reduction based on the V_{SENSE} voltage reduction. During startup, the switching frequency increases corresponding to the voltage on the V_{SENSE} pin increasing from 0 V to 0.827 V.

Feature Description (continued)

7.3.5.1.2 Reverse Overcurrent Protection for the Low-Side FET

The TPS54122 device implements low-side current protection by detecting the voltage drop across the low-side MOSFET. When the DC-DC converter sinks current through the low-side MOSFET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 2 A. The converter protects itself from excessive current during power cycling and start-up into prebiased outputs by implementing this low-side current protection.

7.3.5.2 LDO Internal Current Limit

In addition to the switcher overcurrent protection, the TPS54122 device has an internal current limit on the integrated LDO. The LDO internal current limit helps protect the LDO during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time. The NMOS pass element in the integrated LDO has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at LDOIN. This current is not limited and can damage the LDO, so if extended reverse-voltage operation is anticipated, external limiting is required. Connect a diode from OUT to LDOIN to provide an alternate path for this current.

7.3.6 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can set the switching frequency of the device in two modes: RT and CLK.

7.3.6.1 RT Mode

In RT mode, the $R_{(RT)}$ resistor is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 300 kHz to 2 MHz by using a maximum $R_{(RT)}$ value of 700 kΩ and a minimum value of 85 kΩ, respectively. To determine the value of the RT resistor for a given switching frequency (f_{SW}), use Equation 4 or the curves in Figure 21 or Figure 22:

$$R_{(RT)} \text{ (k}\Omega\text{)} = 311890 \; f_{SW}^{-1.0793} \text{ (kHz)} \tag{4}$$

7.3.6.2 CLK Mode

In CLK mode, an external clock is connected directly to the RT/CLK pin. The DC-DC converter is synchronized to the external clock frequency with an internal phase-locked loop (PLL) circuit. The DC-DC converter is able to automatically detect the required mode and switch from RT mode to CLK mode. CLK mode overrides RT mode. An internal PLL is implemented to allow synchronization between 300 kHz and 2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square-wave clock signal to the RT/CLK pin with a minimum on-time of at least 75 ns. The clock signal amplitude must transition to less than 0.6 V and to greater than 1.6 V. The PH rising edge is synchronized to the RT/CLK pin falling edge.

In applications where the RT mode and CLK mode are required, the device can be configured to have an RT resistor and an external clock connected at the same time to the RT/CLK pin. If no external clock is present, the device functions in RT mode and the switching frequency is set by the $R_{(RT)}$ resistor.

The first time the SYNC pin is pulled above the RT/CLK high threshold (1.6 V), the device switches from RT mode to CLK mode. The RT/CLK pin turns into a high impedance input in clock mode, as the PLL starts to lock on to the frequency of the external clock. After the clocking edges stop, the internal clocking circuitry is re-enabled, and the frequency returns to the switching frequency set by the $R_{(RT)}$ resistor.

7.3.7 Start-Up Time

The TPS54122 device has start-up time control for the LDO and the DC-DC converter.

7.3.7.1 Soft-Start of the DC-DC Converter

The rate at which the output voltage of the switcher rises up to the full operational level during the start-up phase is controlled through the SS pin. The C_{SS} capacitor is connected between the SS pin and ground. The size of the capacitor determines the soft-start ramp-up time (t_{ss}, 10% to 90%), as shown in Equation 5:

$$t_{SS} \text{ (ms)} = C_{SS} \text{ (nF)} \times V_{ref} \text{ (V)} / I_{SS} \text{ (}\mu\text{A)} \tag{5}$$

Feature Description (continued)

The device has an internal pull-up current source (I_{SS}) of 2.2 µA that charges the external soft-start capacitor, C_{SS}. The voltage reference, V_{ref}, for this device is 0.827 V. By sourcing a constant current onto the capacitor, the device linearly ramps up the voltage on the SS pin that corresponds to the voltage on the FB pin, and thus, the output voltage of the switcher. When the voltage on the SS pin exceeds the value of the internal reference, the device starts regulating to the internal reference value.

If the input UVLO is triggered (or the EN pin is pulled below 1.21 V or a thermal shutdown event occurs), then the device stops switching and enters low-current operation. At the subsequent power-up when the shutdown condition is removed, the DC-DC does not start switching until the SS pin is discharged to ground, ensuring proper soft-start behavior.

7.3.7.2 NR Soft-Start Time and LDO Start-Up

The primary purpose of the NR capacitor is to filter the noise from the LDO band gap and thereby reduce the LDO output noise. However, the NR capacitor affects the start-up time of the LDO. The TPS54122 device has a soft-start circuit to charge C_{NR} at a controlled rate for a monotonic soft-start. The controlled voltage ramp of the output reduces peak inrush current during start-up.

The soft-start ramp time depends on the soft-start charging current ($I_{(NR)}$), the external noise-reduction capacitor (C_{NR}), and the internal voltage reference of the LDO, and can be calculated as shown in Equation 6:

$$t_{SS} \text{ (ms)} = 1,096 \times C_{NR} \text{ (F)} \tag{6}$$

7.3.8 Power-Good Indicators

7.3.8.1 Switcher Power Good (PWRGD)

The PWRGD pin is an open-drain output. After the V_{SENSE} pin rises above 93% or falls below 105% of the internal voltage reference, the PWRGD pin pull-down transistor is deasserted and the pin floats, indicating a correct output voltage on the DC-DC converter. The PWRGD pin has a 2% hysteresis, so the pin does not pull down until the V_{SENSE} pin falls below 91% or rises above 107% of the internal voltage reference, indicating an out-of-range output voltage. Use a 1-kΩ to 100-kΩ pull-up resistor to a voltage source that is less than or equal to 6 V. The PWRGD pin is in a defined state after the VIN input voltage exceeds 1.2 V.

The PWRGD pin is pulled low if the input UVLO or thermal shutdown are asserted, or if the EN pin is pulled low.

7.3.8.2 LDO Power Good (PG)

The power-good (PG) pin of the LDO is an open-drain output and can be connected to any 5.5 V or lower voltage rail through an external pull-up resistor. This pin requires at least 1.1 V on the BIAS pin in order to have a valid output. At power-on, the PG output becomes high-impedance when V_{OUT} is greater than 93% of the set output voltage. If V_{OUT} falls below 90% of the set output voltage or if the BIAS pin voltage falls below 1.9 V, the open-drain turns on and pulls the PG output low. The PG pin pulls low when the LDO is disabled. The recommended range for the PG pull-up resistor is from 10 kΩ to 1 MΩ.

7.3.9 Device Enable and Undervoltage Lockout Adjustment

The TPS54122 device provides an independent device enable and undervoltage lockout. The DC-DC converter provides undervoltage lockout adjustment for the DC-DC converter.

Feature Description (continued)

7.3.9.1 Switcher Enable and Undervoltage Lockout

Use the EN pin to turn the switcher on and off. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low I_Q state.

The EN pin has an internal pull-up current source; float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The TPS54122 device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold (typically, 2.6 V).

The EN can be used as a programmable UVLO. Configure the EN pin, as shown in Figure 25, to set the UVLO voltage.
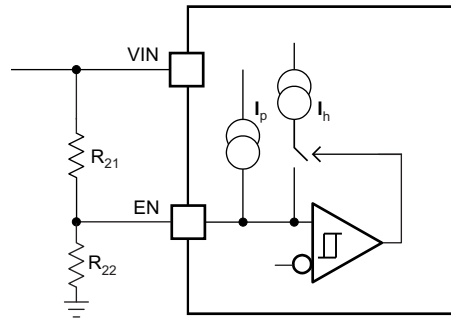
Figure 25. Adjustable VIN Undervoltage Lockout

The EN pin has a small pull-up current (I_p) that sets the state of the pin to enable (default) when no external components are connected. The pullup current controls the voltage hysteresis for the UVLO function because the pullup current increases by I_h when the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 7 and Equation 8:

$$R_{21} = \frac{V_{START}\left(\dfrac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \dfrac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h}$$

(7)

$$R_{22} = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)}$$

where:
- V_{START} is the start-up voltage for the DC-DC converter,
- V_{STOP} is the shutdown voltage for the DC-DC converter,
- $V_{ENFALLING}$ = 1.18 V,
- $V_{ENRISING}$ = 1.25 V,
- I_p = 1.2 µA, and
- I_h = 4.6 µA.

(8)

7.3.9.2 LDO Enable (LDOEN) and Undervoltage Lockout

The TPS54122 LDO enable pin (LDOEN) is active high and compatible with standard digital-signaling levels. The LDOEN pin has hysteresis and deglitching (typically, 50 mV) that allow LDOEN to be used with relatively slow-ramping analog signals, such as an upstream power supply. Typical sequencing applications can be implemented using the TPS54122 DC-DC output or PG, or the output of another power supply. When shutdown capability is not required, EN can be connected to IN.

Feature Description (continued)

The LDO has a fixed UVLO on the BIAS pin to keep the output shut off until the LDO internal circuitry is working properly.

7.3.10 Sequencing

The TPS54122 device is easy to use and suited for applications that require tracking and sequencing. The TPS54122 device has a built-in power-good function to indicate device status, a soft-start circuit to control the output voltage slope during start-up, noise reduction with start-up time for the LDO, and an enable function for independently controlling start-up of the LDO and the switcher. Each of these functions is useful for tracking and sequencing applications.

7.3.11 Switcher Fixed-Frequency PWM Control

The integrated switcher of the TPS54122 uses adjustable, fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the V_{SENSE} pin to an internal voltage reference by an error amplifier that drives the COMP pin. An internal oscillator turns on the high-side power switch. The error amplifier output is converted into a current reference that is compared to the high-side power-switch current. When the power-switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on. The device implements a current limit by clamping the COMP pin voltage to a maximum level. A minimum level clamp is implemented for improved transient-response performance.

7.3.12 Small-Signal Model for Loop Response

Figure 26 shows an equivalent model for the switcher control loop. This model can be run in a circuit simulation program to check frequency and transient responses. The error amplifier is a transconductance amplifier with a g_M of 245 µA/V, and can be modeled using an ideal, voltage-controlled current source. Resistor R_O and capacitor C_O model the open-loop gain and frequency response of the error amplifier. The 1-mV, ac voltage source between nodes *a* and *b* effectively breaks the control loop for the frequency-response measurements. Plotting a / c shows the small-signal response of the frequency compensation. Plotting a / b shows the small-signal response of the overall loop. The transient response can be checked by replacing R_L with a current source using the appropriate load step, amplitude, and slew rate in a time-domain analysis.
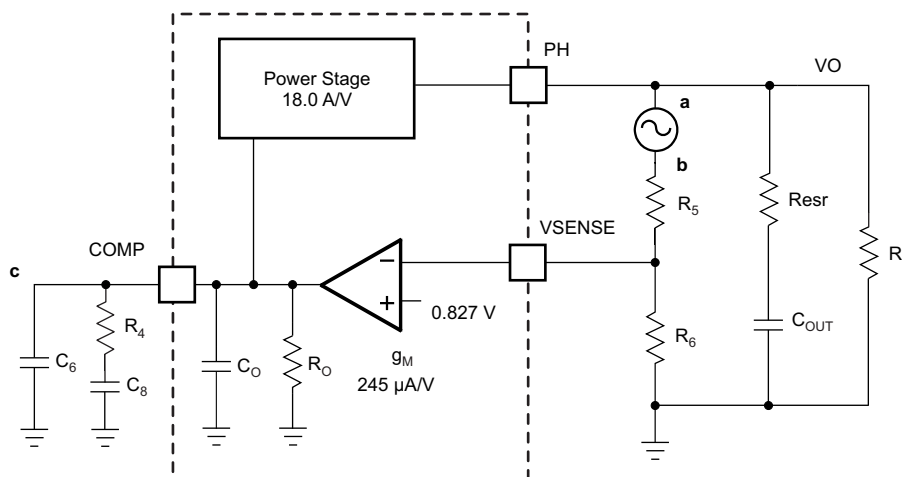

Figure 26. Small-Signal Model for Loop Response

See *Designing Type III Compensation for Current Mode Step-Down Converters* for a more detailed treatment of the small-signal model and compensation for the TPS54122 device.

7.4 Device Functional Modes

7.4.1 Normal Operation

The LDO and DC-DC regulate to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage; see *Dropout Operation* for more details.
- The voltage has previously exceeded the enable rising threshold voltage ($V_{LDOEN} > V_{IH(LDOEN)}$) for the LDO and ($V_{EN} > V_{IH(EN)}$) for the DC-DC and has not yet decreased below the enable falling threshold.
- The LDO output current is less than the LDO current limit and the DC-DC peak inductor current is less than the high-side current limit.
- The device junction temperature is less than the thermal shutdown temperature ($T_J < 160°C$).

7.4.2 Dropout Operation

If the input voltage of the LDO (V_{LDOIN}) is less than the nominal LDO output voltage plus the specified dropout voltage ($V_{DO(LDOIN)}$), but all other conditions are met for normal operation, the LDO operates in input voltage dropout mode. In this mode, the output voltage tracks the input voltage.

The integrated LDO has a BIAS supply voltage that can cause the output to enter dropout. If the BIAS voltage is less than the nominal LDO output voltage plus the specified bias supply dropout voltage ($V_{DO(BIAS)}$), but all other conditions are met for normal operation, the LDO operates in bias voltage dropout mode.

When operating in dropout from either the input or bias supply, the transient performance and PSR of the LDO becomes significantly degraded because the pass device is no longer capable or controlling the current through the LDO. Line or load transients on the LDO input in dropout can result in large output-voltage deviations.

The internal DC-DC regulator has an integrated bootstrap-voltage regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than V_{VIN} and the (BOOT – PH) voltage is below regulation. Use a 0.1-µF ceramic capacitor with an X7R- or X5R-grade dielectric and a voltage rating of 10 V or greater because of the stable characteristics over temperature and voltage provided by these types of capacitors.

To improve dropout, the DC-DC regulator is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.2 V. When the voltage between BOOT and PH drops below the 2.2-V UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on, allowing the boot capacitor to be recharged. The supply current source from the BOOT pin is low; therefore, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Because of this, the effective duty cycle of the switching regulator is nearly 100%.

7.4.3 Disabled

Both the DC-DC regulator and LDO have independent enable pins that enable or disable the output voltage. The LDO output is controlled by the LDOEN pin, and the DC-DC output is controlled by the EN pin. The LDO and DC-DC are disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The input voltage is below the UVLO threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Design Methodology

The TPS54122 device has a low-noise output voltage range from 0.8 V to 3.6 V, with an output current up to 3 A. To simplify design efforts using the TPS54122, see Table 1 for a list of designs for common applications according to the schematic diagram illustrated in Figure 27.

The TPS54122 device can be configured to provide two separate power rails: one from the switching regulator and one from the LDO.

Figure 27 shows a typical application diagram for the TPS54122 device. The first step in the design process is to select the switching frequency for the regulator. Higher switching frequencies produce a smaller solution size using lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, higher switching frequencies cause additional switching losses that negatively impact converter efficiency and thermal performance.

After a switching frequency is determined, the inductor and output capacitor values of the switcher are selected. These two component values are related, and depend on the input and output voltages of the switcher, as well as the current rating. Choosing a high inductor-ripple current affects the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current.

The TPS54122 device requires a high-quality, ceramic (X5R or X7R type), input decoupling capacitor with a value of at least 4.7 µF on the input voltage rail. The voltage rating of the input capacitor must be greater than the maximum input voltage.

The internal LDO of the TPS54122 does not require an output capacitor to be stable. However, for best transient and noise performance, use standard ceramic output capacitors with values of 4.7 µF or greater. TI recommends greater values for better noise performance.

For proper operation, connect a 0.1-µF ceramic capacitor between the BOOT and PH pins. Use a ceramic capacitor with an X5R or better grade dielectric, and a voltage rating of 10-V or greater.

The output voltage of the switcher and the LDO are adjustable using an external-resistor feedback network. The LDO and the switcher have a soft-start function that can be adjusted externally using the C_{SS} and C_{NR} capacitors; see Figure 27.

There are several industry techniques used to compensate DC-DC regulators; see *Designing Type III Compensation for Current Mode Step-Down Converters* for more details about different compensation networks for the TPS54122 device.

Application Information (continued)

8.1.2 Simplified Design Methodology

The TPS54122 device has a low-noise output voltage range from 0.8 V to 3.6 V, with an output current of up to 3 A. To simplify TPS54122 design efforts, see the typical designs for common applications listed in Table 1 based on Figure 27. The designs in Table 1 use the closest standard value components. $C_{DC\text{-}DC\_OUT} = C_9 + C_{10}$ and $C_{OUT} = C_2 + C_3 + C_4$. If the LDO input is connected to the output of the DC-DC, the LDO input capacitance must be added to the DC-DC output capacitance. To execute a complete application design, see *Design Procedures for the TPS54122*. Note that all capacitor values are based on ceramic X5- or X7-type capacitors.

Table 1. Simplified Design Table

| V_{VIN} (V)	DC-DC_OUT (V)	LDO V_{OUT} (V)	I_O (max) (A)	f_{SW} (kHz)	L_1 (µH)	$C_{DC\text{-}DC\_OUT}$ (µF)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	R_4 (kΩ)	R_5 (kΩ)	R_6 (kΩ)	C_8 (nF)	C_{OUT} (µF)	C_1 (nF)	C_{11} (pF)
5.0	3.7	3.3	3.0	500	3.3	4 x 22	3.57	1.15	392	28.7	10	2.87	4.7	122	100	1000
5.0	3.6	3.3	1.0	500	3.3	4 x 22	3.57	1.15	392	16.5	10	2.94	22	122	100	1500
5.0	3.6	2.5	2.0	500	3.3	4 x 22	3.57	1.69	392	23.2	10	2.94	6.8	122	100	1500
5.0	3.3	1.8	3.0	500	3.3	4 x 22	3.57	2.87	392	27.4	10	3.32	3.3	122	100	220
5.0	1.8	1.0	2.0	500	3.3	4 x 22	1.13	4.52	392	16.5	10	8.45	4.7	122	100	680
5.0	2.2	1.8	3.0	500	3.3	4 x 22	3.57	2.87	392	22.1	10	5.90	3.3	122	100	330
5.0	2.1	1.8	1.0	500	3.3	4 x 22	3.57	2.87	392	12.7	10	6.49	15	122	100	680
5.0	1.2	0.8	2.0	500	3.3	4 x 22	short	open	392	13.3	10	22.1	4.7	122	N/A	100
3.3	2.8	2.5	2.0	500	1.0	4 x 22	3.57	1.69	392	20.5	10	4.12	6.8	122	100	1000
3.3	2.2	1.8	3.0	500	2.0	4 x 22	3.57	2.87	392	22.1	10	5.90	3.3	122	100	470
3.3	2.1	1.8	1.0	1000	1.0	4 x 22	3.57	2.87	182	12.7	10	6.49	15	122	100	680
3.3	1.3	1.0	2.0	1000	1.0	4 x 22	1.13	4.52	182	14.0	10	17.4	4.7	122	100	220
3.3	1.1	0.8	2.0	1000	1.0	4 x 22	short	open	182	13.0	10	30.1	4.7	122	N/A	68

8.2 Typical Application
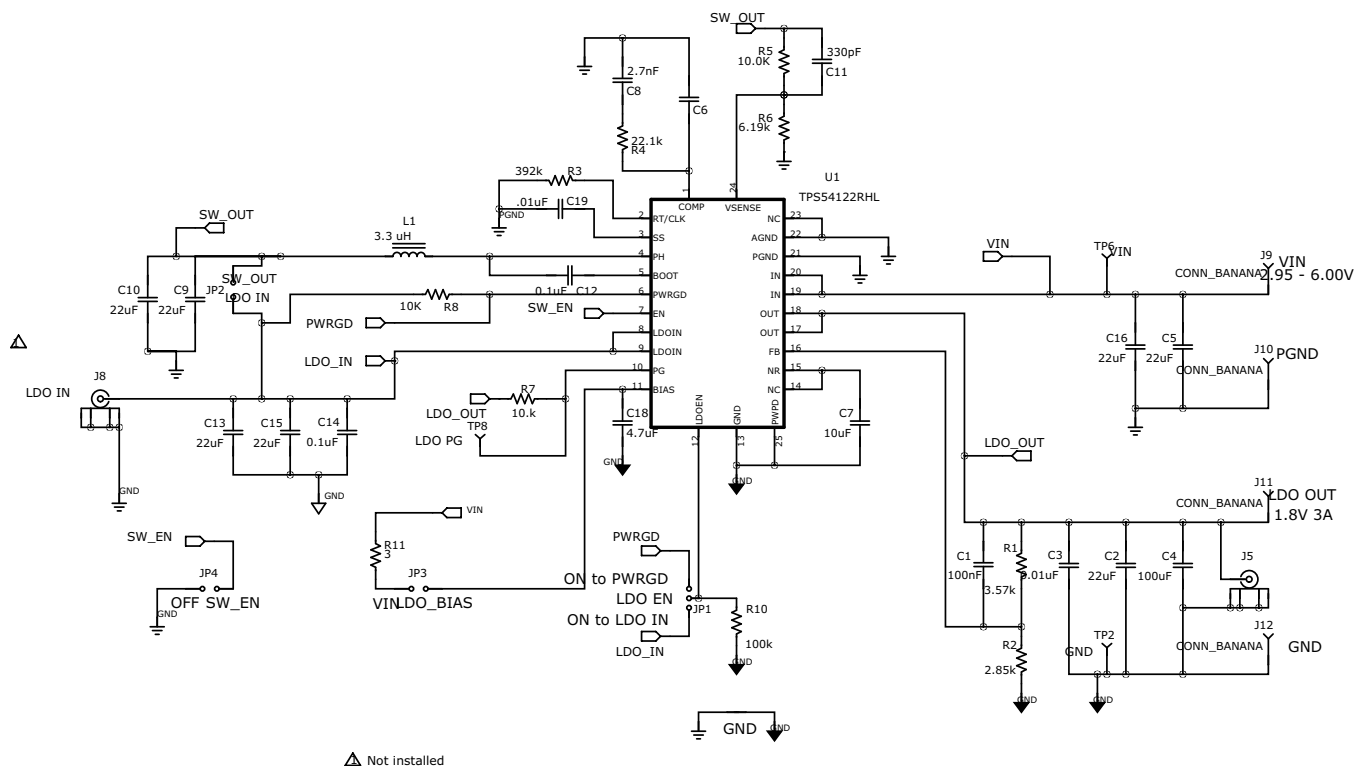
Figure 27. High-Frequency, 1.8-V Output, Low-Noise Power-Supply Design with Adjusted UVLO

Typical Application (continued)

8.2.1 Design Requirements

The application schematic illustrated in Figure 27 meets the parameters of Table 2. This circuit is available in the TPS54122EVM-201 evaluation module. This section details the design procedure. For more information about type-II and type-III frequency compensation circuits, see *Designing Type III Compensation for Current Mode Step-Down Converters*.

Table 2. Design Parameters

PARAMETER	VALUE
SW output voltage (V_{OUT})	2.16 V
LDO output voltage (LDO_{Vout})	1.8 V
Transient response at V_{OUT}	ΔV_{OUT} = 5%
Input voltage VIN	5 V nominal, 3 V to 5.5 V
Output voltage ripple at V_{OUT} ($V_{O(ripple)}$)	< 30 mV_{PP}
Switching frequency (f_{SW})	500 kHz
Output current (I_O)	3 A

8.2.2 Detailed Design Procedure

8.2.2.1 Operating Frequency

The first step of the design procedure is to select a switching frequency for the regulator. This step involves a trade-off between higher and lower switching frequencies. Higher switching frequencies can produce a smaller solution size using lower-valued inductors and smaller-output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes additional switching losses that can negatively impact converter efficiency and thermal performance. In this design, the selection of a moderate switching frequency of 500 kHz achieves a small solution size and high-efficiency operation. The resistor at the RT/CLK pin (R_3) sets this frequency.

Using Equation 9, the required resistance for a switching frequency of 500 kHz is 381 kΩ for this application. This design uses a standard 1%, 392-kΩ resistor.

$$R_3 \, (k\Omega) = 311890 \times f_{SW} \, (kHz)^{(-1.0793)} \tag{9}$$

8.2.2.2 Inductor Selection

Equation 10 is a calculation of the value of the output inductor, where V_{OUT} is the output voltage of the switcher. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Because of this, choosing a high-inductor-ripple current affects the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Typically, the designer selects the inductor ripple value; however, K_{IND} is typically in the range of 0.1 to 0.3 for most applications.

$$L1 = \frac{V_{IN(max)} - V_{OUT}}{I_O \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \tag{10}$$

For this design example, by using K_{IND} = 0.3, the calculated inductor value is 2.9 µH. The chosen standard value is 3.3 µH for this design. When using the output filter inductor, do not exceed the root mean squared (RMS) current and saturation current ratings. Use Equation 11, Equation 12, and Equation 13 to calculate the inductor ripple current, RMS current, and peak inductor current, respectively.

$$I_{RIPPLE} = \frac{V_{IN(max)} - V_{OUT}}{L1} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}}$$

(11)

$$I_{L(rms)} = \sqrt{I_o^2 + \frac{1}{12} \times \left[\frac{V_O \times (V_{IN(max)} - V_O)}{V_{IN(max)} \times L1 \times f_{SW}} \right]^2}$$

(12)

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2}$$

(13)

For this design, the inductor ripple current is 795 mA, the RMS inductor current is 3 A, and the peak inductor current is 3.4 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. The most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switching current limit, rather than the peak inductor current.

8.2.2.3 *Output Capacitor Selection of the Switcher*

Consider the three following primary requirements for selecting the value of the output capacitor of the switcher:
* Minimum capacitance to meet the load transient
* Minimum capacitance to meet the output voltage ripple
* Maximum equivalent series resistance (ESR) to meet the output voltage ripple

Select the output capacitor based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This condition arises if desired hold-up times occur for the regulator, where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is temporarily unable to supply sufficient output current if a large, fast increase occurs in the load current, such as when transitioning from no load to a full load. The regulator typically requires two or more clock cycles for the change in load current and output voltage to affect the control loop and adjust the duty cycle to react to the change. Select the output capacitor size to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles, while allowing only a tolerable amount of droop in the output voltage. The minimum output capacitance required is determined by Equation 14.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where:
* ΔI_{OUT} is the change in output current,
* f_{SW} is the regulator switching frequency, and
* ΔV_{OUT} is the allowable change in the output voltage.

(14)

For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 1 A. Using these numbers (ΔI_{OUT} = 1 A and ΔV_{OUT} = 0.05 × 2.16 = 108 mV) results in a minimum capacitance of 37 μF. This value does not take into account the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is small enough to ignore in this calculation.

Equation 15 calculates the minimum output capacitance required to meet the output voltage ripple specification.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\dfrac{V_{O(ripple)}}{I_{RIPPLE}}}$$

where:
- f_{SW} is the switching frequency,
- $V_{O(ripple)}$ is the maximum allowable output voltage ripple of the switcher output, and
- I_{RIPPLE} is the inductor ripple current calculated to be 795 mA.   (15)

In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 15 yields 6.6 μF.

Equation 16 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 16 indicates the ESR must be less than 38 mΩ.

$$R_{ESR} < \frac{V_{O(ripple)}}{I_{RIPPLE}}$$

(16)

The capacitance of a ceramic capacitor depends on the dc output voltage. Refer to the capacitor data sheet to select output capacitors based on the respective voltage rating. For the minimum capacitance that meets the load step specification of 37 μF, this example uses two effective 22-μF, 6.3-V, X5R ceramic capacitors with 4 mΩ of ESR.

Capacitors generally have limits to the amount of ripple current that can be tolerated without failing or producing excess heat. Use an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the RMS value of the maximum ripple current. Equation 17 can calculate the RMS ripple current the output capacitor must support. For this application, Equation 17 yields 230 mA.

$$I_{Co(rms)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{\sqrt{12} \times V_{IN(max)} \times L1 \times f_{SW}}$$

(17)

8.2.2.4 Input Capacitor

The TPS54122 device requires a high-quality, ceramic, X5R- or X7R-type, 4.7-μF, input decoupling capacitor on the input voltage rail. In some applications, additional bulk capacitance may be required for the LDO BIAS input. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must have a ripple current rating greater than the maximum input current ripple of the TPS54122. Using Equation 18, the input ripple current equals 1.35 A..

$$I_{Ci(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}}$$

(18)

The capacitance of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. The capacitance variations resulting from temperature can be minimized by selecting a dielectric material that is stable over temperature. The high capacitance-to-volume ratio and stability over temperature make the X5R and X7R ceramic dielectrics good selections for power-regulator capacitors. The capacitance value of a capacitor decreases as the dc bias across the capacitor increases. For this example design, a ceramic capacitor with at least a 10-V voltage rating is necessary to support the maximum input voltage. Two 22-µF, 10-V capacitors are connected to VIN and a 4.7-µF, 10-V capacitor is connected at BIAS for this example. The input capacitance value determines the input ripple voltage of the regulator. Use Equation 19 to calculate the input voltage ripple.

$$\Delta V_{IN} = \frac{I_{OUT(max)} \times 0.25}{C_{IN} \times f_{SW}}$$

(19)

Using the design example values where $I_{OUT(max)}$ = 3 A, C_{IN} = 50 µF, and f_{SW} = 500 kHz, Equation 19 yields an input voltage ripple of 30 mV.

8.2.2.5 *Input Capacitor of the LDO*

Although an input capacitor is unnecessary for stability, connecting a 0.1-µF to 1-µF low ESR capacitor across the input supply at the LDO input pin is good analog design practice. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device location is several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability. This design example uses two 22-µF input capacitors.

8.2.2.6 *Output Capacitor of the LDO*

The internal LDO of the TPS54122 is stable with standard ceramic capacitors with capacitance values 4.7 µF or larger. Greater values are recommended for better noise performance. For best noise performance, the evaluated design uses 100-µF, 22-µF, and 0.1-µF ceramic capacitors with a 6.3-V rating. X5R- and X7R-type capacitors are excellent choices because there is minimal variation in value and ESR over temperature.

8.2.2.7 *Slow-Start Capacitor Selection*

The slow-start capacitor determines the minimum amount of time required for the output voltage to reach the nominal programmed value during power-up. This feature is useful if a load requires a controlled voltage slew rate. This feature is useful if the output capacitance is large and requires a large amount of current to charge the capacitor to the output voltage level. The large currents required to charge the capacitor can make the TPS54122 device reach the current limit, or the excessive current draw from the input power supply can cause the input voltage rail to sag. Limiting the output voltage slew rate solves these problems. Use Equation 20 to calculate the soft-start capacitor value.

$$C_{SS} = \frac{T_{SS}\,(ms) \times I_{SS}\,(\mu A)}{V_{REF}\,(V)}$$

(20)

The example circuit has the soft-start time set to an arbitrary value of 3.5 ms, which requires a 10-nF capacitor. In this example using the TPS54122 device, I_{SS} is 2.2 µA and V_{REF} is 0.827 V.

8.2.2.8 *Bootstrap Capacitor Selection*

Connect a 0.1-µF ceramic capacitor between the BOOT and PH pins for proper device operation. Use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a voltage rating of 10-V or greater.

8.2.2.9 Output Voltage Feedback Resistor Selection

Select resistors R_5 and R_6 to set the output voltage of the switcher, and choose R_1 and R_2 to set the output voltage of the LDO. The example for this design uses 6.19 kΩ for R_6 and 2.85 kΩ for R_2. Use Equation 21 and Equation 22 to calculate R_5 and R_1, respectively.

$$R_5 = \frac{V_{OUT} - V_{REF}}{V_{REF}} R_6$$

(21)

$$R_1 = \frac{LDO_{V(out)} - LDO_{V(ref)}}{LDO_{V(ref)}} R_2$$

where:

- V_{OUT} is the output of the switcher,
- $LDO_{V(out)}$ is for the LDO,
- V_{REF} is 0.827 V, and
- $LDO_{V(ref)}$ is 0.8 V.

(22)

The closest 1% resistors from the calculated results of Equation 21 and Equation 22 for R_5 and R_1 are 10 kΩ and 3.57 kΩ, respectively.

8.2.2.10 Switcher Minimum and Maximum Output Voltage

The internal design of the TPS54122 sets a minimum switcher output voltage limit for any given input voltage. The output voltage must never be less than the internal voltage reference; the minimum controllable on-time can limit output voltage. In this case, Equation 23 gives the minimum output voltage:

$$V_{O(min)} = \text{On-Time(min)} \times f_{S(max)} \times [V_{IN(max)} - I_{O(min)} \times 2 \times RDS] - I_{O(min)} \times (R_L + RDS)$$

where:

- $V_{O(min)}$ = minimum achievable output voltage,
- On-Time(min) = minimum controllable on-time (65 ns typical, 120 ns, no load),
- $f_{S(max)}$ = maximum switching frequency, including tolerance,
- $V_{IN(max)}$ = maximum input voltage,
- $I_{O(min)}$ = minimum load current,
- RDS = minimum high-side MOSFET on-resistance (45 mΩ to 64 mΩ), and
- R_L = series resistance of the output inductor.

(23)

There is a maximum achievable output voltage that is limited by the minimum off-time. The maximum output voltage is shown in Equation 24:

$$V_{O(max)} = [1 - \text{Off-Time(max)} \times f_{S(max)}] \times [V_{IN(min)} - I_{O(max)} \times 2 \times RDS] - I_{O(max)} \times (R_L + RDS)$$

where:

- $V_{O(max)}$ = maximum achievable output voltage,
- Off-Time(max) = maximum controllable off-time (60 ns typical),
- $f_{S(max)}$ = maximum switching frequency, including tolerance,
- $V_{IN(min)}$ = minimum input voltage,
- $I_{O(max)}$ = maximum load current,
- RDS = maximum high-side MOSFET on-resistance (81 mΩ to 110 mΩ), and
- R_L = series resistance of the output inductor.

(24)

8.2.2.11 Compensation Component Selection

Several industry techniques can compensate DC-DC regulators. The method used here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. This method ignores the effects of the slope compensation that is internal to the TPS54122 device. This method ignores the slope compensation; therefore, the actual crossover frequency is usually lower than the crossover frequency in the following calculations.

Type-III compensation is used to achieve a high-bandwidth, high-phase-margin design. This design targets a crossover frequency (bandwidth) of 67 kHz. Equation 25 and Equation 26 calculate the power-stage pole and zero at 2.5 kHz and 1809 kHz, respectively. For the output capacitance of the switcher (C_{OUT}), include the two input capacitors on the LDO; therefore, the total capacitance is 4 × 22 µF = 88 µF, and R_{ESR} = 4 mΩ / 4 = 1 mΩ.

$$f\, p_{MOD} = \frac{I_{OUT(max)}}{2\pi \times V_{OUT} \times C_{OUT}}$$

(25)

$$f\, z_{MOD} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

(26)

The compensation components calculations are now possible. First, calculate the value for R_4 that sets the gain of the compensated network at the crossover frequency. Use Equation 27 to calculate the value of R_4.

$$R_4 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{g_{m(ea)} \times V_{REF} \times g_{m(ps)}}$$

(27)

Using Equation 27, R_4 = 22.1 kΩ.

Next, calculate the value of C_8. Together with R_4, C_8 places a compensation zero at the dominant power-stage pole frequency f_p. Use Equation 28 to calculate the value of C_8:

$$C_8 = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_4}$$

(28)

Using Equation 28, the standard value for C_8 equals 2.7 nF.

To provide a zero around the crossover frequency to boost the phase at crossover, add a capacitor (C_{11}) parallel to R_5. Equation 29 shows the value for the C_{11} capacitor. A close standard value for C_{11} is 330 pF.

$$C_{11} = \frac{1}{2\pi \times R_5 \times f_C}$$

(29)

Using the feed-forward capacitor (C_{11}) creates a low, ac-impedance path from the output voltage to the V_{SENSE} input of the integrated circuit that can couple noise at the switching frequency into the control loop. Do not use a feed-forward capacitor for high-output voltage ripple designs (greater than 15 mV peak-to-peak at the V_{SENSE} input) operating at duty cycles of less than 30%. When using C_{11}, always limit the closed-loop bandwidth to no more than one-tenth of the switching frequency.

Use an additional high-frequency pole, if necessary, to cancel the zero from the output capacitor ESR by adding a capacitor in parallel with the series combination of R_4 and C_8. Equation 30 calculates the pole that cancels the zero from the output capacitor ESR. Capacitor C_6 is optional and is not used in this design.

$$C_6 = \frac{R_{ESR} \times C_{OUT}}{R_4}$$

(30)

8.2.2.12 *Noise-Reduction Capacitor*

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS54122 device, the band gap does not contribute significantly to noise. Instead, the output resistor divider and the error amplifier input dominate the noise. To minimize the noise in this application, use a 1-μF noise-reduction capacitor.
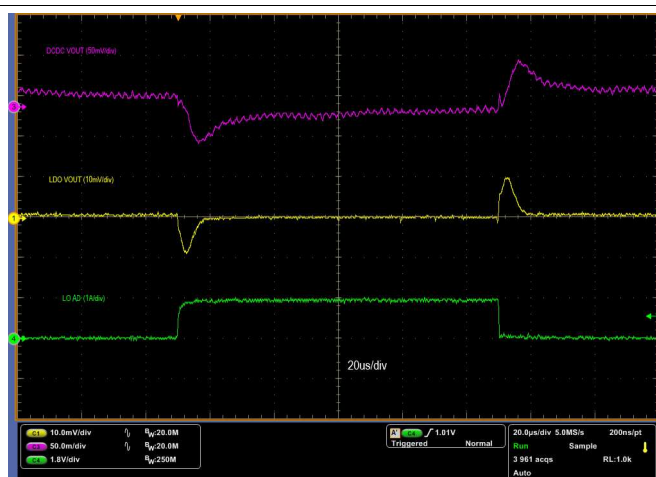
In addition to noise-reduction, the capacitor on the NR pin slows start-up time. Changing the value of C_{NR} can adjust the start-up time of the LDO. In this design, the 1-μF noise-reduction capacitor sets the LDO start-up time to 1 s.

8.2.3 **Application Curves**
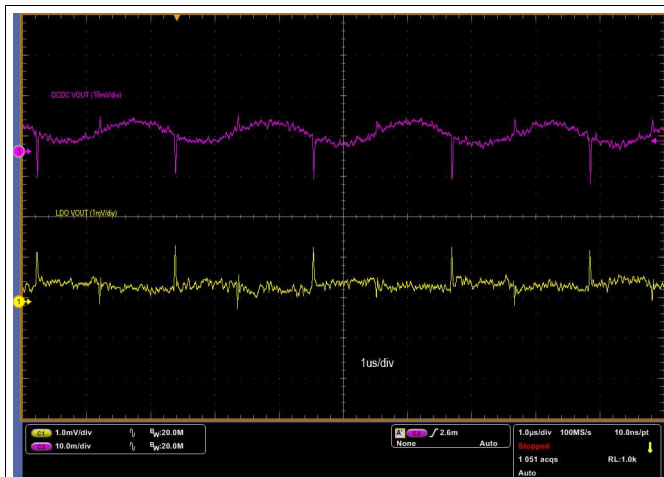
V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A

Figure 28. DC-DC Output Voltage and LDO V_{OUT} ($LDO_{V(out)}$)

V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A to 2 A

Figure 29. Load Transient Response
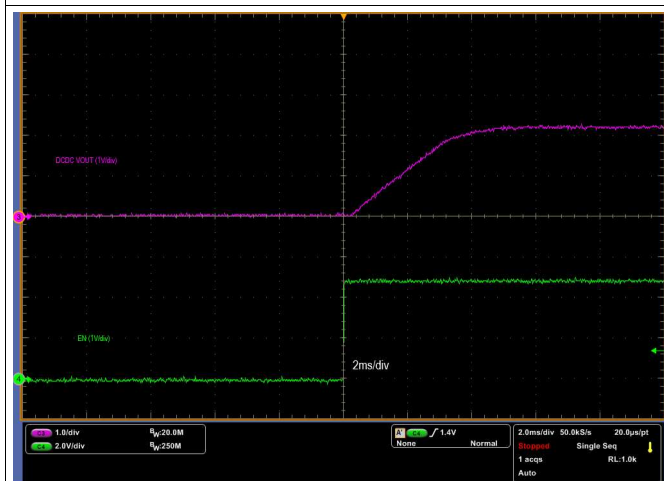
V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A

Figure 30. Start-Up Using DC-DC Enable (EN Pin)

V_{VIN} = 5 V, V_{OUT} = 2.1 V, $LDO_{V(out)}$ = 1.8 V, Load = 1 A

Figure 31. Start-Up Using LDO Enable (LDOEN Pin)

Figure 32. DC-DC Efficiency vs Output Current

9 Power Supply Recommendations

With BIAS connected to VIN, the device is designed to operate from an input voltage supply range of 2.95 V to 5.5 V. This input supply to the DC-DC converter or LDO regulator must be well-regulated. If the input supply is located more than a few inches from the converter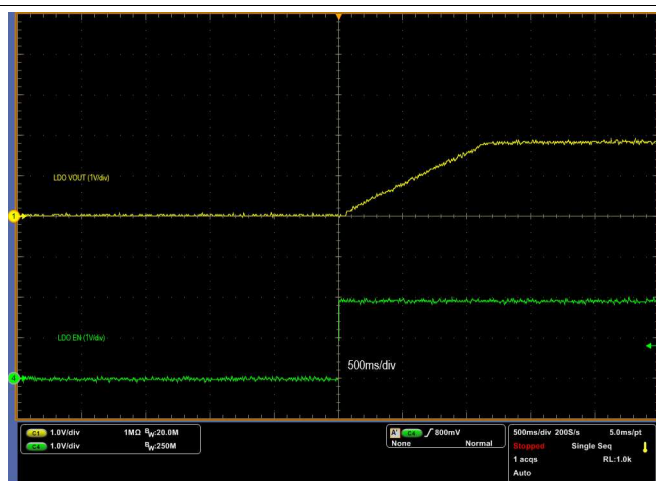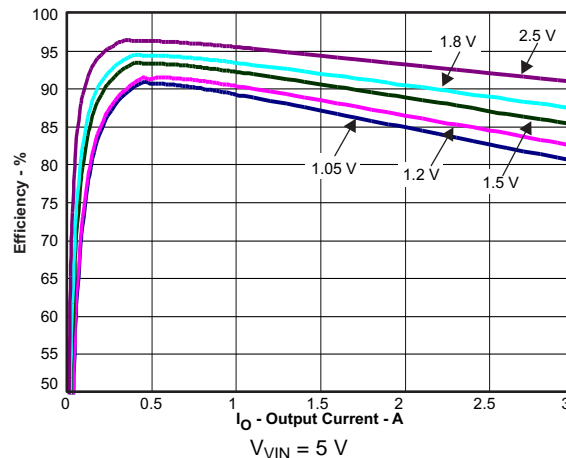, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The added capacitance is not critical; a 47-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

Correct printed circuit board (PCB) layout is a critical portion of good power-supply design and is particularly important for the high PSR and low-noise performance of the TPS54122 device. The following general guidelines are shown below. For a detailed description, see *TPS54122EVM-201, Low-Noise 3-A Power Supply Evaluation Module*.

• Place the inductor, boot capacitor, and output capacitor of the DC-DC converter on the layers of the board (such as the bottom layer) that help minimize the spread of switching noise into the LDO area on the board.

• Connect the boot capacitor and inductor L1 as close as possible to the PH pin to reduce parasitic inductance of long traces.

• To help shield the compensation components (the soft-start capacitors, the CLK/RT resistor, and the DC-DC feedback resistors) from noise, ground these components to a power ground that is shielded from the high-current ground plane. To achieve this shielding, use a separate trace to the PGND pin.

• The RT/CLK pin is sensitive to noise so place the RT resistor as close as possible to the device, routed with a short connection.

• Place the noise-reduction capacitor as close as possible to the device to avoid noise pickup into the LDO reference.

• Isolate the ground planes on the input and output from each other, connected through a separate trace route that parallels the power-loop routing from the DC-DC output to the LDO input.

• Terminate the low-noise analog ground of the LDO circuits (such as the voltage set point divider, the LDO input, and output capacitors) to ground using a wide ground trace separate from the power ground plane.

• Place the LDO input and output capacitors as close to the device as possible.

• Bypass the VIN to ground using a low-ESR ceramic capacitor with an X5R or X7R dielectric, placed as close as possible to the VIN and PGND pins.

• For operation at the full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipation.

• Minimize PCB conductor planes to prevent excessive capacitive coupling.
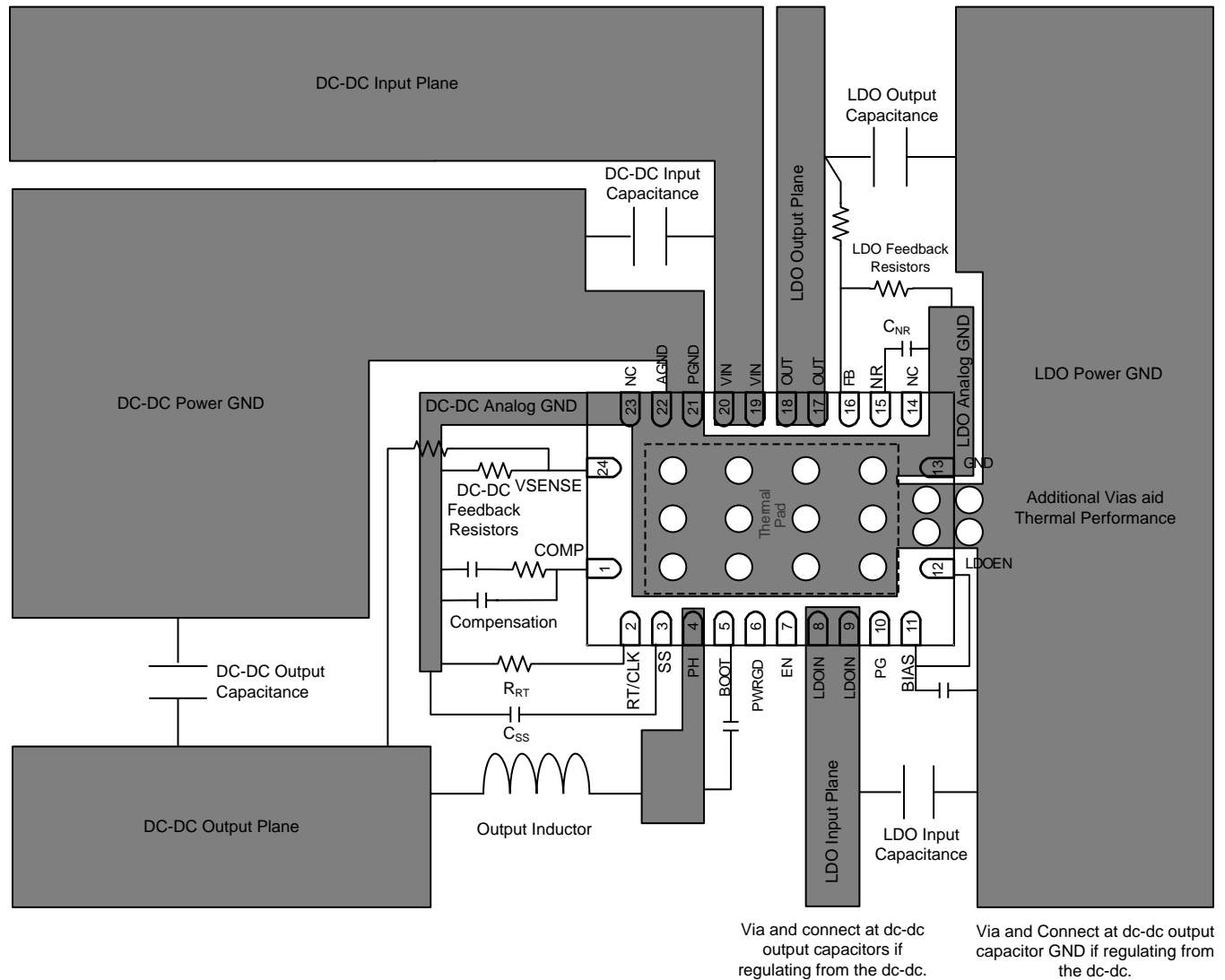
10.2 Layout Example

Figure 33. Example Layout

10.3 Thermal Information

The internal thermal protection circuitry of the device is designed to protect against overload conditions. However, this circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability. The TPS54122 device has thermal protection for the switcher and the LDO, which operate independently.

10.3.1 Thermal Protection of the Switcher

The internal thermal-shutdown circuitry of the switcher forces the device to stop switching if the junction temperature exceeds 165°C (typically). After the device junction temperature drops below 150°C (typically), the DC-DC converter reinitiates the power-up sequence by discharging the SS pin to less than 40 mV.

10.3.2 Thermal Protection of the LDO

Thermal protection of the integrated LDO disables the LDO output of the TPS54122 when the junction temperature rises to 155°C (typically), allowing the device to cool. When the junction temperature cools to 140°C (typically), the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal-protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage resulting from overheating.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TPS54122 器件配套使用，协助评估电路初始性能。可通过评估模块工具文件夹从德州仪器 (TI) 网站上申请获取 TPS54122EVM-201 评估模块（以及相关用户指南）。

11.2 文档支持

11.2.1 相关文档

- *TPS54122EVM-201 低噪声 3A 电源评估模块*
- *TPS54122 设计过程*
- *设计用于电流模式降压转换器的超快回路响应 III 型补偿*

11.3 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

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11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54122RHLR	ACTIVE	VQFN	RHL	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PZFQ	Samples
TPS54122RHLT	ACTIVE	VQFN	RHL	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PZFQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

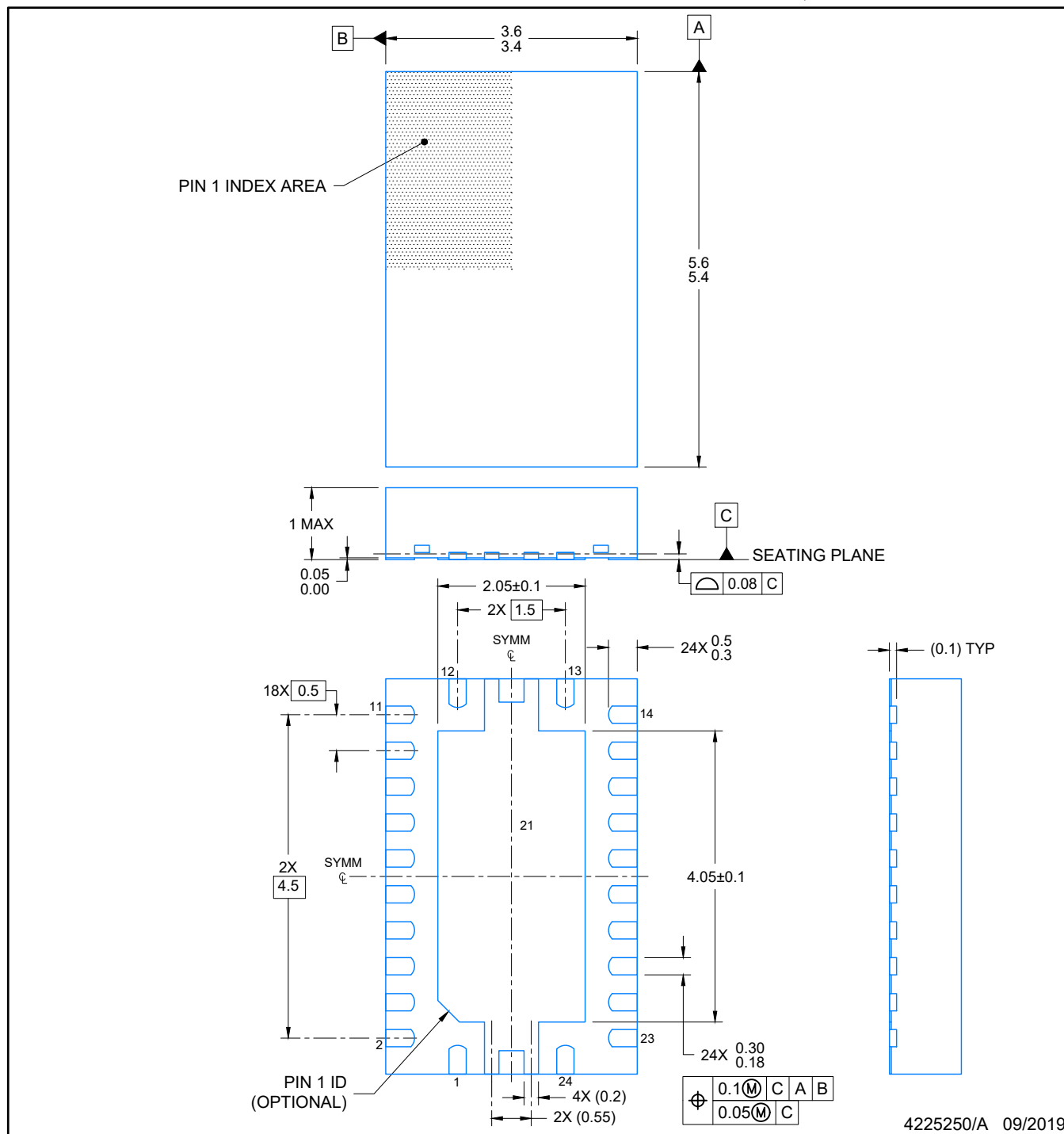*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54122RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
TPS54122RHLT	VQFN	RHL	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54122RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0
TPS54122RHLT	VQFN	RHL	24	250	210.0	185.0	35.0

PIN 1 INDEX AREA

B 3.6 / 3.4 A

5.6 / 5.4

1 MAX

0.05 / 0.00

C SEATING PLANE

0.08 C

2.05±0.1

2X 1.5

SYMM

24X 0.5 / 0.3

18X 0.5

12   13

11   14

21

2X 4.5

SYMM

4.05±0.1

2

23

24X 0.30 / 0.18

PIN 1 ID (OPTIONAL)

1   24

4X (0.2)

2X (0.55)

0.1 Ⓜ C A B
0.05 Ⓜ C

(0.1) TYP
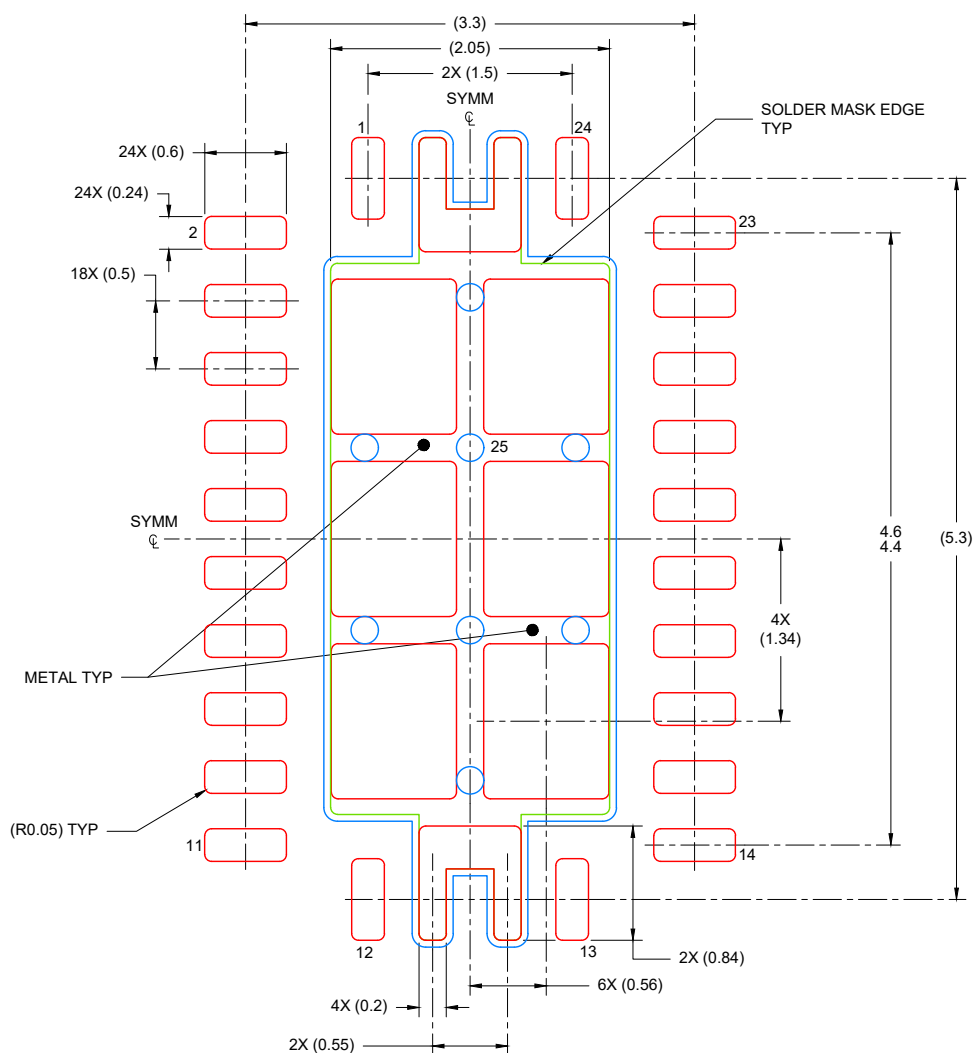
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

(3.3)

(2.05)

2X (1.5)

SYMM

1   24

24X (0.6)

24X (0.24)

2

2X (0.4)

23

18X (0.5)

2X (1.105)

25

6X (0.67)

4.6
4.4

(5.3)

SYMM

(4.05)

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

(Ø 0.2) VIA
TYP

(R0.05) TYP

11   14

12   13

4X
(0.775)

4X (0.2)

2X (0.55)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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