LMZ13608 8A SIMPLE SWITCHER® 具有 36V 最大输入电压的电源模块

查询样品: LMZ13608

特性

- 集成屏蔽式电感器
- 简单印刷电路板 **(PCB)** 布局布线
- 固定开关频率 **(350kHz)**
- 使用外部软启动、跟踪和精密使能的灵活启动排序
- 防止涌入电流和诸如输入欠压闭锁 **(UVLO)** 和输出短路等故障的保护
- **-40°C** 至 **125°C** 的结温范围
- 用于简单装配和制造的单个外露垫和标准引脚分配
- 针对 **WEBENCH®** 电源设计工具完全启用
- 与 **LMZ22010/08**，**LMZ12010/08**，**LMZ23610/08/06H** 和 **LMZ13610/06H** 引脚兼容

应用范围

- 从 **12V** 和 **24V** 输入电源轨的负载点转换
- 时间关键项目
- 空间受限/高热量要求应用
- 负输出电压应用（请参见 **AN-2027**，文献编号SNVA425）

性能优势

- 高效率减少了系统散热
- 符合 **EN55022 B** 类标准的低辐射 **(EMI)**
  - **EN 55022:2006**，**+A1:2007**，**FCC** 部分 **15** 子部分 **B**，已经在具有电磁干扰 **(EMI)** 配置的评估板上进行了测试
- 只有 **7** 个外部组件
- 低输出电压纹波
- 无需外部散热片

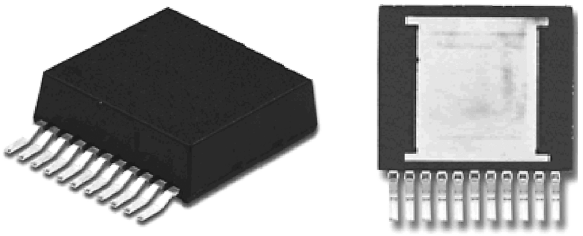
电气规范

- **40W** 最大总输出功率
- 高达 **8A** 输出电流
- 输入电压范围 **6V** 至 **36V**
- 输出电压范围为 **0.8V** 至 **6V**
- 效率高达 **92%**

说明

LMZ13608 SIMPLE SWITCHER 电源模块是一款易于使用的降压 DC-DC 解决方案，此解决方案驱动 8A 的负载。 LMZ13608 采用创新型封装，此封装可提高热性能并可实现手工或机器焊接。

LMZ13608 可接受 6V 到 36V 之间的输入电压轨，提供低至 0.8V 的可调且高精确度输出电压。 LMZ13608 只需 2 个外部电阻器和 3 个外部电容器即可完成此电源解决方案。 LMZ13608 是一款具有以下保护特性的可靠且稳定耐用的设计：热关断、输入欠压闭锁、输出过压保护、短路保护、输出电流限制并允许启动至一个预偏置输出。



Top View Bottom View

Figure 1. PFM 11 Pin Package
15 x 17.79 x 5.9 mm (0.59 x 0.7 x 0.232 in)
θ_{JA} = 9.9°C/W, θ_{JC} = 1.0°C/W (1)
RoHS Compliant

(1) θ_{JA} measured on a 75mm x 90mm four layer PCB.

System Performance

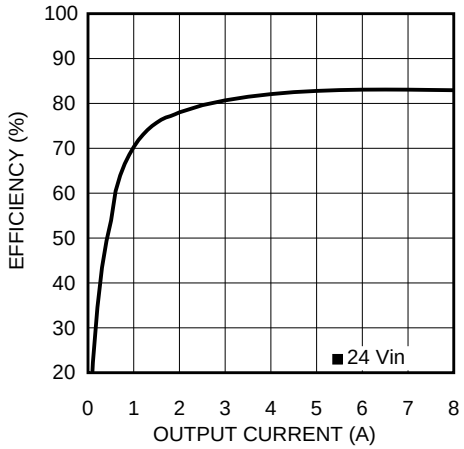


Figure 2. Efficiency V_{IN} = 24V V_{OUT} = 3.3V

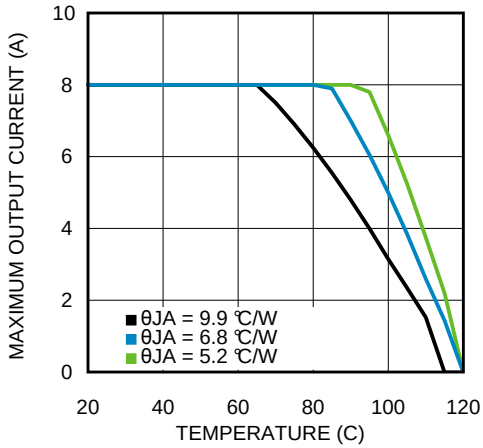


Figure 3. Thermal derating curve
V_{IN} = 24V, V_{OUT} = 3.3V

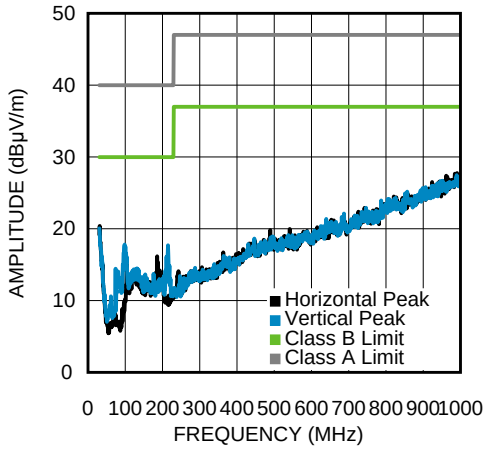
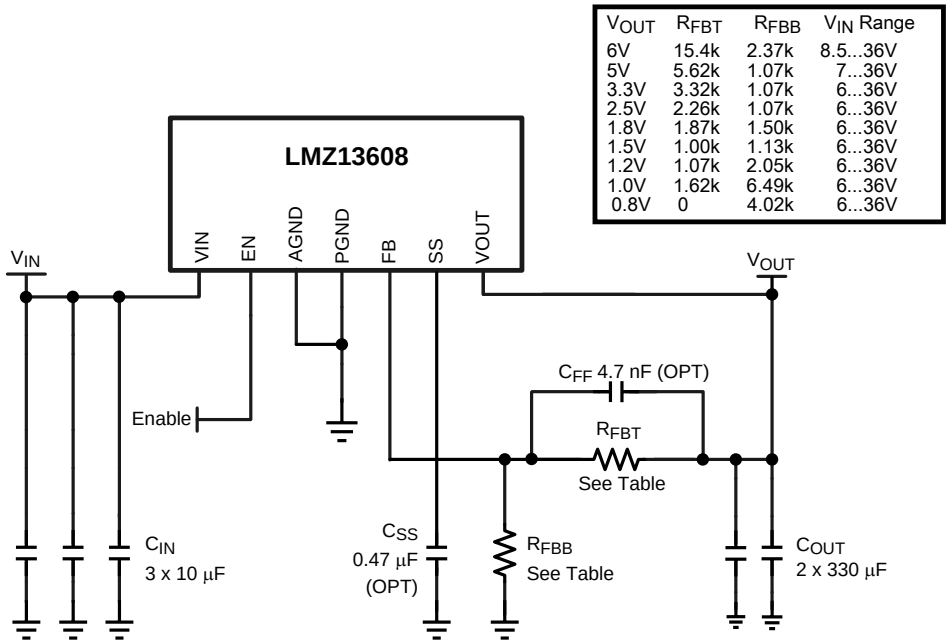


Figure 4. Radiated EMI (EN 55022)
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 8A

Simplified Application Schematic



Connection Diagram

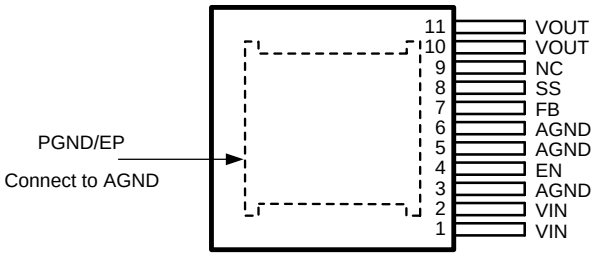


Figure 5. Top View - 11-Lead PFM

PIN DESCRIPTIONS

Pin	Name	Description
1, 2	VIN	Supply input — Nominal operating range is 6V to 36V . A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and PGND.
3, 5, 6	AGND	Analog Ground — Reference point for all stated voltages. Must be externally connected to EP/PGND.
4	EN	Enable — Input to the precision enable comparator. Rising threshold is 1.274V typical. Once the module is enabled, a 20 uA source current is internally activated to accommodate programmable hysteresis.
7	FB	Feedback — Internally connected to the regulation, over-voltage, and short-circuit comparators. The regulation reference point is 0.8V at this input pin. Connect the feedback resistor divider between the output and AGND to set the output voltage.
8	SS	Soft-Start/Track input — To extend the 1.6 mSec internal soft-start connect an external soft start capacitor. For tracking connect to an external resistive divider connected to a higher priority supply rail. See Design Steps for the LMZ13608 Application section.
9	NC	No Connect. This pin must remain floating, do not ground.
10, 11	VOUT	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and PGND.
EP	PGND	Exposed Pad / Power Ground Electrical path for the power circuits within the module. — NOT Internally connected to AGND / pin 5. Used to dissipate heat from the package during operation. Must be electrically connected to pin 5 external to the package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

VIN to PGND	-0.3V to 40V
EN to AGND	-0.3V to 5.5V
SS, FB to AGND	-0.3V to 2.5V
AGND to PGND	-0.3V to 0.3V
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility (3)	± 2 kV
For soldering specifications: see product folder at www.ti.com and literature number SNOA549	

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

OPERATING RATINGS(1)

VIN	6V to 36V
EN	0V to 5.0V
Operation Junction Temperature	−40°C to 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, V_{OUT} = 3.3V

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
SYSTEM PARAMETERS						
Enable Control						
V_{EN}	EN threshold	V_{EN} rising	**1.096**	1.274	**1.452**	V
I_{EN-HYS}	EN hysteresis source current	V_{EN} > 1.274V		13		µA
Soft-Start						
I_{SS}	SS source current	V_{SS} = 0V	**40**	50	**60**	µA
t_{SS}	Internal soft-start interval			1.6		msec
Current Limit						
I_{CL}	Current limit threshold	d.c. average	10.5			A
Internal Switching Oscillator						
f_{osc}	Free-running oscillator frequency		314	359	404	kHz

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, V_{OUT} = 3.3V

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Regulation and Over-Voltage Comparator						
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8V I_O = 8A	**0.775**	0.795	**0.815**	V
V_{FB-OV}	Feedback over-voltage protection threshold			0.86		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non Switching Quiescent Current			3		mA
I_{SD}	Shut Down Quiescent Current	V_{EN} = 0V		32		µA
D_{max}	Maximum Duty Factor			85		%
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis	Falling		15		°C
θ_{JA}	Junction to Ambient (3)	Natural Convection		9.9		°C/W
		225 LFPM		6.8		
		500 LFPM		5.2		
θ_{JC}	Junction to Case			1.0		°C/W
PERFORMANCE PARAMETERS(4)						
ΔV_O	Output voltage ripple	BW@ 20 MHz		24		mV_{PP}
$\Delta V_O/\Delta V_{IN}$	Line regulation	V_{IN} = 12V to 20V, I_{OUT}= 8A		±0.2		%
$\Delta V_O/\Delta I_{OUT}$	Load regulation	V_{IN} = 12V, I_{OUT}= 0.001A to 8A		1		mV/A
η	Peak efficiency	V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 5A		89.5		%
η	Full load efficiency	V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 8A		88.5		%

(3) Theta JA measured on a 3.0” x 3.5” four layer board, with two ounce copper on outer layers and one ounce copper on inner layers, two hundred and ten 12 mil thermal vias, and 2W power dissipation. Refer to evaluation board application note layout diagrams.
(4) Refer to BOM in Typical Application Bill of Materials.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

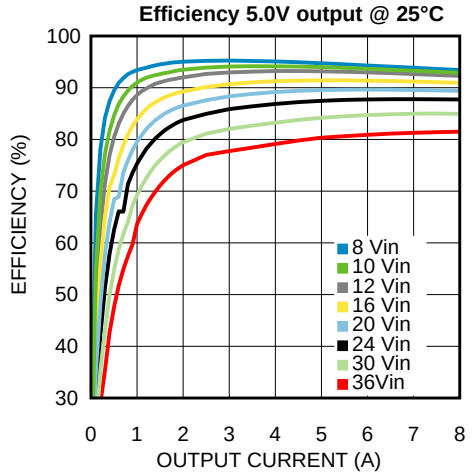


Figure 6.

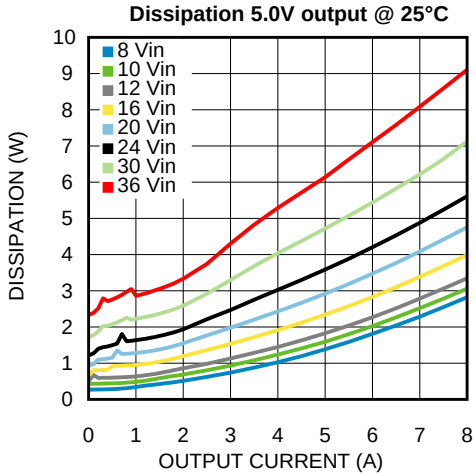


Figure 7.

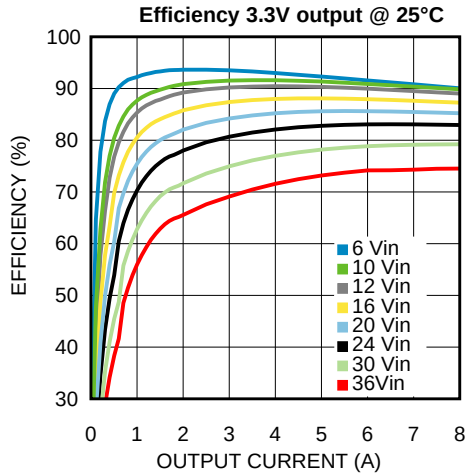


Figure 8.

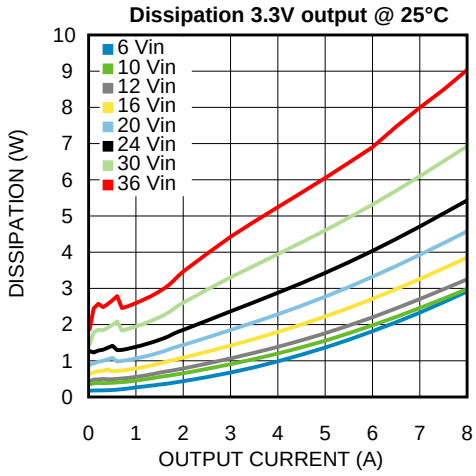


Figure 9.

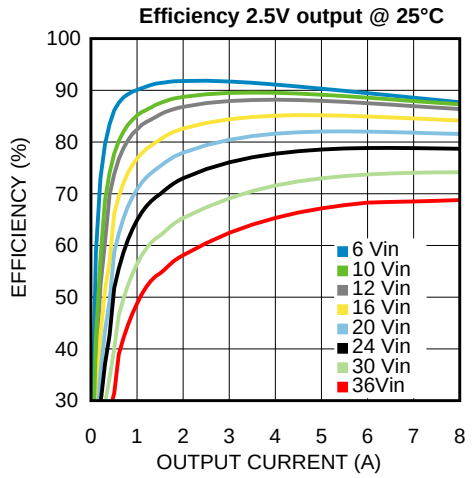


Figure 10.

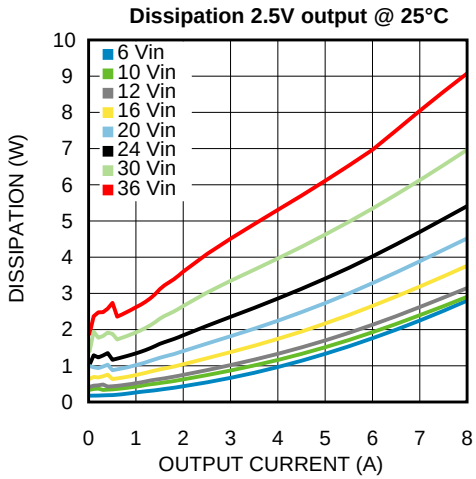


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

Efficiency 1.8V output @ 25°C

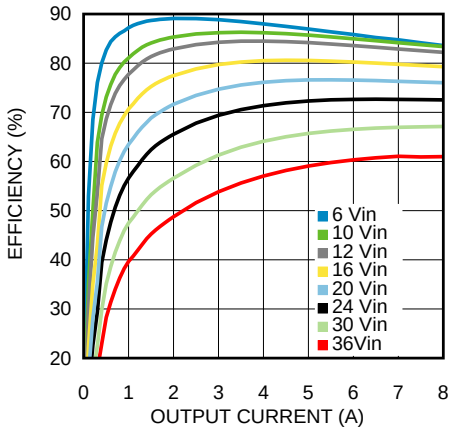


Figure 12.

Dissipation 1.8V output @ 25°C

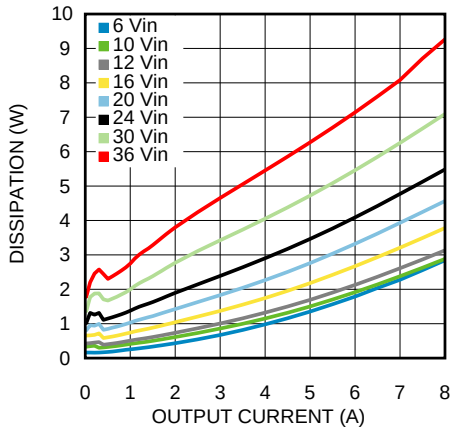


Figure 13.

Efficiency 1.5V output @ 25°C

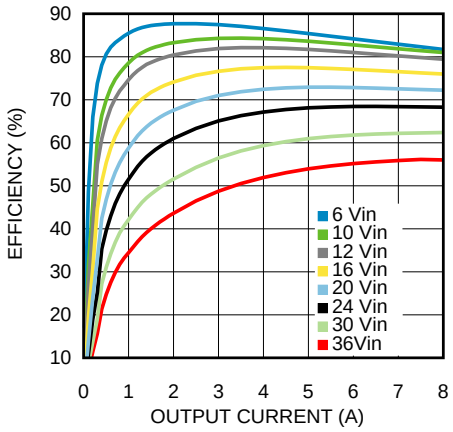


Figure 14.

Dissipation 1.5V output @ 25°C

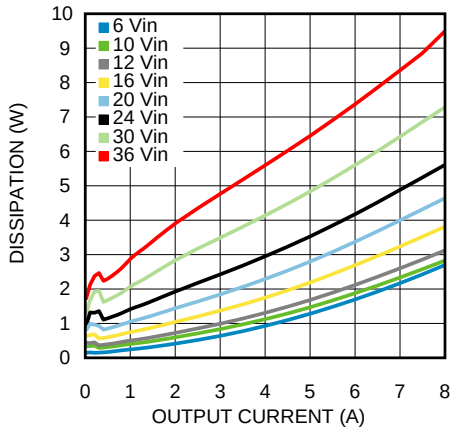


Figure 15.

Efficiency 1.2V output @ 25°C

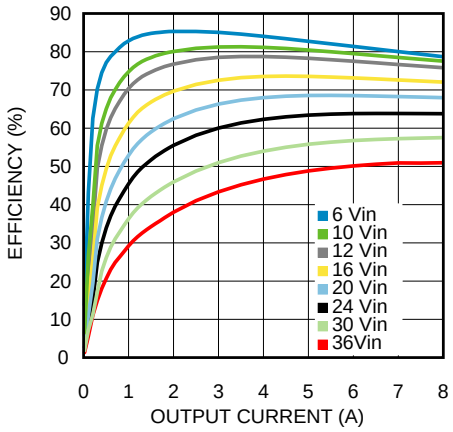


Figure 16.

Dissipation 1.2V output @ 25°C

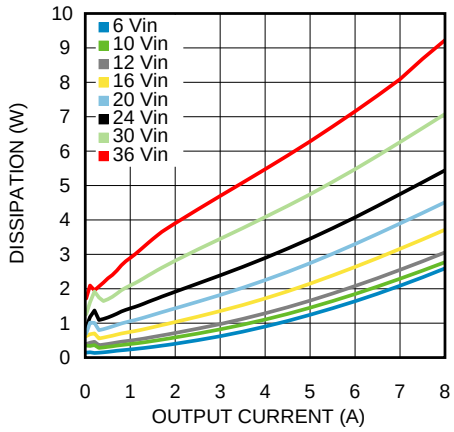


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

Efficiency 1.0V output @ 25°C

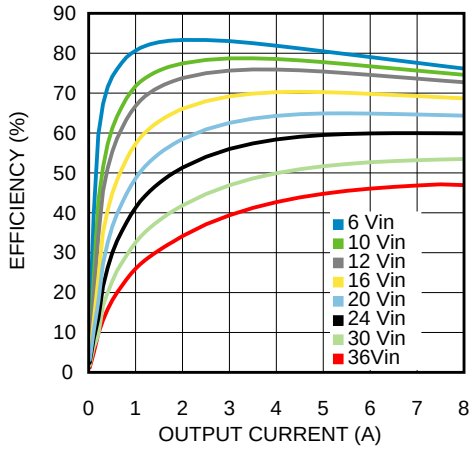


Figure 18.

Dissipation 1.0V output @ 25°C

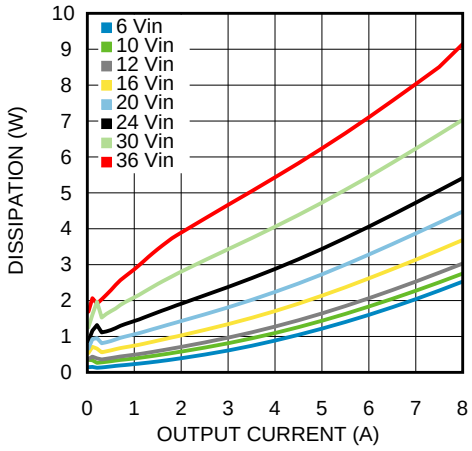


Figure 19.

Efficiency 5.0V output @ 85°C

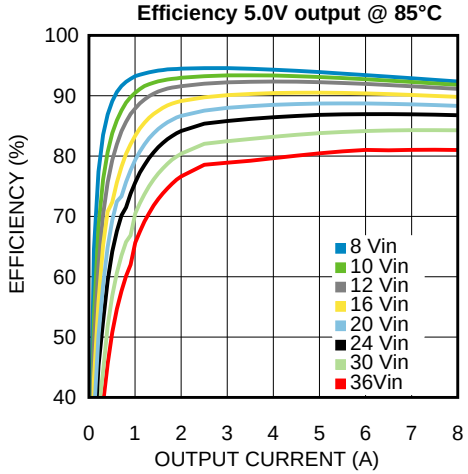


Figure 20.

Dissipation 5.0V output @ 85°C

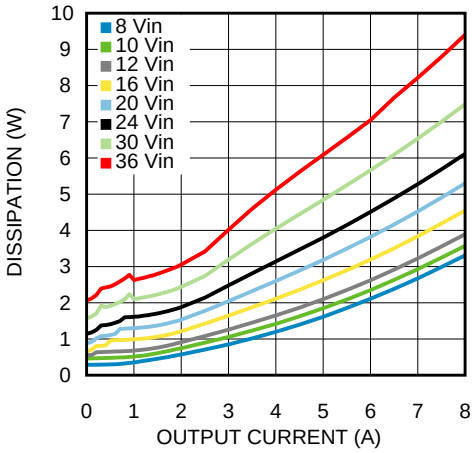


Figure 21.

Efficiency 3.3V output @ 85°C

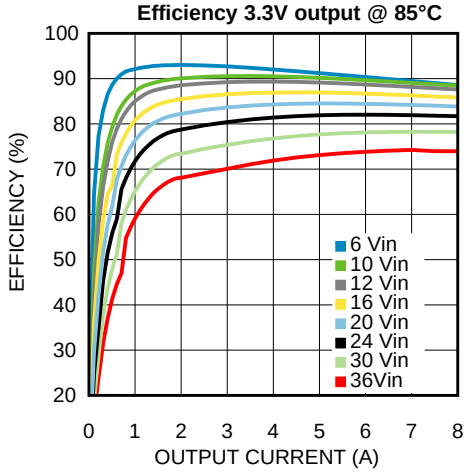


Figure 22.

Dissipation 3.3V output @ 85°C

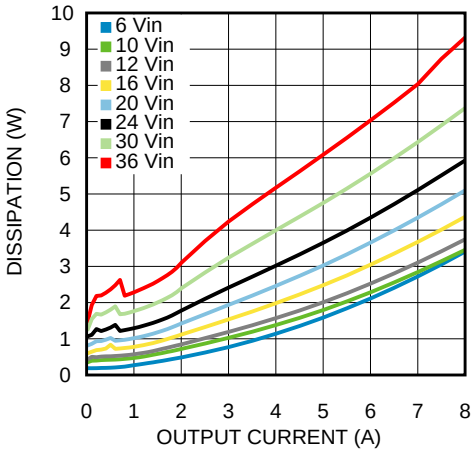


Figure 23.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

Efficiency 2.5V output @ 85°C

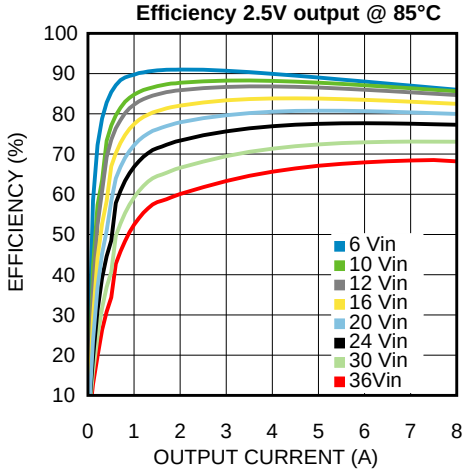


Figure 24.

Dissipation 2.5V output @ 85°C

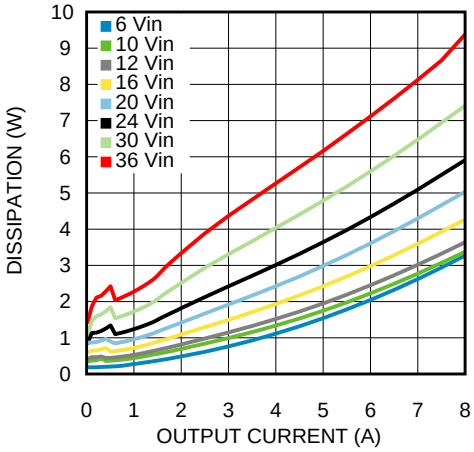


Figure 25.

Efficiency 1.8V output @ 85°C

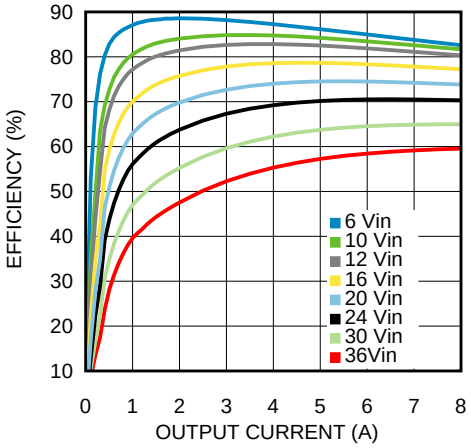


Figure 26.

Dissipation 1.8V output @ 85°C

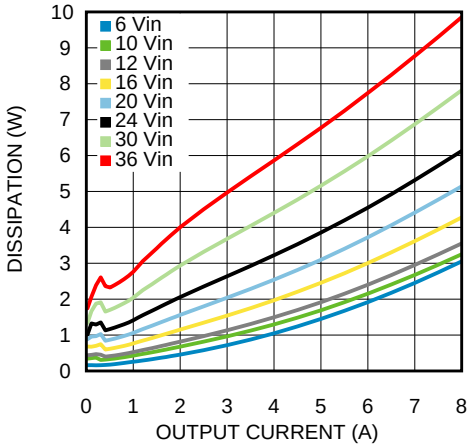


Figure 27.

Efficiency 1.5V output @ 85°C

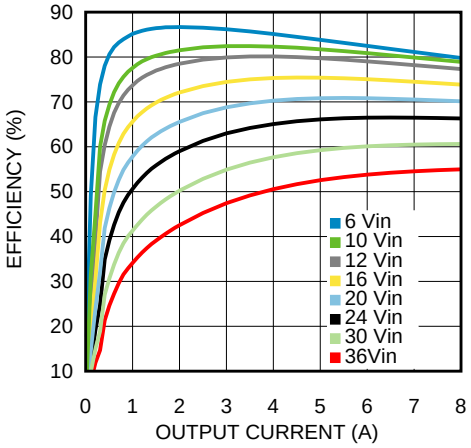


Figure 28.

Dissipation 1.5V output @ 85°C

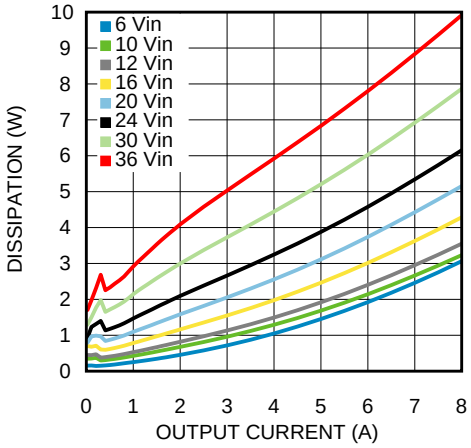


Figure 29.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

Efficiency 1.2V output @ 85°C

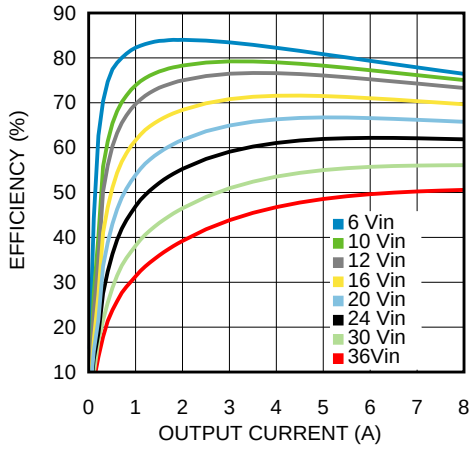


Figure 30.

Dissipation 1.2V output @ 85°C

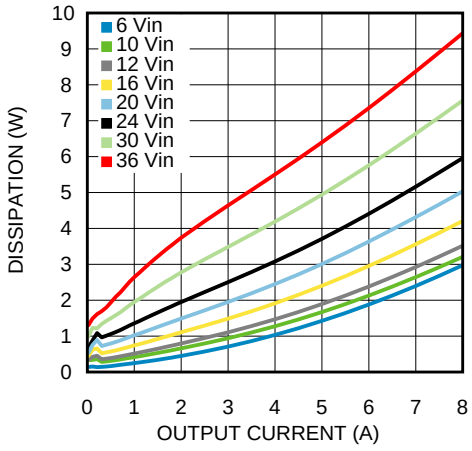


Figure 31.

Efficiency 1.0V output @ 85°C

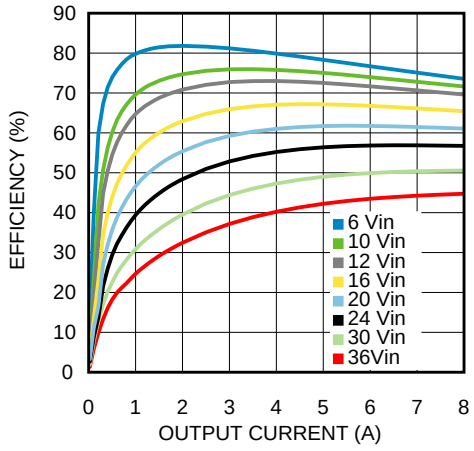


Figure 32.

Dissipation 1.0V output @ 85°C

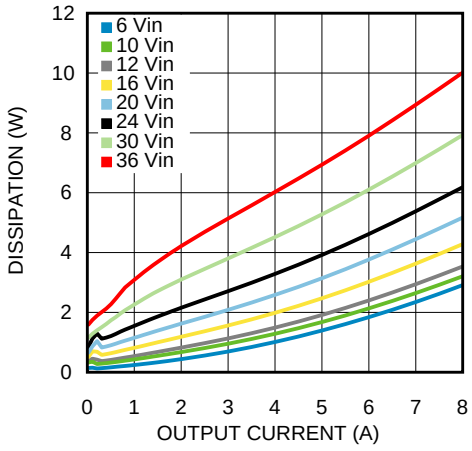


Figure 33.

Normalized line and load regulation V_{OUT} = 3.3V

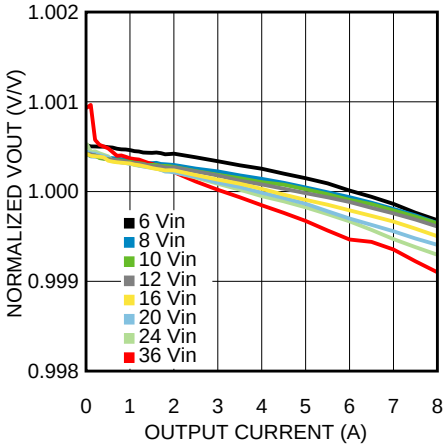


Figure 34.

Thermal derating V_{IN} = 24V, V_{OUT} = 5.0V

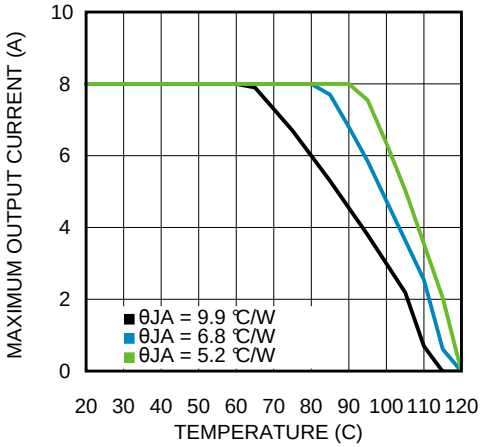


Figure 35.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

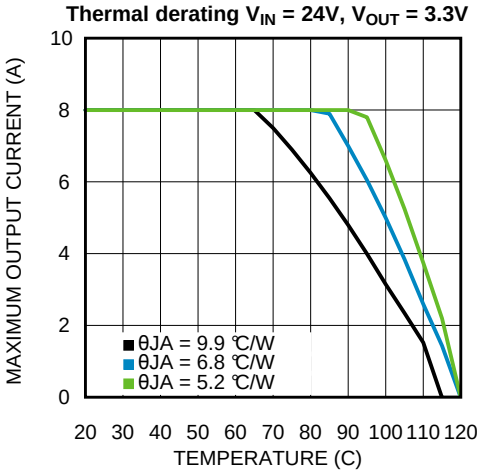


Figure 36.

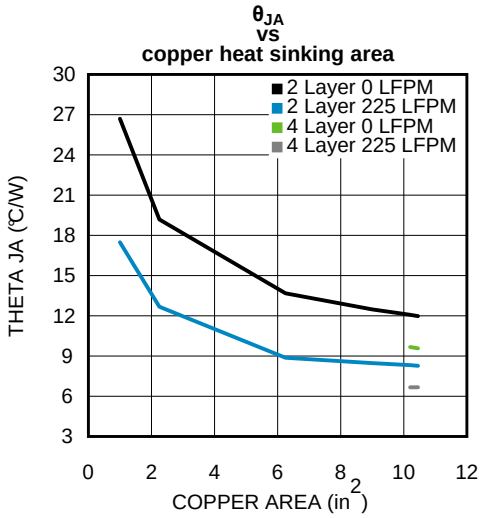


Figure 37.

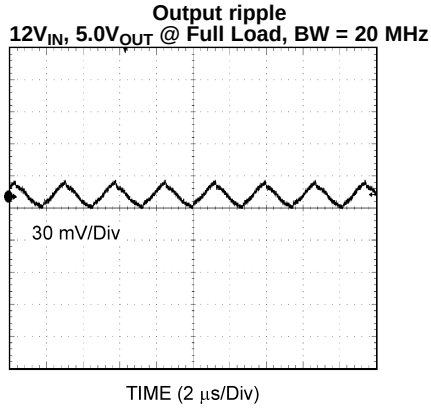


Figure 38.

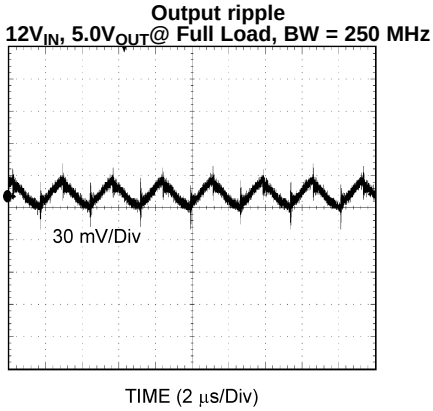


Figure 39.

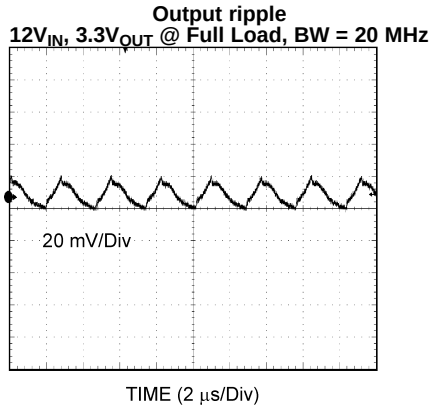


Figure 40.

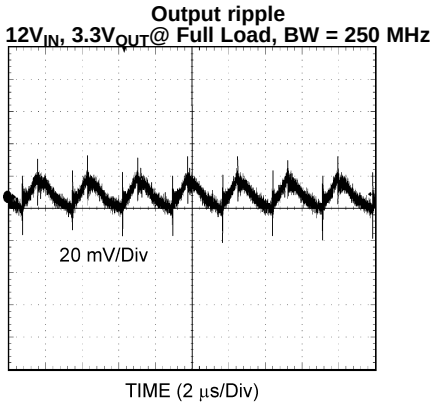


Figure 41.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

Output ripple
$12V_{IN}$, $1.2V_{OUT}$ @ Full Load, BW = 20 MHz

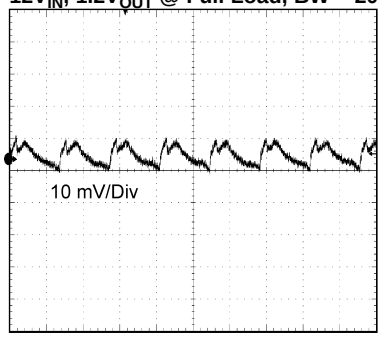


Figure 42.

Output ripple
$12V_{IN}$, $1.2V_{OUT}$@ Full Load, BW = 250 MHz

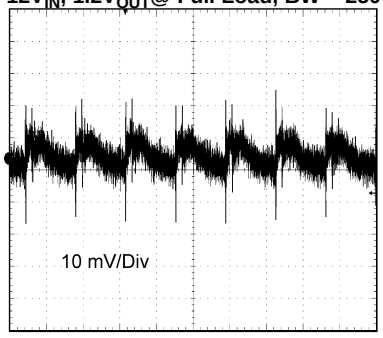


Figure 43.

Transient response
$12V_{IN}$, $5.0V_{OUT}$ 1 to 8A Step

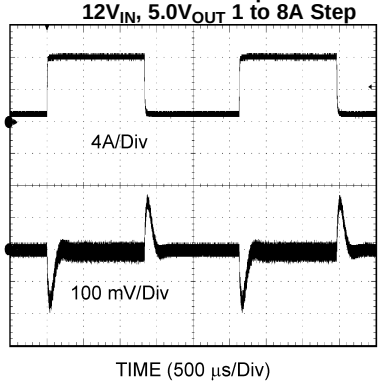


Figure 44.

Transient response
$12V_{IN}$, $3.3V_{OUT}$ 1 to 8A Step

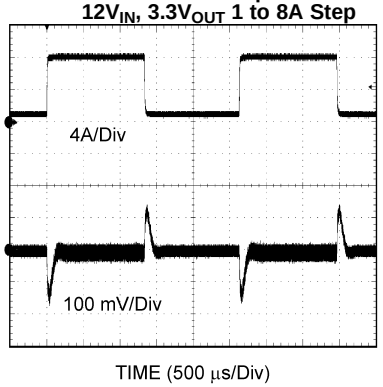


Figure 45.

Transient response
$12V_{IN}$, $1.2V_{OUT}$ 1 to 8A Step

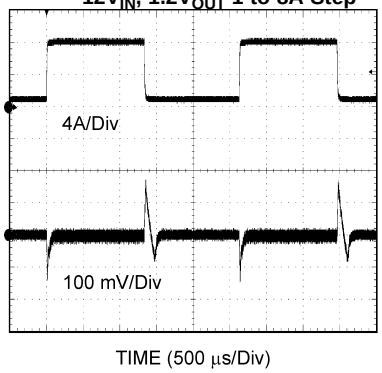


Figure 46.

Short circuit current
vs
input voltage

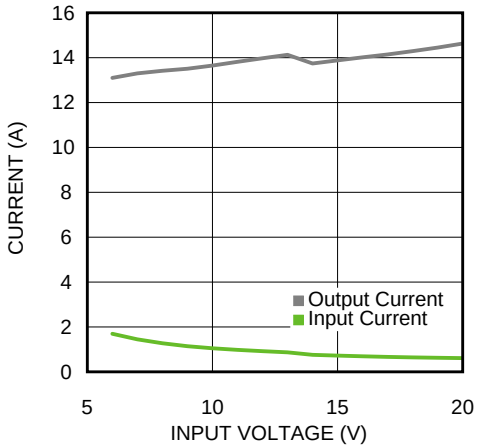


Figure 47.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; C_{IN} = three x 10µF + 47nF X7R Ceramic; C_{OUT} = two x 330µF Specialty Polymer + 47 uF Ceramic + 47nF Ceramic; C_{FF} = 4.7nF; Tambient = 25° C for waveforms. All indicated temperatures are ambient.

3.3V_{OUT} Soft Start, no C_{SS}

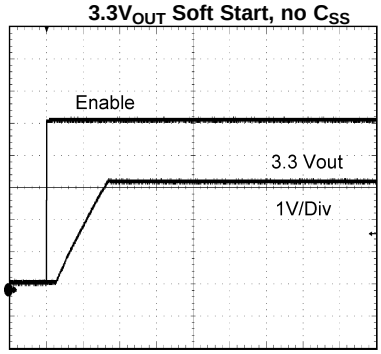


Figure 48.

3.3V_{OUT} Soft Start, C_{SS} = 0.47uF

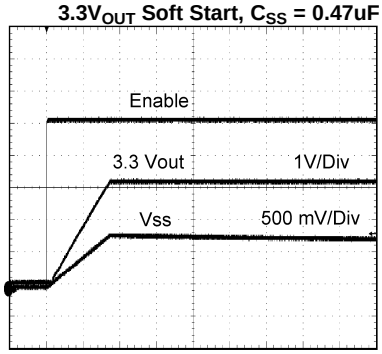
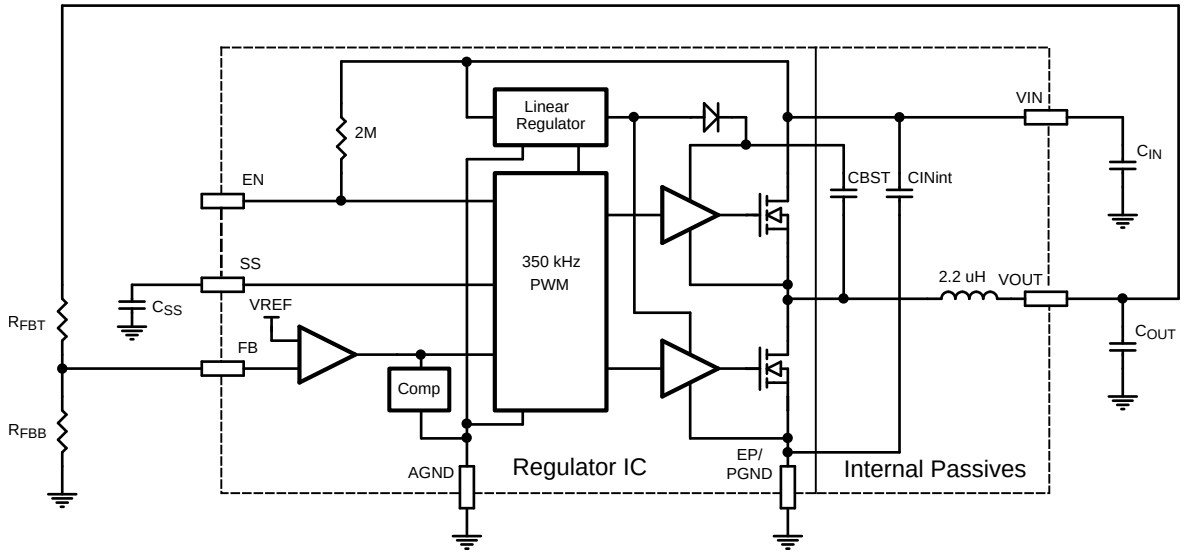


Figure 49.

BLOCK DIAGRAM



DESIGN STEPS FOR THE LMZ13608 APPLICATION

The LMZ13608 is fully supported by WEBENCH which offers: component selection, electrical and thermal simulations. Additionally, there are both evaluation and demonstration boards that may be used as a starting point for design. The following list of steps can be used to manually design the LMZ13608 application.

All references to values refer to the typical applications schematic.

- Select minimum operating V_{IN} with enable divider resistors
- Program V_{OUT} with FB resistor divider selection
- Select C_{OUT}
- Select C_{IN}
- Determine module power dissipation
- Layout PCB for required thermal performance

ENABLE DIVIDER, R_{ENT}, R_{ENB} AND R_{ENH}SELECTION

Internal to the module is a 2 mega ohm pull-up resistor connected from V_{IN} to Enable. For applications not requiring precision under voltage lock out (UVLO), the Enable input may be left open circuit and the internal resistor will always enable the module. In such case, the internal UVLO occurs typically at 4.3V (V_{IN} rising).

In applications with separate supervisory circuits Enable can be directly interfaced to a logic source. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ13608 output rail.

Enable provides a precise 1.274V threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. Additionally there is 13 µA (typ) of switched offset current allowing programmable hysteresis. See Figure 50.

The function of the enable divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of a programmable UVLO. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.274V) - 1 \quad (1)$$

The LMZ13608 typical application shows 12.7kΩ for R_{ENB} and 42.2kΩ for R_{ENT} resulting in a rising UVLO of 5.51V. Note that this divider presents 4.62V to the EN input when V_{IN} is raised to 20V. This upper voltage should always be checked, making sure that it never exceeds the Abs Max 5.5V limit for Enable. A 5.1V Zener clamp can be applied in cases where the upper voltage would exceed the EN input's range of operation. The zener clamp is not required if the target application prohibits the maximum Enable input voltage from being exceeded.

Additional enable voltage hysteresis can be added with the inclusion of R_{ENH}. It is possible to select values for R_{ENT} and R_{ENB} such that R_{ENH} is a value of zero allowing it to be omitted from the design.

Rising threshold can be calculated as follows:

$$V_{EN}(rising) = 1.274\ (\ 1 + (R_{ENT} || \ 2\ meg) / R_{ENB}) \quad (2)$$

Whereas the falling threshold level can be calculated using:

$$V_{EN}(falling) = V_{EN}(rising) - 13\ \mu A\ (\ R_{ENT} || \ 2\ meg\ ||\ R_{ENTB} + R_{ENH}\ ) \quad (3)$$

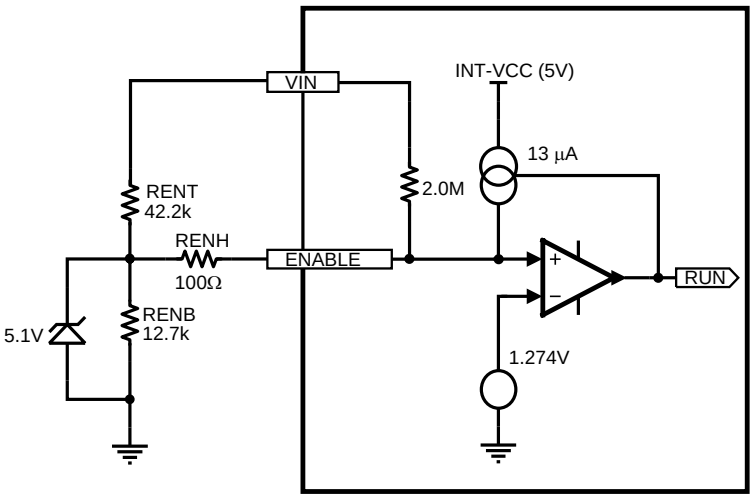


Figure 50. Enable input detail

OUTPUT VOLTAGE SELECTION

Output voltage is determined by a divider of two resistors connected between V_{OUT} and AGND. The midpoint of the divider is connected to the FB input.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_{OUT} = 0.795V * (1 + R_{FBT} / R_{FBB}) \quad (4)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_{OUT} / 0.795V) - 1 \quad (5)$$

These resistors should generally be chosen from values in the range of 1.0 kΩ to 10.0 kΩ.

For V_{OUT} = 0.8V the FB pin can be connected to the output directly and R_{FBB} can be set to 8.06kΩ to provide minimum output load.

A table of values for R_{FBT} , and R_{FBB}, is included in the Simplified Application Schematic.

SOFT-START CAPACITOR SELECTION

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time.

Upon turn-on, after all UVLO conditions have been passed, an internal 1.6msec circuit slowly ramps the SS input to implement internal soft start. If 1.6 msec is an adequate turn–on time then the Css capacitor can be left unpopulated. Longer soft-start periods are achieved by adding an external capacitor to this input.

Soft start duration is given by the formula:

$$t_{SS} = V_{REF} * C_{SS} / Iss = 0.795V * C_{SS} / 50uA \quad (6)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} * 50\mu A / 0.795V \quad (7)$$

Using a 0.22µF capacitor results in 3.5 msec typical soft-start duration; and 0.47µF results in 7.5 msec typical. 0.47 µF is a recommended initial value.

As the soft-start input exceeds 0.795V the output of the power stage will be in regulation and the 50 µA current is deactivated. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal current sink.

- The Enable input being pulled low
- A thermal shutdown condition
- V_{IN} falling below 4.3V (TYP) and triggering the V_{CC} UVLO

TRACKING SUPPLY DIVIDER OPTION

The tracking function allows the module to be connected as a slave supply to a primary voltage rail (often the 3.3V system rail) where the slave module output voltage is lower than that of the master. Proper configuration allows the slave rail to power up coincident with the master rail such that the voltage difference between the rails during ramp-up is small (i.e. <0.15V typ). The values for the tracking resistive divider should be selected such that the effect of the internal 50uA current source is minimized. In most cases the ratio of the tracking divider resistors is the same as the ratio of the output voltage setting divider. Proper operation in tracking mode dictates the soft-start time of the slave rail be shorter than the master rail; a condition that is easy to satisfy since the C_{SS} cap is replaced by R_{TKB}. The tracking function is only supported for the power up interval of the master supply; once the SS/TRK rises past 0.795V the input is no longer enabled and the 50 uA internal current source is switched off.

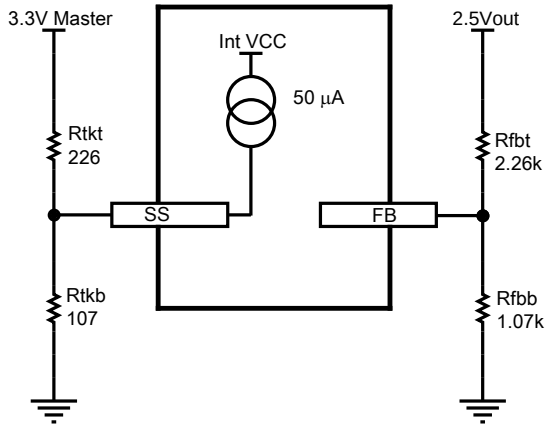


Figure 51. Tracking option input detail

C_{OUT} SELECTION

None of the required C_{OUT} output capacitance is contained within the module. A minimum value ranging from 330 µF for $6V_{OUT}$ to 660 µF for $1.2V_{OUT}$ applications is required based on the values of internal compensation in the error amplifier. These minimum values can be decreased if the effective capacitor ESR is higher than 15 mOhms.

A Low ESR (15 mOhm) tantalum, organic semiconductor or specialty polymer capacitor types in parallel with a 47nF X7R ceramic capacitor for high frequency noise reduction is recommended for obtaining lowest ripple. The output capacitor C_{OUT} may consist of several capacitors in parallel placed in close proximity to the module. The output voltage ripple of the module depends on the equivalent series resistance (ESR) of the capacitor bank, and can be calculated by multiplying the ripple current of the module by the effective impedance of your chosen output capacitors (for ripple current calculation, see Equation 18). Electrolytic capacitors will have large ESR and lead to larger output ripple than ceramic or polymer types. For this reason a combination of ceramic and polymer capacitors is recommended for low output ripple performance.

The output capacitor assembly must also meet the worst case ripple current rating of Δi_L, as calculated in Equation 18 below. Loop response verification is also valuable to confirm closed loop behavior.

For applications with dynamic load steps; the following equation provides a good first pass approximation of C_{OUT} for load transient requirements.

$$C_{OUT} \geq \frac{I_{step}}{(\Delta V_{OUT} - I_{STEP} \times ESR) \times (\frac{f_{SW}}{V_{OUT}})} \quad (8)$$

For $12V_{IN}$, $3.3V_{OUT}$, a transient voltage of 5% of V_{OUT} = 0.165V (ΔV_{OUT}), a 7A load step (I_{STEP}), an output capacitor effective ESR of 3 mOhms, and a switching frequency of 350kHz (f_{SW}):

$$C_{OUT} \geq \frac{8A}{(0.165V - 8A \times 0.003) \times (\frac{350e3}{3.3V})}$$

$$\geq 535\ \mu F \quad (9)$$

Note that the stability requirement for minimum output capacitance must always be met.

One recommended output capacitor combination is two 330µF, 15 mOhm ESR tantalum polymer capacitors connected in parallel with a 47 uF 6.3V X5R ceramic. This combination provides excellent performance that may exceed the requirements of certain applications. Additionally some small 47nF ceramic capacitors can be used for high frequency EMI suppression.

C_{IN} SELECTION

The LMZ13608 module contains two internal ceramic input capacitors. Additional input capacitance is required external to the module to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. This input capacitance should be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I_{CIN\text{-}RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

where

- $D \cong V_{OUT} / V_{IN}$ (10)

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 * V_{OUT}$).

Recommended minimum input capacitance is 30 uF X7R (or X5R) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature derating of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this parameter.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) to be maintained then the following equation may be used.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{f_{SW} \times \Delta V_{IN}} \quad (11)$$

If ΔV_{IN} is 200 mV or 1.66% of V_{IN} for a 12V input to 3.3V output application and f_{SW} = 350 kHz then:

$$C_{IN} \geq \frac{8A \times \left(\frac{3.3V}{12V}\right) \times \left(1 - \frac{3.3V}{12V}\right)}{350\ kHz \times 200\ mV} \geq 22.4\ \mu F \quad (12)$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines. The LMZ13608 typical applications schematic and evaluation board include a 150 µF 50V aluminum capacitor for this function. There are many situations where this capacitor is not necessary.

POWER DISSIPATION AND BOARD THERMAL REQUIREMENTS

When calculating module dissipation use the maximum input voltage and the average output current for the application. Many common operating conditions are provided in the characteristic curves such that less common applications can be derived through interpolation. In all designs, the junction temperature must be kept below the rated maximum of 125°C.

For the design case of V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 8A, and $T_{A\text{-}MAX}$ = 50°C, the module must see a thermal resistance from case to ambient (θ_{CA}) of less than:

$$\theta_{CA} < \frac{T_{J\text{-}MAX} - T_{A\text{-}MAX}}{P_{IC\_LOSS}} - \theta_{JC} \tag{13}$$

Given the typical thermal resistance from junction to case (θ_{JC}) to be 1.0 °C/W. Use the 85°C power dissipation curves in the Typical Performance Characteristics section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 3.9W.

$$\theta_{CA} < \frac{125℃ - 50℃}{3.9\ W} - 1.0\frac{℃}{W} < 18.23\frac{℃}{W} \tag{14}$$

To reach θ_{CA} = 18.23, the PCB is required to dissipate heat effectively. With no airflow and no external heat-sink, a good estimate of the required board area covered by 2 oz. copper on both the top and bottom metal layers is:

$$\text{Board Area\_cm}^2 \geq \frac{500}{\theta_{CA}} \cdot \frac{℃\ x\ cm^2}{W} \tag{15}$$

As a result, approximately 27.42 square cm of 2 oz copper on top and bottom layers is the minimum required area for the example PCB design. This is 5.23 x 5.23 cm (2.06 x 2.06 in) square. The PCB copper heat sink must be connected to the exposed pad. For best performance, use approximately 100, 12mil (305 µm) thermal vias spaced 59 mil (1.5 mm) apart connect the top copper to the bottom copper.

Another way to estimate the temperature rise of a design is using θ_{JA}. An estimate of θ_{JA} for varying heat sinking copper areas and airflows can be found in the typical applications curves. If our design required the same operating conditions as before but had 225 LFPM of airflow. We locate the required θ_{JA} of

$$\theta_{JA} < \frac{T_{J\text{-}MAX} - T_{A\text{-}MAX}}{P_{IC\_LOSS}}$$

$$\theta_{JA} < \frac{(125 - 50)\ ℃}{3.9\ W} < 19.23\frac{℃}{W} \tag{16}$$

On the Theta JA vs copper heatsinking curve, the copper area required for this application is now only 1 square inches. The airflow reduced the required heat sinking area by a factor of four.

To reduce the heat sinking copper area further, this package is compatible with D3-PAK surface mount heat sinks.

For an example of a high thermal performance PCB layout for SIMPLE SWITCHER power modules, refer to AN-2093 (SNVA460), AN-2084 (SNVA456), AN-2125 (SNVA473), AN-2020 (SNVA419) and AN-2026 (SNVA424).

PC BOARD LAYOUT GUIDELINES

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules. A good layout example is shown in Figure 56.

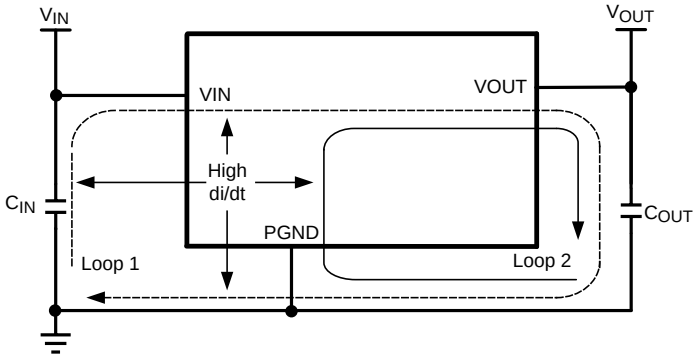


Figure 52. High Current Loops

1. Minimize area of switched current loops.

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout as shown in Figure 52. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (C_{IN}) is placed at a distance away from the LMZ13608. Therefore place C_{IN} as close as possible to the LMZ13608 VIN and PGND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad (EP).

2. Have a single point ground.

   The ground connections for the feedback, soft-start, and enable components should be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Additionally provide a single point ground connection from pin 4 (AGND) to EP/PGND.

3. Minimize trace length to the FB pin.

   Both feedback resistors, R_{FBT} and R_{FBB} should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB} should be routed away from the body of the LMZ13608 to minimize possible noise pickup.

4. Make input and output bus connections as wide as possible.

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. For best results use a 10 x 10 via array or larger with a minimum via diameter of 12mil (305 µm) thermal vias spaced 46.8mil (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

ADDITIONAL FEATURES

OUTPUT OVER-VOLTAGE PROTECTION

If the voltage at FB is greater than a 0.86V internal reference, the output of the error amplifier is pulled toward ground, causing V_{OUT} to fall.

CURRENT LIMIT

The LMZ13608 is protected by both low side (LS) and high side (HS) current limit circuitry. The LS current limit detection is carried out during the off-time by monitoring the current through the LS synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 13A (typical) the current limit comparator disables the start of the next switching period. Switching cycles are prohibited until current drops below the limit. It should also be noted that d.c. current limit is dependent on duty cycle as illustrated in the graph in the Typical Performance Characteristics. The HS current limit monitors the current of top side MOSFET. Once HS current limit is detected (16A typical) , the HS MOSFET is shutoff immediately, until the next cycle. Exceeding HS current limit causes V_{OUT} to fall. Typical behavior of exceeding LS current limit is that f_{SW} drops to 1/2 of the operating frequency.

THERMAL PROTECTION

The junction temperature of the LMZ13608 should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 150 °C (typ Hyst = 15°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures.

PRE-BIASED STARTUP

The LMZ13608 will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The following scope capture shows proper behavior in this mode. Trace one is Enable going high. Trace two is 1.8V pre-bias rising to 3.3V. Trace three is the SS voltage with a C_{SS}= 0.47uF. Risetime determined by C_{SS}.

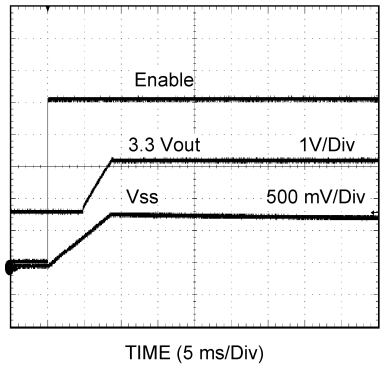


Figure 53. Pre-Biased Startup

DISCONTINUOUS CONDUCTION AND CONTINUOUS CONDUCTION MODES

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM, inductor current is maintained to an average value equaling Iout . In DCM the low-side switch will turn off when the inductor current falls to zero, this causes the inductor current to resonate. Although it is in DCM, the current is allowed to go slightly negative to charge the bootstrap capacitor.

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time.

Following is a comparison pair of waveforms showing both the CCM (upper) and DCM operating modes.

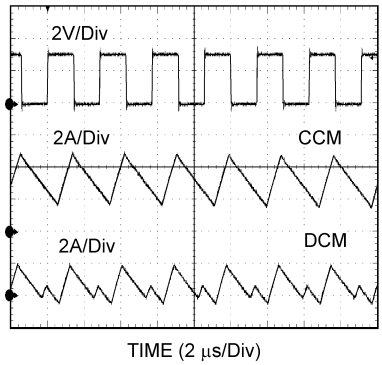


Figure 54. CCM and DCM Operating Modes
V_{IN} = 12V, V_O = 3.3V, I_O = 3A/0.3A

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f_{SW}} \quad (17)$$

The inductor internal to the module is 2.2 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (Δi_L). Δi_L can be calculated with:

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

where

- V_{IN} is the maximum input voltage
- f_{SW} is typically 359 kHz (18)

If the output current I_{OUT} is determined by assuming that $I_{OUT} = I_L$, the higher and lower peak of Δi_L can be determined.

Typical Application Schematic Diagram and BOM

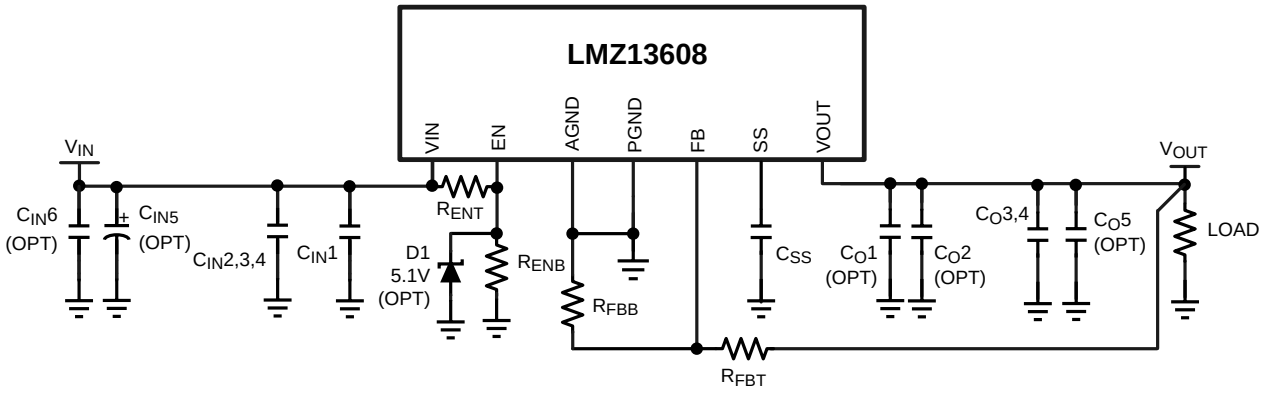


Figure 55.

Table 1. Typical Application Bill of Materials

Ref Des	Description	Case Size	Manufacturer	Manufacturer P/N
U1	SIMPLE SWITCHER	PFM-11	Texas Instruments	LMZ13608TZ
C_{IN}1,6 (OPT)	0.047 µF, 50V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_{IN}2,3,4	10 µF, 50V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{IN}5 (OPT)	CAP, AL, 150µF, 50V	Radial G	Panasonic	EEE-FK1H151P
C_O1,5 (OPT)	0.047 µF, 50V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_O2 (OPT)	47 µF, 10V, X7R	1210	Murata	GRM32ER61A476KE20L
C_O3,4	330 µF, 6.3V, 0.015 ohm	CAPSMT_6_UE	Kemet	T520D337M006ATE015
R_{FBT}	3.32 kΩ	0805	Panasonic	ERJ-6ENF3321V
R_{FBB}	1.07 kΩ	0805	Panasonic	ERJ-6ENF1071V
R_{ENT}	42.2 kΩ	0805	Panasonic	ERJ-6ENF4222V
R_{ENB}	12.7 kΩ	0805	Panasonic	ERJ-6ENF1272V
C_{SS}	0.47 µF, ±10%, X7R, 16V	0805	AVX	0805YC474KAT2A
D1 (OPT)	5.1V, 0.5W	SOD-123	Diodes Inc.	MMSZ5231BS-7-F

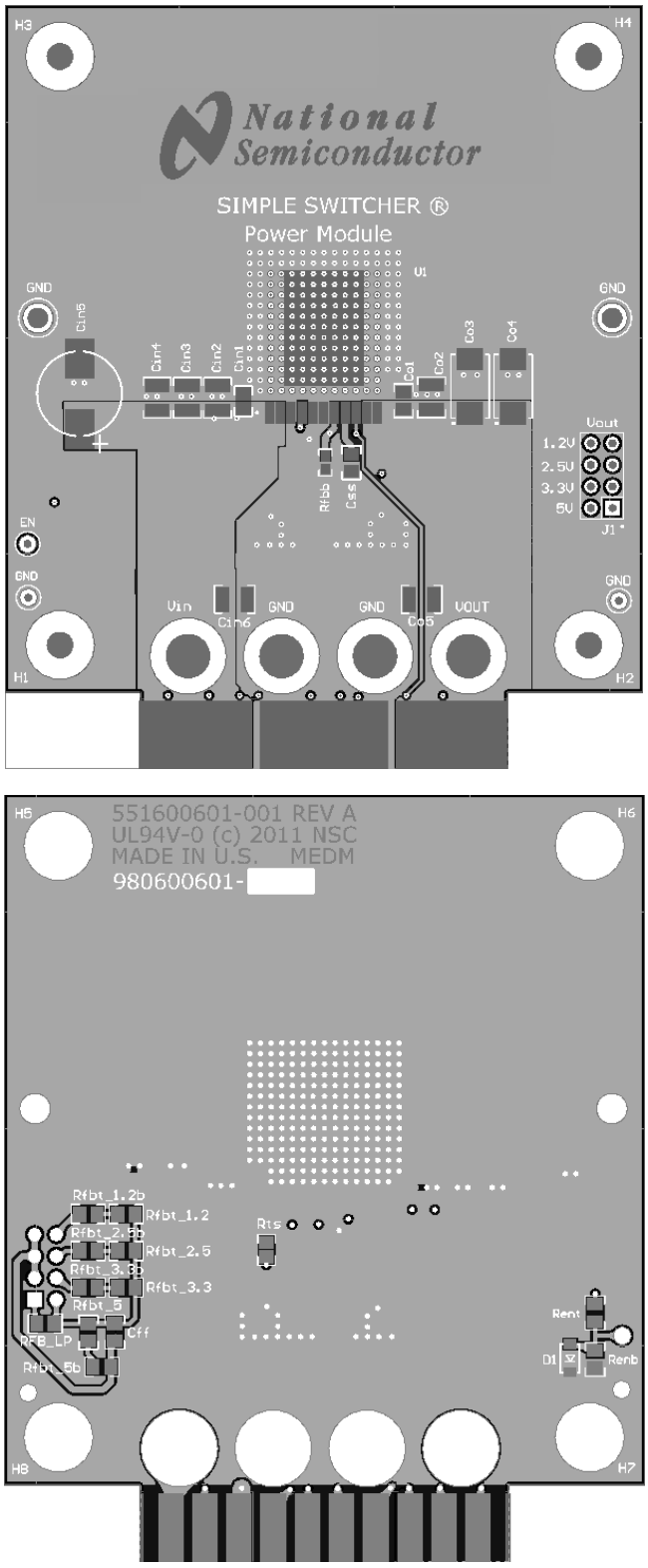


Figure 56. Layout example

REVISION HISTORY

Changes from Revision E (July 2013) to Revision F **Page**

- Changed the Simplified Application Schematic. 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ13608TZ/NOPB	ACTIVE	PFM	NDY	11	32	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 85	LMZ13608	Samples
LMZ13608TZE/NOPB	ACTIVE	PFM	NDY	11	250	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 85	LMZ13608	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

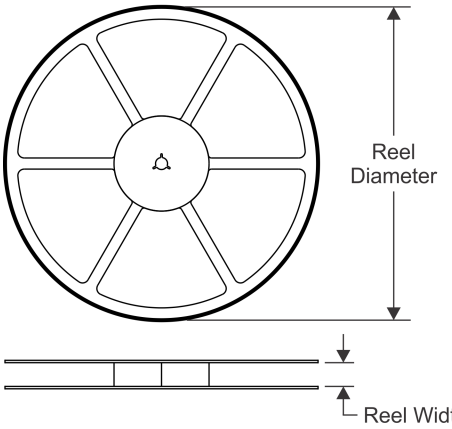
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

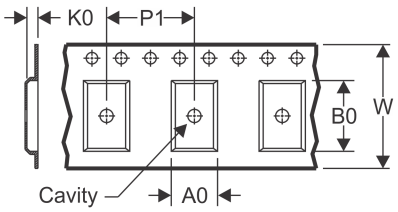
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

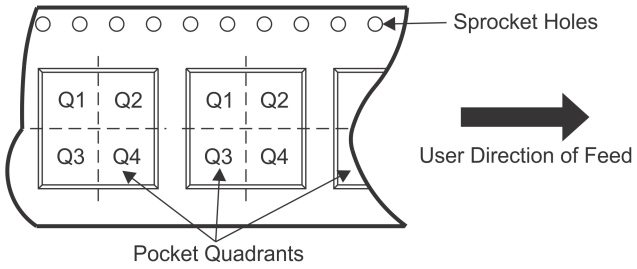


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

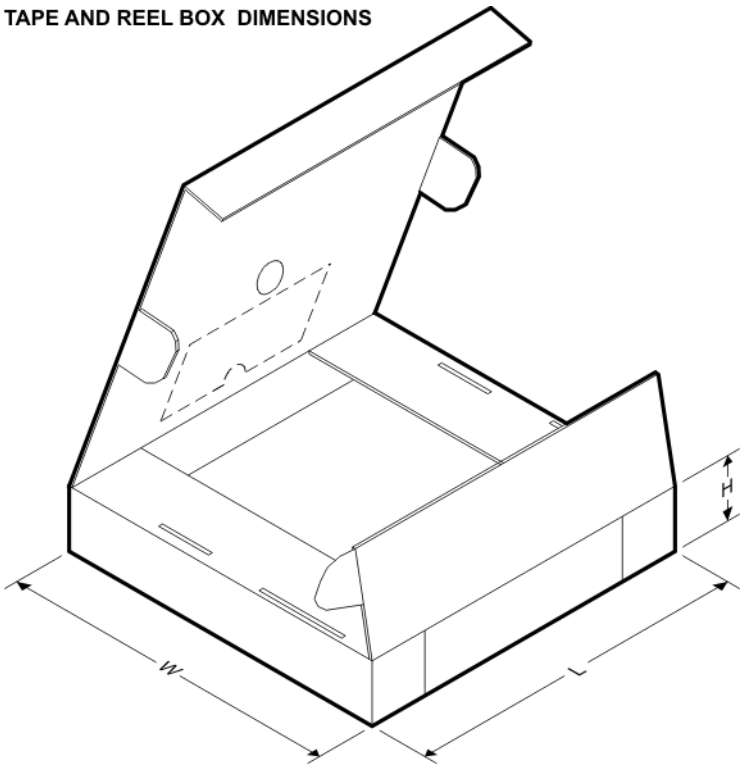
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ13608TZE/NOPB	PFM	NDY	11	250	330.0	32.4	15.45	18.34	6.2	20.0	32.0	Q2

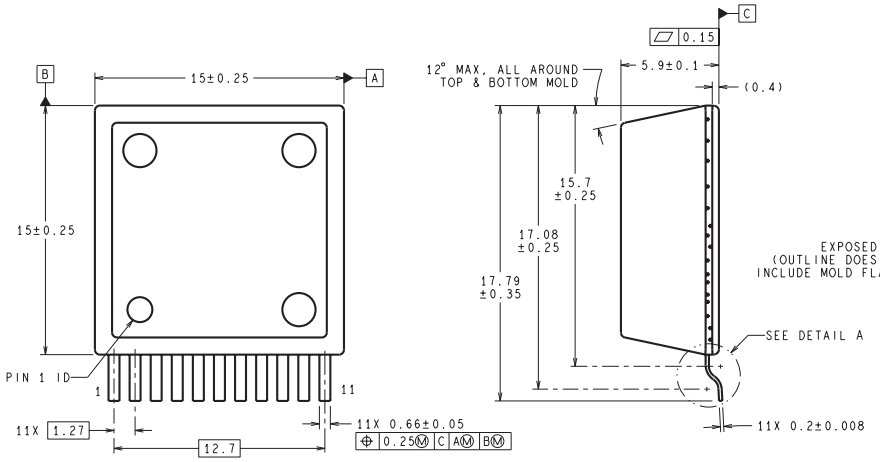
TAPE AND REEL BOX DIMENSIONS



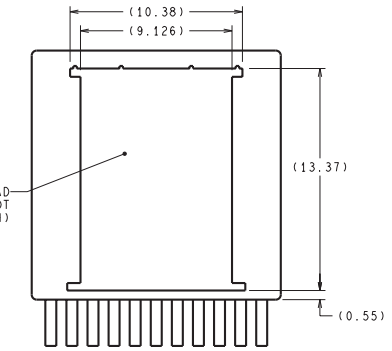
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ13608TZE/NOPB	PFM	NDY	11	250	367.0	367.0	55.0

NDY0011A

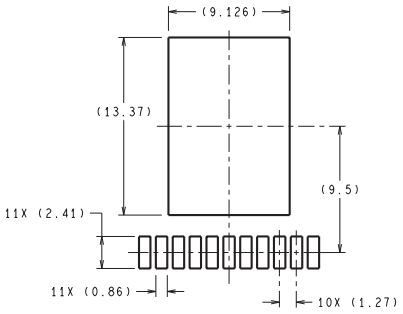


TOP SIDE OF PACKAGE

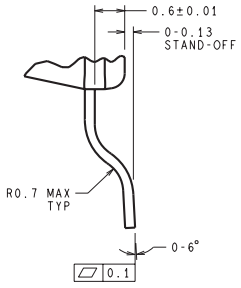


BOTTOM SIDE OF PACKAGE

DIMMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



DETAIL A
TYPICAL

TZA11A (Rev F)

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