

# 适用于 DDR2、DDR3、DDR3L 和 DDR4 且具有 VTTREF 缓冲基准的 TPS51206 2A 峰值灌电流/拉电流 DDR 终端稳压器

## 1 特性

- 电源输入电压：支持 3.3V 和 5V 电源轨
- VLDOIN 输入电压范围：VTT+0.4V 至 3.5V
- VTT 端接稳压器
  - 输出电压范围：0.5V 至 0.9V
  - 2A 峰值灌电流和拉电流
  - 仅需 10μF 的多层陶瓷电容 (MLCC) 输出电容
  - ±20mV 精度
- VTTREF 缓冲参考输出
  - VDDQ/2 ± 1% 精度
  - 10mA 灌/拉电流
- 支持高阻态 (S3 状态) 和软停止 (S4 和 S5 状态)，通过 S3 和 S5 输入选择
- 过热保护
- 10 引脚 2mm × 2mm 小外形尺寸无引线 (SON) (DSQ) 封装

## 2 应用

- DDR2、DDR3、DDR3L 和 DDR4 存储器电源
- SSTL\_18、SSTL\_15、SSTL\_135 和 HSTL 终端
- 电信和数据通信、GSM 基站、液晶 (LCD) 电视和等离子 (PDP) 电视、复印机和打印机、机顶盒

## 3 说明

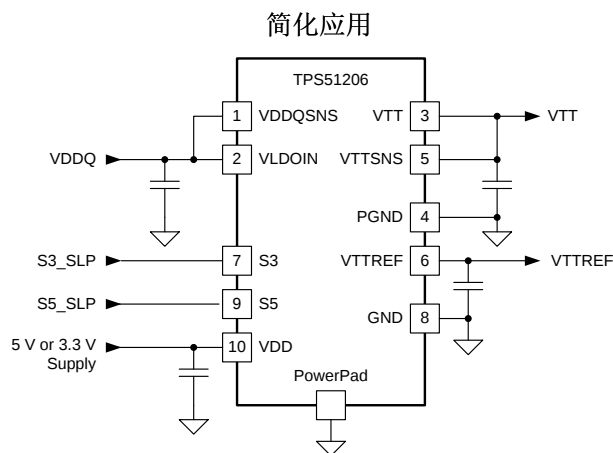
TPS51206 器件是具有 VTTREF 缓冲基准输出的灌电流/拉电流双倍数据速率 (DDR) 终端稳压器。该器件专门针对低输入电压、低成本、低外部组件数的空间受限型系统而设计。该器件可保持快速的瞬态响应，并且仅需 1 个 10μF 的陶瓷输出电容。该器件支持遥感功能，并且可满足 DDR2、DDR3 和低功耗 DDR3 (DDR3L) 及 DDR4 VTT 总线的所有电源要求。VTT 具有 ±2A 峰值电流能力。该器件支持所有 DDR 电源状态，在 S3 状态下将 VTT 置于高阻态（挂起到 RAM）；在 S4/S5 状态下使 VTT 和 VTTREF 放电（挂起到磁盘）。

TPS51206 器件采用 10 引脚 2mm × 2mm SON (DSQ) PowerPAD™封装，额定工作温度范围为 -40°C 至 105°C。

### 器件信息<sup>(1)</sup>

| 器件型号     | 封装       | 封装尺寸 (标称值)      |
|----------|----------|-----------------|
| TPS51206 | WSO (10) | 2.00mm x 2.00mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

### Changes from Revision D (March 2018) to Revision E Page

- 已更改 将“额定工作温度范围为  $-40^{\circ}\text{C}$  至  $85^{\circ}\text{C}$ ”更改为“额定工作温度范围为  $-40^{\circ}\text{C}$  至  $105^{\circ}\text{C}$ ”（“说明”部分） ..... 1
- Changed maximum operating temperature from " $85^{\circ}\text{C}$ " to " $105^{\circ}\text{C}$ " in *Recommended Operating Conditions* table ..... 4

### Changes from Revision C (August 2016) to Revision D Page

- 已添加 VTTREF tolerance at 100  $\mu\text{A}$  condition ..... 5

### Changes from Revision B (December 2014) to Revision C Page

- 已添加 参考至 DDR4 兼容性 ..... 1
- 已添加 [接收文档更新通知](#) 部分 ..... 19
- 已添加 [社区资源](#) 部分 ..... 19

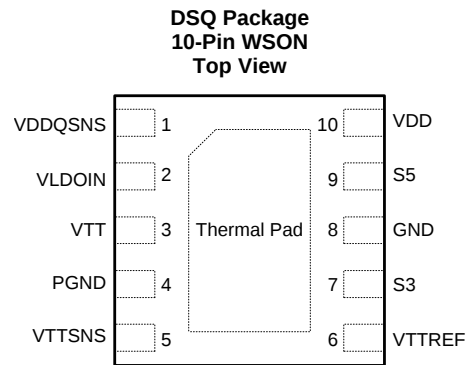
### Changes from Revision A (October 2013) to Revision B Page

- 已添加 引脚配置和功能部分，ESD 额定值表，特性 说明 部分、器件功能模式、应用和实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 ..... 1

### Changes from Original (MAY 2011) to Revision A Page

- 已添加 minimum and maximum values to the wake up condition of the VDD UVLO threshold voltage specification ..... 5

## 5 Pin Configuration and Functions



### Pin Functions

| PIN         |     | I/O | DESCRIPTION                                                                                                                 |
|-------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO. |     |                                                                                                                             |
| GND         | 8   | —   | Signal ground                                                                                                               |
| PGND        | 4   | —   | Power GND for VTT LDO                                                                                                       |
| S3          | 7   | I   | S3 signal input                                                                                                             |
| S5          | 9   | I   | S5 signal input                                                                                                             |
| VDD         | 10  | I   | Device power supply input (3.3 V or 5 V)                                                                                    |
| VDDQSNS     | 1   | I   | VDDQ sense input, reference input for VTTREF                                                                                |
| VLDOIN      | 2   | I   | Power supply input for VTT/ VTTREF                                                                                          |
| VTT         | 3   | O   | Power output for VTT LDO, need to connect 10-μF or greater MLCC for stability. No maximum limit for VTT output capacitance. |
| VTTREF      | 6   | O   | VTTREF buffered reference output. Connect to MLCC between 0.22-μF and 1-μF for stability. The VTTREF pin can not be open.   |
| VTTSNS      | 5   | I   | VTT LDO voltage sense input                                                                                                 |
| Thermal Pad |     | —   | Solder to the ground plane for increased thermal performance.                                                               |

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

|                                                |                         | MIN  | MAX | UNIT |
|------------------------------------------------|-------------------------|------|-----|------|
| Input voltage <sup>(2)</sup>                   | VDD, S3, S5             | –0.3 | 7   | V    |
|                                                | VLDOIN, VTTSNS, VDDQSNS | –0.3 | 3.6 | V    |
|                                                | PGND                    | –0.3 | 0.3 |      |
| Output voltage <sup>(2)</sup>                  | VTT, VTTREF             | –0.3 | 3.6 |      |
| Operation junction temperature, T <sub>J</sub> |                         | –40  | 150 | °C   |
| Storage temperature, T <sub>stg</sub>          |                         | –55  | 150 | °C   |

- (1) Stresses beyond those listed under [Absolute Maximum Ratings<sup>\(1\)</sup>](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|                                                |                         | MIN  | NOM | MAX | UNIT |
|------------------------------------------------|-------------------------|------|-----|-----|------|
| Supply voltage                                 | VDD                     | 3.1  |     | 6.5 | V    |
| Input voltage range <sup>(1)</sup>             | S3, S5                  | –0.1 |     | 6.5 | V    |
|                                                | VLDOIN, VTTSNS, VDDQSNS | –0.1 |     | 3.5 |      |
|                                                | PGND                    | –0.1 |     | 0.1 |      |
| Output voltage range <sup>(1)</sup>            | VTT, VTTREF             | –0.1 |     | 3.5 | V    |
| Operating free-air temperature, T <sub>A</sub> |                         | –40  |     | 105 | °C   |

- (1) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS51206   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | DSQ (WSON) |      |
|                               |                                              | 10 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 70.3       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 46.3       |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 33.8       |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 2.9        |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 33.5       |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 16.3       |      |

- (1) 有关传统和新热指标的更多信息，请参见应用报告《半导体和 IC 封装热指标》（文献编号：SPRA953）。

## 6.5 Electrical Characteristics

Over operating free-air temperature range,  $V_{DD} = 5\text{ V}$ , VLDOIN is connected to VDDQSNS,  $V_{S3} = V_{S5} = 5\text{ V}$  (unless otherwise noted)

| PARAMETER                          |                                             | TEST CONDITION                                                                                                   | MIN             | TYP  | MAX    | UNIT             |
|------------------------------------|---------------------------------------------|------------------------------------------------------------------------------------------------------------------|-----------------|------|--------|------------------|
| <b>SUPPLY CURRENT</b>              |                                             |                                                                                                                  |                 |      |        |                  |
| $I_{VDD(S0)}$                      | VDD supply current, in S0                   | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 5\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$                |                 | 170  |        | $\mu\text{A}$    |
| $I_{VDD(S3)}$                      | VDD supply current, in S3                   | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$ |                 | 80   |        | $\mu\text{A}$    |
| $I_{VDDSDN}$                       | VDD shutdown current, in S4 and S5          | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{VDDQSNS} = 1.8\text{ V}$                |                 |      | 1      | $\mu\text{A}$    |
| $I_{VLDOIN(S0)}$                   | VLDOIN supply current, in S0                | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 5\text{ V}$ , $V_{LDION} = 1.8\text{ V}$                  |                 |      | 5      | $\mu\text{A}$    |
| $I_{VLDOIN(S3)}$                   | VLDOIN supply current, in S3                | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{LDION} = 1.8\text{ V}$   |                 |      | 5      | $\mu\text{A}$    |
| $I_{VLDOINSDN}$                    | VLDOIN shutdown current, in S4 and S5       | $T_A = 25^\circ\text{C}$ , No load, $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{LDION} = 1.8\text{ V}$                  |                 |      | 5      | $\mu\text{A}$    |
| <b>VTTREF OUTPUT</b>               |                                             |                                                                                                                  |                 |      |        |                  |
| $V_{VTTREF}$                       | Output voltage                              |                                                                                                                  | $V_{VDDQSNS}/2$ |      |        | V                |
| $V_{VTTREFTOL}$                    | Output voltage tolerance to $V_{VDDQSNS}$   | $ I_{VTTREF}  \leq 10\text{ mA}$ , $1.5\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$                             | 49%             |      | 51%    |                  |
|                                    |                                             | $ I_{VTTREF}  \leq 10\text{ mA}$ , $1.2\text{ V} \leq V_{VDDQSNS} < 1.5\text{ V}$                                | 48.75%          |      | 51.25% |                  |
|                                    |                                             | $ I_{VTTREF}  \leq 100\text{ }\mu\text{A}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$                   | 49%             |      | 51%    |                  |
| $I_{VTTREFSRC}$                    | Source current                              | $V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTTREF} = 0\text{ V}$                                                         | 10              |      |        | mA               |
| $I_{VTTREFSNK}$                    | Sink current                                | $V_{VDDQSNS} = 0\text{ V}$ , $V_{VTTREF} = 1.8\text{ V}$                                                         | 10              |      |        | mA               |
| $I_{VTTREFDIS}$                    | VTTREF Discharge current                    | $T_A = 25^\circ\text{C}$ , $V_{S3} = V_{S5} = 0\text{ V}$ , $V_{VTTREF} = 0.5\text{ V}$                          |                 | 1.3  |        | mA               |
| <b>VTT OUTPUT</b>                  |                                             |                                                                                                                  |                 |      |        |                  |
| $V_{VTT}$                          | Output voltage                              |                                                                                                                  | $V_{VDDQSNS}/2$ |      |        | V                |
| $V_{VTTTOL}$                       | Output voltage tolerance to $V_{VDDQSNS}/2$ | $ I_{VTT}  \leq 10\text{ mA}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}$                                | -20             |      | 20     | mV               |
|                                    |                                             | $ I_{VTT}  < 1\text{ A}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}^{(1)}$                               | -30             |      | 30     |                  |
|                                    |                                             | $ I_{VTT}  < 2\text{ A}$ , $1.4\text{ V} \leq V_{VDDQSNS} \leq 1.8\text{ V}^{(1)}$                               | -40             |      | 40     |                  |
|                                    |                                             | $ I_{VTT}  \leq 10\text{ mA}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.4\text{ V}$                                | -20             |      | 20     |                  |
|                                    |                                             | $ I_{VTT}  < 1\text{ A}$ , $1.2\text{ V} \leq V_{VDDQSNS} \leq 1.4\text{ V}^{(1)}$                               | -30             |      | 30     |                  |
|                                    |                                             | $ I_{VTT}  < 1.5\text{ A}$ , $1.2\text{ V} \leq V_{VDDQSNS} < 1.4\text{ V}^{(1)}$                                | -40             |      | 40     |                  |
| $I_{VTTCLSRC}$                     | Source current limit                        | $V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTT} = V_{VTTNS} = 0.7\text{ V}$                                              | 2               |      |        | A                |
| $I_{VTTCLSNK}$                     | Sink current limit                          | $V_{VDDQSNS} = 1.8\text{ V}$ , $V_{VTT} = V_{VTTNS} = 1.1\text{ V}$                                              | 2               |      |        | A                |
| $I_{VTTLK}$                        | Leakage current                             | $T_A = 25^\circ\text{C}$ , $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTT} = V_{VTTREF}$                |                 |      | 5      | $\mu\text{A}$    |
| $I_{VTTNSBIAS}$                    | VTTNS input bias current                    | $V_{S3} = 5\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTTNS} = V_{VTTREF}$                                         | -0.1            |      | 0.1    | $\mu\text{A}$    |
| $I_{VTTNSLK}$                      | VTTNS leakage current                       | $V_{S3} = 0\text{ V}$ , $V_{S5} = 5\text{ V}$ , $V_{VTTNS} = V_{VTTREF}$                                         | -0.1            |      | 0.1    | $\mu\text{A}$    |
| $I_{VTTDIS}$                       | VTT Discharge current                       | $T_A = 25^\circ\text{C}$ , $V_{S3} = V_{S5} = V_{VDDQSNS} = 0\text{ V}$ , $V_{VTT} = 0.5\text{ V}$               |                 | 7    |        | mA               |
| <b>VDDQ INPUT</b>                  |                                             |                                                                                                                  |                 |      |        |                  |
| $I_{VDDQSNS}$                      | VDDQSNS input current                       | $V_{VDDQSNS} = 1.8\text{ V}$                                                                                     |                 | 30   |        | $\mu\text{A}$    |
| <b>UVLO/LOGIC THRESHOLD</b>        |                                             |                                                                                                                  |                 |      |        |                  |
| $V_{VDDUV}$                        | VDD UVLO threshold voltage                  | Wake up                                                                                                          | 2.67            | 2.90 | 3.00   | V                |
|                                    |                                             | Hysteresis                                                                                                       |                 | 0.2  |        |                  |
| $V_{LL}$                           | S3 and S5 low-level voltage                 |                                                                                                                  |                 |      | 0.5    | V                |
| $V_{LH}$                           | S3 and S5 high-level voltage                |                                                                                                                  | 1.8             |      |        | V                |
| $V_{LHYS}$                         | S3 and S5 hysteresis voltage                |                                                                                                                  |                 | 0.3  |        | V                |
| $I_{LHLK}$                         | S3 and S5 input leak current                |                                                                                                                  | -1              |      | 1      | $\mu\text{A}$    |
| <b>OVER-TEMPERATURE PROTECTION</b> |                                             |                                                                                                                  |                 |      |        |                  |
| $T_{OTP}$                          | Over temperature protection                 | Shutdown temperature <sup>(1)</sup>                                                                              |                 | 150  |        | $^\circ\text{C}$ |
|                                    |                                             | Hysteresis <sup>(1)</sup>                                                                                        |                 | 10   |        |                  |

(1) Ensured by design. Not production tested.

## 6.6 Typical Characteristics

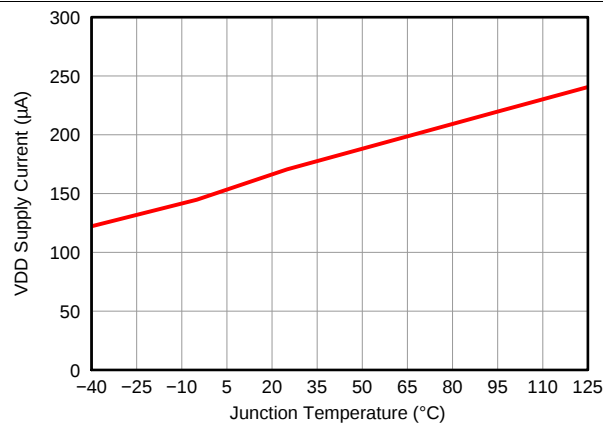


图 1. VDD Supply Current vs. Junction Temperature

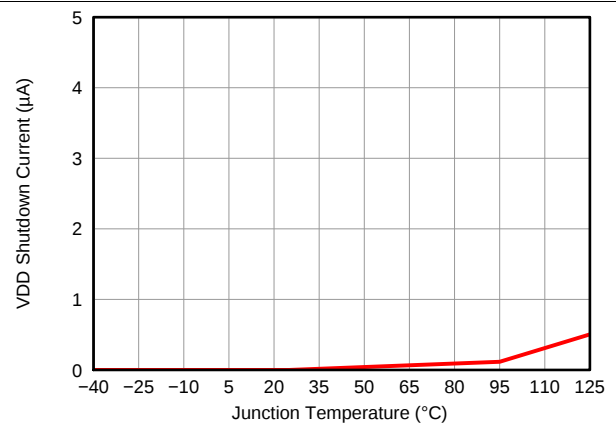


图 2. VDD Shutdown Current vs. Junction Temperature

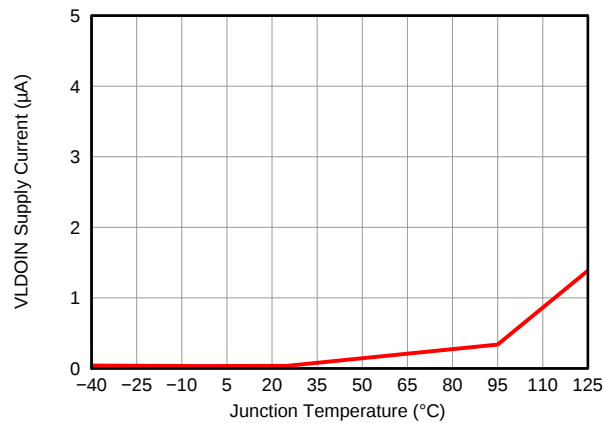


图 3. VLDOIN Supply Current vs. Junction Temperature

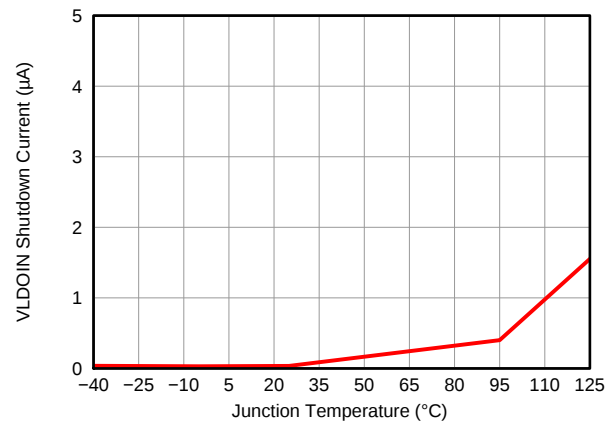


图 4. VLDOIN Shutdown Current vs. Junction Temperature

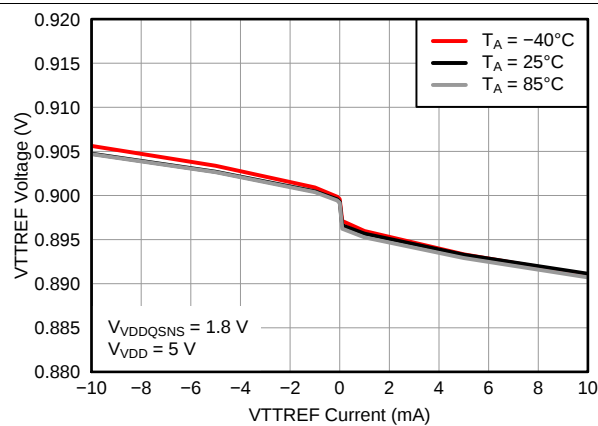


图 5. VTTREF Load Regulation (0.9 V)

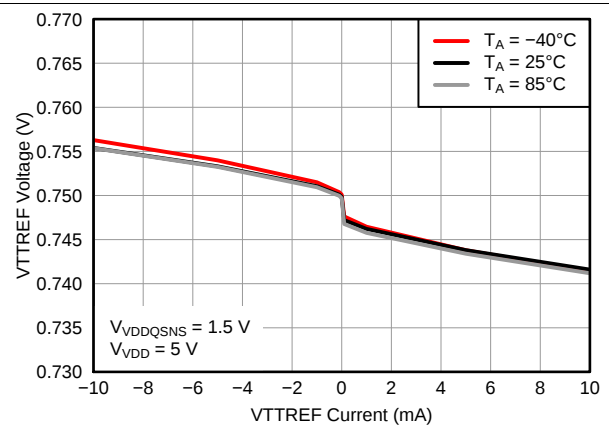


图 6. VTTREF Load Regulation (0.75 V)

## Typical Characteristics (接下页)

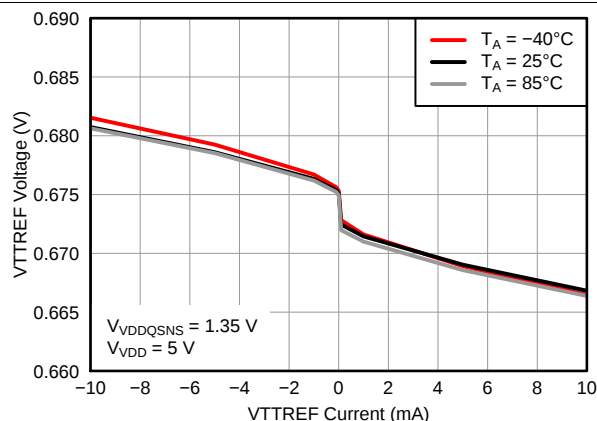


图 7. VTTREF Load Regulation (0.675 V)

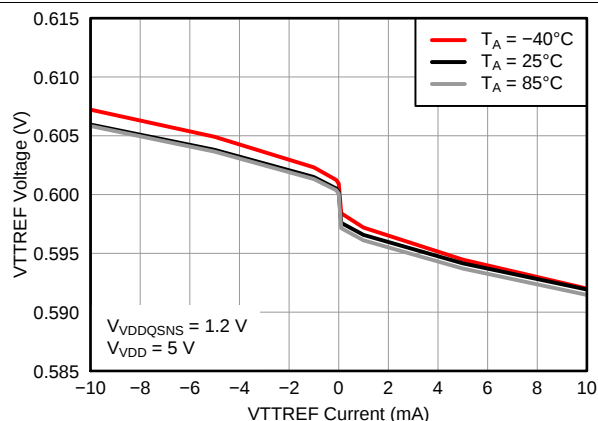


图 8. VTTREF Load Regulation (0.6 V)

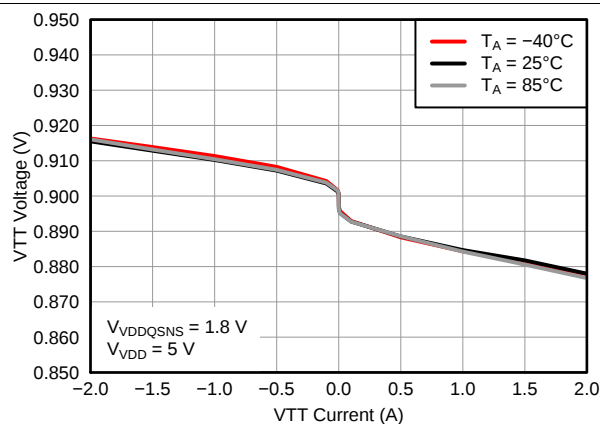


图 9. VTT Load Regulation (0.9 V)

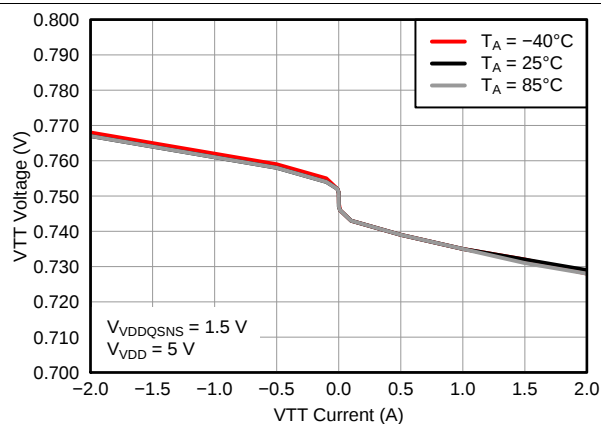


图 10. VTT Load Regulation (0.75 V)

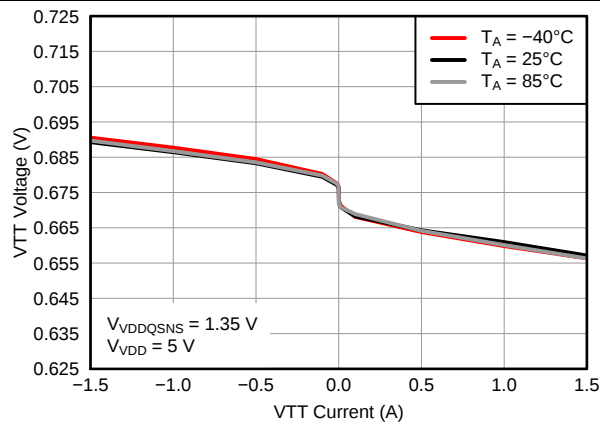


图 11. VTT Load Regulation (0.675 V)

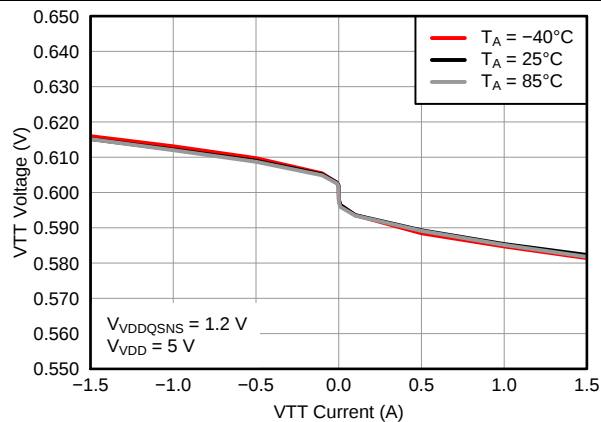


图 12. VTT Load Regulation (0.6 V)

## Typical Characteristics (接下页)

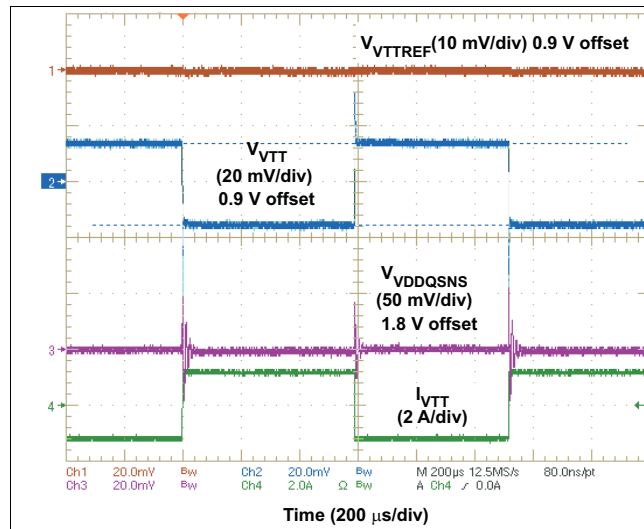


图 13. VTT Load Transient Response (0.9 V)

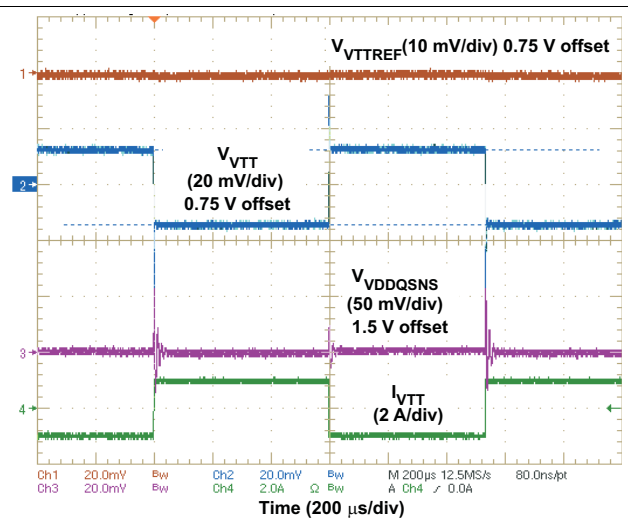


图 14. VTT Load Transient Response (0.75 V)

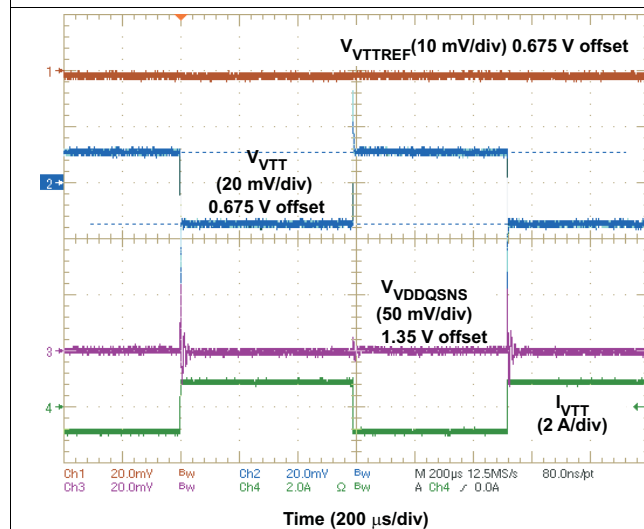


图 15. VTT Load Transient Response (0.675 V)

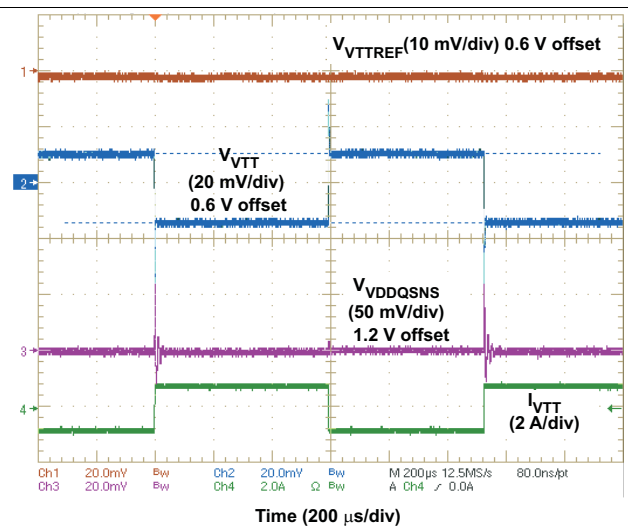


图 16. VTT Load Transient Response (0.6 V)

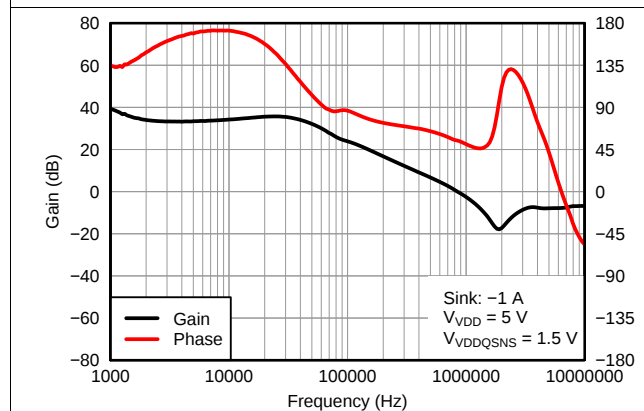


图 17. VTT (Sink: -1 A) Bode Plot (0.75 V)

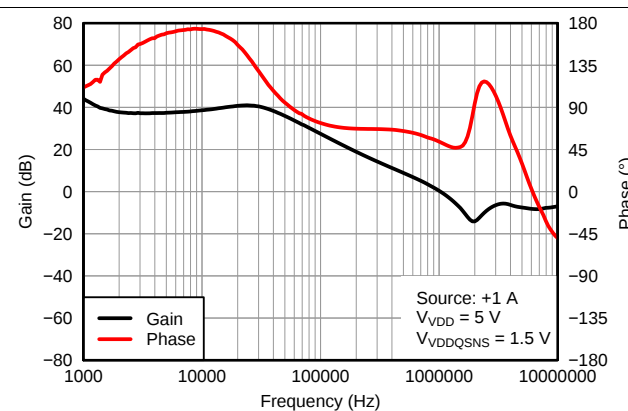


图 18. VTT (Source: +1 A) Bode Plot (0.75 V)

## Typical Characteristics (接下页)

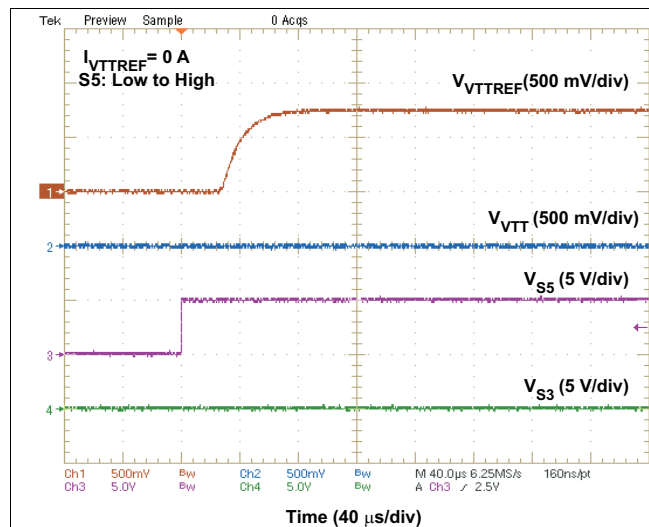


图 19. Start-Up Waveforms (S5: Low to High)

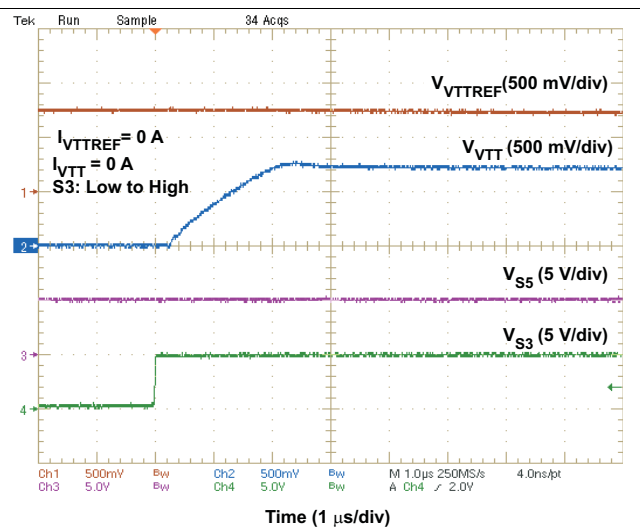


图 20. Start-Up Waveforms (S3: Low to High)

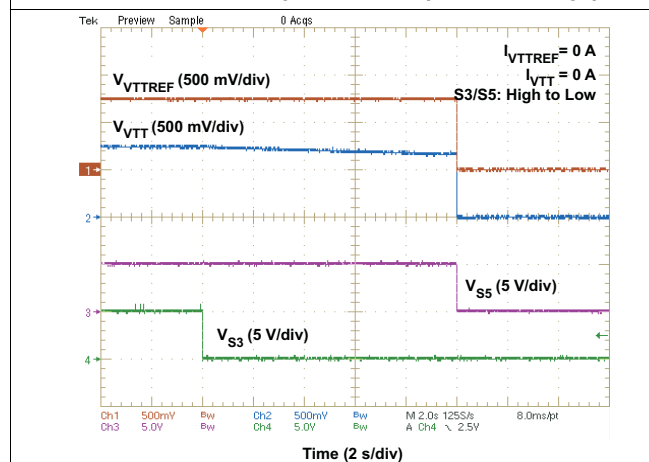


图 21. Shutdown Waveforms (S3/ S5: High to Low)

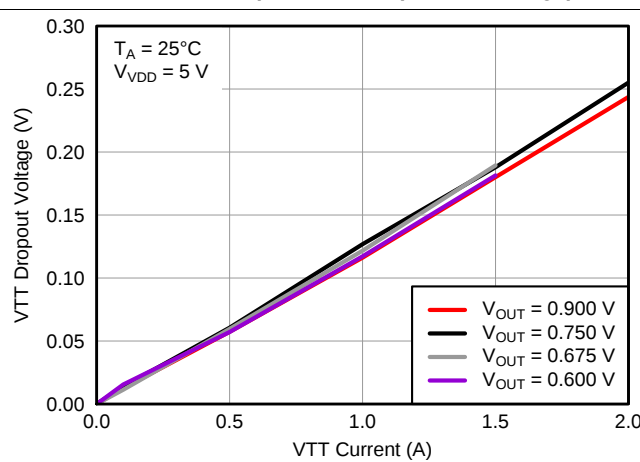


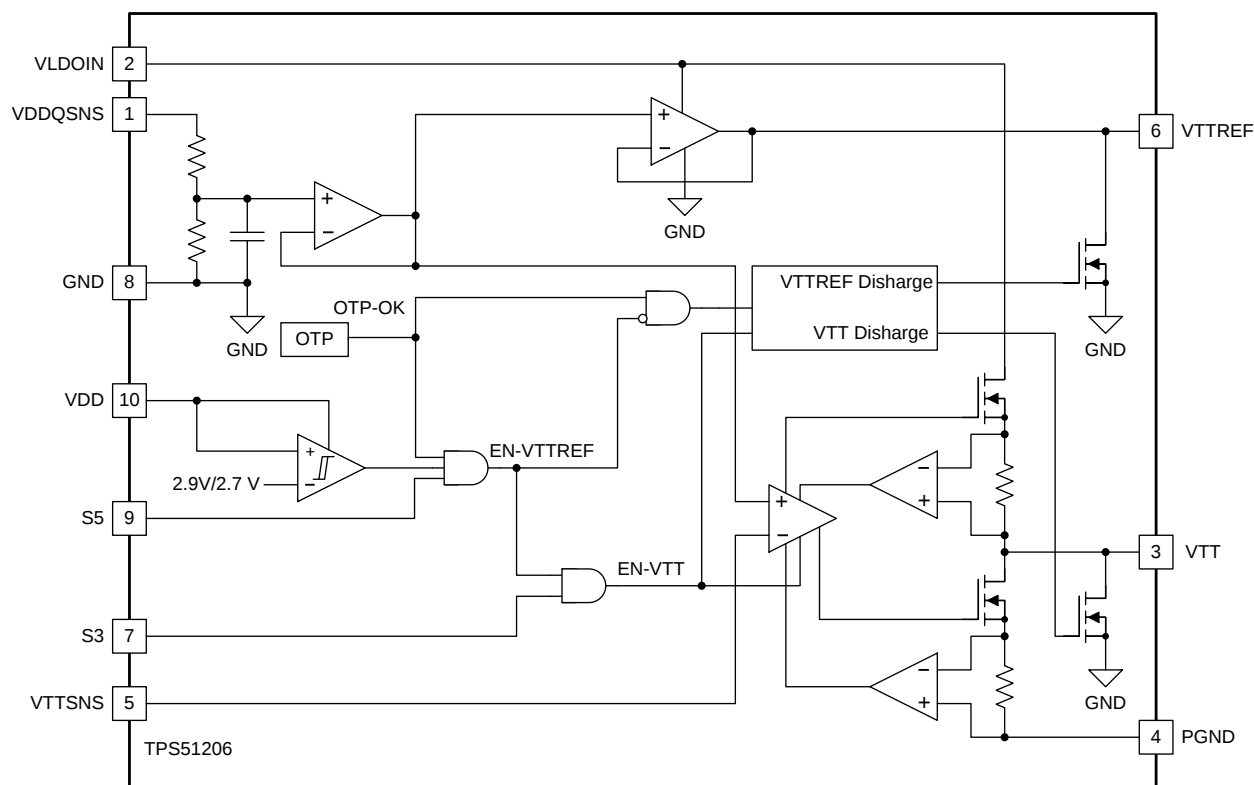
图 22. VTT Dropout Voltage

## 7 Detailed Description

### 7.1 Overview

The TPS51206 device is a sink or source double data rate (DDR) termination regulator with VTTREF buffered reference output.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 VTT Sink and Source Regulator

The TPS51206 device is a sink or source tracking termination regulator specifically designed for low input voltage, low cost, and low external component count systems where space is a key application parameter. The device integrates a high-performance, low-dropout (LDO) linear regulator (VTT) that has ultimate fast response to track  $\frac{1}{2}$  VDDQSNS within 40 mV at all conditions, and its current capability is 2 A for both sink and source directions. A 10- $\mu$ F (or greater) ceramic capacitor(s) need to be attached close to the VTT terminal for stable operation. A grade of X5R or better is recommended. To achieve tight regulation with minimum effect of trace resistance, the remote sensing terminal, VTTSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from the VTT pin.

The device has a dedicated pin, VLDOIN, for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 0.4 V above the  $\frac{1}{2}$  VDDQSNS voltage.

#### 7.3.2 VTTREF

The VTTREF pin includes 10 mA of sink or source current capability, and tracks  $\frac{1}{2}$  of VDDQSNS with  $\pm 1\%$  accuracy. The VTTREF pin can not be open. A 0.22- $\mu$ F ceramic capacitor needs to be attached close to the VTTREF terminal for stable operation; X5R or better grade is recommended.

## Feature Description (接下页)

### 7.3.3 VDD Undervoltage Lockout Protection

The TPS51206 device input voltage (VDD) includes undervoltage lockout protection (UVLO). When the VDD pin voltage is lower than UVLO threshold voltage, VTT and VTTREF are shut off. This is non-latch protection.

### 7.3.4 VTT Current Limit

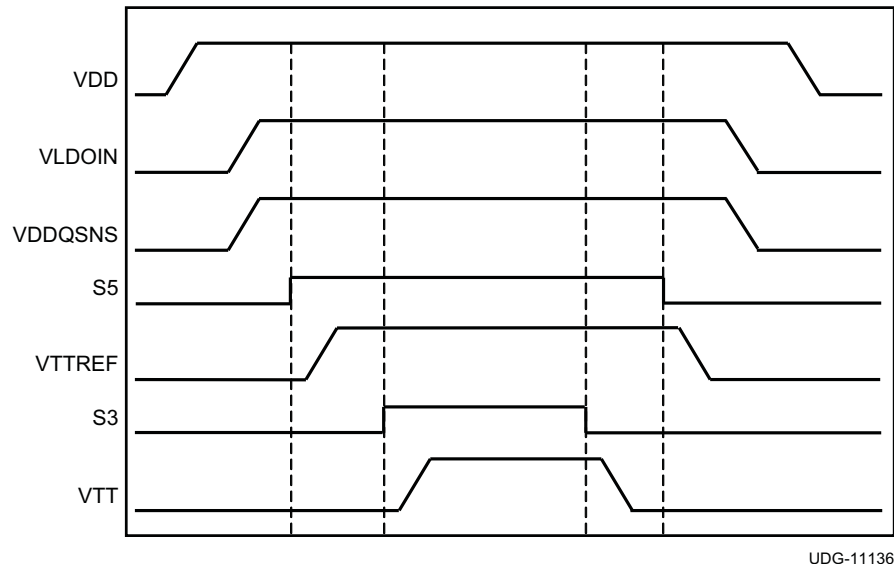
The TPS51206 device has VTT sink and source current limit capability. When the VTT current is higher than 2 A, the current is limited and VTT voltage is out of regulation. When the current is below 2 A, the VTT voltage is in regulation. This is non-latch protection.

### 7.3.5 Overtemperature Protection

This device features internal temperature monitoring. If the temperature exceeds the threshold value, VTT and VTTREF are shut off. This is a non-latch protection.

### 7.3.6 Power On and Off Sequence

图 23 is the recommended power on and off sequence. During power on, it is allowed to turn on VDD, S3 and S5 first, then turn on VLDOIN and VDDQSNS. During power off, it is allowed to turn off VDD, S3 and S5 first, then turn off VLDOIN and VDDQSNS.



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图 23. Typical Timing Diagram

## 7.4 Device Functional Modes

### 7.4.1 Power State Control

The TPS51206 device has two input pins, S3 and S5, to provide simple control of the power state. 表 1 describes S3 and S5 terminal logic state and corresponding state of VTTREF and VTT outputs. VTT is turn-off and placed to high impedance (High-Z) state in S3. The VTT output is floated and does not sink or source current in this state. When both S5 and S3 pins are LOW, the power state is set to S4 and S5 . In S4 and S5 state, all the outputs are turn-off and discharged to GND.

**表 1. S3 and S5 Control Table**

| STATE     | S3 | S5 | VTTREF         | VTT            |
|-----------|----|----|----------------|----------------|
| S0        | HI | HI | ON             | ON             |
| S3        | LO | HI | ON             | OFF(High-Z)    |
| S4 and S5 | LO | LO | OFF(Discharge) | OFF(Discharge) |

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

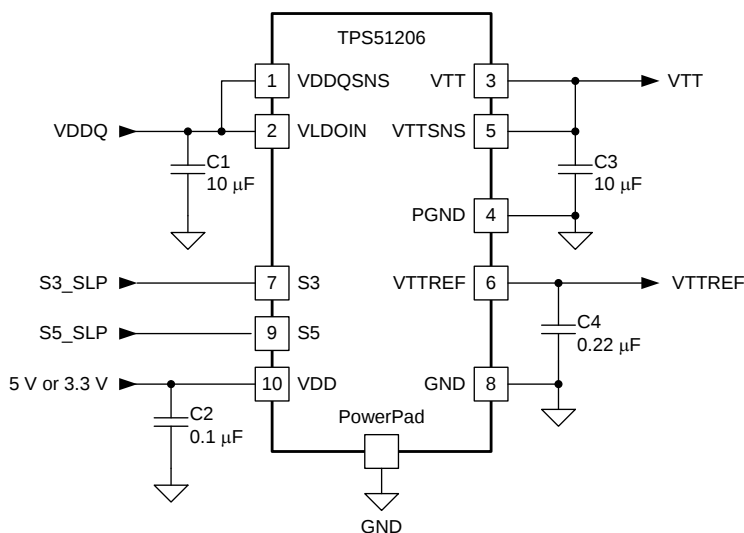
### 8.1 Application Information

The TPS51206 device is typically used as a sink and source tracking termination regulator which converts a voltage from VTT+0.4 V to 3.5 V

### 8.2 Typical Applications

#### 8.2.1 VLDOIN = VDDQ Configuration

图 24 shows an application diagram for a configuration where VLDOIN and VDDQ are connected.



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图 24. VLDOIN = VDDQ Configuration

#### 8.2.1.1 Design Requirements

表 2. Design Parameters

| PARAMETER            | EXAMPLE VALUE |
|----------------------|---------------|
| Supply Voltage (VDD) | 3.3 V or 5 V  |
| VLDOIN = VDDQ        | 1.5 V         |
| Output Current       | ±2 A          |

### 8.2.1.2 Detailed Design Procedure

**表 3. VLDOIN = VDDQ Configuration Components**

| REFERENCE DESIGNATOR | SPECIFICATION                         | MANUFACTURER | PART NUMBER   |
|----------------------|---------------------------------------|--------------|---------------|
| C1, C3               | 10 $\mu$ F, 6.3 V, X5R, 1608 (0603)   | Taiyo Yuden  | JMK107BJ106MA |
| C2                   | 0.1 $\mu$ F, 6.3 V, X5R, 1005 (0402)  | Taiyo Yuden  | JWK105BJ104MP |
| C4                   | 0.22 $\mu$ F, 6.3 V, X5R, 1005 (0402) | Taiyo Yuden  | JMK105BJ224KV |

#### 8.2.1.2.1 VDD Capacitor

Add a ceramic capacitor, with a value 0.1  $\mu$ F (or greater) and X5R grade (or better), placed close to the VDD terminal, to stabilize the bias supply voltage from any parasitic impedance from the power supply rail.

#### 8.2.1.2.2 VLDOIN Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10- $\mu$ F (or greater) and X5R grade (or better) ceramic capacitor to supply this transient charge.

#### 8.2.1.2.3 VTTREF Capacitor

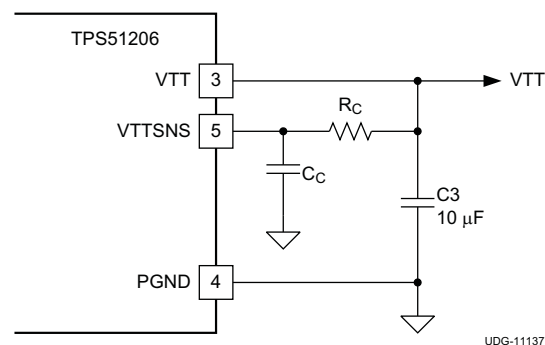
Add a ceramic capacitor, with a value 0.22  $\mu$ F and X5R grade (or better), placed close to the VTTREF terminal for stable operation.

#### 8.2.1.2.4 VTT Capacitor

For stable operation, a 10- $\mu$ F (or greater) and X5R (or better) grade ceramic capacitor(s) need to be attached close to the VTT terminal. This capacitor is recommended to minimize any additional equivalent series resistance (ESR) and/or equivalent series inductance (ESL) of ground trace between the PGND terminal and the VTT capacitor(s).

#### 8.2.1.2.5 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, the VTTSNS pin should be connected to the positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 m $\Omega$ . The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.



**图 25. R-C Filter for VTTSNS**

#### 8.2.1.2.6 VDDQSNS Connection

VDDQSNS is a reference input of the VTTREF and VTT. Trace should be routed away from noise-generating lines.

### 8.2.1.3 Application Curves

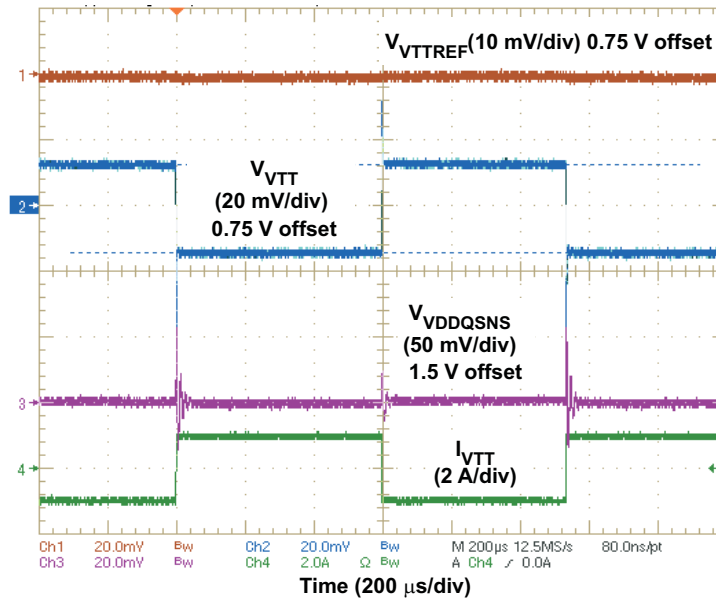
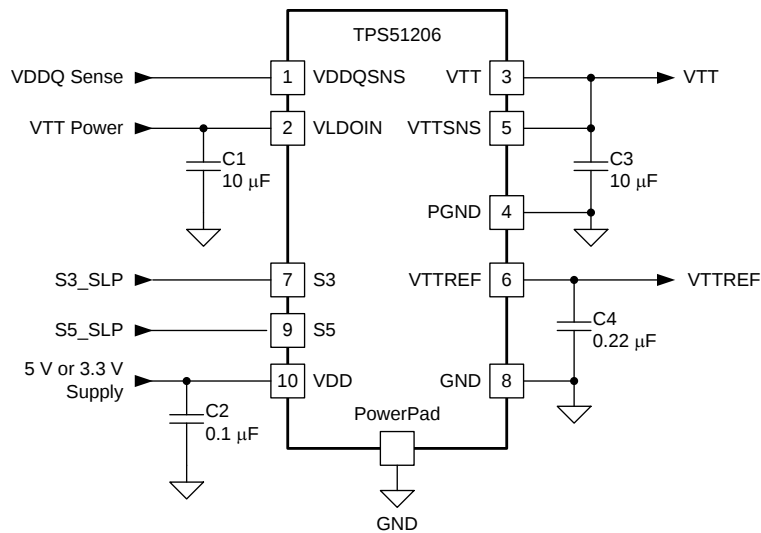


图 26. VTT Load Transient Response (0.75 V)

### 8.2.2 VLDOIN Separated from VDDQ Configuration

图 27 shows an application diagram for a configuration where VLDOIN and VDDQ are separated.



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图 27. VLDOIN Separated from VDDQ Configuration

### 8.2.2.1 Design Requirements

表 4. Design Parameters

| PARAMETER            | EXAMPLE VALUE |
|----------------------|---------------|
| Supply Voltage (VDD) | 3.3 V or 5 V  |
| VLDOIN = VDDQ        | 1.5 V         |
| Output Current       | ±2 A          |

### 8.2.2.2 Detailed Design Procedure

表 5. VLDOIN Separated from VDDQ Configuration Components

| REFERENCE DESIGNATOR | SPECIFICATION                        | MANUFACTURER | PART NUMBER   |
|----------------------|--------------------------------------|--------------|---------------|
| C1, C3               | 10 $\mu$ F, 6.3V, X5R, 1608 (0603)   | Taiyo Yuden  | JMK107BJ106MA |
| C2                   | 0.1 $\mu$ F, 6.3V, X5R, 1005 (0402)  | Taiyo Yuden  | JWK105BJ104MP |
| C3                   | 10 $\mu$ F, 6.3V, X5R, 1608 (0603)   | Taiyo Yuden  | JMK107BJ106MA |
| C4                   | 0.22 $\mu$ F, 6.3V, X5R, 1005 (0402) | Taiyo Yuden  | JMK105BJ224KV |

### 8.2.2.3 Application Curves

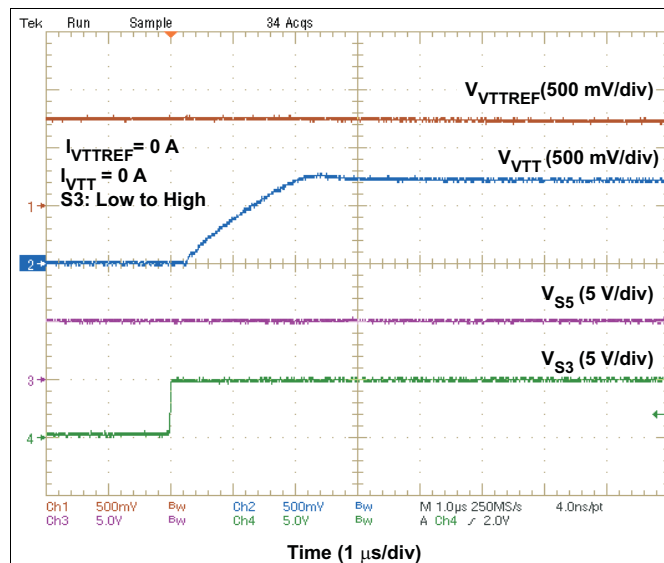


图 28. Start-Up Waveforms (S3: Low to High)

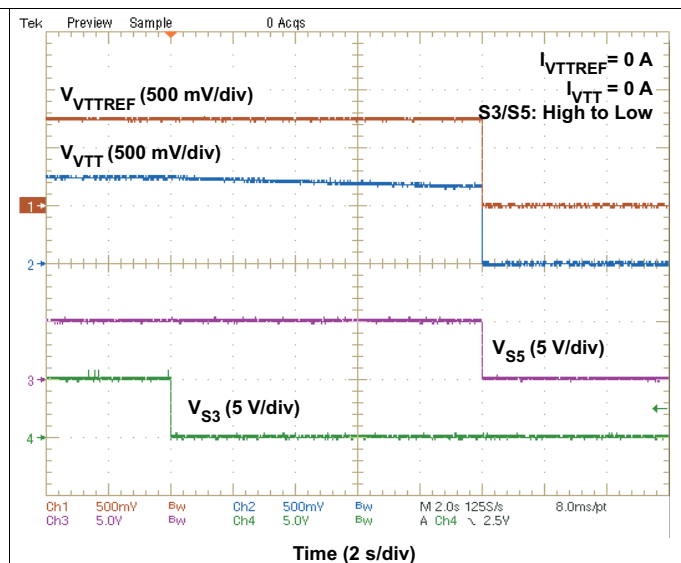


图 29. Shutdown Waveforms (S3 / S5: High to Low)

## 9 Power Supply Recommendations

TPS51206 device is designed for a sink / source double data rate (DDR) termination regulator with VTTREF buffered reference output. Supply input voltage (VDD) supports 3.3-V rail and 5-V rail; VLDOIN input voltage supports VTT+0.4 V to 3.5 V.

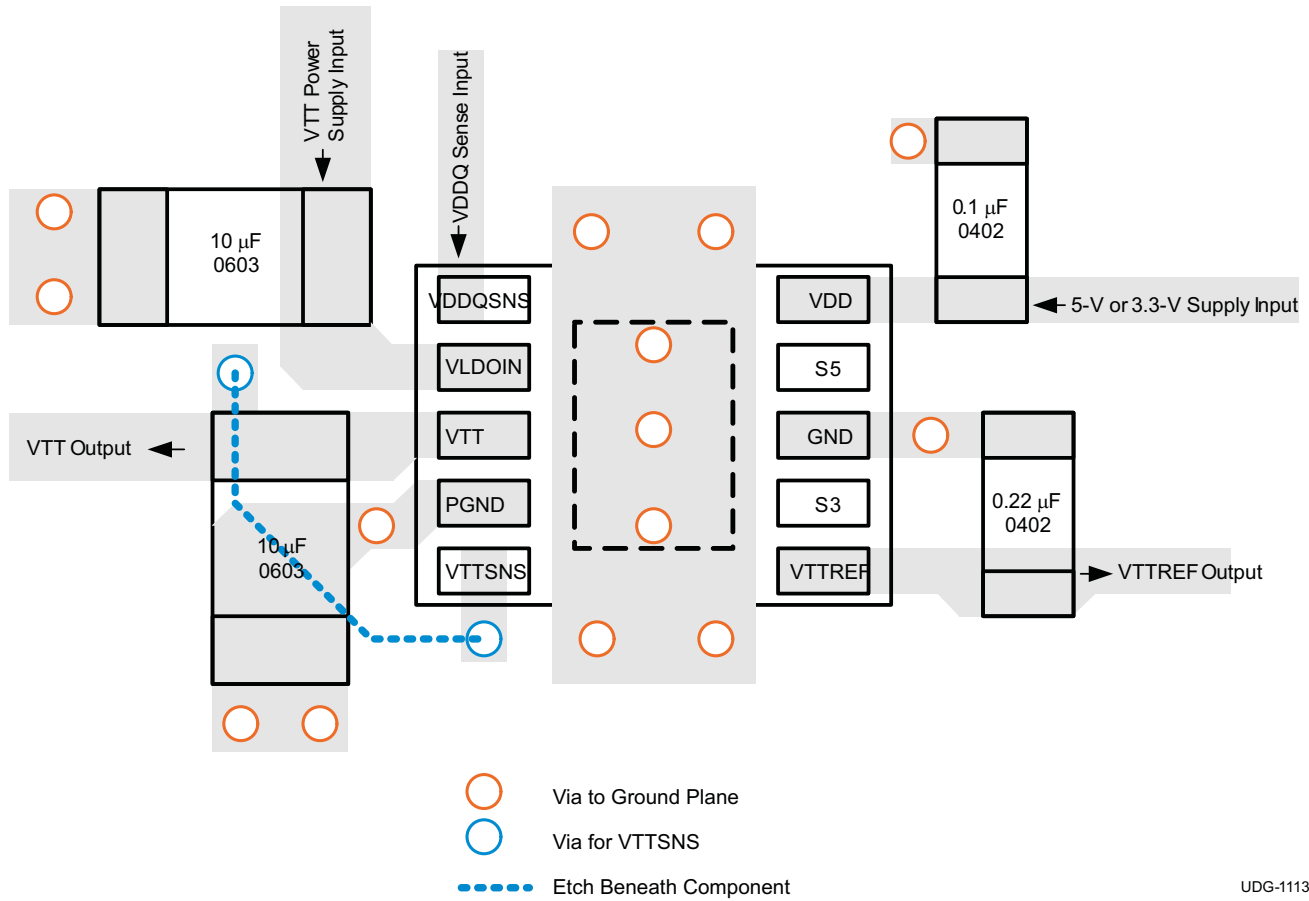
## 10 Layout

### 10.1 Layout Guidelines

Consider the following before beginning a TPS51206 device layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the terminal with short and wide connections.
- The output capacitor for VTT should be placed close to the terminals (VTT and PGND) with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current VTT power trace. In addition, VTTSNS trace should be routed away from high current trace, on the separate layer is recommended. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor(s) at that point. In addition, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the VTT capacitor(s).
- The GND pin (and the negative node of the VTTREF output capacitor) and PGND pins (and the negative node of the VTT output capacitor) should be connected to the internal system ground planes (for better result, use at least two internal ground planes) with multiple vias. Use as many vias as possible to reduce the impedance between GND pin or PGND pin and the system ground plane.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder side ground plane(s) should also be used to help dissipation. Consult the [TPS51206-EVM User's Guide](#) for more detailed layout recommendations.

## 10.2 Layout Example



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**图 30. PCB Layout Guideline**

## 10.3 Thermal Considerations

Because the TPS51206 device is a linear regulator, the VTT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between  $V_{VLDOIN}$  and  $V_{VTT}$  times  $I_{VTT}$  (VTT current) current becomes the power dissipation as shown in [公式 1](#).

$$P_{DISS(src)} = (V_{VLDOIN} - V_{VTT}) \times I_{VTT(src)} \quad (1)$$

In this case, if the VLDOIN pin is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation can be calculated by [公式 2](#).

$$P_{DISS(snk)} = V_{VTT} \times I_{VTT(snk)} \quad (2)$$

Maximum power dissipation allowed by the package is calculated by [公式 3](#).

$$P_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}}$$

where

- $T_{J(max)}$  is 125°C
- $T_{A(max)}$  is the maximum ambient temperature in the system
- $\theta_{JA}$  is the thermal resistance from junction to ambient

(3)

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 第三方产品免责声明

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下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 术语表

**SLYZ022** — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS51206DSQR     | ACTIVE        | WSO          | DSQ                | 10   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 105   | 1206                    | <a href="#">Samples</a> |
| TPS51206DSQT     | ACTIVE        | WSO          | DSQ                | 10   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 105   | 1206                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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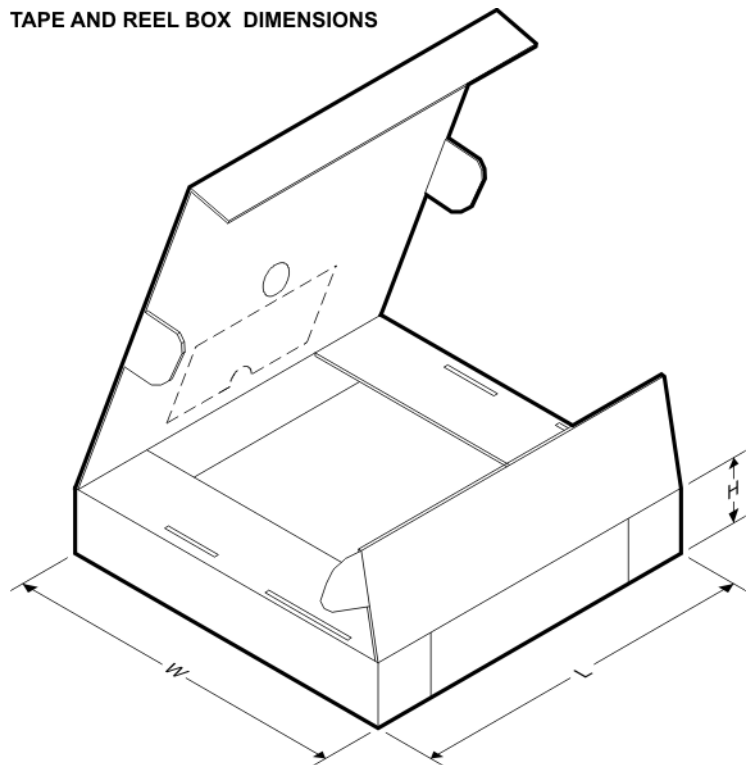


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

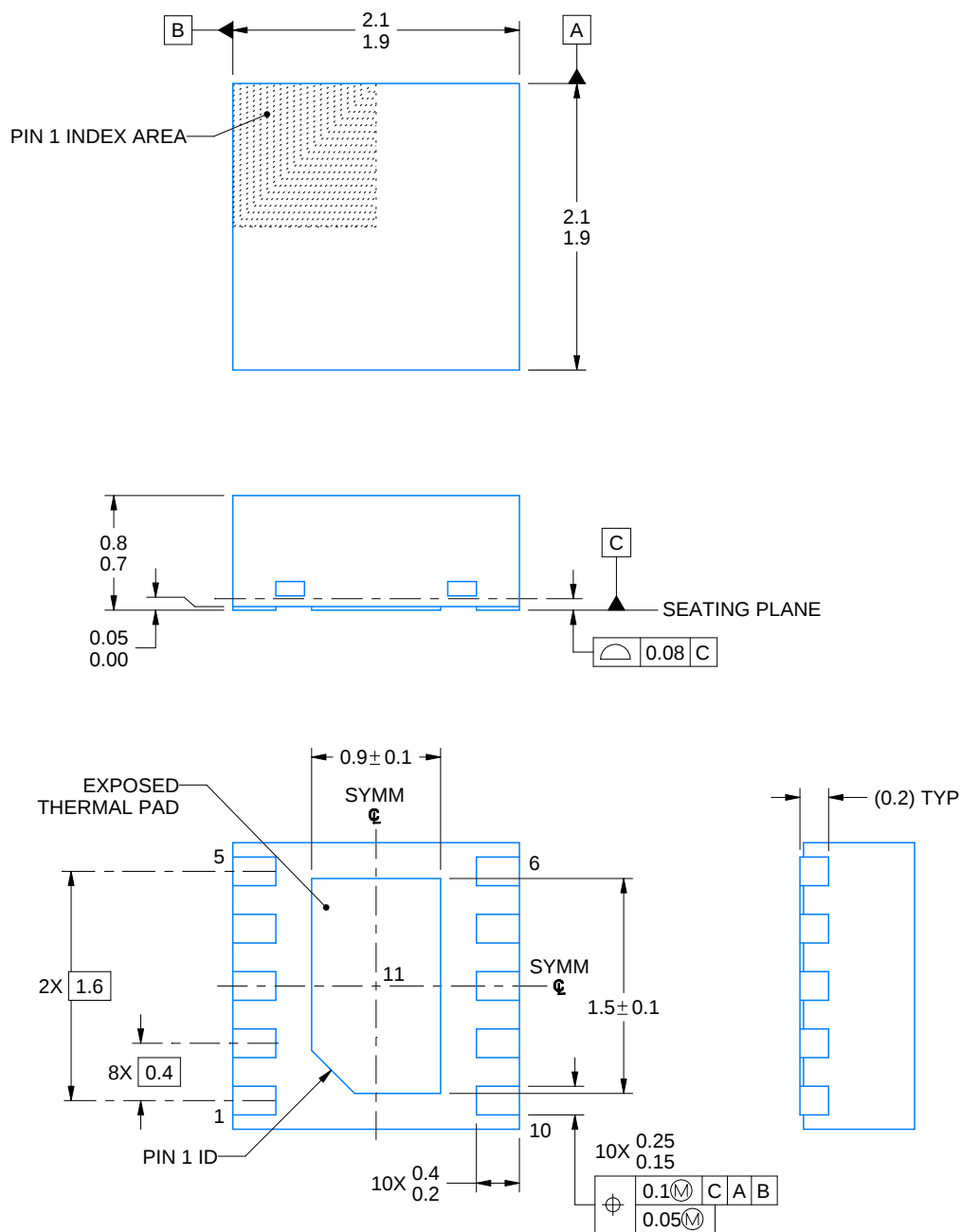
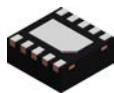
| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS51206DSQR | WSO          | DSQ             | 10   | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS51206DSQR | WSO          | DSQ             | 10   | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS51206DSQT | WSO          | DSQ             | 10   | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS51206DSQR | WSN          | DSQ             | 10   | 3000 | 210.0       | 185.0      | 35.0        |
| TPS51206DSQR | WSN          | DSQ             | 10   | 3000 | 210.0       | 185.0      | 35.0        |
| TPS51206DSQT | WSN          | DSQ             | 10   | 250  | 210.0       | 185.0      | 35.0        |



4218906/A 04/2019

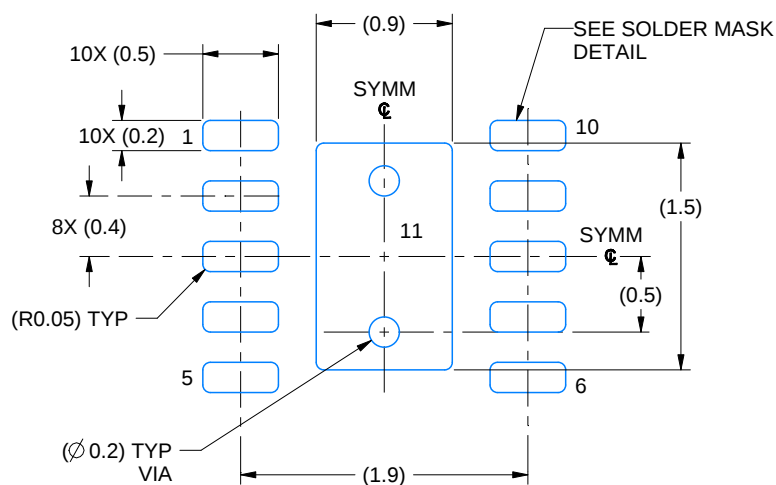
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**DSQ0010A**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



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NOTES: (continued)

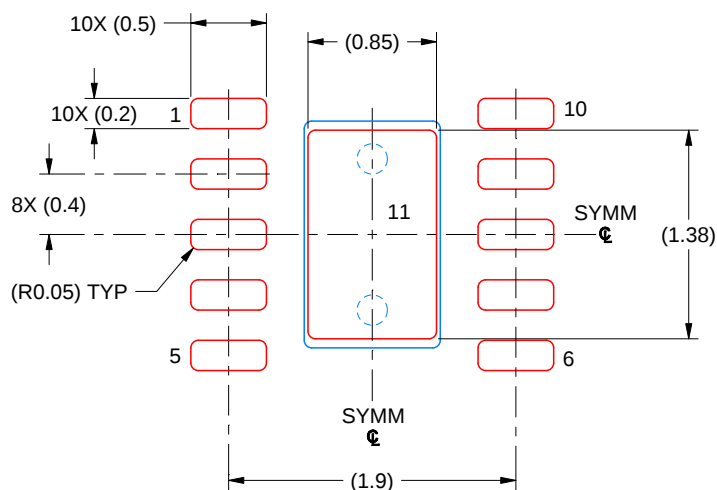
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

DSQ0010A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 11  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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