





100V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{DS} (V)	100
$R_{DS(ON)}(\Omega)$	10

Description and Applications

This MOSFET utilises a structure that combines low input capacitance with relatively low on-resistance and has an intrinsically higher pulse current handling capability in linear mode than a comparable trench technology structure. This MOSFET is suitable for general purpose applications.

- General purpose 100V FET
- Power management
- Disconnect switches
- Telecoms
- Complementary Type ZVP3310F

Features and Benefits

- · High pulse current handling in linear mode
- Low input capacitance
- Fast switching speed
- Lead Free By Design/RoHS Compliant (Note 1)

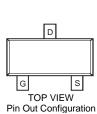
Mechanical Data

- Case: SOT-23
- Case Material: UL Flammability Classification Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

SOT-23



TOP VIEW



Gate Source
Equivalent Circuit

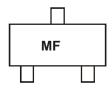
Ordering Information (Note 2)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel	
ZVN3310FTA	MF	7	8	3000	

Notes:

- 1. No purposefully added lead.
- 2. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



MF = Product Type Marking Code





Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units	
Drain-Source Voltage	V_{DSS}	100	V	
Gate-Source Voltage	V_{GSS}	±20	V	
Continuous Drain Current	I _D	100	mA	
Pulsed Drain Current	I _{DM}	2	А	

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation @T _A = 25°C	P_{D}	330	mW
Operating and Storage Temperature Range	$T_{J_1}T_{STG}$	-55 to +150	°C

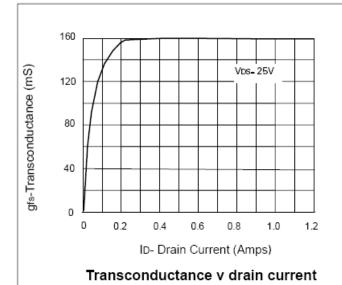
Electrical Characteristics @T_A = 25°C unless otherwise specified

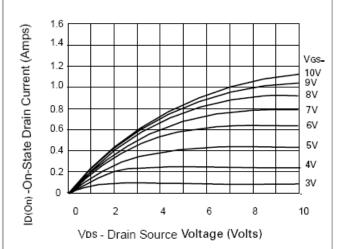
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition		
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage	BV _{DSS}	100	_		V	$I_D = 1 \text{mA}, V_{GS} = 0 \text{V}$		
Zero Gate Voltage Drain Current $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$ (Note 4)	I _{DSS}	_	_	1 50	μА	$V_{DS} = 100V, V_{GS} = 0V$ $V_{DS} = 80V, V_{GS} = 0V$		
Gate-Source Leakage	I_{GSS}	_	_	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$		
Gate Threshold Voltage	V _{GS(th)}	0.8	_	2.4	V	$V_{DS} = V_{GS}$, $I_D = 1mA$		
ON CHARACTERISTICS (Note 3)								
On-State Drain Current	I _{D (ON)}	500	_	_	mA	$V_{DS} = 25V, V_{GS} = 10V$		
Static Drain-Source On-Resistance	R _{DS} (ON)	_	_	10	Ω	$V_{GS} = 10V, I_D = 500mA$		
DYNAMIC CHARACTERISTICS (Note 4)								
Forward Transconductance (Note 3)	g_{fs}	100	_	_	mS	$V_{DS} = 25V, I_D = 500mA$		
Input Capacitance	C _{iss}	_	_	40		V 05V V 0V		
Output Capacitance	Coss	_	_	15	pF	$V_{DS} = 25V, V_{GS} = 0V$ f = 1.0MHz		
Reverse Transfer Capacitance	Crss	_	_	5		I = 1.0IVID2		
Turn-On Delay Time (Note 5)	t _{D(on)}	_	3	5				
Turn-On Rise Time (Note 5)	t _r	_	5	7		$V_{DD} \approx 25V$, $I_D = 500$ mA		
Turn-Off Delay Time (Note 5)	t _{D(off)}	_	4	6	ns			
Turn-Off Fall Time (Note 5)	t _f	_	5	7				

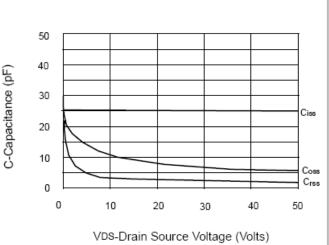
Notes:

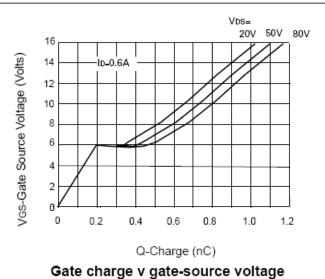
- 3. Measured under pulsed conditions. Width = $300\mu s$. Duty cycle $\leq 2\%$
- Sample test.
- 5. Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.





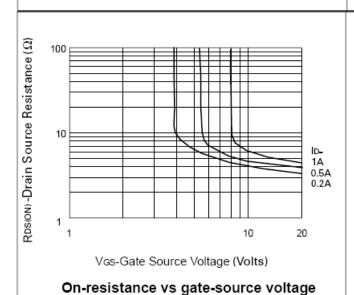


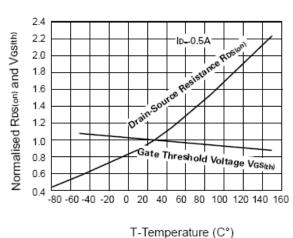




Saturation Characteristics

Capacitance v drain-source voltage

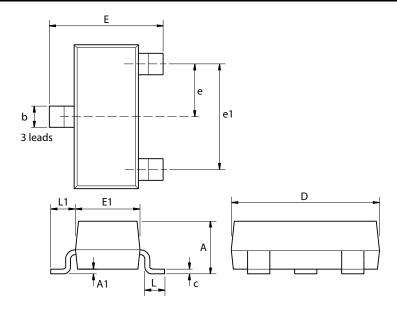




Normalised Rds(on) and Vgs(th) vs Temperature



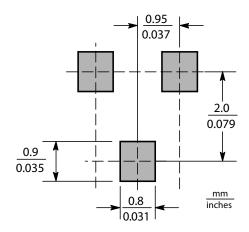
Package Outline Dimensions



Dim.	Millimeters		Inches		Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
Α	-	1.12	-	0.044	e1	1.90	NOM	0.075 NOM	
A1	0.01	0.10	0.0004	0.004	Е	2.10	2.64	0.083	0.104
b	0.30	0.50	0.012	0.020	E1	1.20	1.40	0.047	0.055
С	0.085	0.20	0.003	0.008	L	0.25	0.60	0.0098	0.0236
D	2.80	3.04	0.110	0.120	L1	0.45	0.62	0.018	0.024
е	0.95 NOM		0.037	NOM	-	-	-	-	-

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

Suggested Pad Layout







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