6 PORT GIGABIT ETHERNET TRANSCEIVER

FEATURES

- **Six 1.25 Gigabits Per Second (Gbps) Synchronizable Transceivers (Support for 100 Mbps 100Base-FX Mode)**
- **Configurable 1, 2, 3, 4, 5, or 6 Port Operation via MDIO**
- **Low Power Consumption <1.5W at 1.25Gb/sec**
- **IEEE 802.3z Gigabit Ethernet Compliant**
- **Differential VML Transmit Outputs With no External Components Necessary**
- **Programmable High Speed Output Pre-Emphasis Levels**
- **Nibble Wide RTBI/RGMII Compliant Interface**
- **Selectable Clock Tolerance Compensation**
- **Selectable on Chip Physical Coding Sublayer (PCS) Functions Including 8b/10b IEEE 802.3z Compliant Encoder and Decoder**
- **1/10th Rate Capability for 125 Mbps Operation With Automatic Rate Sense Capability**
- **JEDEC 1.5V HSTL (Extendable to 1.8 V) on Parallel Data Busses**
- **JEDEC 1.8/2.5/3.3 V LVCMOS on REFCLK and Control Pins**
- **Internal Series Termination on HSTL Outputs to Drive 50 Ω Lines**
- **Standard Parallel Interface Timing:**
  - **Source Centered/Aligned Timing on Inputs**
  - **Source Centered/Aligned Timing on Outputs**
- **Comprehensive Suite Of Built-In Testability**
- **IEEE 802.3 Clause 22 Management Data Interface (MDIO) Support**
- **IEEE 1149.1 JTAG Support**
- **Hot Plug Protection on Serial I/O**
- **No External Filter Components Required for PLLs**
- **Small Footprint 15 × 15 mm, 196-Pin, 1,0 mm Ball Pitch BGA**
- **Advanced Low Power 0.18 μm CMOS Technology**
- **Commercial Temperature Rating (0°C to 70°C)**
- **Repeater Mode:**
  - **In the Serial Domain Using Recovered Clock (Non-Retiming)**
  - **In the Parallel Domain Using REFCLK (Retiming)**
- **Jumbo Packet (9300 Byte) Support**
- **Clause 36A Test Pattern Gen/Ver**
- **SGMII Mode Support (10/100/1000 Mbps)**
- **Parallel Port Swap Mode**

FUNCTIONAL OVERVIEW

The TLK2226 is the third generation of Gigabit Ethernet transceivers from Texas Instruments combining high port density and ultra-low power in a small form factor footprint. The TLK2226 provides for high-speed full-duplex point-to-point data transmissions based on the IEEE802.3z 1000Mbps Ethernet specification. The TLK2226 supports data rates from 1.0 Gbps through 1.3 Gbps. Each channel is capable of operating at 125 Mbps for IEEE Ethernet 100FX mode, and the rate for each channel may be set through MDIO or automatically sensed and set by the TLK2226.The primary application of this device is to provide building blocks for developing point-to-point baseband data transmission over controlled impedance media of 50 Ω. The transmission media can be printed circuit board traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

This device performs the data encoding, decoding, serialization, deserialization, clock extraction and clock tolerance compensation functions for a physical layer interface device. Each channel operates at up to 1.3 Gbps providing up to 7.5 Gbps of aggregate data bandwidth over a copper or optical media interface.

The TLK2226 has six channels of SERDES each with 5 bit busses clocked double data rate (DDR). The parallel interface accepts un-encoded or 5-bit wide encoded data aligned to both the rising and falling edge of the transmit clock. The data is clocked low-order bits first, (i.e. bits 0–4 of the 8b/10b encoded data) on the rising edge of the transmit clock and the high-order bits (i.e. bits 5–9 of the 8b/10b encoded data) are clocked on the falling edge of the clock. The receive path interface is clocked in the same manner.

The TLK2226 supports two modes that can repeat data from a channel's serial receiver to the adjacent channel's serial transmitter: serial repeater mode and retiming repeater mode. In serial repeater mode, the clock/data recovery (CDR) function will lock onto the incoming data stream and will pass this data stream over to the adjacent channel to be retransmitted. In serial repeater mode, the data stream stays in the same clock domain as the incoming data; there is no clock tolerance compensation function performed to align the data stream to the reference clock domain. In retiming repeater mode, the CDR function will lock onto the incoming data stream but the data will be deserialized and passed through the CTC FIFO and then serialized for transmission on the adjacent channel. In both repeater modes, the received data for Channel A is retransmitted on the output for channel B while the received data for Channel B is retransmitted on the output for Channel A. Likewise, Channel C is paired with Channel D, and Channel E is paired with Channel F. The repeater modes can be enabled on a channel by channel basis through the use of register control bits programmed through the MDIO interface.

The recovered data clock frequency can be aligned to the reference clock on each channel by means of a clock tolerance compensation circuit and internal FIFO that will insert or drop Idle 20-bit IDLE codes as needed in the absence of data. The received data for all channels are aligned to a single receive data clock that is a buffered version of the reference clock.

The TLK2226 supports a selectable IEEE802.3z compliant 8b/10b encoder/decoder in all its 1.25Gbps modes of operation, and a IEEE802 compliant 4b/5b encoder/decoder in its 125Mbps mode of operation.

The TLK2226 supports selectable RTBI and RGMII interface to supervision ASIC.

The TLK2226 automatically locks onto incoming data without the need to pre-lock.

Detection of whether the incoming data stream is at 1.25 Gbps or 125 Mbps data rate is automatic.

A comprehensive series of built-in tests for self-test purposes including loopback and PRBS generation and verification is provided. An IEEE 1149.1 JTAG port is also supported to aid in board manufacturing test.

This device is housed in a small form factor 15 $\times$ 15 mm, 196-pin, BGA with 1,0 mm ball pitch and is characterized to support the commercial temperature range of 0°C to 70°C.

Expect the TLK2226 to consume less than 1.5 W, when operating at 1.25 Gbps.

The TLK2226 is designed to be hot plug capable. A power-on reset puts the parallel side output signal pins in a high-impedance state during power-up as well as pulls both TX+ and TX– to VDDA through 500 Ω.

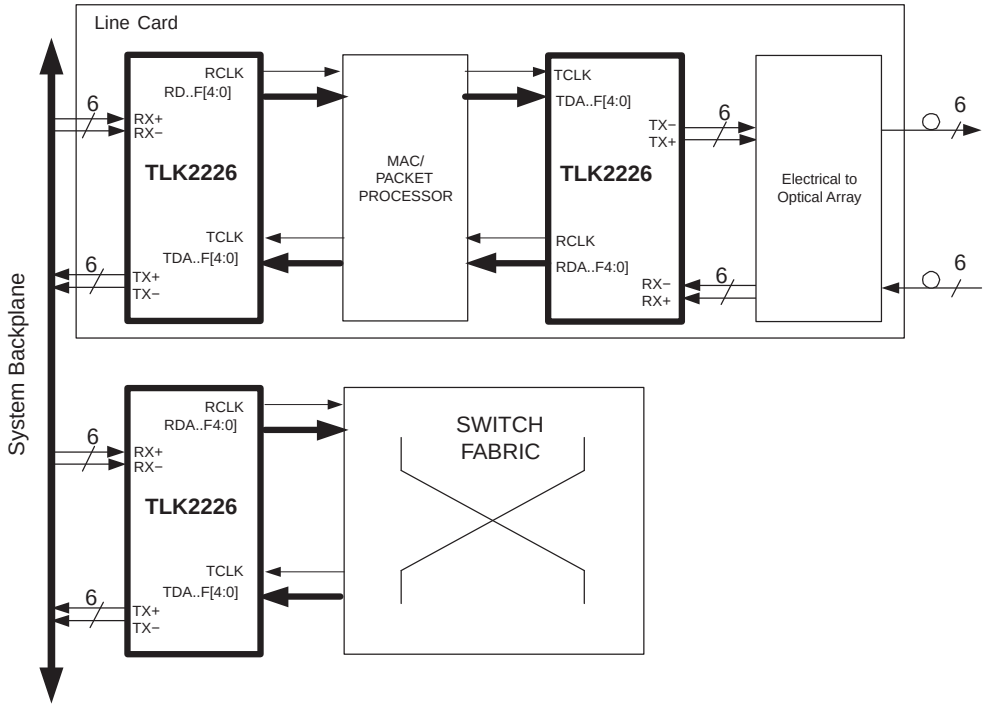


Figure 1. TLK2226 System Implementation Diagram

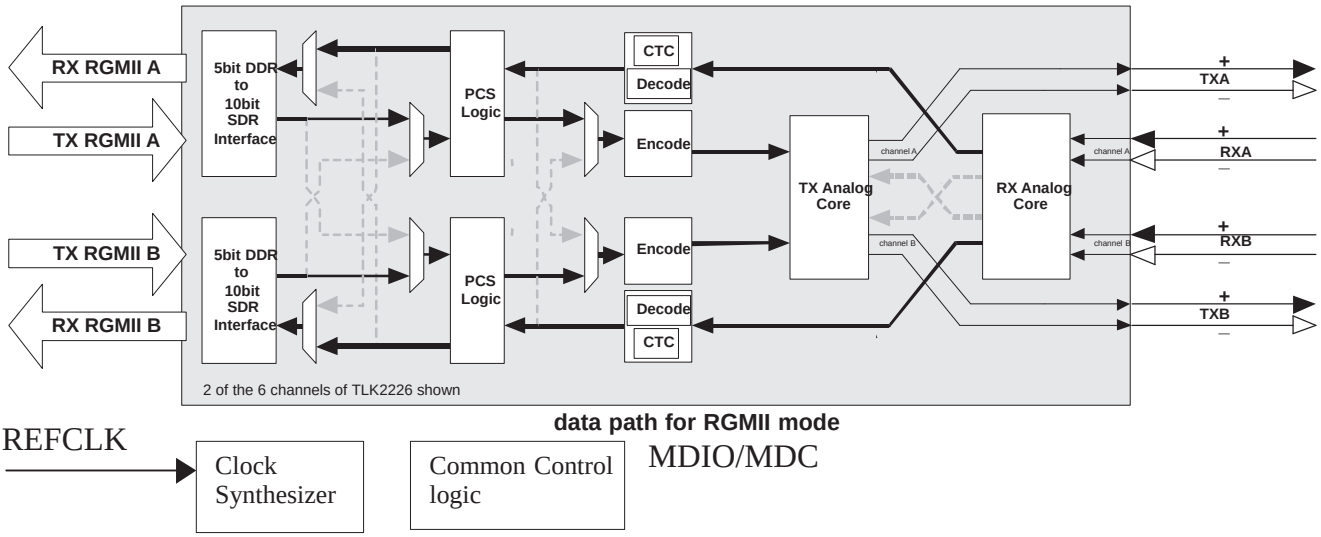


Figure 2. TLK2226 Block Diagram

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_{DDQ}	I/O Supply voltage(2)		–0.3 to 2.5	V
V_{DDS}	I/O Supply voltage(2)		–0.3 to 3.6	V
V_{DD} , V_{DDA}	Core Supply voltage(2)		–0.3 to 2.5	V
V_I	Input voltage	LVCMOS	–0.5 to 3.6	V
		HSTL	–0.5 to 2.5	
	DC Input voltage (I/O)		–0.3 to 2.5	V
	Storage temperature		–65 to 85	°C
	Electrostatic discharge		HBM: 2KV, CDM:750	V
	Characterized free-air operating temperature range		0 to 70	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	Peak-peak AC noise in the 1–10 MHz range may not exceed 100 mV	1.7	1.8	1.9	V
V_{DDQ}	HSTL I/O supply voltage	1.5 V HSTL Class 1 peak-peak AC noise may not exceed 150 mV	1.4	1.5	1.6	V
		1.8 V HSTL Class 1 peak-peak AC noise may not exceed 150 mV	1.7	1.8	1.9	V
V_{DDS}	LVCMOS I/O supply voltage	1.8 V CMOS peak-peak AC noise may not exceed 150 mV	1.7	1.8	1.9	V
		2.5 V CMOS peak-peak AC noise may not exceed 150 mV	2.375	2.5	2.625	V
		3.3 V CMOS peak-peak AC noise may not exceed 150 mV	3.14	3.3	3.47	V
V_{DDA}	Analog supply voltage	Peak-peak AC noise in the 1–10 MHz range may not exceed 100 mV	1.7	1.8	1.9	V
V_{REF}	Input reference voltage(1)	1.5 V HSTL Class 1	0.7	0.75	0.8	V
		1.8 V HSTL Class 1	0.85	0.9	0.95	
I_{DD}	Core supply current	R_ω = 125 MHz, V_{DD} = 1.8 V			390	mA
$I_{\_HSTL}$	HSTL I/O supply current	R_ω = 125 MHz, V_{DDQ} = 1.5 V			146	mA
		R_ω = 125 MHz, V_{DDQ} = 1.8 V			204	
I_{DDS}	LVCMOS I/O supply current	R_ω = 125 MHz, V_{DDS} = 1.8 V			1	mA
		R_ω = 125 MHz, V_{DDS} = 2.5 V			3	
		R_ω = 125 MHz, V_{DDS} = 3.3 V			7	
I_{DDA}	Analog supply current	R_ω = 125 MHz, V_{DDA} = 1.8 V			183	mA
P_D	Total power consumption	R_ω = 125 MHz, V_{DDQ} = 1.8 V			1.50	W
I_{DDQ}	Shutdown current	ENABLE = low		30		mA

(1) Typically, the value of VREF is expected to be 0.5 V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.

LVCMOS ELECTRICAL CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –400 µA, V_{DDS} = MIN	V_{DDS}– 0.2		V_{DDS}	V

(1) Unused inputs that do not hold an integrated pull up or pull down circuit need to be terminated to either GND or VDDQ respectively to avoid extensive currents and life time degradation.

LVCMOS ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, V_{DDS} = MIN	0	0.25	0.5	V
V_{IH}	High-level input voltage	V_{DDS} = 1.8 V	1.4		V_{DDS} +0.2	V
		V_{DDS} = 2.5 V	1.55		V_{DDS} +0.2	
		V_{DDS} = 3.3 V	2.0		V_{DDS} +0.2	
V_{IL}	Low-level input voltage	V_{DDS} = 1.8 V	–0.2		0.63	V
		V_{DDS} = 2.5 V	–0.2		0.7	
		V_{DDS} = 3.3 V	–0.2		1.4	
I_H	High input current	V_{DDS} = MAX, V_{IN} = 2.0 V			400	µA
I_L	Low input current	V_{DDS} = MAX, V_{IN} = 2.0 V			–600	µA
C_{IN}	Input capacitance				4	pF

HSTL ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage	DC output, logic high	V_{DDQ}–0.4		V_{DDQ}	V
$V_{OL(dc)}$	Low-level output voltage	DC output, logic low			0.4	V
$V_{IH(dc)}$	High-level input voltage	DC input, logic high	V_{REF}+0.10		V_{DDQ}+0.3	V
$V_{IL(dc)}$	Low-level input voltage	DC input, logic low	–0.5		V_{REF}–0.10	V
$V_{IH(ac)}$	High-level input voltage	AC input, logic high, V_{DDQ} = 1.5 V	V_{REF}+0.20			V
		AC input, logic high, V_{DDQ} = 1.8 V	V_{REF}+0.35			
$V_{IL(ac)}$	Low-level input voltage	AC input, logic low, V_{DDQ} = 1.5 V			V_{REF}–0.20	V
		AC input, logic low, V_{DDQ} = 1.8 V			V_{REF}–0.35	
I_{IH}	High input current	Receiver only			±10	µA
I_{IL}	Low input current					
$I_{OH(dc)}$	High output current	V_{DDQ} = 1.5 V	–8			mA
$I_{OL(dc)}$	Low output current	V_{DDQ} = 1.5 V	8			mA
C_{IN}	Input capacitance				4	pF

REFERENCE CLOCK TIMING REQUIREMENTS (REFCLK)(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
R_ω	Frequency	Minimum data rate	TYP–0.01%	125	TYP+0.01%	MHz
		Maximum data rate	TYP–0.01%	125	TYP+0.01%	MHz
	Accuracy		–100		100	ppm
	Duty cycle		40%	50%	60%	
	Jitter	Random and deterministic			40	ps_{pp}

(1) This clock should be crystal referenced to meet the requirements of this table (Contact TI for specific clocking recommendations). Rate activity of REFCLK is internally monitored. As soon as REFCLK is disconnected the device will initiate a global power-down mode; PLLs will be turned off, output divers disabled and other current sources such as pull-up's and pull down's will be disabled to avoid power consumption. To re-activate the device, restart REFCLK.

SERIAL TRANSMITTER/RECEIVER CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p)}$	TX output voltage magnitude TX Amp. Control 16.14 = 1	Pre-Emphasis 16.1:0 = 11. See Figure 3. Differential and common-mode output voltage definitions.	650	950	1250	mV
		Pre-Emphasis 16.1:0 = 10. See Figure 3. Differential and common-mode output voltage definitions.	625	900	1125	mV
		Pre-Emphasis 16.1:0 = 01. See Figure 3. Differential and common-mode output voltage definitions.	575	850	1075	mV
$V_{OD(d)}$		Pre-Emphasis 16.1:0 = 00. See Figure 3. Differential and common-mode output voltage definitions.	550	800	1000	mV
$V_{OD(p)}$	TX output voltage magnitude TX Amp. Control 16.14 = 0	Pre-Emphasis 16.1:0 = 11. See Figure 3. Differential and common-mode output voltage definitions.	Not Supported	Not Supported	Not Supported	mV
		Pre-Emphasis 16.1:0 = 10. See Figure 3. Differential and common-mode output voltage definitions.	Not Supported	Not Supported	Not Supported	mV
		Pre-Emphasis 16.1:0 = 01. See Figure 3. Differential and common-mode output voltage definitions.	375	500	675	mV
$V_{OD(d)}$		Pre-Emphasis 16.1:0 = 00. See Figure 3. Differential and common-mode output voltage definitions.	275	400	500	mV
$V_{OD(pp)}$	TX output differential peak-to-peak voltage swing TX Amp. Control 16.14 = 1	Pre-Emphasis 16.1:0 = 11. See Figure 3. Differential and common-mode output voltage definitions.	1300	1900	2500	mVp-p
		Pre-Emphasis 16.1:0 = 10. See Figure 3. Differential and common-mode output voltage definitions.	1250	1800	2250	mVp-p
		Pre-Emphasis 16.1:0 = 01. See Figure 3. Differential and common-mode output voltage definitions.	1150	1700	2150	mVp-p
$V_{OD(pd)}$		Pre-Emphasis 16.1:0 = 00. See Figure 3. Differential and common-mode output voltage definitions.	1100	1600	2000	mVp-p
$V_{OD(pp)}$	TX output differential peak-to-peak voltage swing TX Amp. Control 16.14 = 0	Pre-Emphasis 16.1:0 = 11. See Figure 3. Differential and common-mode output voltage definitions.	Not Supported	Not Supported	Not Supported	mVp-p
		Pre-Emphasis 16.1:0 = 10. See Figure 3. Differential and common-mode output voltage definitions.	Not Supported	Not Supported	Not Supported	mVp-p
		Pre-Emphasis 16.1:0 = 01. See Figure 3. Differential and common-mode output voltage definitions.	750	1000	1350	mVp-p
$V_{OD(pd)}$		Pre-Emphasis 16.1:0 = 00. See Figure 3. Differential and common-mode output voltage definitions.	550	800	1000	mVp-p
V_{CMT}	TX output common mode voltage range	See Figure 3. Differential and common-mode output voltage definitions.	750		1200	mV
V_{ID}	RX input voltage magnitude away from common mode	See Figure 5	200		900	mV
$V_{ID(p)}$	RX input differential peak-to-peak voltage swing	See Figure 5	400		2500	mVp-p
I_{LKG}	RX input leakage current		–10		10	µA
C_I	RX input capacitance				2	pF

SERIAL TRANSMITTER/RECEIVER CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 3		150	220	ps
		R_L = 50 Ω, C_L = 5 pF, See Figure 3 For Half amplitude condition without Pre-Emphasis		165	260	ps
J_{TOL}	Jitter Tolerance, Total Jitter at Serial Input	Zero crossing, See Figure 6			0.75	UI(1)
J_{DR}	Serial Input Deterministic Jitter	Zero crossing, See Figure 6			0.462	UI
J_T	Serial Output Total Jitter Alternating disparity	K28.5 1.25 Gbps		0.15	0.24	UI
J_D	Serial Output Deterministic Jitter	Alternating disparity K28.5 1,25 Gbps			0.10	UI
$R_{(LATENCY)}$	From MDI /T/ to RGMII RX_DV de-assert	1000Base-X Operating Mode			192	Bits
$T_{(LATENCY)}$	From the assertion of TX_EN to MDI output of /S/				136	Bits
$R_{(LATENCY)}$	MDI Input to RX_DV de-assert	100Base-FX Operating Mode			32	Bits
$T_{(LATENCY)}$	TX_EN sampled to MDI output				14	Bits

(1) Unit Interval = one serial bit time (min 800 ps)

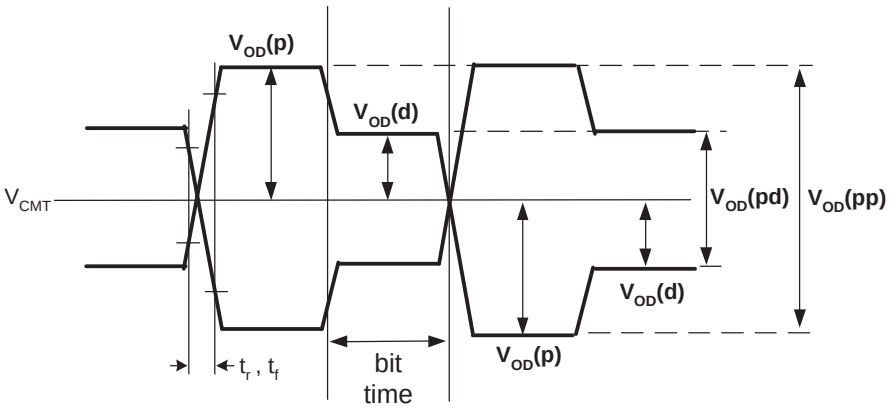


Figure 3. Differential and Common-Mode Output Voltage Definitions

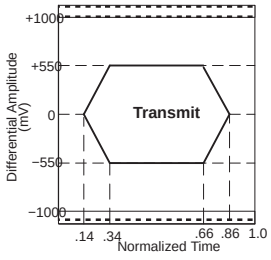


Figure 4. Transmit Template

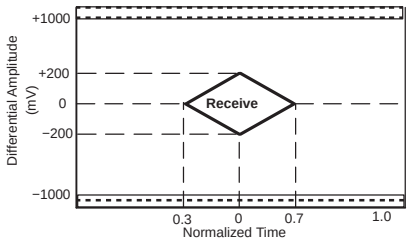
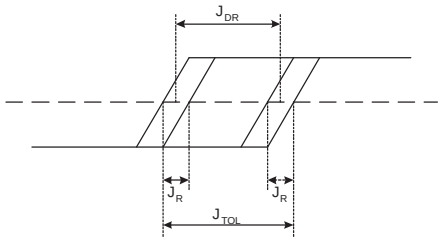


Figure 5. Receive Template



NOTE: $J_{TOL} = J_R + J_{DR}$, where J_{TOL} is the receive jitter tolerance, J_{DR} is the received deterministic jitter, and J_R is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12}.

Figure 6. Input Jitter

HSTL OUTPUT SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
T_r	Clock and data rise time	80% to 20% output voltage, see Figure 7, C = 10 pF			1.5	ns
T_f	Clock and data fall time	80% to 20% output voltage, see Figure 7, C = 10 pF			1.8	ns
T_{OSU}	RD[4:0] valid (setup) prior to RCLK transition high or low	See Figure 7, timing relative to 0.5×VDDQ, 25 MHz and 125 MHz	1.2			ns
T_{OHD}	RD[4:0] valid (hold) after RCLK transition high or low	See Figure 7, timing relative to 0.5×VDDQ, 25 MHz and 125 MHz	1.2			ns
T_{suav}	RCLK transition high or low to data valid window beginning (RD[4:0]).	See Figure 8, timing relative to 0.5×VDDQ, 25 MHz and 125 MHz			800	ps
T_{hdav}	RCLK transition high or low to data valid window ending (RD[4:0]).	See Figure 8 , timing relative to 0.5×VDDQ, 25 MHz and 125 MHz	3.2			ns

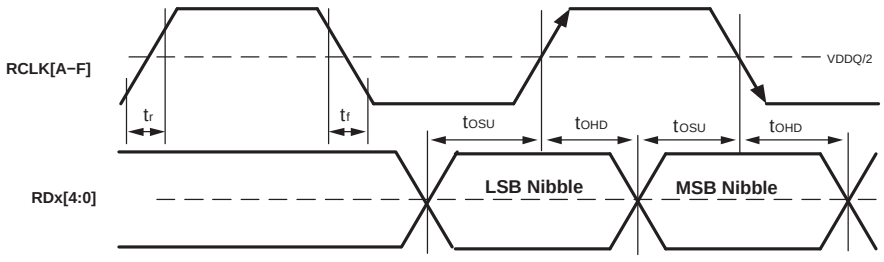


Figure 7. HSTL Receive Output Timing Requirements (Centered)

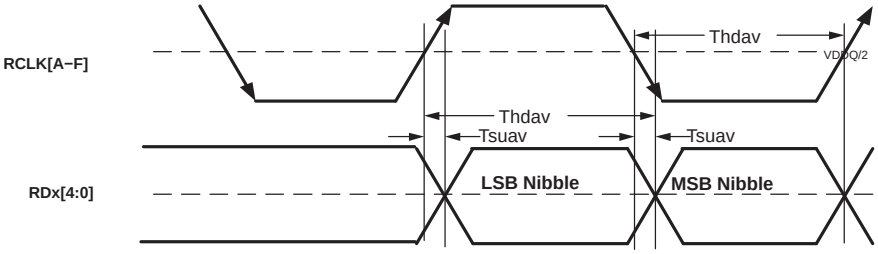


Figure 8. HSTL Receive Output Timing Requirements (Aligned)

HSTL INPUT TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP(1)	MAX	UNIT
T_{ISU}	TDx[4:0] setup prior to TCLK transition high or low	Figure 19 timing relative to 0.5×VDDQ, 25 MHz and 125 MHz	0.6			ns
T_{IHD}	TDx[4:0] hold after TCLK transition high or low	Figure 19, timing relative to 0.5×VDDQ, 25 MHz and 125 MHz	0.6			ns
T_{suav}	RCLK transition high or low to data valid window beginning (RD[4:0]).	Figure 18, timing relative to 0.5×VDDQ, 25 MHz and 125 MHz			1.4	ns
T_{hdav}	RCLK transition high or low to data valid window ending (RD[4:0]).	Figure 18, timing relative to 0.5×VDDQ, 25 MHz and 125 MHz	2.6			ns

(1) All typical values are at 25°C and with a nominal supply.

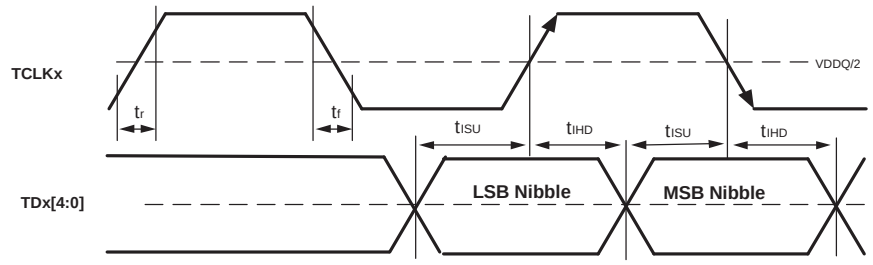


Figure 9. HSTL Data Input Timing Requirements (Centered)

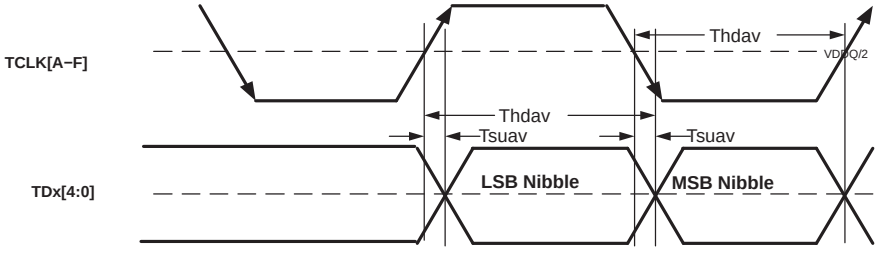


Figure 10. HSTL Data Input Timing Requirements (Aligned)

MDIO TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{period}	MDC period	See Figure 11	400			ns
t_{setup}	MDIO setup to ↑ MDC	See Figure 11	10			ns
t_{hold}	MDIO hold to ↑ MDC	See Figure 11	10			ns
T_{data}	MDC ↑ to MDIO valid		0		300	ns

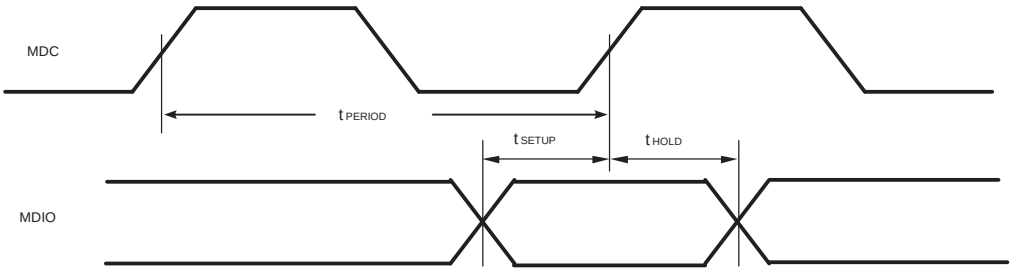


Figure 11. MDIO Read/Write Timing

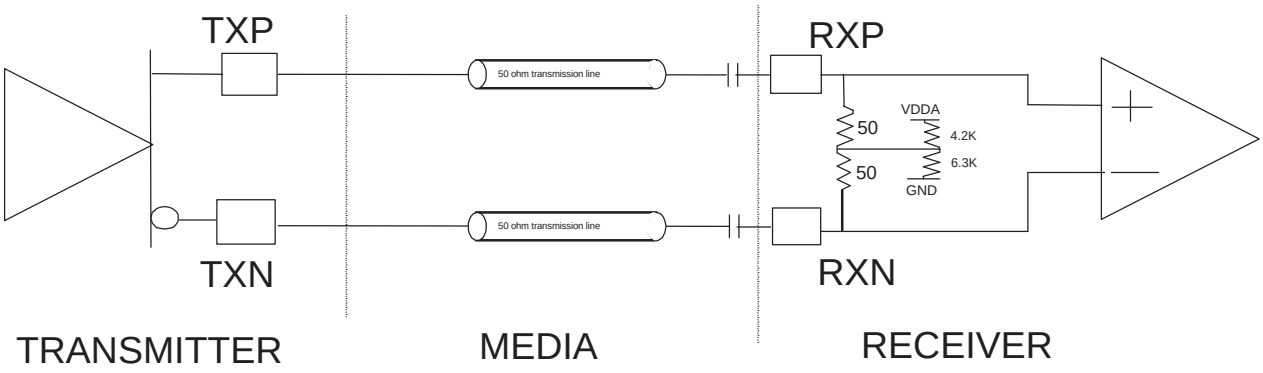


Figure 12. Example High Speed I/O AC Coupled Mode

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	14
13	TXA+	RXA+	RXB+	TXB+	GNDA	TXC+	RXC+	RXD+	TXD+	GNDA	TXE+	RXE+	RXF+	TXF+	13
12	TXA−	RXA−	RXB−	TXB−	VDDA	TXC−	RXC−	RXD−	TXD−	VDDA	TXE−	RXE−	RXF−	TXF−	12
11	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDD	VDD	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	11
10	TDA0	TDA1	TDA2	TDA3	RESET	VDD	VDD	VDD	VDD	SYNC EN	TDF3	TDF2	TDF1	TDF0	10
9	TCLKA	VDDQ	TDA4	RDA4	EN-ABLE	GND	GND	GND	GND	DVAD4	RDF4	TDF4	VDDQ	TCLKF	9
8	RDA0	GND	RDA3	VDDQ	TCLK SEL	GND	GND	GND	GND	DVAD3	VDDQ	RDF3	GND	RDF0	8
7	RCLKA	RDA1	RDA2	GND	SGMII	GND	GND	GND	GND	SWAP	GND	RDF2	RDF1	RCLKF	7
6	TDB0	VDDQ	TDB1	TDB2	CODE	GND	GND	GND	GND	REPEATB	TDE2	TDE1	VDDQ	TDE0	6
5	TCLKB	GND	TDB3	VDDQ	LPBK	PRBSEN	TRSTN	CTC_EN	RSVD	REPEATA	VDDQ	TDE3	GND	TCLKE	5
4	RDB0	RDB1	TDB4	GND	RDC2	RDC4	TDI	TDO	RDD4	RDD2	GND	TDE4	RDE1	RDE0	4
3	RCLKB	VDDQ	RDB2	RDB3	RDC1	RDC3	TCLK	TMS	RDD3	RDD1	RDE3	RDE2	VDDQ	RCLKE	3
2	RDB4	GND	TDC2	TDC4	RDC0	MDIO	VREF	GND	VDDS	RDD0	TDD4	TDD2	GND	RDE4	2
1	TDC0	TDC1	TCLKC	TDC3	RCLKC	MDC	VDDS	REFCLK	GND	RCLKD	TDD3	TCLKD	TDD1	TDD0	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

NOTE: Unused inputs that do not hold an integrated pull up or pull down circuit need to be terminated to either GND or VDDQ respectively to avoid extensive currents and life time degradation.

Figure 13. Terminal Diagram

SIGNAL TERMINAL DESCRIPTION

SIGNAL	LOCATION	TYPE	DESCRIPTION
Serial I/O Signals			
TXA+, TXA– TXB+, TXB– TXC+, TXC– TXD+, TXD– TXE+, TXE– TXF+, TXF–	A13, A12, D13, D12, F13, F12, J13, J12, L13, L12, P13, P12	VML Output	**Differential Output Transmit**. TX[A-F]+ and TX[A-F]- are differential serial outputs that interface to a copper or an optical I/F module. TX[A-F]+ and TX[A-F]- are pulled to VDDA through 500 ohms when LPBK = high or when the LOOPBACK (deep only) bit for a particular channel in the MDIO registers is set.
RXA+, RXA– RXB+, RXB– RXC+, RXC– RXD+, RXD– RXE+, RXE– RXF+, RXF–	B13, B12, C13, C12, G13, G12, H13, H12, M13, M12, N13, N12	PECL-compatible Input	**Differential input receive.** RX[A-F]+ and RX[A-F]- are the differential serial input interface from a copper or an optical I/F module. Differential resistive termination is built-in for these terminals.
Transmit Data Bus and Clock Signals			
REFCLK	H1	LVCMOS Input	**Reference Clock.** REFCLK is an external input clock that provides the clock reference.
TCLKA, TCLKB, TCLKC, TCLKD, TCLKE, TCLKF	A9, A5, C1, M1, P5, P9	HSTL Input	**Transmit Data Clock Channels A, B, C, D, E, and F.** RTBI/RGMII mode: When in Independent Transmit channel mode (TCLKSEL = 1) these pins are used to latch data for their respective channels on both the rising and falling edges. TCLKA latches data for channel A. TCLKB latches data for channel B. TCLKC latches data for channel C. TCLKD latches data for channel D. TCLKE latches data for channel E. TCLKF latches data for channel F. When in synchronous transmit channel mode (TCLKSEL = 0) only TCLKC is used as the transmit clock for all 6 parallel transmit busses.
TDA[4:0]	C9, D10, C10, B10, A10	HSTL Input	**Transmit Data Channel A.** RTBI/RGMII mode: The parallel data is clocked into the transceiver on the rising and falling edge of TCLKx and transmitted as a serial stream with TDx0 rising edge data sent as the first bit. Data is input low-order bits first aligned to the rising edge of TCLKx following by high order bits aligned to the falling edge.
TDB[4:0]	C4, C5, D6, C6, A6	HSTL Input	**Transmit Data Channel B.**
TDC[4:0]	D2, D1, C2, B1, A1	HSTL Input	**Transmit Data Channel C.**
TDD[4:0]	L2, L1, M2, N1, P1	HSTL Input	**Transmit Data Channel D.**
TDE[4:0]	M4, M5, L6, M6, P6	HSTL Input	**Transmit Data Channel E.**
TDF[4:0]	M9, L10, M10, N10, P10	HSTL Input	**Transmit Data Channel F**
Receive Data Bus and Clock Signals			
RCLKA RCLKB RCLKC RCLKD RCLKE RCLKF	A7, A3, E1, K1, P3, P7	HSTL Output	**Individual Receive Byte Clock Channels A through F**. RTBI/RGMII mode: Recovered byte clock for channels A through F. These clocks are used by the protocol device to latch the received data output for channels A through F. Data is aligned to both the rising and falling edges. If the internal CTC FIFO is disabled for a channel, the clock for that channel is 1/10th the clock recovered from the incoming data stream. If CTC is enabled for a channel, the clock for that channel is a buffered version of REFCLK. These pins are internally series terminated to provide direct connection to a 50-Ω transmission line.

SIGNAL TERMINAL DESCRIPTION (continued)

SIGNAL	LOCATION	TYPE	DESCRIPTION
RDA[4:0]	D9, C8, C7, B7, A8	HSTL Output	**Receive Data Channel A.** RTBI/RGMII mode: Output data is aligned to the rising and falling edge of the RCLKA. Channel data is output low-order bits first aligned to the rising edge of RCLKA followed by high order bits aligned to the falling edge. These pins are internally series terminated to provide direct connection to a 50-Ω transmission line.
RDB[4:0]	A2, D3, C3, B4, A4	HSTL Output	**Receive Data Channel B**
RDC[4:0]	F4, F3, E4, E3, E2	HSTL Output	**Receive Data Channel C**
RDD[4:0]	J4, J3, K4, K3, K2	HSTL Output	**Receive Data Channel D**
RDE[4:0]	P2, L3, M3, N4, P4	HSTL Output	**Receive Data Channel E**
RDF[4:0]	L9, M8, M7, N7, P8	HSTL Output	**Receive Data Channel F**
Management Data Interface Signals			
MDIO	F2	LVCMOS I/O with P/U	**Management Data I/O.** MDIO is the bi-directional serial data path for the transfer of management data to and from the protocol device.
MDC	F1	LVCMOS with P/U	**Input Management Data Clock.** MDC is the clock reference for the transfer of management data to and from the protocol device.
DVAD[4-3]	K9, K8	LVCMOS Input with P/D	**Management Address.** Device Address: DVAD[4:3] is the externally set physical address given to this device used to distinguish one device from another.
JTAG Interface Signals			
TCK	G3	LVCMOS input	**Test Clock**. IEEE1149.1 (JTAG) TCK is used to clock state information and test data into and out of the device during the operation of the test port.
TDI	G4	LVCMOS Input with P/U	**Test Data Input.** IEEE1149.1 (JTAG) TDI is used to serially shift test data and test instructions into the device during the operation of the test port.
TDO	H4	LVCMOS Output	**Test Data Output.** IEEE1149.1 (JTAG) TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state.
TMS	H3	LVCMOS Input with P/U	**Test Mode Select.** IEEE1149.1 (JTAG) TMS is used to control the state of the internal test-port controller.
TRSTN	G5	LVCMOS Input with P/U	**JTAG Reset.** IEEE1149.1 (JTAG) TRSTN is used to reset the internal JTAG controller.
Miscellaneous Signals			
CODE	E6	LVCMOS Input with P/U	**PCS Functions Enable.** When high, the Physical Coding Sublayer (PCS) functions are enabled. This pin is logically AND'd with MDIO register PCS_EN.
ENABLE	E9	LVCMOS Input	**Device Enable.** Pulling this pin high will enable all outputs of the device. A low on this pin will tri-state all outputs of the device, and causes the serial outputs to be pulled to VDDA through 500 Ω. This signal must be externally held high during JTAG manufacturing test on the customer application board. See Appendix A for more details.
CTC_EN	H5	LVCMOS Input with P/U	**CTC Enable.** This pin is AND'd with the CTC register bit. Setting this pin to logic 1 activates the CTC FIFO. A low on this pin disables the clock tolerance compensation function. This function should only be activated in transceiver mode (CODE=1).
TCLKSEL	E8	LVCMOS Input with P/D	**Independent Channel Transmit Clock Select.** A logic 0 selects latching of all channels synchronous to TCLKC. A logic 1 selects individual clocking. This pin bit is logically OR'd with the TCLKSEL input MDIO register bit.
RESET	E10	LVCMOS Input with P/D	**Chip Reset (FIFO Clear)** Pulling this terminal high re-centers the transmit skew buffers, receive channel synchronization FIFO's, and will reset MDIO flags to default settings. Reset should be asserted for 100 µs after all power supplies and input clock frequencies are within specification. Alternatively, a soft reset could be issued after clock and power stabilization.
LPBK	E5	LVCMOS Input with P/D	**Loopback Enable.** When set high, TX+/– outputs are pulled to VDDA through 500 ohms. The serial TX+/– output data is internally looped to RX+/– inputs. External data applied to RX+/– inputs is ignored.

SIGNAL TERMINAL DESCRIPTION (continued)

SIGNAL	LOCATION	TYPE	DESCRIPTION
PRBSEN	F5	LVCMOS Input with P/D	**PRBS Enable.** When this terminal is asserted high, the pseudo-random bit stream generator and comparator circuits are inserted into the transmit and receive data paths on all channels, respectively. If this pin is not used it can be tied to the GND reference. TX+– are transmitting 2^7-1 PRBS bit streams. RX+– are comparing incoming data to 2^7-1 PRBS bit stream. Results of the RX comparison can be read from the MDIO.
SYNCEN	K10	LVCMOS Input with P/U	**SYNC Enable.** When enabled, the TLK2226 byte-aligns incoming data on RX+/– on positive RD (running disparity) commas (001 1111b). This pin is AND'd with the COMM_DET register bit.
SWAP	K7	LVCMOS Input with P/D	**Parallel Port Swap.** When enabled, the parallel port for channel B is routed to the serial port for channel A, and the parallel port for channel A is routed to the serial port for channel B. Likewise, the parallel ports for channels C and D, E and F are swapped. This pin is logically OR'd with the PORT_SWAP register bits.
REPEATA	K5	LVCMOS Input with P/D	**Repeater Mode Ports A, C, E.** When enabled, the serial data on the channel B receiver pins is repeated out on the channel A serial transmit pins. Likewise, Channel D serial receive data is repeated out on channel C serial transmit pins, and Channel F serial receive data is repeated out on channel E serial transmit pins. This pin is logically OR'd with the REPEATER register bits for channels A, C, and E.
REPEATB	K6	LVCMOS Input with P/D	**Repeater Mode Ports B, D, F.** When enabled, the serial data on the channel A receiver pins is repeated out on the channel B serial transmit pins. Likewise, Channel C serial receive data is repeated out on channel D serial transmit pins, and Channel E serial receive data is repeated out on channel F serial transmit pins. This pin is logically OR'd with the REPEATER register bits for channels B, D, and F.
RSVD	J5	RESERVED	**Reserved:** This signal is reserved for TI internal testing. These should be connected to GND in customer applications.
SGMII	E7	LVCMOS Input with P/D	**SGMII Mode** When asserted, enables SGMII mode. When low, SGMII mode is deasserted. This pin sets the default value of the SGMII register bit (16.4) on the falling (deasserting) edge of the RESET pin.
Power and Reference Pins			
VDDQ	B3, B6, B9, D5, D8, L5, L8, N3, N6, N9	Supply	**HSTL I/O Supply Voltage.** 1.5 V or 1.8 V
VDD	F10, G10, G11, H10, H11, J10	Supply	**Digital Logic Power:** Provides power for all digital circuitry. Nominally 1.8 V.
VDDS	G1, J2	Supply	**Secondary voltage LVCMOS I/O Supply Voltage** 1.8 V OR 2.5 V OR 3.3 V
VDDA	A11, B11, C11, D11, E11, E12, F11, J11, K11, K12, L11,M11, N11, P11	Supply	**Analog Power.** VDDA provides a supply reference for the high-speed analog circuits, receiver and transmitter. Nominally 1.8 V.
VREF	G2	Reference	**Voltage Reference**– for HSTL reference
GNDA	A14, B14, C14, D14, E13, E14, F14, G14, H14, J14, K13, K14, L14, M14, N14, P14	Ground	**Analog Ground.** GNDA provides a ground reference for the high-speed analog circuits, RX and TX.
GND	B2, B5, B8, D4, D7, F6, F7, F8, F9, G6, G7, G8, G9, H2, H6, H7, H8, H9, J1, J6, J7, J8, J9, L4, L7, N2, N5, N8	Ground	**Digital Logic Ground.** Provides a ground for the logic circuits and digital I/O buffers.

DETAILED DESCRIPTION

REFERENCE CLOCK SYNTHESIZER (PLL)

The TLK2226 employs a mature Phase Lock Loop (PLL) design in use for Gigabit Ethernet transceivers and high-speed serial links by Texas Instruments since 1997 on both standard products and custom ASIC designs. This PLL design is used to synthesize the serial line rate bit clock from the REFCLK input as well as generate clocks for the receiver sampling circuitry. The PLL and associated high speed circuitry is powered by the analog power supply pins (VDDA) with isolated grounds (GNDA). Care should be taken in providing a low noise environment in a system. It is recommended to supply the VDDA reference by separate isolated plane within the system printed circuit board (PCB). It is recommended that systems employing switching power supplies provide proper filtering of the fundamental and harmonic components in the 1MHz-10Mhz band to avoid bit errors from injected noise. It is strongly recommended that no PLL based clock synthesizer circuit be used as the source for the REFCLK. This could cause accumulation of jitter between the two PLL's

OPERATING MODES

The TLK2226 has two operational modes with respect to the Physical Coding Sublayer (PCS) functions called RTBI mode and RGMII mode. The RTBI or RGMII mode is selectable via the CODE bit in MDIO register space or the CODE pin as described in Table 1. The CODE pin is gated with the internal CODE register such that setting the pin to a logic zero disables the PCS functions, setting the CODE pin to a logic one enables PCS functions and permits these functions to be disabled on a channel by channel basis via MDIO control. In addition, all PCS functions except the CTC FIFO may be enabled if the CTC FIFO is to be implemented in the protocol device. The CTC FIFO may be disabled by way of the CTC_EN pin or the CTC_EN bit in the MDIO register space. Besides the RTBI or RGMII modes, additional modes of operation include the serial repeater mode with CTC FIFO mode, serial repeater without CTC FIFO mode, RGMII port swap mode, and 1/10 rate for 100FX mode.

Table 1. PCS Operational Modes

CODE	OPERATING MODES
Low	**RTBI mode.** Disables PCS functions for each channel. Refer to *Byte Alignment Logic* section, for additional description over this mode.
High	**RGMII mode.** Enables PCS functions for each channel. Data on the transmit and receive data bus is treated as un-coded data.

RTBI MODE

In RTBI mode, the transmit data bus for each channel accepts 5-bit wide encoded data on the transmit data bus pins. Data is latched on the rising and falling edge of the transmit data clock. The encoded data is then phase-aligned, serialized and transmitted sequentially beginning with bit 0 over the differential high speed serial transmit pins. The receive data bus for each channel outputs 5-bit wide data. Data is output relative to both the rising and falling edge of the receive clock.

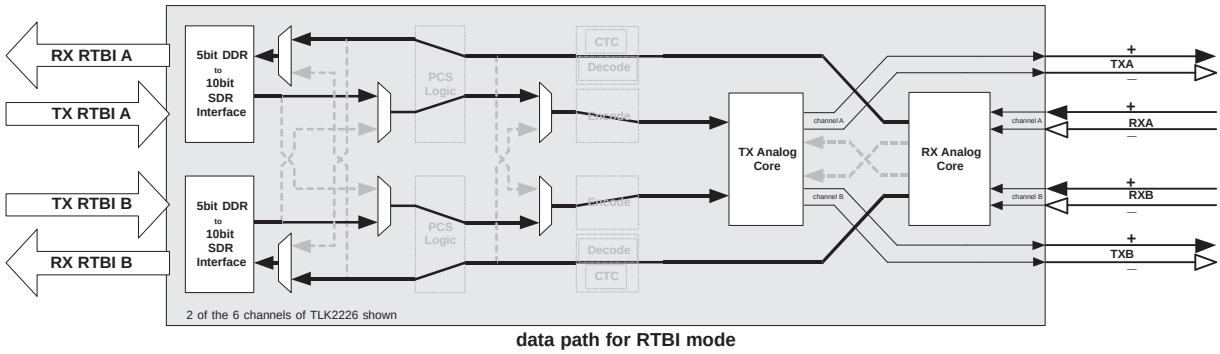


Figure 14. RTBI Mode Block Diagram

RGMII MODE

In RGMII mode, the transmit data bus for each channel accepts 4-bit wide un-coded parallel data plus the two GMII control bits TX_EN and TX_ER (on bit4 of TDx[4:0]). Data is sampled on the rising and falling edge of the transmit clock. The data is first aligned to the reference clock (REFCLK), then 8B/10B encoded and passed to the serializer. The receive data bus for each channel outputs un-coded 4-bit wide parallel data plus the two GMII status bits RX_DV and RX_ER (on bit4 of RDx[4:0]).

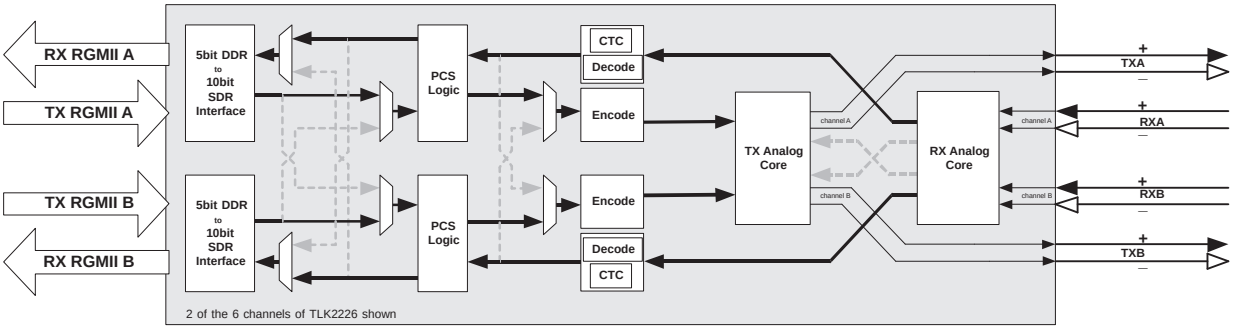


Figure 15. RGMII Mode Block Diagram

In RGMII mode, all of the PCS functions are implemented as required by the IEEE802.3 specification, including the 8b/10b encoding, decoding, Clock Tolerance Compensation, insertion of the Start of Frame and End of Frame codes, and the auto-negotiation state machine. In RGMII mode, it is also possible to bypass the CTC FIFOs in which case the received data will be output with a recovered byte clock that remains in the clock domain of the received serial data stream.

SERIAL REPEATER MODE (WITHOUT CTC)

The serial repeater mode operation can be selected on a per channel basis. The serial inputs on one channel are transmitted back out serially on the adjacent channel. Channel A receive data is repeated out on channel B transmit while channel B receive data is repeated out on channel A transmit. In this manner channels A and B can form a full-duplex repeater. Likewise, channels C and D, and E and F can be used to form full-duplex repeaters.

Repeater mode for channels A and B can be chosen separately, if desired. That is, serial data received on channel A can be repeated out on channel B transmit pins without also choosing to repeat channel B serial receive data out on channel A. In fact, the repeater mode selection bit for a given channel may be thought of as simply selecting whether the data to be transmitted for that port comes from the parallel port for that channel or the serial data from the adjacent channel. In this way, a channel may be used as a normal RGMII or RTBI channel while the incoming serial data is also repeated out on the adjacent channel. When repeater mode for a given channel is selected, any data presented to the parallel transmit bus for that channel will be ignored.

While in repeater mode, the incoming serial data will still go through the deserializer function, and the PCS functions if enabled, and the deserialized data will still be presented out on the parallel transmit bus. Since the Clock Tolerance compensation functions are disabled in this mode, the data presented on the parallel port will reflect the CTC function being disabled as well.

Repeater mode without CTC is chosen by setting the repeater mode register bit active while also setting the CTC_EN register bit inactive at the same time.

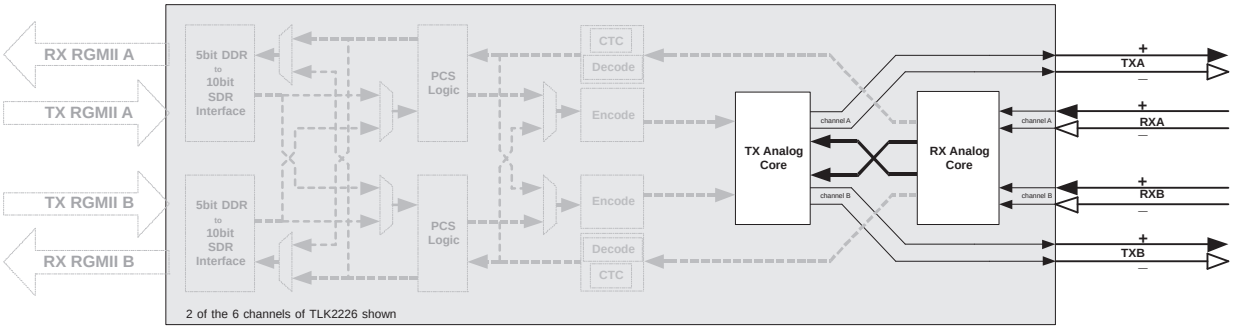


Figure 16. Serial Repeater Mode Block Diagram

In serial repeater mode, a clock/data recovery function (CDR) locks to the incoming data stream and then sends that data out on the transmit port of the adjacent channel. The CDR function will lock to the data stream so that Inter-Symbol Interference (ISI) jitter is filtered out from the retransmitted data. Retransmitted data will remain in the clock domain of the incoming data stream, since there is no clock tolerance compensation FIFO to adjust the data stream to the REFCLK clock domain. Since the CDR function will track any frequency wander on the data stream that is lower than the bandwidth of the CDR, any such wander components will remain in the retransmitted data stream. Also, since the jitter tolerance specification for the CDR function is such that the recovered bit clock must work with a minimum eye opening of 0.2513UI (equal to 201ps at 1.25GB/s), and the jitter generation specification for a transmitted data stream is 0.24UI (equal to 192 ps at 1.25Gb/s), it is not guaranteed that the re-transmitted serial data will meet the IEEE802.3 jitter generation specifications.

SERIAL RETIMING REPEATER MODE (WITH CTC)

The TLK2226 also provides another serial repeater mode serial repeater mode except the data stream is deserialized and passed through a Clock Tolerance Compensation FIFO. The CTC FIFO will add or drop IDLE codes as needed (or CONFIG codes) to match the data stream to the REFCLK clock domain. The data stream is then retransmitted out the TX of the adjacent channel. In serial retiming repeater mode the CTC FIFO ensures that any frequency wander passed through the CDR function will not appear in the transmit data stream. The retransmitted data can be guaranteed to meet the transmit jitter generation specifications for IEEE802.3.

Repeater mode with CTC is chosen by setting the repeater mode register bit active while also setting the CTC_EN register bit active at the same time. As in serial repeater mode, the repeater path from channel A to channel B may be selected separately from the repeater path for channel B to channel A.

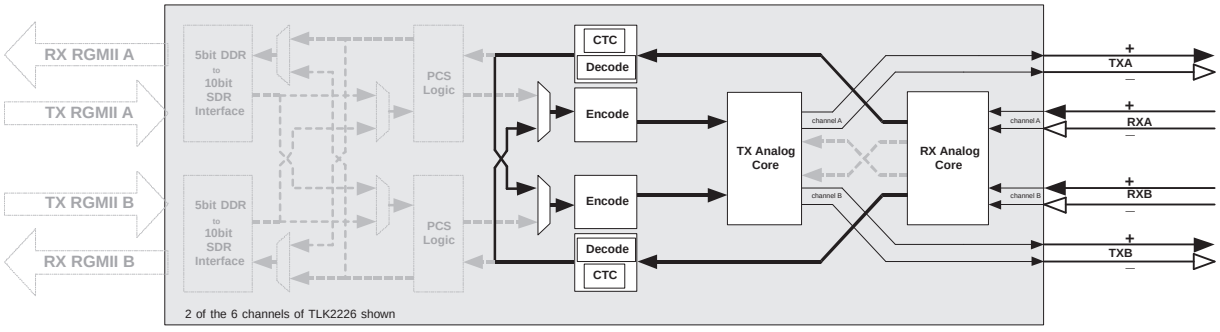


Figure 17. Serial Retiming Repeater Mode Block Diagram

RGMII PORT-SWAP MODE

The TLK2226 provides a set of multiplexors on the parallel busses between pairs of channels such that the RGMII port for Channel A can be steered to the serial port for Channel B, while at the same time the RGMII port for Channel B can be steered to the serial port for Channel A. See Figure 18 for the block diagram illustrating this mode. Likewise, the RGMII ports for channels C and D may be swapped, as may the RGMII ports for Channels E and F,

The selection of swapping a pair of RGMII ports is accomplished by setting the appropriate register bit in MDIO register space.

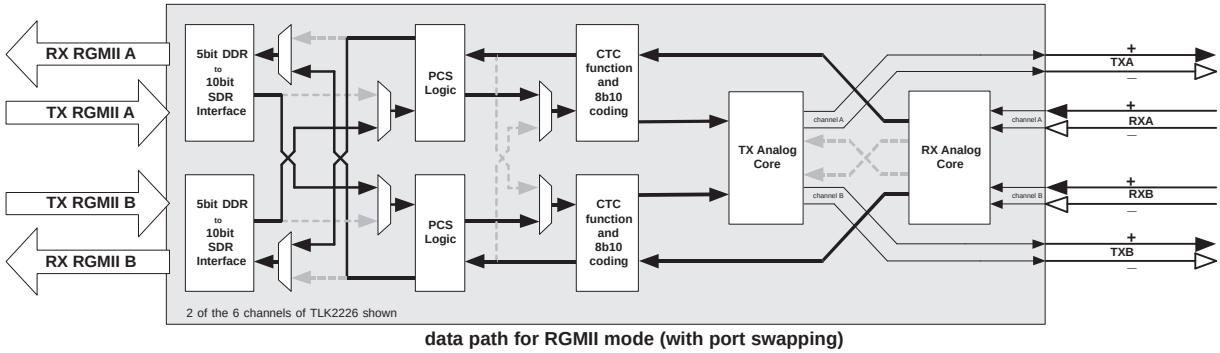


Figure 18. RGMII Mode with Port Swapping

100FX 125Mbps MODE

The TLK2226 can be set to operate at 125 Mbps on a per channel basis. While in 100FX mode, the PCS functions are enabled for RGMII mode, but the transmit and recovered byte clocks are at 25 MHz. When a channel is in 100FX mode the PCS functions for that channel will comply with the IEEE802.3 100 base-x specifications, including the 4b/5b coding, NRZI Encoding, and nibble alignment.

While a channel is in 100FX mode, the reference clock for that channel will still be the 125MHz reference clock input for the TLK2226. For this reason, the transmit clock for that channel's RGMII port must be a 25MHz derivative of the reference clock without any ppm frequency offset. The recovered byte clock for that channel's RGMII port will be divided down to 25 MHz.

Auto rate select for a channel will operate primarily off of transition density of the incoming serial data stream. The Clock and Data Recovery (CDR) function of the channel receiver will always operate at the 1.25Gbps rate. If the incoming data stream is properly coded 8b/10b data for 1.25Gbs data then the transition density of the incoming data will be detected and that channel will operate at 1.25Gbps. If properly 4B/5B and NRZI Encoded data for 100FX operation received, then the incoming transition density will be detected as a maximum 1 transition per 10bit input word, and that channel will operate at 125 Mbps. When a channel is operating at 125Mbps, the actual SERDES front end will still be operating at 10 times that rate by transmitting every 100FX bit 10 times in a row and by over-sampling every incoming 100FX bit by a factor of 10.

SGMII (Serial GMII) (1000 Mbps/100 Mbps/ 10 Mbps) MODE

The TLK2226 can be set to operate in SGMII mode (register bit 16.4). In this mode, the serial side of TLK2226 always operates at 1.25 Gbps. The parallel interface speed is directly selected through mdio register bits 0.6 and 0.13. In 10 Mbps mode, the parallel interface runs at 2.5 MHz. In 100 Mbps mode, the parallel interface runs at 25 MHz. In 1000 Mbps mode, the parallel interface runs at 125 MHz. In all three modes, the slightly modified (per the SGMII document) auto-negotiation state machine (if enabled) is active.

In 1000 Mbps SGMII mode the parallel interface operates identical to the 1000Base-X case with SGMII disabled. In both 10 and 100 Mbps SGMII modes, the parallel data is transferred on the parallel interface at the lower provisioned rate, and replicated either 10 or 100 times for transmission (and deleted accordingly in the receive direction) by the PCS layer out the serial interface. Note that in both the transmit and receive directions for both

10 and 100 Mbps SGMII modes, the nibble transferred on the rising edge is repeated on the negative edge of the parallel interface clock. For a given packet byte, the lower nibble is placed on the parallel interface during the first clock period (the data is duplicated on falling edge), followed by the upper nibble of the packet byte on the next clock period (data is duplicated on the falling edge). Also note that the control bits for the byte are duplicated according to the RGMII standard across the two clock periods.

All test related and data path functional modes for TLK2226 are capable of operating in the SGMII mode. Specifically, all three loopback modes, transceiver, port swap, and all repeater modes operate properly.

PARALLEL INTERFACE MODES

The TLK2226 provides an RTBI compliant interface or an RGMII compliant interface. Each parallel channel provides 5 bit busses clocked in Double Data Rate (DDR) fashion. The five least significant bits of data are latched on the rising edge of the transmit clock are put together with the 5 most significant bits of data latched on the falling edge of the clock.

The parallel transmit busses may be configured such that a single transmit clock (TCLKC) is used to clock in the parallel data for all 6 channels, or each parallel transmit bus may have its own transmit clock. The transmit clocks must not have any frequency deviation relative to REFCLK. Each transmit channel employs a small FIFO to allow for arbitrary phase relationships between the transmit clock and REFCLK, but the transmit FIFO will not account for frequency variance between the transmit clocks and REFCLK. On the receive side, if the CTC FIFO is used for a given channel, then the receive data bus for that channel will be clocked out by a buffered version of REFCLK. If the CTC FIFO is not used, then the recovered byte clock for that channel will be 1/10th the rate of the incoming serial data stream.

The interface modes can be controlled via CODE and CTC. A summary of the TLK2226 parallel interface modes is shown in Table 2.

Table 2. Parallel Interface Modes

<table>
<tr><th colspan="2">CODE
Low=RTBI
High=RGMII</th><th>CTC
Low=disable
High=enable</th><th>DESCRIPTION</th></tr>
<tr><td>Low</td><td>RTBI Mode
Bit[4] Data[4] Data[9]
Bit[3] Data[3] Data[8]
Bit[2] Data[2] Data[7]
Bit[1] Data[1] Data[6]
Bit[0] Data[0] Data[5]
CLK ↑ ↑</td><td>x</td><td>RTBI channel mode:
• No clock tolerance compensation is performed on Receive data.
• Data towards MAC are aligned to individual RCLKs on a source-centered/aligned mode per channel basis</td></tr>
<tr><td rowspan="2">High</td><td rowspan="2">RGMII Mode
Bit[4] CTRL1 CTRL2
Bit[3] Data[3] Data[7]
Bit[2] Data[2] Data[6]
Bit[1] Data[1] Data[5]
Bit[0] Data[0] Data[4]
CLK ↑ ↑</td><td>Low</td><td>RGMII (without CTC) channel mode:
• No clock tolerance compensation is performed
• Data towards MAC are aligned to individual RCLKs on a source-centered/aligned per channel basis.</td></tr>
<tr><td>High</td><td>RGMII channel mode
• All data towards MAC are aligned to RCLKx thru CTC FIFO. (TLK2226
• accepts +/-200ppm frequency offset on the receive data relative to the transmit data.)
Each RCLKx is a buffered version of REFCLK, source centered/aligned relative to the receive data.</td></tr>
</table>

TRANSMIT DATA PATH

The transmit logic converts parallel data into an NRZ serial bit stream with a differential VML output at a rate of from 1.0 to 1.3Gbps

Transmit Clock Interface

Transmit clocks for all channels is expected to be the same frequency as the reference clock, REFCLK, but of arbitrary phase relationship to REFCLK.

Transmit Parallel Interface

In **synchronous channel mode**, parallel data to be transmitted is latched by both the rising and falling edges of TCLKC. TCLKC must be frequency synchronous with REFCLK (0 ppm), but may have any phase relationship with respect to REFCLK. While in synchronous channel mode, it is recommended that the unused individual channel clocks TCLKx be grounded to minimize noise.

In **independent channel mode**, parallel data to be transmitted on channel A is latched on the rising and falling edges of TCLKA. The transmit data bus for channel B is latched on the rising and falling edges of TCLKB, the transmit data bus for channel C is latched on the rising and falling edges of TCLKC and so on.

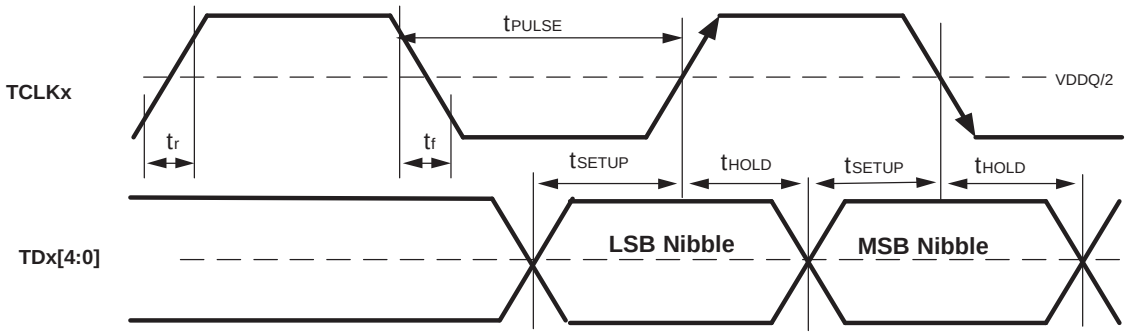


Figure 19. Transmit Timing (Clock Centered)

Serializer

The parallel-to-serial shift register on each channel takes in an internally generated 10-bit wide word from either the 8b/10b encoders, if enabled, or directly derived from the 5-bit to 10-bit converter and converts it to a serial stream. The shift register is clocked by the internally generated bit clock, which is 10 times the reference clock (REFCLK) frequency. The least significant bit (LSB) for each channel is transmitted first.

Serial Output Drivers

The TLK2226 serial transmitter utilizes a Voltage Mode Logic (VML) driver that drives both the high level and low level of the output signal swing. Thus, no external pull-up resistors are needed as in the case of Current Mode Logic (CML) drivers, nor are pull-down resistors needed as in the case of Emitter-Coupled Logic (ECL). The output voltage swing is set at a nominal 800 mV on each leg of the differential signal, making the output signal swing compatible with PECL systems.

The TLK2226 output driver has a pre-emphasis option (selectable through MDIO) for improved performance over lossy media such as backplane traces.

RECEIVE DATA PATH

The receiver input data must be ac-coupled and have a rate of 1.0–1.3 Gbps (or 1/10th that rate for 100FX mode). Resistive termination is implemented on-chip to match 50Ω.traces. The clock recovery circuitry retimes the input data by extracting a clock from the input data, and passes on the serial data and this recovered clock to the deserializer. Byte alignment is performed on K-characters per IEEE 802.3z while in 1.25Gbps operation (see byte alignment logic section for details). Byte alignment is performed on the NRZI Encoded IDLE pattern while in 125Mbps mode.

Serial Input Samplers

The TLK2226 strobes the received serial data with an internal high-speed clock that is locked to the data stream by the clock recovery function. The differential serial receive data buffers internally terminate the transmission line with 50Ohm termination resistors. It is expected that the serial receive data is AC coupled, so the internal termination also biases the signal to the common mode level that is optimum for the input samplers. No external components are needed apart from the AC coupling capacitors themselves

Clock Recovery

A baud rate clock is extracted from the 10-bit encoded serial data stream independently on each channel. After powering up the device, it takes approximately 8 μs before data is received and the device is ready to transmit. The receive clock locks to the input within 2 μs after a valid input data stream is applied. The received data is de-serialized and byte aligned to IEEE802.3z /K28.5-characters (while in 1.25Gbps mode). In the absence of input data, the clock recovery circuit will lock onto the reference clock frequency REFCLK; once valid data is again presented at the serial inputs, a time will elapse before the channel reacquires lock and performs data and clock recovery functions.

Deserializer

For each channel, serial data is received on the RXx+/RXx– pins. The interpolator and clock recovery circuit will lock to the data stream if the clock to be recovered is within ±200 PPM of the internally generated bit rate clock, assuming a ±100 PPM tolerance on the reference clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. If enabled, the 10-bit wide parallel data is then fed into 8b/10b decoders. The parallel data for each channel is fed into a FIFO buffer where the output is synchronized to REFCLK when CTC is on. In case CTC is off data is synchronized to 1/10th of the received bit clock.

Byte Alignment Logic (1.25 Gbps mode)

Under default conditions, the TLK2226 uses the IEEE802.3z defined 10-bit K28.5 character (comma character, positive disparity) word alignment scheme . The following sections explain how this scheme works and how it realigns itself. When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally, this is accomplished through use of a synchronization pattern. This is a unique a pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8B/10B encoding makes allowance for a special pattern called the comma (B'0011111') which is used by the byte alignment circuit to align the received serial data back to its original byte boundary. The decoder detects the comma pattern in the K28.5 character, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data. It is important to note that the comma can be either a (B'0011111') or the inverse (B'1100000') depending on the running disparity. The TLK2226 decoder will detect only the (B'0011111') pattern. Therefore, since synchronization is achieved on the positive comma, two consecutive K-codes containing commas are required to guarantee byte boundary synchronization (see Table 3 Valid K characters for K-codes containing positive commas).

During all operations, the TLK2226 receive clocks (RCLKx) are a constant duty cycle and frequency. There are no stretched nor shortened clock pulses.

Table 3. Valid K Characters

K CHARACTER	RECEIVE DATA BUS	ENCODED K-CODE	
		NEGATIVE RUNNING DISPARITY	POSITIVE RUNNING DISPARITY
K28.0	000 11100	001111 0100	110000 1011
K28.1	001 11100	001111 1001 (1)	110000 0110
K28.2	010 11100	001111 0101	110000 1010
K28.3	011 11100	001111 0011	110000 1100
K28.4	100 11100	001111 0010	110000 1101
K28.5	101 11100	001111 1010 (2)	110000 0101
K28.6	110 11100	001111 0110	110000 1001
K28.7	111 11100	001111 1000 (2)	110000 0111
K23.7	111 10111	111010 1000	000101 0111
K27.7	111 11011	110110 1000	001001 0111
K29.7	111 11101	101110 1000	010001 0111
K30.7	111 11110	011110 1000	100001 0111

(1) Setting COMMA_DET=0, or SYNCEN pin K10 by changing its value via MDIO 17.8 would disable comma detection, and byte alignment would take place on any bit boundary; this permits external byte alignment on different bit sequences, and allows for the use of different bit balancing algorithms.
(2) A comma is contained within this K-code.

Receive Parallel Interface

The receive data bus for all channels may be output in either a source-centered fashion (with the bus clock transitions in the center of the data eye) or a source-aligned fashion (with the bus clock transitions aligned to the data transitions) allowing direct connection to the protocol device.

Parallel data to be transferred to the protocol device is output referenced to both the rising and falling edges of RCLKx. RCLKx is frequency synchronous with REFCLK when the Clock Tolerance Compensation logic is enabled, but RCLKx has no set phase relationship with respect to REFCLK. Each channel is output on RDx[4:0] respectively, as shown in Figure 20.

Parallel data to be transferred to the protocol device on channel A (RDA[4:0]) is output referenced to both the rising and falling edges of the RCLKA, Channel B (RDB [4:0]) is output referenced to both the rising and falling edges of RCLKB. Channels C through F are output in the same fashion with their respective clocks. Nibble ordering is such that least significant bits are output first and on the rising edge of the clock.

It is important to note, that when the Clock Tolerance Compensation logic is enabled, all recovered byte clocks (RCLKx) are buffered versions of REFCLK. When the Clock Tolerance Compensation circuit is disabled, the RCLKx for a channel will be the true 1/10th rate clock recovered from the incoming data stream. Like transmit timing options, receive clocks RCLKx are either Source Centered or Aligned meeting specified output setup and hold times. Clock Tolerance Compensation is only available in RGMII mode.

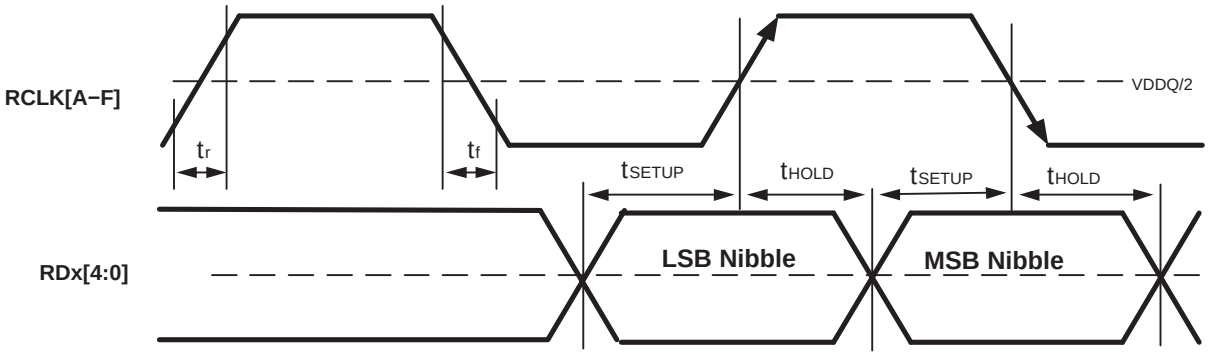


Figure 20. RTBI Receive Timing (Clock Centered)

PHYSICAL CODING SUBLAYER (PCS) FUNCTIONS (1.25 Gbps MODE)

8b/10b Encoder

All true serial interfaces require a method of encoding to insure sufficient transition density for the receiving PLL to acquire and maintain lock. The encoding scheme also maintains the signal DC balance by keeping the number of ones and zero's the same which allows for AC coupled data transmission. The TLK2226 uses the 8B/10B encoding algorithm that is used by Fibre Channel and Gigabit Ethernet. This provides good transition density for clock recovery and improves error checking. The 8B/10B encoder function is enabled for all channels by the assertion of the CODE bit. When enabled, the TLK2226 will internally encode the data such that the user actually writes 8-bit data out on each channel. The encoded 10 bit data will then be transmitted.

When enabled (CODE = high), the 8B/10B encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes D-characters, used for transmitting data, and K-characters, used for transmitting protocol information. Each K or D character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

The TLK2226 will transmit and receive all of the valid K-characters used in the IEEE802.3 Gigabit Ethernet ordered sets.

8b/10b Decoder

The 8B/10B decoder function is enabled for all channels by the assertion of the CODE bit. When enabled, the TLK2226 will internally decode the deserialized data such that the user actually reads the decoded bytes out on each channel.

Clock Tolerance Compensation (CTC) FIFOs

The TLK2226 compensates for the possibility that incoming serial data rate on any channel can be as much as 100 ppm faster or slower than the REFCLK frequency (±100ppm). Each channel independently and dynamically compensates for any frequency difference by use of an elasticity buffer. If the incoming data rate is faster than the REFCLK frequency, the elasticity buffer will fill. As it approaches the FILL limit, it will delete or drop a 20-bit IDLE code(3) found in the IPG (inter packet gap) between Ethernet packets. If the incoming data rate is slower than the REFCLK, the elasticity buffer will empty. As it approaches the EMPTY limit, it will add or insert the 20-bit IDLE code found in the gap between Ethernet packets. Idle code selection defaults to IDLE2, a K28.5 followed by a D16.2. No running disparity is affected due either the addition or the deletion of the IDLE2 code as the IDLE2 code has a balanced number of 1's and 0's. Note that a deletion of a 20-bit IDLE2 code could reduce the inter-packet gap below the minimum inter-packet gap of 12 bytes (120 bits).

The CTC function will only add or delete IDLE codes in the inter-packet gap. Thus the CTC FIFO depth is sized to insure that maximum size Ethernet packets (9300 bytes) can be continuously received at the frequency offset extremes without loss of data or synchronization and still meet latency requirements per the standard. The CTC function can be disabled for all channels via the MDIO registers or through its dedicated pin. The CTC function is available only when the TLK2226 is set in the transceiver mode by MDIO or CODE pin or activation.

During Auto-negotiation the TLK2226 will support clock tolerance during config word (which are converted to idles by the PCS receive state machine) reception, so that FIFO overrun or underrun does not occur during auto-negotiation.

AutoNegotiation (AN)

AN is initialized for all channels at power-up once all PLL's have locked. AN can be restarted on a per channel basis by writing a logic HIGH to the MDIO reg0x00[9] for the specific channel. The AN process is implemented according to IEEE 802.3z clause 37. The Status and results of the AN process can be read from the MDIO.

TLK2226 also supports the transmit of NextPage (NP) information provided by it's management device via MDIO.

CODE needs to be asserted and 'AN Enable' register in the MDIO 0x00[12] is set to a logic HIGH.

(3) IEEE802.3z specifies an IDLE as a 20-bit code consisting of an IDLE1 code (/K28.5/D5.6) or an IDLE2 code (/K28.5/D16.2).

Framing (Encapsulation)

Upon the assertion of TX_EN, TLK2226 encapsulates data asserted by the MAC on the parallel interface (TDx) into a code_group stream according to IEEE 802.3z clause 36.

Upon the receipt of a valid code_group stream at the serial RX interface, TLK2226 decodes the incoming data, extracts packets and passes the decoded data to the MAC via the parallel RDx interface according to IEEE 802.3z clause 36.

The 5-bit parallel interfaces of TLK2226 (RX and TX) are compliant to the RGMII specification version 2.0 from 04/01/2002.

CODE needs to be asserted a logic HIGH to perform framing.

PHYSICAL CODING SUBLAYER (PCS) FUNCTIONS (125 Mbps MODE)

4b/5b Encoder/Decoder

The TLK2226 shall implement the 4b/5b encoder and decoder functions according to IEEE802.3 Clause 24 when in 100FX mode instead of the 8b/10b coding functions.

NRZI Encoder/Decocer

The TLK2226 shall implement the cipher scrambling and descrambling functions according to ISO/IEC 9314-3:1990.

Nibble Alignment

The TLK2226 will align the first properly NRZI decoded /I/J/K/ pattern.

PER CHANNEL RATE DETECTION DETERMINATION

The actual rate per channel is determined by Table 4.

Table 4. Per Channel Rate Determination

0.12 Auto Negotiation Enable	16.5 Rate Sense Enable	0.6 Speed Selection (MSB)	0.13 Speed Selection (LSB)	16.4 SGMII Mode Enable	TLK2226 Behavior
1	1	X	X	0	Auto Rate Sense (Default Behavior)
1	0	X	X	0	1000Base-X Rate
0	1	X	X	0	Auto Rate Sense
0	0	1	0	0	1000Base-X Rate
0	0	0	1	0	100Base-FX Rate
X	X	1	0	1	SGMII (1000 Mbps Data path Operation)
X	X	0	1	1	SGMII (100 Mbps Data path Operation)
X	X	0	0	1	SGMII (10 Mbps Data path Operation)

The resulting value of the per channel rate may be read in read only register bit 28.14. This bit indicates the actual serial rate of a channel as a function of the above bits shown in Table 4.

CONTROL LOGIC

MDIO Management Interface

The TLK2226 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK2226 is possible without use of this interface since all of the essential signals necessary for operations are accessible via the device pins. However, some additional features are accessible only through the MDIO. The PHY address contained in the MDIO protocol allows to individually access/address

4 TLK2226 devices connected to the same MDIO bus. The address of the individual device is set by the pins DVAD[4:3]. PHYAD[4:3] correspond to DVAD[4:3] and is used to select the device. In order to read/write information from/to the IEEE defined registers for a specific channel within TLK2226, PHYAD[2:0] are to be used in the PHY Address section. Channel A would be addressed by setting PHYAD[2:0] to 3'b000, Channel B would be addressed by setting PHYAD[2:0] to 3'b001 and so on.

IEEE defined registers (from 0x00 to 0x08 and 0x0F) are duplicated for each individual channel of TLK2226. Whether or not additional registers are specific to a single channel or to all channels is lined out in the register map below.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The timing required to read from the internal registers is shown in Figure 21. The timing required to write to the internal registers is shown in Figure 22.

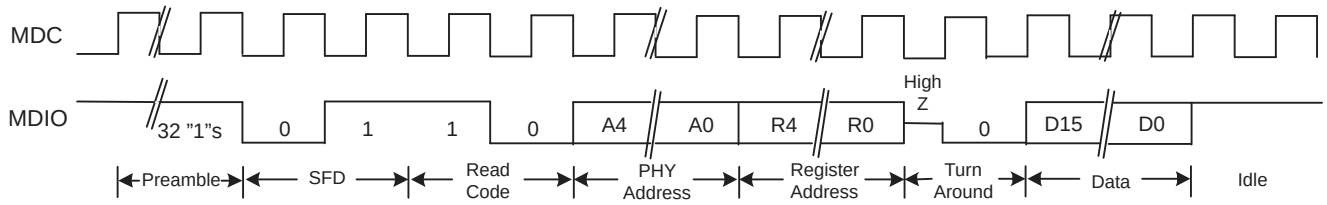


Figure 21. Management Interface Read Timing

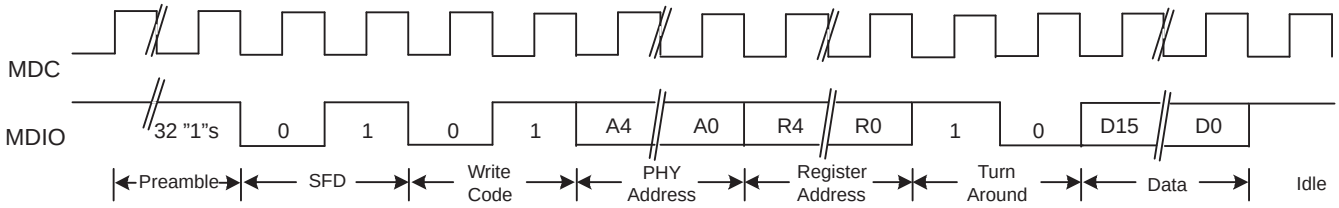


Figure 22. Management Interface Write Timing

The MDIO Interface allows up to 32 (16-bit) internal registers. Sixteen registers are defined by the IEEE 802.3 Clause 22 specification. Additional registers are allowed for expanded functionality. The TLK2226 employs all IEEE defined registers for PCS layer devices. The TLK2226 also implements additional registers for expanded functionality. The IEEE defined registers and the expanded functionality registers are outlined in Table 5.

All latching bits need to be read twice after device initialization to read current/correct status.

The legend for the register map summary is:

1. Self Clearing
2. ReadWrite
3. Read Only
4. Latched High
5. Latched Low

Table 5. MDIO Register Map Summary

DEC	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Name (Hex Reset Val)
0	0	Reset(1)	Loopback(2)	Speed Sl lsb(2)	AN Enable(2)	Power Down(2)	Isolate	Restart AN(1)	Duplex Mode(3)	Collision Tst(3)	Speed Sl msb(2)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Control 1 (0x1140)
1	1	1000Base T-4(3)	100Base XFD(3)	100Base -XHD(3)	10Mb/s FD(3)	10Mb/s HD(3)	100Base -T2 FD(3)	100Base -T2 HD(3)	Extended Stat(3)	RSVD(3)	MF Preа Supp(3)	AN Complete(3)	Remote Fault(3)	AN Ability(3)	Link Status(5)	Jabber Detect(3)	Extended Cap(3)	Status 1 (0x4149)
2	2	Organizationally Unique Identifier[3:18](3)																PHY ID0 (0x4000)
3	3	Organizationally Unique Idendifier (19-24)(3)						Manufacturer Model Number(3)						Manufacturer Revision Number(3)				PHY ID1 (0x5060)
		0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	
4	4	Next Page(2)	RSVD(3)	Remote Fault[1:0](2)		RSVD(3)	RSVD(3)	RSVD(3)	Technology Ability[3:0] (2)				RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	ANEG ADV (0x0020)
5	5	LP Next Page(3)	LP Ack(3)	LP Remote Fault(3)		RSVD(3)	RSVD(3)	RSVD(3)	LP Technology Ability[3:0](3)				RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	AN LP Ability (0x0020)
6	6	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Next Page Able(3)	Page Received(4)	RSVD(3)	AN Expansion (0x0004)
7	7	Next Page(2)	RSVD(3)	Msg Page(2)	Acknowl. 2(2)	NP Toggle(3)	Msg/Unformatted Code Field[10:0](2)											AN Next Page (0x2001)
8	8	LP Next Page(3)	RSVD(3)	LP Msg Page(3)	LP Ack 2(3)	LP Toggle(3)	LP Msg/Unformatted Code Field[10:0](3)											LP AN Next Page (0x0000)
9 — 14	9 — 0E	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Reserved Registers (0x0000)
15	0F	1000Base-X FD(3)	1000Base-X HD(3)	1000Base-T FD(3)	1000Base-T HD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Extended Status (0x8000)
16	10	Global Write(1)	TX Amp(2)	CTC Enable(2)	PCS Enable(2)	Swap Enable(2)	Repeat Enable(2)	Shallow Loopbk(2)	Farend Loopback(2)	PRBS Ver Enab(2)	PRBS Enable(2)	Rate Sense EN(2)	SGMII EN(2)	TCLK Sel(2)	Comma Det(2)	Premphasis[1:0](2)		CH Contrl 0 (0x7024)
17	11	Global Write(1)	SyncStat Override(2)	TX PMA Order(2)	RX PMA Order(2)	RSVD(2)	RSVD(2)	RSVD(2)	RX_LOCKREFN(2)	RSVD(2)	Chan Soft Reset	RSVD(2)	TX DP Override(2)	PSC 1GX TX EN(2)	PCS 1GX RX EN(2)	TX Src Centered(2)	RX Src Centered(2)	CH Control 1 (0x3F0F)
18	12	RX CTC Reset(4)	RX CTC Insert(4)	RX CTC Delete(4)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Rx CTC Status (0x0000)
19	13	TX FIFO Rst 1GX(4)	TX FIFO Rst 100FX(4)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	TX FIFO Stat (0x0000)
20	14	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	TP Gen En(2)	TP Ver En(2)	Test Pattern Sel[2:0](2)			Test Pattern Control (0x0000)
21	15	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Test Pat Sync(3)	CRPAT Sync(3)	Test Pattern Sync Status (0x0000)

(1) (1) - Self Clearing, (2) - Read/Write, (3) - Read Only, (4) - Latched High, (5) - Latched Low

Table 5. MDIO Register Map Summary (continued)

DEC	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Name (Hex Reset Val)
22	16	Fixed Test Pattern Counter [15:0](3)																Test Pattern Counter (0xFFFD)
23	17	CRPAT Error Counter1 [31:16] MSB(3)																CRPAT Error Counter1 (0xFFFF)
24	18	CRPAT Error Counter2 [15:0] LSB(3)																CRPAT Error Counter2 (0xFFFD)
25	19	RSVD(3)	SYNC_1GX(5)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Descrambler Status (0x0000)
26	1A	PG1.0 vs PG2.0(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	TX DLL Offset[2:0](2)			RSVD(3)	RX DLL Offset[2:0](2)			RSVD(2)	RSVD(2)	RSVD(3)	RSVD(3)	Scrambler/DLL Control (0x0004)
27	1B	Test MUX Select [3:0](2)				Test MUX En(2)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Test Mode Control (0x0000)
28	1C	TI Test(3)	Actual Rate(3)	Encoder Inval(4)	Decoder Inval(4)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	RSVD(3)	Channel Status (0x4000)
29	1D	PRBS High Speed Test Counter [15:0](3)																PRBS HS Test Counter (0xFFFD)
30	1E	RSVD(3)	RSVD(3)	RX RAMP[1:0](2)	RX Ramp Dir(2)	RX Ramp Dir(2)	Rx Ramp EN(2)	RX Tstclk EN(2)	TX Testclk EN(2)	Clock Watch(2)	RSVD(3)	TCLK Gating(2)	Global Write(2)	DLL Filter(2)	RSVD(3)	Link Time[1:0](2)		Global Test Control (0x008B)
31	1F	PRBS Low Speed Test Counter [15:0](3)																PRBS LS Test Counter (0xFFFD)

(2) (1) - Self Clearing, (2) - Read/Write, (3) - Read Only, (4) - Latched High, (5) - Latched Low

Table 6. Control 1 Register (0x00) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
0.15	1B'0	Reset	Logically OR'd with the RESET pin. 1= Global Resets including FIFO clear 0= Normal operation (default)	Read/Write Self Clearing(1)
0.14	1B'0	Loopback	Logically OR'd with LPBK pin. (Also referred to as deep loopback) 1=enable loopback mode per channel 0=disable loopback mode per channel	Read/Write
0.13	1B'0	Speed Selection(LSB)	This is the least significant bit of the speed selection bits (MSB is 0.6). {0.6,0.13} = 2'b10 1000Base-X Rate {0.6,0.13} = 2'b01 100Base-FX Rate {0.6,0.13} = 2'b00 10 Mbps (SGMII Mode Only) TLK2226 will not allow writes of 2'b11 to {0.6,0.13}, since it is an unsupported rate.	Read/Write
0.12	1B'1	Auto-Negotiation Enable	It allows the device to perform an Auto-Negotiation as described in IEEE802.3 clause 37. 1= Auto-Negotiation enabled (default) 0= Auto-Negotiation disabled	Read/Write
0.11	1B'0	Power Down	Setting this bit high powers down the device, with exception that MDIO interface stays active. All zero's are sent on the receive parallel interface when this bit is set. 1 = Power Down mode is enabled. 0 = Normal operation (default).	Read/Write
0.10	1B'0	Isolate	Setting this bit high isolates the channel from the RGMII interface. Inputs are ignored; Outputs are set to high impedance. 1 = Isolate is enabled 0 = Normal operation (default)	Read/Write
0.9	1B'0	Restart Auto-Negotiation	Restarts an Auto-Negotiation sequence as described in IEEE802.3 clause 37. 1= Restart Auto-Negotiation 0= Normal operation (default)	Read/Write Self Clearing
0.8	1B'1	Duplex Mode	Only Full Duplex is supported. Write is ignored, Read will return a '1'.	Read Only
0.7	1B'0	Collision Test	Not Applicable. Read will return a 0.	Read Only
0.6	1B'1	Speed Selection (MSB)	This is the most significant bit of the speed selection bits (LSB is 0.13). {0.6,0.13} = 2'b10 1000Base-X Rate {0.6,0.13} = 2'b01 100Base-FX Rate {0.6,0.13} = 2'b00 10 Mbps (SGMII Mode Only) TLK2226 will not allow writes of 2'b11 to {0.6,0.13}, since it is an unsupported rate.	Read/Write
0.5:0	6B'00 0000	Reserved	Write is ignored and returns 0 when read.	Read only

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 7. Status 1 Register (0x01) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
1.15	1B'0	1000Base-T4	Read will return 0, writes will be ignored.	Read Only
1.14	1B'1	100Base-X FD	Read will return 1, writes will be ignored	Read Only
1.13	1B'0	100Base-X HD	Read will return 0, writes will be ignored	Read Only
1.12	1B'0	10Mb/s FD	Read will return 0, writes will be ignored	Read Only
1.11	1B'0	10Mb/s HD	Read will return 0, writes will be ignored	Read Only
1.10	1B'0	100Base-T2 FD	Read will return 0, writes will be ignored	Read Only
1.9	1B'0	100Base-T2 HD	Read will return 0, writes will be ignored	Read Only
1.8	1B'1	Extended Status	Read will return 1 indicating extended status information is held in register 0x0F.	Read Only
1.7	1B'0	Reserved	Read will return 0, writes will be ignored	Read Only
1.6	1B'1	MF Prea Supp	Read will return 1 indicating the capability to accept a MDIO command without preceding preamble. Writes will be ignored .	Read Only
1.5	1B'0	AN Complete	Read will return the status if Auto Negotiation is completed. 0 = AN not completed 1 = AN has been completed successful	Read Only
1.4	1B'0	Remote Fault	Not Applicable. Read will return a 0.	Read Only
1.3	1B'1	AN Ability	Read will return 1, indicating, that device is able to perform a Auto Negotiation, writes will be ignored	Read Only
1.2	1B'0	Link Status	Read will return the Link Status of the selected channel past auto negotiation has completed according to IEEE 802.3z clause 37 in 1000Base-X mode. Will return the Link Status of the link monitor state machine when in 100Base-FX mode. Note, the link status will always indicate high when in deep loopback or shallow loopback. In remote loopback mode, the bit represents the normal bit function. 1 = Link UP 0 = Link DOWN	Read Only/ Latched Low
1.1	1B'0	Jabber Detect	Read will return 0, writes will be ignored	Read Only
1.0	1B'1	Extended Capability	Read will return 1 indicating extended register capability	Read Only

The identifier code is composed of bits 3-24 of the 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by the IEEE. The 6-bit Manufacturer Model Number is unique to the TLK2226. The Manufacturer Revision Number denotes the current revision of the TLK2226.

Table 8. PHY ID0 Identifier (0x02) Bit Definitions

OUI Address Bits 3–18															
2.15	**2.14**	**2.13**	**2.12**	**2.11**	**2.10**	**2.9**	**2.8**	**2.7**	**2.6**	**2.5**	**2.4**	**2.3**	**2.2**	**2.1**	**2.0**
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9. PHY ID1 Identifier (0x03) Bit Definitions

OUI Address Bits 19-24						Manufacturer Model Number						Manufacturer Revision Number			
3.15	**3.14**	**3.13**	**3.12**	**3.11**	**3.10**	**3.9**	**3.8**	**3.7**	**3.6**	**3.5**	**3.4**	**3.3**	**3.2**	**3.1**	**3.0**
0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0

Table 10. Autonegotiation Advertisement Register (0x04) Bit Definitions(1)

Bit(s)	Default Value	Name	Description	Read/Write
4.15	1B'0	Next Page	Writing a "1" will signal the link partner that a next page of information is available to be sent after the base page during autonegotiation. 0 = normal operation. See IEEE 802.3 clause 37. Section 37.2.1.7	Read/Write
4.14	1B'0	Reserved	Read will return 0, writes will be ignored	Read Only
4.13:12	2B'00	Remote Fault	00 = No Error (Link OK) 01 = Offline 10 = Link Failure 11 = Auto-Negotiation Error See IEEE 802.3 clause 37. Section 37.2.1.5	Read/Write
4.11:9	3B'000	Reserved	Read will return 0, writes will be ignored	Read Only
4.8:5	4B'0001	Technology Ability Field	0001 = Full Duplex See IEEE 802.3 clause 37. Sections 37.2.1.2 to 37.2.1.4	Read/Write
4.4:0	5B'0_0000	Reserved	Read will return 0, writes will be ignored	Read Only

(1) In SGMII mode, values written to the Autonegotiation Advertisement Register (0x04) will not be used to configure the functions of the local device. Instead, 16'h40001 value is advertised as the ability of the local device per the SGMII specification.

Table 11. AN Link Partner Ability Base Page Register (0x05) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
5.15	1B'0	LP Next Page	A "1" will indicate that the link partner has information for a next page at autonegotiation. 0 = LP has no information for a next page See IEEE 802.3 clause 37. Section 37.2.1.7	Read Only
5.14	1B'0	LP Acknowledge	1 = Indicates that the link partner has successfully received a base or next page 0 = Link partner has not received a base or next page See IEEE 802.3 clause 37. Section 37.2.1.6	Read Only
5.13:12	2B'00	LP Remote Fault	00 = No Error (Link OK) 01 = Offline 10 = Link Failure 11 = Auto-Negotiation Error See IEEE 802.3 clause 37. Section 37.2.1.5	Read Only
5.11:9	3B'000	Reserved	Reading these three bits will reflect the Base page ability bits sent by the link partner through rx_config.	Read Only
5.8:5	4B'0001	Link Partner Technology Ability Field	0001 = Full Duplex See IEEE 802.3 clause 37. Sections 37.2.1.2 to 37.2.1.4	Read Only
5.4:0	5B'0_0000	Reserved	Reading these five bits will reflect the Base page ability bits sent by the link partner through rx_config.	Read Only

Table 12. AN Expansion Register (0x06) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
6.15:3	13B'0000_0000_0000_0	Reserved	Read will return 0, writes will be ignored	Read Only
6.2	1B'1	Next Page Able	Read will return 1, writes will be ignored	Read Only
6.1	1B'0	Page Received	0 = no new page was received 1 = a new page has been received	Read Only/ Latched High
6:0	1B'0	Reserved	Read will return 0, writes will be ignored	Read Only

Table 13. AN Next Page Transmit Register (0x07) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
7.15	1B'0	Next Page	Writing a "1" will signal the link partner that a next page of information is available to be sent after the base page during autonegotiation. See IEEE 802.3 clause 37. Section 37.2.1.7	Read/Write
7.14	1B'0	Reserved	Read will return 0, writes will be ignored	Read Only
7.13	1B'1	Msg Page	0 = unformatted page 1 = message page	Read/Write
7.12	1B'0	Acknowledge 2	0 = cannot comply with message 1 = will comply with message	Read/Write
7.11	1B'0	NP Toggle	0 = prev. value of transmitted link code words equals 1'b1 1 = prev. value of transmitted link code words equals 1'b0	Read Only
7.10:0	11B'000_0000_0001	Msg/Unformated Code Field	See IEEE 802.3 annex 28C for details	Read/Write

Table 14. AN Link Partner Ability Next Page Register (0x08) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
8.15	1B'0	LP Next Page	A "1" will indicate that the link partner has information for a next page at autonegotiation. 0 = LP has no information for a next page See IEEE 802.3 clause 37. Section 37.2.1.7	Read Only
8.14	1B'0	Reserved	Reserved. Ignore on read.	Read Only
8.13	1B'0	LP Msg Page	0 = unformatted page 1 = message page	Read Only
8.12	1B'0	LP Acknowledge 2	0 = cannot comply with message 1 = will comply with message	Read Only
8.11	1B'0	LP Toggle	0 = prev. value of transmitted link code words equals 1'b1 1 = prev. value of transmitted link code words equals 1'b0	Read Only
8.10:0	11B'000_0000_0000	LP Msg/Unformated Code Field	See IEEE 802.3 annex 28C for details	Read Only

Table 15. Reserved Registers (0x09…0x0E) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
9.15:0… 14.15:0	16B'0000_0000_0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only

Table 16. Extended Status Register (0x0F) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
15.15	1B'1	1000Base-X FD	Always reads 1, indicating device supports Full Duplex mode.	Read Only
15.14	1B'0	1000Base-X HD	Read will return 0, writes will be ignored.	Read Only
15.13	1B'0	1000Base-T FD	Read will return 0, writes will be ignored.	Read Only
15.12	1B'0	1000Base-T HD	Read will return 0, writes will be ignored.	Read Only
15.11:0	12B'0000_0000_0000	Reserved	Read will return 0, writes will be ignored.	Read Only

Table 17. (Vendor Specific) CH Control Register 0 (0x10) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
16.15	1B'0	Global write	When written as 1 the settings in 16.14:0 will affect all channels of one device simultaneously. When written as 0 the settings in 16.14:0 are only valid for the addressed channel. This value always reads zero.	Read/Write Self Clearing
16.14	1B'1	TX Amplitude Control	1 = Transmitter Amplitude is at full value. 0 = Transmitter Amplitude is half value. This should be set to 0 during SGMII mode.	Read/Write
16.13	1B'1	CTC Enable	Logically AND'd with the CTC_EN pin. 0 = clock tolerance compensation is disabled 1 = CTC is enabled (default)	Read/Write
16.12	1B'1	PCS Enable	Logically AND'd with the CODE pin. 0 = PCS functions are disabled 1 = PCS functions are enabled (default)	Read/Write
16.11	1B'0	Swap Enable	When logic high the parallel interfaces of two adjacent channels are swapped. For example data coming in at TDA will be sent out at TXB. Data coming in at RXA will be sent out at RDB in this example. This bit is always valid for a channel pair like AB, CD, or EF. Logically OR'd with the SWAP pin. 0 = Swap function disabled. 1 = Swap function enabled.	Read/Write
16.10	1B'0	Repeat Enable	When logic high the channel will ignore the data presented to its transmit parallel interface but will send the data coming in at the serial receive interface of its partner channel. The partner channel is the other one of the pair AB, CD, or EF. Logically OR'd with REPEATA or REPEATB pins.	Read/Write
16.9	1B'0	Serial Shallow Loopback	Applicable only when standard loopback bit (Register 0.14) is low and the external loopback pin (LPBK) is low. When asserted high the data presented at the parallel transmit interface is looped back to the parallel receive interface of the same channel. 0 = Serial shallow loopback is disabled. 1 = Serial shallow loopback is enabled.	Read/Write
16.8	1B'0	Farend Loopback	When asserted high the data presented at the serial receive interface is looped back to the serial transmit interface of the same channel via the deserializer, the serializer and if enabled the PCS function. If 1GX PCS is not enabled (i.e. RTBI or 100Base-FX modes), the incoming data rate must be frequency locked (ppm 0) with REFCLK. Also referred to as remote loopback. 0 = Farend Loopback is disabled. 1= Farend loopback is enabled.	Read/Write
16.7	1B'0	PRBS Verifier Enable	A logic 1 enables the PRBS verifier in the receive data path. Logically OR'd with the PRBSEN pin.	Read/Write
16.6	1B'0	PRBS Enable	A logic 1 enables the PRBS generator in the transmit data path. Logically OR'd with the PRBSEN pin.	Read/Write
16.5	1B'1	Rate Sense Enable	A logic 1 will enable auto rate sensing between 1.25 Gbps data and 125 Mbps data.	Read/Write
16.4	SGMII Pin Value at Rising Edge of RESET.	SGMII Mode Enable	When set to 1, enables SGMII mode. When set to 0 (default), disables SGMII mode. When set to 1, the standard based bits 0.6 and 0.13 directly determine the parallel data rate of operation, according to the "Per Channel Rate Determination" table.	Read/Write
16.3	1B'0	TCLK Select	Logically OR'd with the TCLKSEL pin. 0 = parallel transmit data is latched synchronous to TCLKC (default) 1 = parallel transmit data is latched synchronous to TCLK of the according channel.	Read/Write
16.2	1B'1	Comma Detect	A logic 1 enables the comma detection in the serial receive circuit.	Read/Write

Table 17. (Vendor Specific) CH Control Register 0 (0x10) Bit Definitions (continued)

Bit(s)	Default Value	Name	Description	Read/Write
			When set to logic 0 the byte boundary of the received data stream is ignored. Logically AND'd with the SYNCEN pin.	
16.1:0	2B'00	Preemp	Pre-emphasis control 2B'00 = no Pre-emphasis (default) 2B'01 = low Pre-emphasis 2B'10 = medium Pre-emphasis 2B'11 = high Pre-emphasis	Read/Write

Table 18. (Vendor Specific) CH Control 1 Register (0x11) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
17.15	1B'0	Global write	When written as 1 the settings in 17.14:0 will affect all channels of one device simultaneously. When written as 0 the settings in 17.14:0 are only valid for the addressed channel. This bit always reads zero.	Read/Write Self Clearing
17.14	1B'0	Sync Status Override	1 = Causes an override of the sync state 1000Base-X synchronization state machine to reflect a "1" in the sync_1GX (25.14) bit. 0 = Original (normal operation) sync_1GX value is represented in bit 25.14. (Default)	Read/Write
17.13	1'B1	TX PMA Bit Order	When asserted, allows the ten bits of data given to the parallel side of the SERDES TX macro to be flipped. This is normally set since the SERDES transmits MSB first, and the 1000Base-X standard requires LSB to be transmitted first. For standard based operation, the customer may leave this bit alone.	Read/Write
17.12	1'B1	RX PMA Bit Order	When asserted, allows the ten bits of data received from the parallel side of the SERDES RX macro to be flipped. This is normally set since the SERDES receives MSB first, and the 1000Base-X standard requires LSB to be received first. For standard based operation, the customer may leave this bit alone.	Read/Write
17.11:9	3B'111	Reserved	Reserved for TI test.	Read/Write
17.8	1B'1	RX_LOCKREFN	1 = Enables clock recovery loop to lock onto incoming data rate. 0 = Clock recovery loop ignores incoming data rate and locks to REFCLK.	Read/Write
17.7	1B'0	Reserved	Reserved for TI test.	Read/Write
17.6	1'B0	Channel Soft Reset	1 = Resets channel logic excluding MDIO registers.	Read/Write Self-Clearing
17.5	1B'0	Reserved	Reserved for TI test.	Read Only
17.4	1B'0	TX Datapath Override	1 = Allows Transmit Datapath to Send Normal Data Traffic Regardless of Errors in the Receive Datapath (In 1000Base-X Mode, Auto-Negotiation should also be disabled). 0 = Normal Chip Operation (Standard Based)	Read/Write
17.3	1'B1	PCS 1GX TX Enable	1 = Enables 1000Base-X PCS TX Function 0 = Disables 1000Base-X PCS TX Function	Read/Write
17.2	1'B1	PCS 1GX Rx Enable	1 = Enables 1000Base-X PCS Rx Function 0 = Disables 1000Base-X PCS Rx Function	Read/Write
17.1	1B'1	TX Source Centered	0 = Source synchronous timing on transmit parallel interface. Data is latched 2ns after clock edge. 1 = Source centered timing on transmit parallel interface. Data is latched at clock edge.	Read/Write
17.0	1B'1	RX Source Centered	0 = Source synchronous timing on receive parallel interface. Data changes at clock edge. 1 = Source centered timing on receive parallel interface. Data changes 2ns after clock edge.	Read/Write

Table 19. (Vendor Specific) RX CTC FIFO Status (0x12) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
18.15	1B'0	RX_CTC_Reset	When high indicates overflow or underflow has occurred in CTC FIFO and FIFO has been reset.	Read Only/ Latched High
18.14	1B'0	RX_CTC_Insert	When high indicates RX CTC has inserted at least one ordered set.	Read Only/ Latched High
18.13	1B'0	RX_CTC_Delete	When high indicates RX CTC has deleted at least one ordered set.	Read Only/ Latched High
18.12:0	13B'0_0000_0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only

Table 20. (Vendor Specific) TX FIFO Status (0x13) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
19.15	1B'0	TX_FIFO_Reset_1Gx	When high indicates collision has occurred in TX FIFO and the FIFO is reset in 1gx mode.	Read Only/ Latched High
19.14	1B'0	TX_FIFO_Reset_100Fx	When high indicates collision has occurred in TX FIFO and the FIFO is reset in 100fx mode.	Read Only/ Latched High
19.13:0	14B'00_0000_0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only

Table 21. Vendor Specific) Test Pattern Control Registers (0x14) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
20.15:5	11B'000_ 0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only
20.4	1B'0	Test Pattern Generator Enable	When high activates the generator selected by bits 20.2:0.	Read/Write
20.3	1B'0	Test Pattern Verifier Enable	When high activates the verifier selected by bits 20.2:0.	Read/Write
20.2:0	2B'00	Pattern Select	Test Pattern Selection 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long 100 = CRPAT Short Others = Reserved	Read/Write

Table 22. (Vendor Specific) Test Pattern Sync Status (0x15) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
21.15:2	14B'00_0000_0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only
21.1	B'0	Test Pattern Sync	When high indicates alignment has been determined and a correct pattern has been received for fixed test patterns.	Read Only
21.0	1B'0	CRPAT Sync	When high indicates alignment has been determined and a correct pattern has been received for continuous test patterns.	Read Only

Table 23. (Vendor Specific) Test Pattern Counter (0x16) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
22.15:0	16B'1111_1111_1111_1101	Fixed Test Pattern Error Counter	This counter reflects error count for high, Mixed, and Low Frequency test patterns. Counter increments for each received character that has an error. Counter clears upon read.	Read Only

Table 24. (Vendor Specific) CRPAT Error Counter1 (0x17) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
23.15:0	16B'1111_1111_1111_1111	Reserved	MSB of CRPAT Error Counter. This counter reflects errors for CRPAT Test. Counter increments by one for each received character that has an error. Counter clears upon read.	Read Only

Table 25. (Vendor Specific) CRPAT Error Counter2 (0x18) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
24.15:0	16B'1111_1111_1111_1101	Reserved	LSB of CRPAT Error Counter. This counter reflects errors for CRPAT Test. Counter increments by one for each received character that has an error. Counter clears upon read.	Read Only Note: Register 23 has to be read first.

Table 26. (Vendor Specific) Descrambler Status (0x19) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
25.15	1B'0	Reserved	Read will return 0, writes will be ignored.	Read Only
25.14	1'B0	Sync_1GX	When low, indicates PCS synchronization has lost sync. When high, indicates PCS synchronization is currently in sync.	Read Only Latched Low
25.13:0	14B'000_0000_0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only

Table 27. (Vendor Specific) Scrambler/DLL control (0x1A) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
26.15	PG1.0 : 1'b1 PG2.0 : 1'b0	PG1.0 –vs- PG2.0	PG1.0 : Read/Write Default to One PG2.0 : Read Only, Read will return 0	PG1.0 : Read/Write PG2.0: Read Only
26.14:11	4B'0000	Reserved	Read will return 0, writes will be ignored	Read Only
26.10:8	3B'000	TX DLL Offset[2:0]	Unit delay offset setting for TX DLL. If [2] (MSB) is 1'b1, then delay can be increased by [1:0] (LSB's) unit delays. If [2] (MSB) is 1'b0, then delay can be decreased by [1:0] (LSB's) unit delays.	Read/Write
26.7	1B'0	Reserved	Read will return 0, writes will be ignored	Read Only
26.6:4	3B'000	RX DLL Offset[2:0]	Unit delay offset setting for Rx DLL. If [2] (MSB) is 1'b1, then delay can be increased by [1:0] (LSB's) unit delays. If [2] (MSB) is 1'b0, then delay can be decreased by [1:0] (LSB's) unit delays.	Read/Write
26.3:0	4B'0100	Reserved	Read will return 0, writes will be ignored	Read Only

Table 28. (Vendor Specific) Reserved Test Mode Control Registers (0x1B) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
27.15.12	4'B1111	Test MUX Select	Must be set to 4'B1010 to allow PRBS_PASS and PRBS_SYNC to be output on the partner RD[1] and RD[2] parallel interface pins.	Read/Write
27.11	1'b0	Test MUX Enable	When asserted, allows the test MUX data to be driven onto the parallel interface (data from the partner channel).	Read/Write
27.10:0	11B'000_0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only

Table 29. (Vendor Specific) Reserved Channel Status Registers (0x1C) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
28.15	1B'0	TI Test	Reserved for TI test	Read Only
28.14	1'B1	Actual Channel Rate	When high, indicates the serial side of the channel is currently operating in 1.25 Gbps mode. When low, indicates the channel is currently operating in 125 Mbps mode.	Read Only
28.13	1'B0	Encoder Invalid Code Word	When high, indicates that the 1000Base-X encoder received an invalid control word.	Read Only Latched High
28.12	1'B0	Decoder Invalid Code Word	When high, indicates that the 1000Base-X decoder received an invalid code word.	Read Only Latched High
28.11:0	12B'0000_0000_0000	Reserved	Read will return 0, writes will be ignored	Read Only

Table 30. (Vendor Specific) PRBS High Speed Test Counter (0x1D) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
29.15:0	16B'1111_1111_1111_1101	PRBS High Speed Test Counter	This counter reflects errors for high speed PRBS test pattern (1000Base-X). Counter increments by one for each received character that has error. This counter saturates at 16'hffff. When read, it resets to zero and continues to count.	Read Only

Table 31. (Vendor Specific) Global Test Control Register (0x1E) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
30.15:14	2B'00	Reserved	Read will return 0, writes will be ignored	Read Only
30.13:12	2'B00	RX Ramp Rate	Ramp Rate control during Ramp test mode This bit value can be changed per serdes macro by addressing to the lead channel of a particular macro (Channel A or C or E)	Read/Write
30.11	2'b0	RX Ramp Direction	Ramp Rate direction during Ramp test mode This bit value can be changed per serdes macro by addressing to the lead channel of a particular macro (Channel A or C or E)	Read/Write
30.10	1B'0	Rx Ramp Enable	When set enables Ramp test mode in serdes macro This bit value can be changed per serdes macro by addressing to the lead channel of a particular macro (Channel A or C or E)	Read/Write
30.9	1B'0	RX Testclock Enable	When set enables test clock in all receive SERDES macros This bit value can be changed by addressing to any channel.	Read/Write
30.8	1B'0	TX Testclock Enable	When set enables test clock in all transmit SERDES macros This bit value can be changed by addressing to any channel.	Read/Write
30.7	1'B1	Clock Watch	When set enables Reference Clock Watchdog function This bit value can be changed by addressing to any channel.	Read/Write
30.6	1B'0	Reserved	Read will return 0, writes will be ignored	Read Only
30.5	1'B0	TCLK Gating	For TI Test Purposes Only This bit value can be changed per serdes macro by addressing to the lead channel of a particular macro (Channel A or C or E)	Read/Write
30.4	1'B0	Global Write	If set all write accesses to MDIO Control (R/W) registers between 0x00 to 0x0F and registers 0x14, 0x1A, and 0x1E affect all channels in the device. This bit value can be changed by addressing to any channel.	Read/Write
30.3	1B'1	DLL Filter	For TI test purposes This bit value can be changed by addressing to any channel.	Read/Write
30.2	1B'0	Reserved	Read will return 0, writes will be ignored	Read Only
30.1:0	2B'11	Link Time	Sets the link time used for 1000Base-X autonegotiation. Be aware: only default setting complies with IEEE802.3. 2B'00 = 500 ns 2B'01 = 10 µs 2B'10 = 1.6 ms 2B'11 = 10 ms (default) In 100Base-FX mode, these bits are also used. They are used to set the Far End Fault Link Monitor period. Only the default setting will comply with the IEEE802.3 standard. 2B'00 = 120 ns 2B'01 = 131 µs 2B'10 = 262 µs 2B'11 = 524 µs (default) This bit value can be changed per channel.	Read/Write

Table 32. (Vendor Specific) PRBS Low Speed Test Counter (0x1F) Bit Definitions

Bit(s)	Default Value	Name	Description	Read/Write
31.15:0	16B'1111_1111_ 1111_1101	PRBS Low Speed Test Counter	This counter reflects errors for low speed PRBS test pattern (100Base-FX). Counter increments by one for each received character that has error. This counter saturates at 16'hffff. When read, it resets to zero and continues to count.	Read Only

JTAG Interface

The TLK2226 provides the full five pin JTAG interface as defined in IEEE 1149.1 to support manufacturing test.

SOFTWARE PROCEDURES

The following are per channel sequences.

- 1000Base-X Transceiver Mode (PCS On/CTC on)
    1. write 0x8000 to location 0x00
    2. verify actual speed detected bit (28.14). If wrong, manually provision.
    3. poll bit 2 set at location 0x01 (link status)
    4. channel is carrying traffic
- 1000Base-X Transceiver Mode (PCS On/CTC Off)
    1. write 0x8000 to location 0x00
    2. write 0x1027 to location 0x10
    3. verify actual speed detected bit (28.14). If wrong, manually provision.
    4. poll bit 2 set at location 0x01 (link status)
    5. channel is carrying traffic
- 1000Base-X Transceiver Mode (PCS Off)
    1. write 0x8000 to location 0x00
    2. write 0x0027 to location 0x10
    3. verify actual speed detected bit (28.14). If wrong, manually provision.
    4. poll bit 2 set at location 0x01 (link status)
    5. channel is carrying traffic
- 100Base-FX Transceiver Mode
    1. write 0x8000 to location 0x00
    2. verify actual speed detected bit (28.14). If wrong, manually provision.
    3. poll bit 2 set at location 0x01 (link status)
    4. channel is carrying traffic
- 1000Base-X Port Swap (PCS On/CTC On)
    1. write 0x8000 to location 0x00
    2. write 0x3827 to location 0x10
    3. verify actual speed detected bit (28.14). If wrong, manually provision
    4. poll bit 2 set at location 0x01 (link status)
    5. channel is carrying traffic
- 1000Base-X Port Swap (PCS On/CTC Off)
    1. write 0x8000 to location 0x00
    2. write 0x1827 to location 0x10
    3. verify actual speed detected bit (28.14). If wrong, manually provision.
    4. poll bit 2 set at location 0x01 (link status)
    5. channel is carrying traffic
- 1000Base-X Port Swap (PCS Off)
    1. write 0x8000 to location 0x00

2. write 0x0827 to location 0x10
3. verify actual speed detected bit (28.14). If wrong, manually provision.
4. poll bit 2 set at location 0x01 (link status)
5. channel is carrying traffic

- 1000Base-X Retiming Repeater (PCS On/CTC On)
  1. write 0x8000 to location 0x00
  2. write 0x3427 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Non-Retiming Repeater (PCS On/CTC Off)
  1. write 0x8000 to location 0x00
  2. write 0x1427 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Non-Retiming Repeater (PCS Off)
  1. write 0x8000 to location 0x00
  2. write 0x0427 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Remote Loopback (PCS On/CTC On)
  1. write 0x8000 to location 0x00
  2. write 0x3127 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Remote Loopback (PCS On/CTC Off)
  1. write 0x8000 to location 0x00
  2. write 0x1127 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Remote Loopback (PCS Off)
  1. write 0x8000 to location 0x00
  2. write 0x0127 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 100Base-FX Remote Loopback
  1. write 0x8000 to location 0x00
  2. write 0x3127 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Local Loopback (Shallow) (PCS On/CTC On)

1. write 0x8000 to location 0x00
2. write 0x3227 to location 0x10
3. verify actual speed detected bit (28.14). If wrong, manually provision.
4. poll bit 2 set at location 0x01 (link status)
5. channel is carrying traffic

- 1000Base-X Local Loopback (Shallow) (PCS On/CTC Off)
  1. write 0x8000 to location 0x00
  2. write 0x1227 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Local Loopback (Shallow) (PCS Off)
  1. write 0x8000 to location 0x00
  2. write 0x0227 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 100Base-FX Local Loopback (Shallow)
  1. write 0x8000 to location 0x00
  2. write 0x3227 to location 0x10
  3. verify actual speed detected bit (28.14). If wrong, manually provision.
  4. poll bit 2 set at location 0x01 (link status)
  5. channel is carrying traffic
- 1000Base-X Local Loopback (Deep) (PCS On/CTC On)
  1. write 0x8000 to location 0x00
  2. write 0x4000 to location 0x00
  3. write 0x3027 to location 0x10
  4. verify actual speed detected bit (28.14). If wrong, manually provision.
  5. poll bit 2 set at location 0x01 (link status)
  6. channel is carrying traffic
- 1000Base-X Local Loopback (Deep) (PCS On/CTC Off)
  1. write 0x8000 to location 0x00
  2. write 0x4000 to location 0x00
  3. write 0x1027 to location 0x10
  4. verify actual speed detected bit (28.14). If wrong, manually provision.
  5. poll bit 2 set at location 0x01 (link status)
  6. channel is carrying traffic
- 1000Base-X Local Loopback (Deep) (PCS Off)
  1. write 0x8000 to location 0x00
  2. write 0x4000 to location 0x00
  3. write 0x0027 to location 0x10
  4. verify actual speed detected bit (28.14). If wrong, manually provision
  5. poll bit 2 set at location 0x01 (link status)
  6. channel is carrying traffic
- 100Base-FX Local Loopback (Deep)
  1. write 0x8000 to location 0x00
  2. write 0x4000 to location 0x00

3. verify actual speed detected bit (28.14). If wrong, manually provision.
4. poll bit 2 set at location 0x01 (link status)
5. channel is carrying traffic

JITTER TEST PATTERN GENERATION AND VERIFICATION

Use one of the following procedures to generate and verify the respective jitter test pattern:

- **High/Mixed/Low Frequency Test Pattern:**
  - Issue a hard or soft reset
  - Write a zero to 0.12 (disable auto-negotiation).
  - Write a zero to 16.5 (disable auto rate sense enable).
  - Write a one to 0.6 (1000Base-X rate).
  - Write a zero to 0.13 (1000Base-X rate).
  - Write “0” to the PCS 1Gx Rx Enable bit (bit 2) of the Channel Control_1 register (Reg 17) to disable decoder/ PCS 1Gx RX function.
  - Write “0” to Comma Detect bit (bit 2) of the Channel Control_0 register (Reg 16) to disable comma detect function.
  - Write “000” to the Pattern_select(bit 2:0) field of the Test Pattern Control register (Reg 20) to select high frequency test pattern, or “001” to select the low frequency test pattern, or “010” to select the mixed frequency test pattern. .
  - Write “1” to the Generator Enable (20.4).
  - Read the test pattern error counter register(Reg 22) for the channel to clear the counters.
  - Write “1” to the Verifier Enable (20.3)
  - In order for the Test Pattern Verifier to start checking the test pattern, it has to achieve sync to the test pattern. To make sure that the test pattern checking has started, read bit 1(Test pattern sync) of Test pattern Sync Status (Reg 21) register. Make sure that the Fixed Test Pattern Sync bit is HIGH for the corresponding lane. If the sync status is not high, this indicates that the verifier never achieved sync, which may indicate a more severe link problem.
  - At this point the pattern verification is in progress
  - Errors are reported in the error counter at Test Pattern Counter Register (Reg 22).
  - Reading the counters has no effect on the test except clearing the counters, i.e. the verification of the pattern continues until the test pattern enable bit(bit 4) of the Test Pattern Control register(Reg 20) is cleared.
- **Long/Short Continuous Random Test Pattern (Long/Short CRPAT**
  - Issue a hard or soft reset
  - Write a zero to 0.12 (disable auto-negotiation).
  - Write a zero to 16.5 (disable auto rate sense enable).
  - Write a one to 0.6 (1000Base-X rate).
  - Write a zero to 0.13 (1000Base-X rate).
  - Write “011” to the Pattern_select(bit 2:0) field of the Test Pattern Control register (Reg 20) to select CRPAT Long test pattern, or “100” to select the CRPAT Short test pattern.
  - Write “1” to the Generator Enable (20.4).
  - Read the CRPAT Error Counter_1 register and CRPAT Error Counter_2 register (Reg 23 & Reg 24) to clear
  - Write “1” to the Verifier Enable (20.3).
  - In order for the Test Pattern Verifier to start checking the test pattern, it has to receive the Preamble /SFD that is sent at every packet from the test pattern generator. To make sure that the test pattern checking has started, read bit 0 of the Test Pattern Sync Status Register(Reg 21). Make sure that the CRPAT Sync bit is HIGH. If the sync status is not high, this indicates that the verifier never received the Preamble, which may indicate a more severe link problem.
  - At this point the pattern verification is in progress. Perform the test as long as desired.
  - Read the MSB of the error counter by reading CRPAT Error Counter_1 (Reg 23), then read the LSB of the error counter at CRPAT Error Counter_2 (Reg 24). If user reads register 24 without reading register 23 first, the count value read through 24 may not be correct.
  - If another test is to be performed go to the first step

PRBS GENERATION AND VERIFICATION PROCEDURE

- Issue a hard or soft reset
- Write a zero to 0.12 (disable auto-negotiation).
- Write a zero to 16.5 (disable auto rate sense enable).
- Write a one to 0.6 (1000Base-X rate) or zero to 0.6 (100Base-FX rate).
- Write a zero to 0.13 (1000Base-X rate) or one to 0.13 (100Base-FX rate).
- Write “0” to the PCS Enable bit (bit 12) of the Channel Control_0 register (Reg 16) to disable PCS function.
- Write “0” to Comma Detect bit (bit 2) of the Channel Control_0 register (Reg 16) to disable comma detect function.
- Write “1” to the PRBS Generator Enable (bit 6) field of the Channel Control_0 register (Reg 16) to enable PRBS generator.
- For 1000Base-X mode, Read the PRBS high speed test error counter (Reg 29) to clear the counter
- For 100fx mode, Read the PRBS low speed test error counter (Reg 31) to clear the counter
- Write “1” to the PRBS Verifier Enable (bit 7) fields of the Channel Control_0 register (Reg 16) to enable PRBS verifier
- At this point the pattern verification is in progress
- Errors are reported in PRBS high speed test error counter (Reg 29) for 1000Base-X and PRBS low speed test error counter (Reg 31) for 100fx mode.
- Reading the counters has no effect on the test except clearing the counters, i.e. the verification of the pattern continues until the PRBS Generator/PRBS Verifier Enable (bit 7:6) of the Channel Control_0 register (Reg 16) is cleared

TESTABILITY

Serial Loopback (Shallow and Deep)

The TLK2226 can provide a self-test function by enabling the internal loop-back path for all channels with the assertion of LPBK. The loopback for individual channels can be enabled via the MDIO registers or for all channels through the LPBK pin. The parallel data output can be compared to the parallel input data for that channel to provide functional verification. The external differential output is held in a high-impedance state (pulled to VDDA through 500 Ω) during deep loop-back testing. Loopback for all channels (called deep loopback) may be enabled by assertion of the LPBK pin (putting all channels into deep loopback simultaneously) or setting register bit 0.14 (on an individual channel basis). This causes transmit serial data from a channel to be input on the serial input for that channel, testing the entire path of the serializer/deserializer (except the output driver/receiver).

Shallow loopback may be enabled by setting the shallow loopback register bit 16.9. This will loop the parallel transmit data bus for an individual channel to the parallel receive bus on that channel.

Far-End Loopback

The TLK2226 can provide a self-test function by enabling the internal far end loop-back (also referred to as remote loopback) path for a channel with the assertion of MDIO register bit 16.8. The serial data output can be compared to the serial input data for selected channels to perform functional verification of high speed RX and TX. The parallel input data during far end loopback test are disregarded. The external parallel outputs are optionally in a high-impedance state via MDIO control bit (0.10).

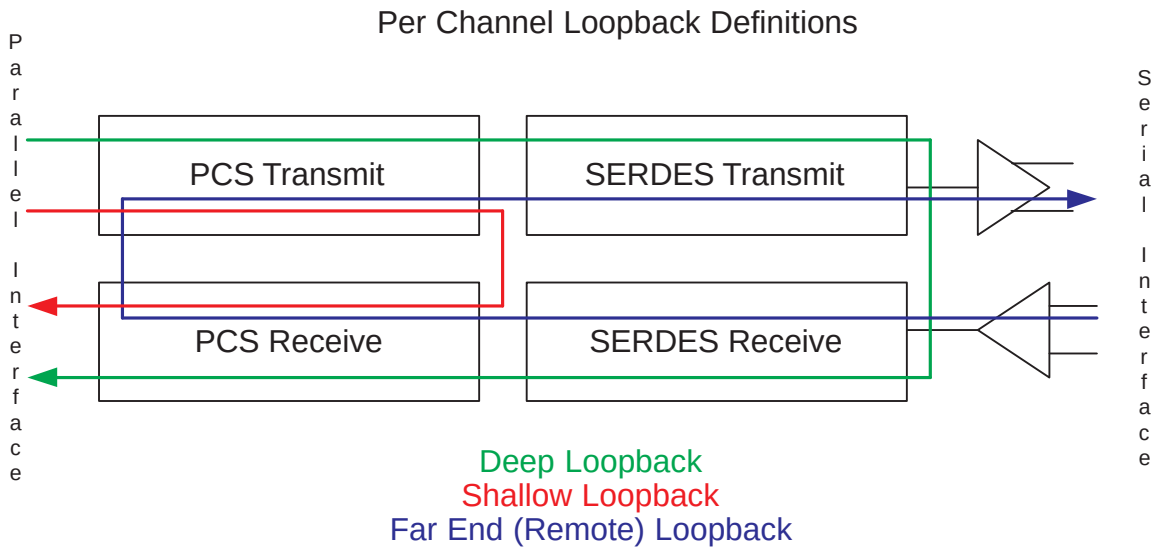


Figure 23. Per Channel Loopback Definitions

Power-On Reset

Upon application of minimum valid power, the TLK2226 generates an internal power-on reset. During the power-on reset the receive data outputs are tri-stated. The length of the power-on reset cycle is dependent upon the power supply's ramp curve. The power-on reset is sourced by the digital core supply voltage VDD.

PRBS generator and comparator

The TLK2226 has a built-in 27-1 PRBS (Pseudo Random Bit Stream) self test function available on each channel. Compared to all 8B/10B data pattern combinations, the PRBS is a worst-case bit pattern. The self-test function is enabled using the PRBSEN pin or setting the PRBS Enable bit in the MDIO registers. When the self-test function is enabled, a PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data on the Transmit Data Bus inputs to the TLK2226 are ignored during the PRBS test mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (Bit Error Rate Tester) or the receiver of another TLK2226 channel.

Setting the PRBSEN pin has the following effect:

A PRBS datastream is generated on the TX ±ports.

The RX ± ports expect PRBS pattern at their inputs and status signals could be monitored on RD bus or MDIO. While the PRBS test function is in operation, a real-time signal PRBS_PASS is available on RDx[1] or RDx[2] of partnering channel depends on whether the rate is 1.25 Gbps or 125Mbps; other signals on the RDx[4:0] busses have no meaning during PRBS testing. Alternately, the result can be read from the MDIO vendor specific register 29 and 31. Register 29 is the error counter for high speed(1.25Gbps) PRBS Verifier. Register 31 is the error counter for low speed(125Mbps) PRBS. These are counters that increment by one for each received character that has error. Reading the MDIO register clear the counter information in the MDIO.

The PRBS test function can also be activated through MDIO by activating the PRBS_EN Register 16.7:6.

The PRBS function can be used in conjunction with the serial loopback function. This can be done by asserting the PRBS generators via the PRBSEN pin or MDIO register 16.7:6, and assertion of the LPBK pin or loopback control provided via MDIO register 0.14. The result from PRBS verification at the RX ports of the device can be read from the MDIO registers 29 and 31.

Simultaneous assertion of the PRBS_EN and PRBS_VE register bits in MDIO register 16.7:6, and the serial loopback enable, puts the device in a test mode which provides PRBS generation and verification at the local transmitter and receiver internal to the TLK2226

POWER SUPPLY SEQUENCING

TI ASIC I/O design allows either the core supply (V_{DD}) or the I/O supply (V_{DDS}) to be powered up for an indefinite period of time while the other power supply is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions
- All warnings about exposure to maximum rated and recommended conditions, particularly junction temperature. These apply to power transitions as well as normal operation.
- Guidelines for the number and placement of I/O pins
- No bus contention

Bus contention while V_{DDS} is powered up must be limited to 100 hours over the projected lifetime of the device.

Bus contention while V_{DDS} is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

Table 33. Device Thermal Characteristics

Package Thermal Theta Values		
	Airflow (m/s)	Value
θ_{JA}	0	32.7 (C/W)
	1	28.7 (C/W)
	2.5	27.5 (C/W)
θ_{JB}	19.8 (C/W)	
θ_{JC}	14.8 (C/W)	
Device Maximum Characteristics		
Maximum Junction Temperature	115°C	
Maximum Power Dissipation	1.5 Watts	

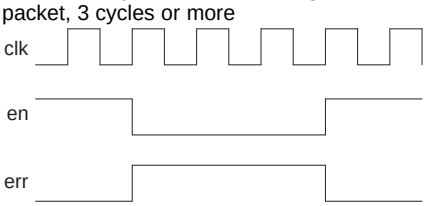
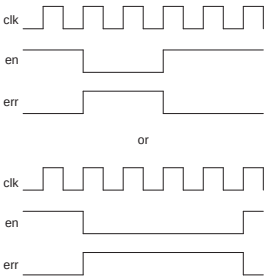
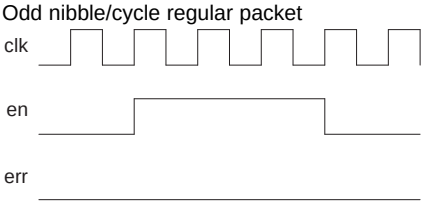
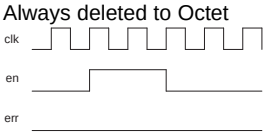
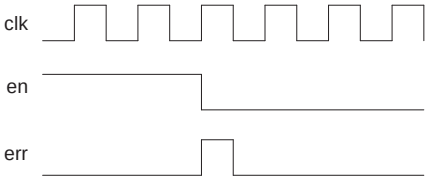
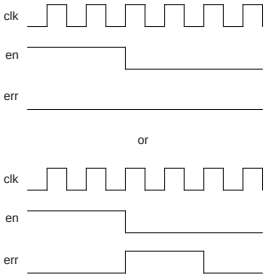
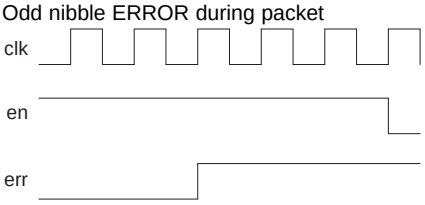
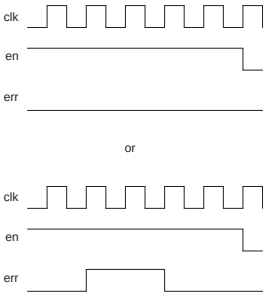
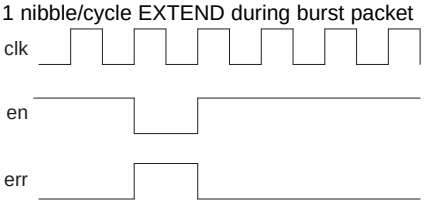
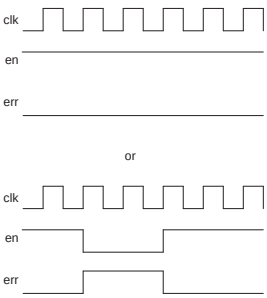
APPENDIX A

Known issues with the TLK2226 device:

1. ENABLE Input Signal – ENABLE signal must be held high during JTAG operation. Failure to do so will cause data compare errors on the parallel side data path input signals. A possible solution is that a pull-up resistor exclusively drives the ENABLE signal on the customer application board. Alternatively, the customer must guarantee ENABLE is asserted high during JTAG operation.

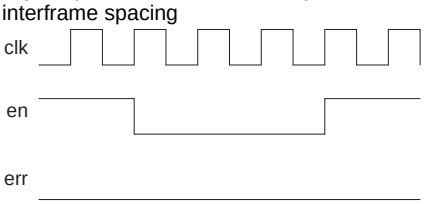
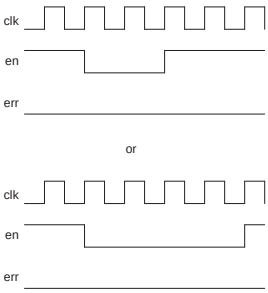
APPENDIX B – SGMII 10/100 ODD NIBBLE PACKET/IPG HANDLING

SGMII 10/100 Nibble Processing Assumptions

Case	Input (from Mac)	Output(Rate adaptation)	Assumptions
1	Odd nibble/cycle EXTEND during burst packet, 3 cycles or more 		Odd nibble CARRIER EXTEND (3 or more) possible during burst. We will stuff or delete to octet boundary for PCS encoding. Packets are not corrupted. (1)
2	Odd nibble/cycle regular packet 	Always deleted to Octet 	Packet ends on non octet boundary. We drop the nibble to form last octet for PCS encoding. (non valid packet anyway)
3	Odd nibble EOP EXTEND 		Odd nibble EOP EXTEND. We do not know if this is valid thus output to the PCS will be either NO EXTEND or EXTEND. (1)
4	Odd nibble ERROR during packet 		TX_ERR asserted only during 1 nibble. We do not know if this is a real error, thus output to PCS encoding will either have an error indicated on a byte(2 cycles) or no error.
5	1 nibble/cycle EXTEND during burst packet 		End of Packet extend only 1 nibble during burst. Output to PCS will either be a corrupted burst with nibble extended or joined into 1 big corrupted packet. We cannot always extend as there is no CTC on the TX side. Following packets will not be affected

(1) Note that in the case of an odd EXTEND and if it is stuffed, the PCS TX state machine will embed an |V| (error). The last nibble alone does not contain enough bits to build a meaningful encoding byte (8'h0F). The packets themselves are not corrupted.

APPENDIX B – SGMII 10/100 Odd Nibble Packet/IPG Handling (continued)

Case	Input (from Mac)	Output(Rate adaptation)	Assumptions
6	regular packet with odd nibble/cycle interframe spacing 		Interframe gap will be padded or shortened by 1 nibble to meet octet boundary requirements. Packets will not be corrupted unless interframe gap falls below 3 nibbles.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK2226GEA	ACTIVE	BGA	GEA	196	126	Non-RoHS & Green	SNPB	Level-3-220C-168 HR	0 to 70	TLK2226GEA	Samples
TLK2226ZEA	ACTIVE	BGA	ZEA	196	126	RoHS & Green	SNAGCU	Level-3-260C-168 HR		TLK2226ZEA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

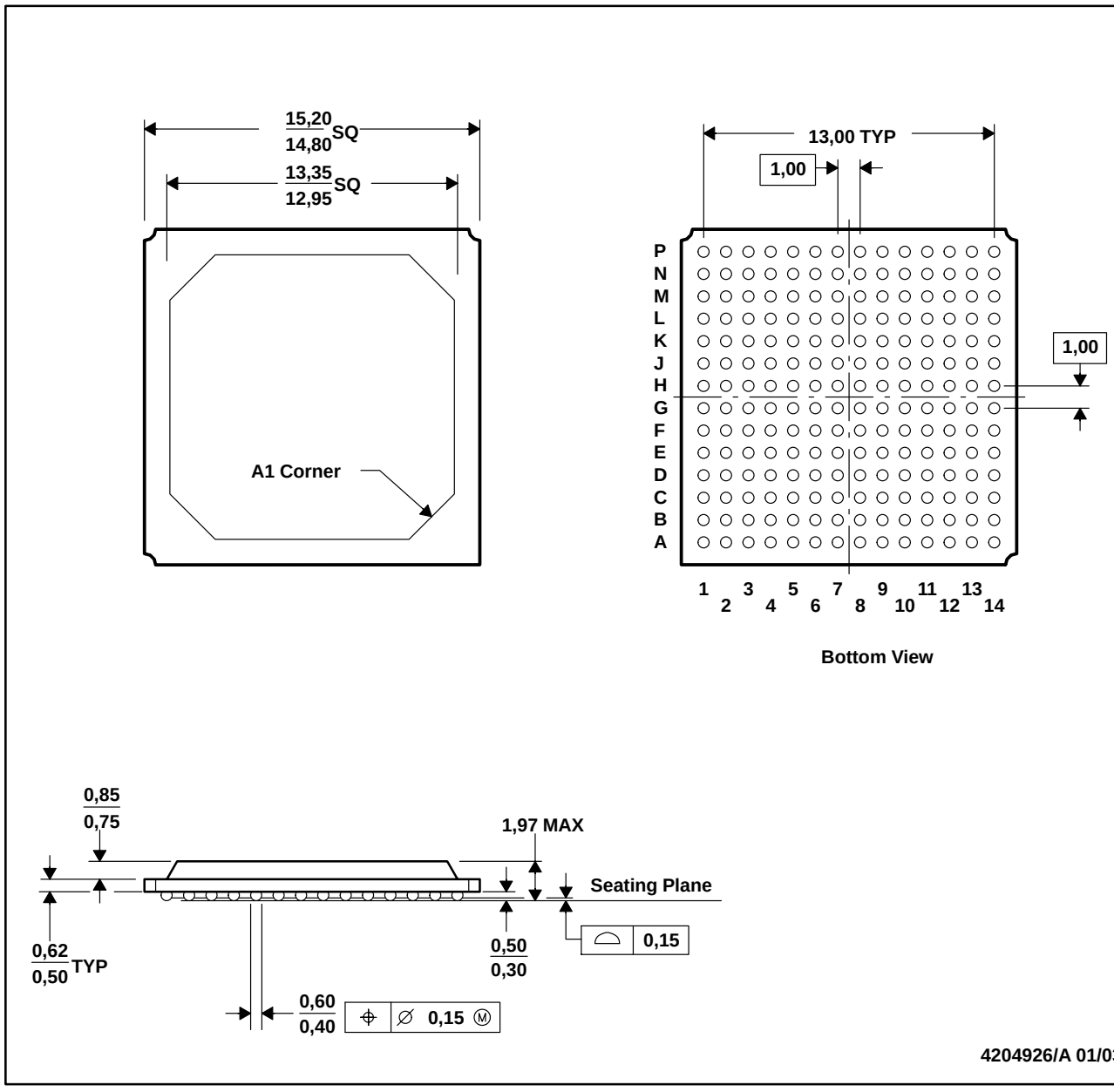
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GEA (S-PBGA-N196) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-151

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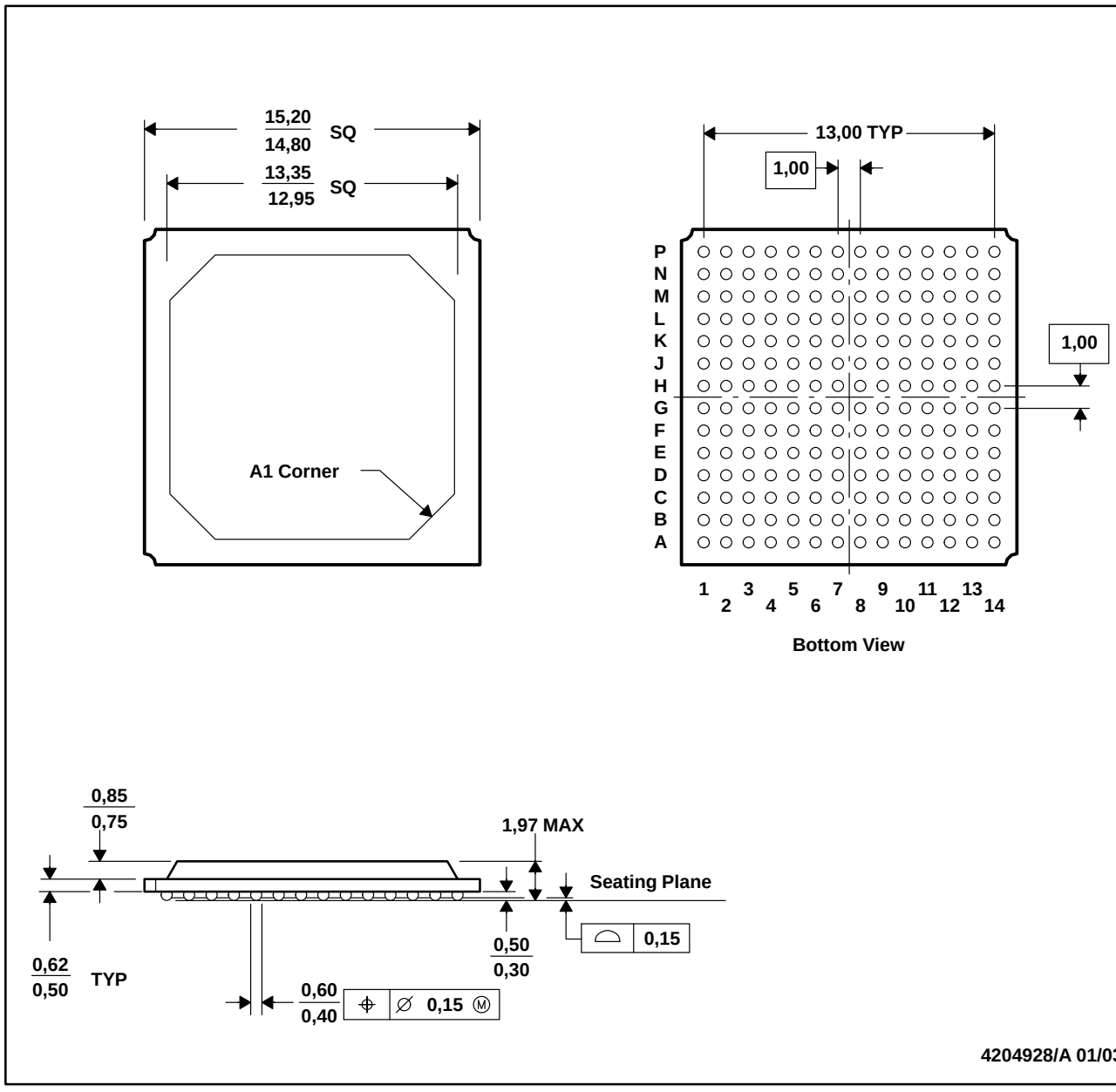
ZEA (S-PBGA-N196) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-151
D. This package is Lead-free.

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