(PCILynx-2) IEEE 1394 LINK LAYER CONTROLLER

FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **IEEE Standard for 1394-1995 Compliant**
- **IEEE Standard for 1212-1991 Compliant**
- **Supports IEEE 1394-1995 Link Layer Control**
- **PCI Local Bus Specification Rev. 2.1 Compliant**
- **Supports IEEE 1394 Transfer Rates of 100, 200, and 400 Mbit per Second**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **3.3-V Core Logic While Maintaining 5-V Tolerant Inputs**
- **Performs the Function of 1394 Cycle Master**
- **Provides 4 KBytes of Configurable FIFO RAM**
- **Provides Five Scatter-Gather DMA Channels**
- **Provides Software Control of Interrupt Events**
- **Provides Four General-Purpose Input/Outputs**
- **Supports Plug-and-Play (PnP) Specification**
- **Generates 32-Bit CRC for Transmission of 1394 Packets**
- **Performs 32-Bit CRC Checking on Reception of 1394 Packets**
- **Provides PCI Bus Master Function for Supporting DMA Operations**
- **Provides PCI Slave Function for Read/Write Access of Internal Registers**
- **Supports Distributed DMA Transfers Between 1394 and Local Bus RAM, ROM, AUX, or Zoomed Video**
- **Advanced Submicron, Low-Power CMOS Technology**
- **Packaged in a 176-Pin PQFP (PGF)**

DESCRIPTION

The TSB12LV21B (PCILynx-2) provides a high-performance IEEE 1394-1995 interface with the capability to transfer data between the 1394 PHY-link interface, the PCI bus interface, and external devices connected to the local bus interface. The 1394 PHY-link interface provides the connection to the 1394 physical layer device; it is supported by the onboard link layer controller (LLC). The LLC provides the control for transmitting and receiving 1394 packet data between the FIFO and PHY-link interface at rates of 100 Mbit/s, 200 Mbit/s, and 400 Mbit/s. The link layer also provides the capability to receive status from the physical layer device and to access the physical layer control and status registers by the application software. The PCILynx-2 complies with

- PCI Local Bus Specification, Revision 2.1
- IEEE Standard for a 1394-1995 High Performance Serial Bus
- IEEE Standard 1212-1991
- IEEE Standard Control and Status Register (CSR) Architecture for Microcomputer Buses

An internal 4 Kbyte memory can be configured as multiple variable-size FIFOs, eliminating the need for external FIFOs. Separate FIFOs are user configurable to support 1394 receive, asynchronous transmit, and isosynchronous transmit transfer operations.

The PCI interface supports 32-bit burst transfers up to 33 MHz and is capable of operating both as a master and as a target device. Configuration registers can be loaded from an external serial EEPROM, allowing board and system designers to assign their own unique identification codes. An autoboot mode allows data-moving systems (such as docking stations) to be designed to operate on the PCI bus without the need for a host CPU.

The DMA controller uses packet control list (PCL) data structures to control the transfer of data and allow the DMA to operate without host CPU intervention. These PCLs can reside in PCI memory or in memory that is connected to a local bus port. The PCLs implement an instruction set that allows linking, conditional branching, 1394 data transfer control, auxiliary support commands, and status reporting. Five DMA channels accommodate programmable data types. PCLs can be chained together to form a channel control program that can be developed to support each DMA channel. Data can be stored in either big endian or little endian format, eliminating the need for the host CPU to perform byte swapping. Data can be transferred either to 4-byte aligned locations, to provide the highest performance, or to nonaligned locations, to provide the best memory use.

The RAM, ROM, AUX, ZV, and general-purpose I/O (GPIO) ports collectively make up the local bus interface. These ports mapped into the PCI address, can be accessed either through the PCI bus or through internal DMA transactions. Internal transactions do not appear on the external PCI bus, thereby conserving PCI bandwidth. DMA packet control lists or other data may be stored in external RAM or ROM attached to the local bus interface. This further reduces PCI bus use and generally improves performance. The ZV local bus port is designed to transfer data from 1394 video devices to an external device connected to the PCILynx-2 ZV port. This interface provides a method for receiving 1394 digital camera packets directly from a ZV-compliant device attached to the local bus interface.

Built-in test registers, a dedicated test output terminal, and four GPIO terminals allow observation of internal states and provide a convenient software debug capability. Programmable interrupts are available to inform driver software of important events, such as 1394 bus resets and DMA-to-PCL transfer completion.

The 3.3-V internal operation provides reduced power consumption, while maintaining compatibility with 5-V signaling environments. The PCI interface is compatible with both 3-V and 5-V PCI systems.

The TSB12LV21B is characterized for operation over the military temperature range of –55°C to 125°C.

NOTE:

For a complete data sheet (literature number SLLS879) or more information, contact support@ti.com.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	176-Pin PQFP	PGF	TSB12LV21BMPGFEP	12LV21BMPGFEP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB12LV21BMPGFEP	ACTIVE	LQFP	PGF	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	12LV21BMPGFEP	Samples
V62/08625-01XE	ACTIVE	LQFP	PGF	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	12LV21BMPGFEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TSB12LV21B-EP :

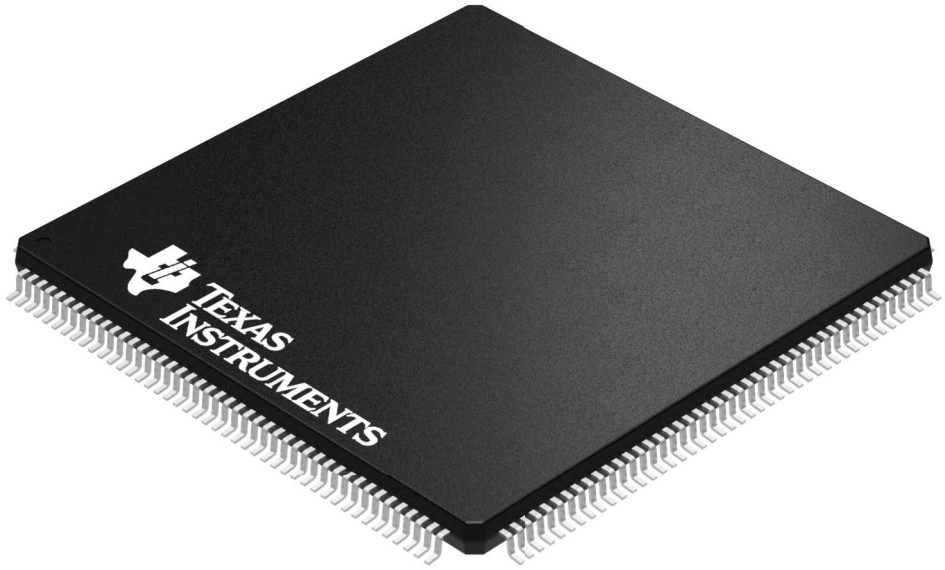
- Catalog: TSB12LV21B

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PGF 176 LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



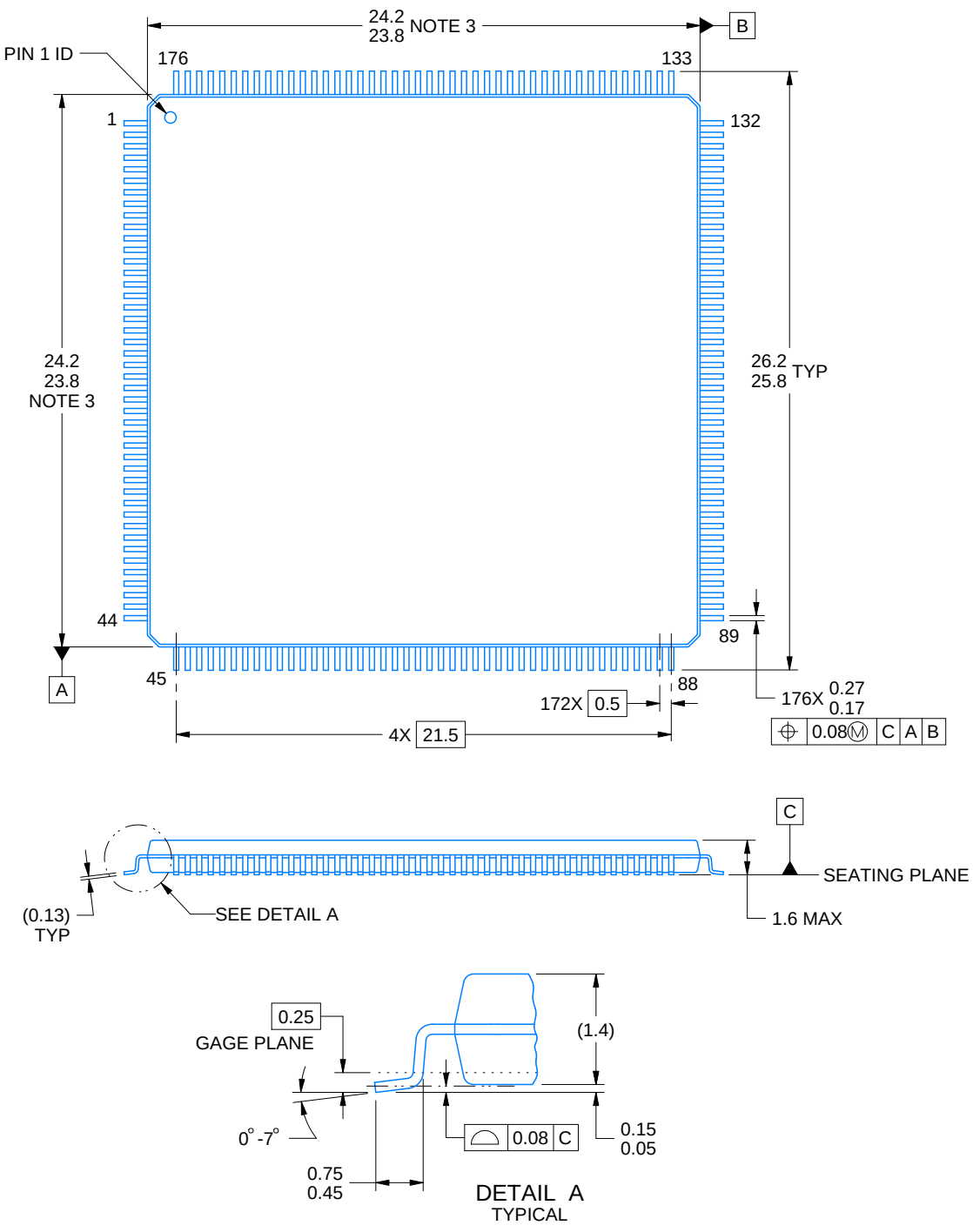
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PGF0176A

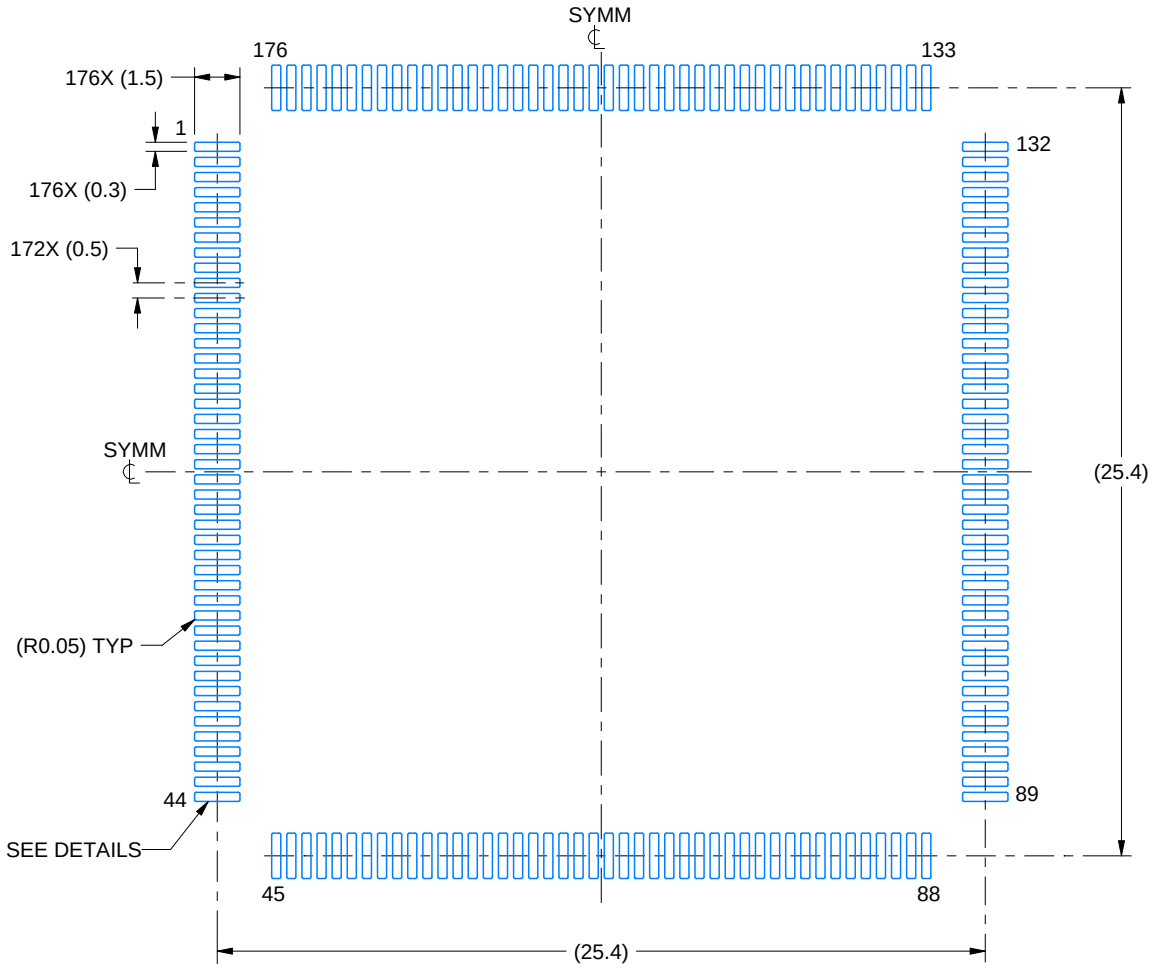
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

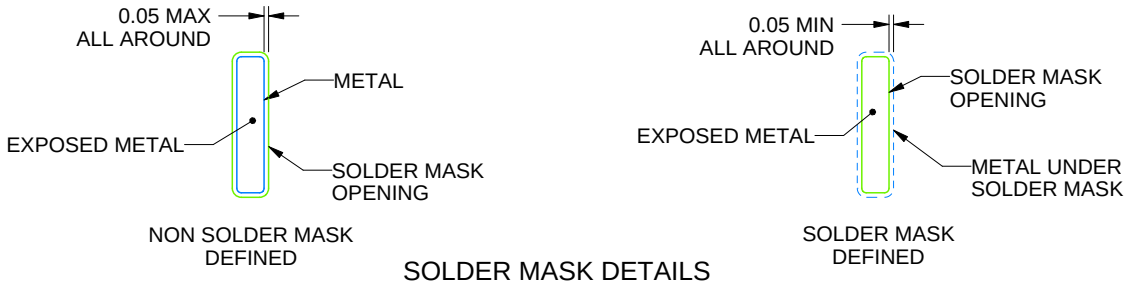


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



SOLDER MASK DETAILS

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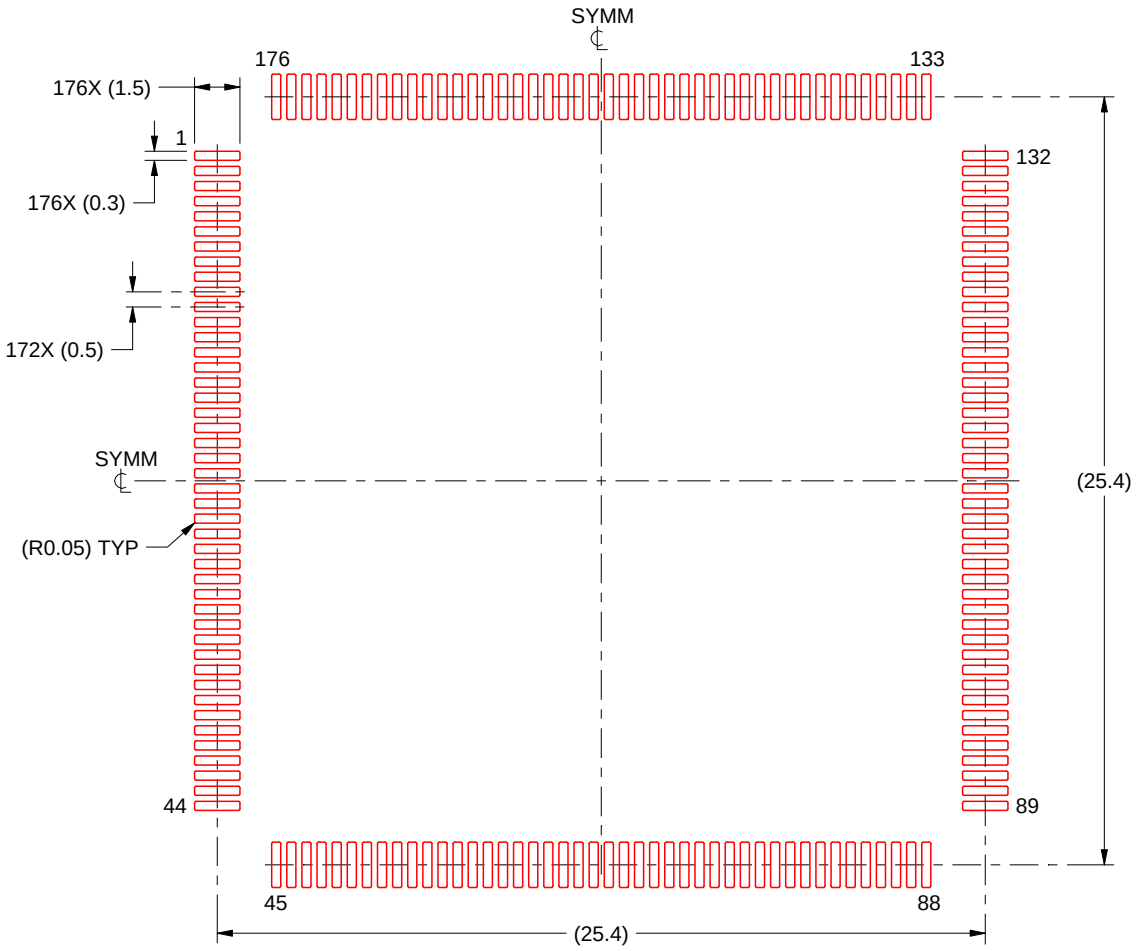
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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