

## RAD-TOLERANT CLASS V, DUAL DIFFERENTIAL LINE RECEIVER

### FEATURES

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- $\pm 15$ -V Common-Mode Input Voltage Range
- $\pm 15$ -V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls
- Designed for Use With Dual Differential Drivers SN55183 and SN75183
- Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A
- Rad-Tolerant: >40 kRad (Si) ELDRS
- QML-V Qualified, SMD 5962-79008

### DESCRIPTION/ORDERING INFORMATION

The SN55182 dual differential line receiver is designed to sense small differential signals in the presence of large common-mode noise. This device gives TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel can be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input (STRB) is provided that, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power-supply and ground terminals.

The SN55182 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

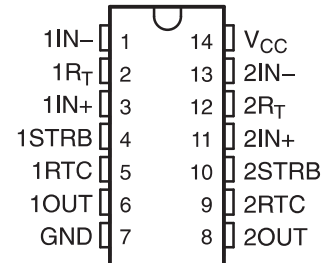
### PACKAGING/ORDERING INFORMATION<sup>(1)</sup>

TEMPERATURE	PACKAGED DEVICES	
	CERAMIC FLATPACK W (14) <sup>(2)</sup>	SYMBOL
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	5962-7900801VDA	5962-7900801VDA

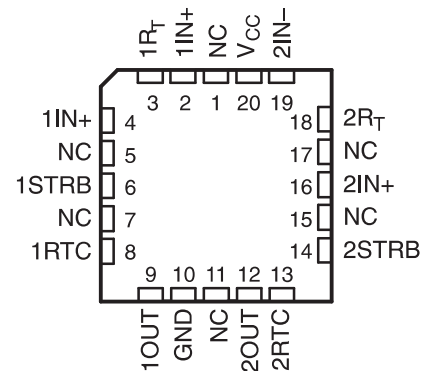
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packageing](http://www.ti.com/packageing).

SN55182... J OR W PACKAGE  
SN75182... N PACKAGE  
(TOP VIEW)



SN55182... FK PACKAGE  
(TOP VIEW)



NC – No internal connection



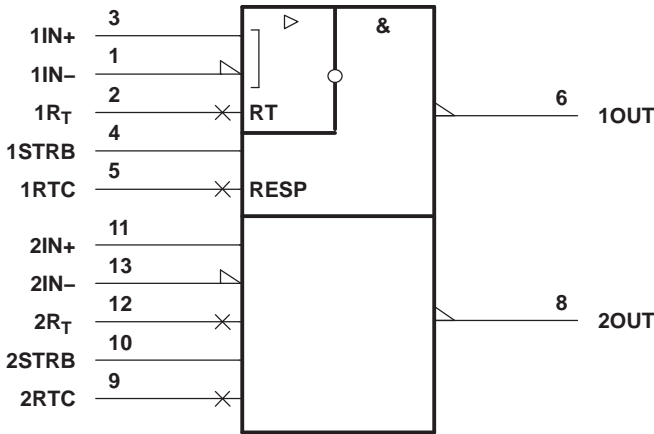
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE<sup>(1)</sup>**

INPUTS		OUTPUT OUT
STRB	V <sub>ID</sub>	
L	X	H
H	H	H
H	L	L

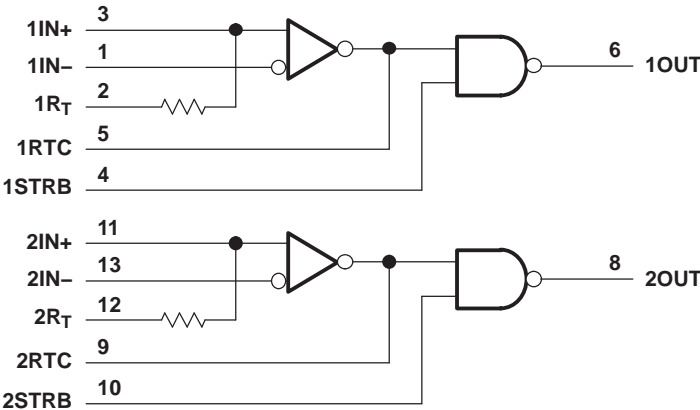
- (1) H =  $V_I \geq V_{IH}$  min or  $V_{ID}$  more positive than  $V_{TH}$  max  
L =  $V_I \leq V_{IL}$  max or  $V_{ID}$  more negative than  $V_{TL}$  max  
X = irrelevant

**LOGIC SYMBOL**



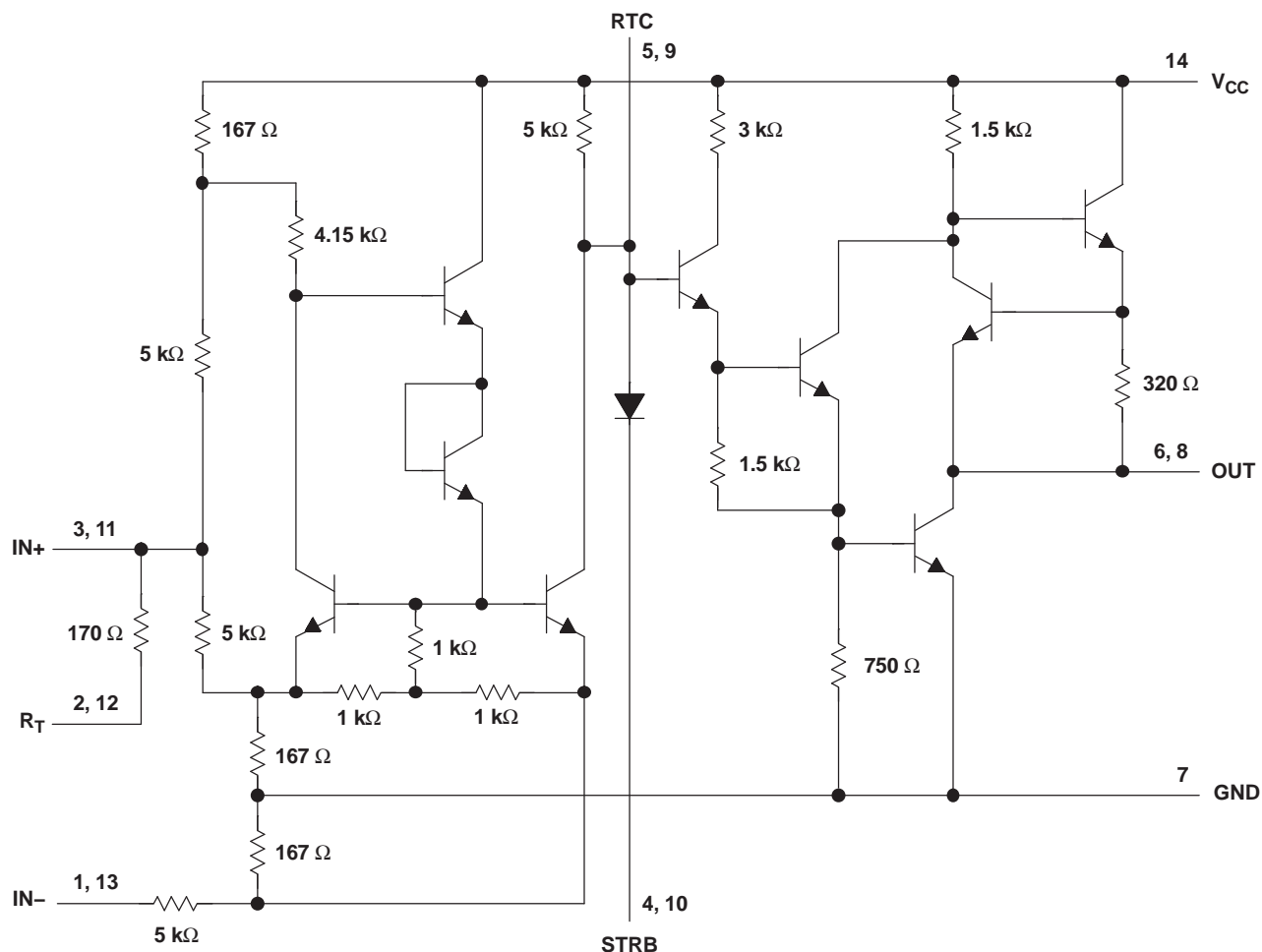
This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the J, N, and W packages.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the J, N, and W packages.

# SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.  
Pin numbers shown are for the J, N, and W packages.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		UNIT
$V_{CC}$	Supply voltage <sup>(2)</sup>	8 V
$V_{IC}$	Common-mode input voltage	$\pm 20$ V
$V_{ID}$	Differential input voltage <sup>(3)</sup>	$\pm 20$ V
$V_{I(STRB)}$	Strobe input voltage	8 V
$I_O$	Output sink current	50 mA
	Continuous total power dissipation	See Dissipation Rating Table
$T_{stg}$	Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	$300^{\circ}\text{C}$

- (1) The absolute maximum ratings under any condition are limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
W <sup>(1)</sup>	1000 mW	8.0 mW/°C	640 mW	200 mW

(1) In the FK, J, and W packages, SN55182 chips are alloy mounted.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IC}$	Common-mode input voltage			±15	V
$V_{IH(STRB)}$	High-level strobe input voltage	2.1		5.5	V
$V_{IL(STRB)}$	Low-level strobe input voltage	0		0.9	V
$I_{OH}$	High-level output current			–400	μA
$I_{OL}$	Low-level output current			16	mA
$T_A$	Operating free-air temperature	–55		125	°C

## ELECTRICAL CHARACTERISTICS

over recommended ranges of  $V_{CC}$ ,  $V_{IC}$ , and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage		V <sub>O</sub> = 2.5 V, I <sub>OH</sub> = −400 μA	V <sub>IC</sub> = −3 V to 3 V			0.5	V
				V <sub>IC</sub> = −15 V to 15 V			1	
V <sub>IT−</sub>	Negative-going input threshold voltage		V <sub>O</sub> = 0.4 V, I <sub>OL</sub> = 16 mA	V <sub>IC</sub> = −3 V to 3 V			−0.5	V
				V <sub>IC</sub> = −15 V to 15 V			−1	
V <sub>OH</sub>	High-level output voltage		V <sub>ID</sub> = 1 V, V <sub>(STRB)</sub> = 2.1 V, I <sub>OH</sub> = −400 μA		2.5	4.2	5.5	V
			V <sub>ID</sub> = 1 V, V <sub>(STRB)</sub> = 0.4 V, I <sub>OH</sub> = −400 μA		2.5	4.2	5.5	
V <sub>OL</sub>	Low-level output voltage		V <sub>ID</sub> = −1 V, V <sub>(STRB)</sub> = 2.1 V, I <sub>OL</sub> = 16 mA			0.25	0.4	V
I <sub>I</sub>	Input current	Inverting input	V <sub>IC</sub> = 15 V			3	4.2	mA
			V <sub>IC</sub> = 0			0	−0.5	
			V <sub>IC</sub> = −15 V			−3	−4.2	
		Noninverting input	V <sub>IC</sub> = 15 V			5	7	
			V <sub>IC</sub> = 0			−1	−1.4	
			V <sub>IC</sub> = −15 V			−7	−9.8	
I <sub>IH(STRB)</sub>	High-level strobe input current		V <sub>(STRB)</sub> = 5.5 V				5	μA
I <sub>IL(STRB)</sub>	Low-level strobe input current		V <sub>(STRB)</sub> = 0			−1	−1.4	mA
r <sub>I</sub>	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		
Line-terminating resistance			T <sub>A</sub> = 25°C		120	170	250	Ω
I <sub>OS</sub>	Short-circuit output current		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	−2.8	−4.5	−6.7	mA
I <sub>CC</sub>	Supply current (average per receiver)		V <sub>IC</sub> = 15 V,	V <sub>ID</sub> = −1 V		4.2	6	mA
			V <sub>IC</sub> = 0,	V <sub>ID</sub> = −0.5 V		6.8	10.2	
			V <sub>IC</sub> = −15 V,	V <sub>ID</sub> = −1 V		9.4	14	

(1) Unless otherwise noted,  $V_{(STRB)} \geq 2.1\text{ V}$  or open.

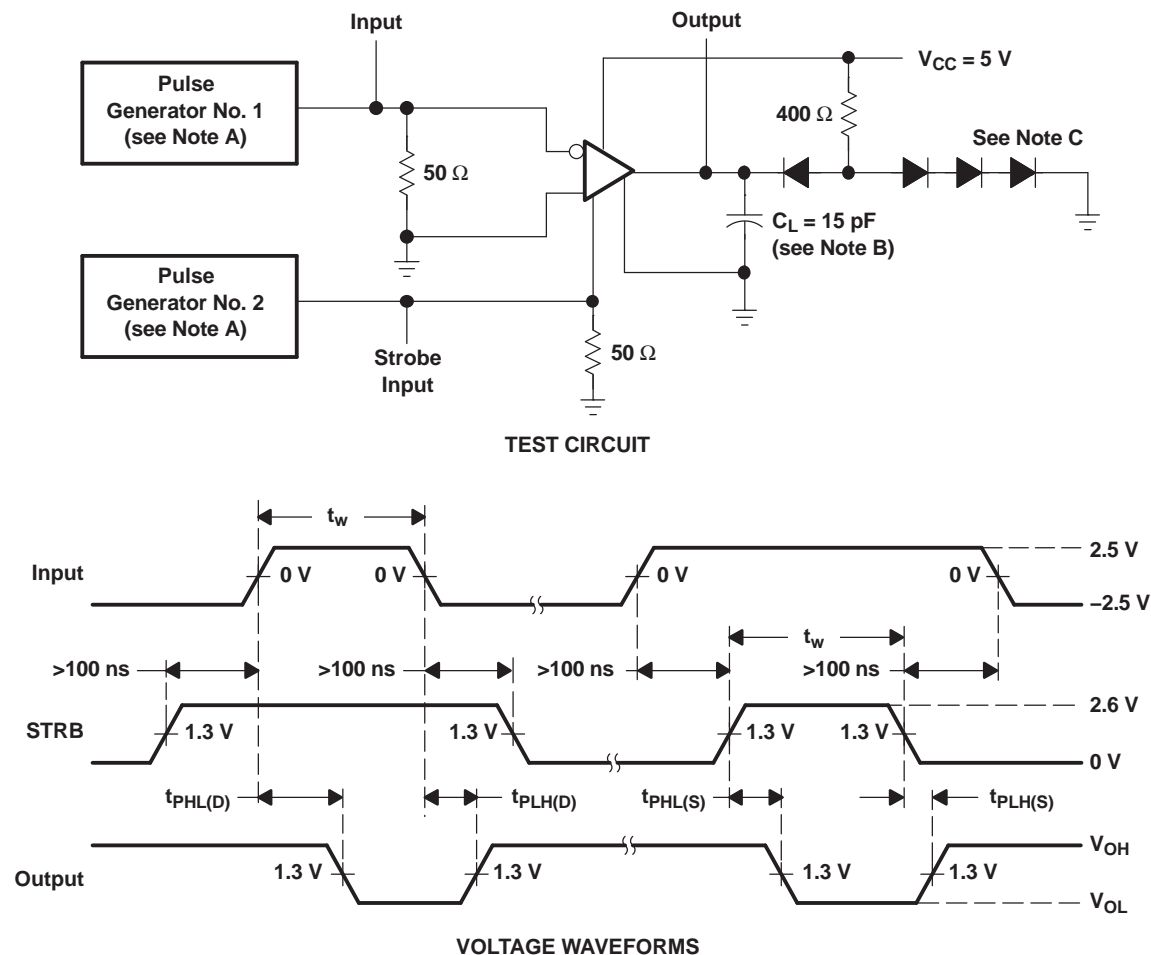
(2) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $V_{IC} = 0$ , and  $T_A = 25^\circ\text{C}$ .

## SWITCHING CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output from differential input	$R_L = 400\text{ }\Omega$ ,	$C_L = 15\text{ pF}$ , See <a href="#">Figure 1</a>		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high- to low-level output from differential input	$R_L = 400\text{ }\Omega$ ,	$C_L = 15\text{ pF}$ , See <a href="#">Figure 1</a>		31	45	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output from STRB input	$R_L = 400\text{ }\Omega$ ,	$C_L = 15\text{ pF}$ , See <a href="#">Figure 1</a>		9	30	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output from STRB input	$R_L = 400\text{ }\Omega$ ,	$C_L = 15\text{ pF}$ , See <a href="#">Figure 1</a>		15	25	ns

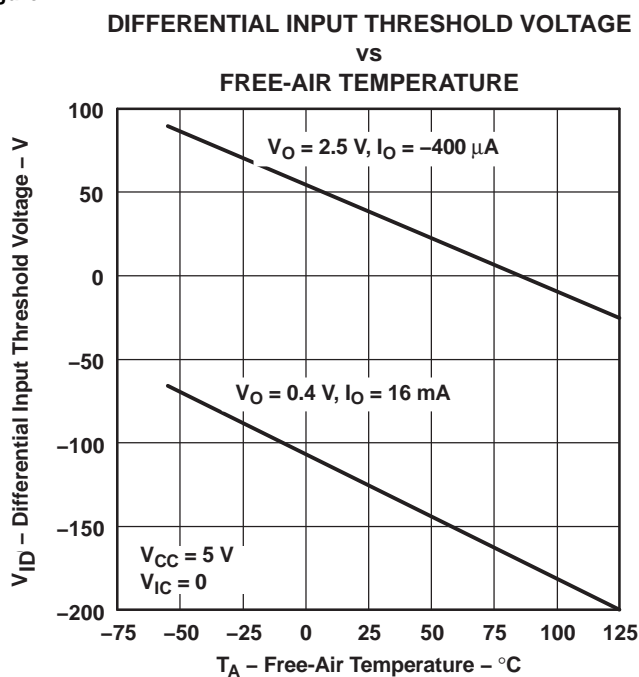
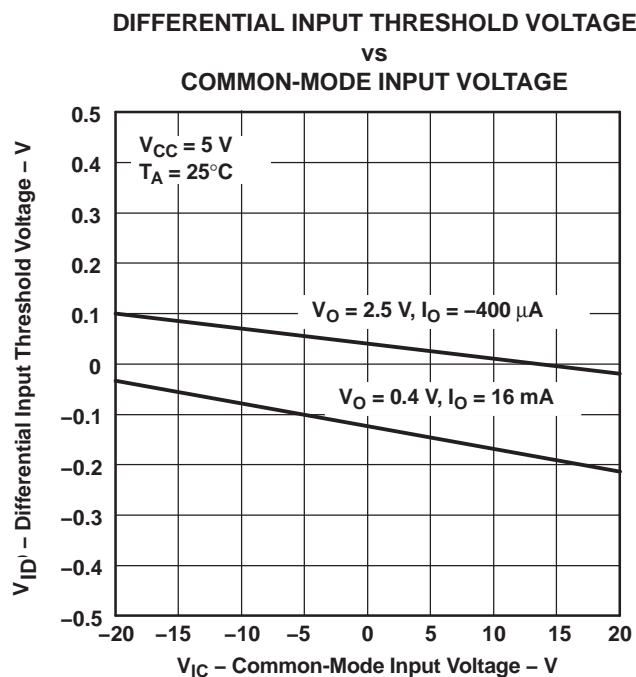
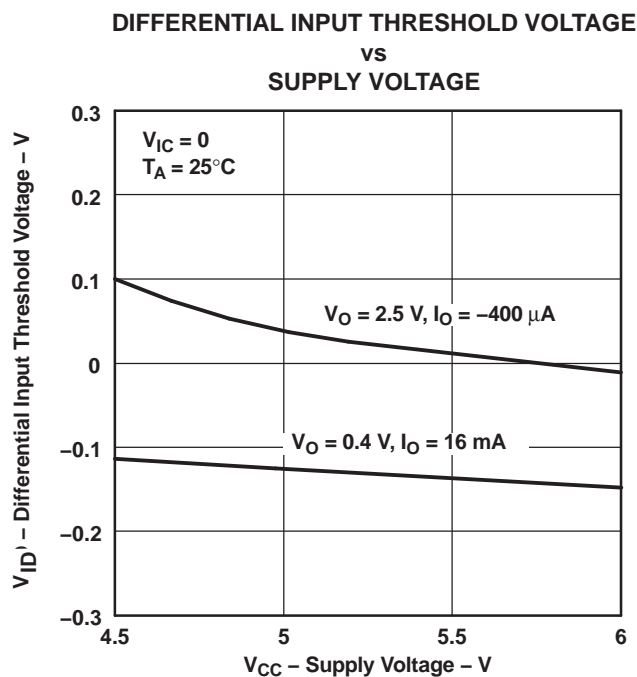
## PARAMETER MEASUREMENT INFORMATION



- The pulse generators have the following characteristics: Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 10 ns, t<sub>f</sub> ≤ 10 ns, t<sub>w</sub> = 0.5 ± 0.1 μs, PRR ≤ 1 MHz.
- C<sub>L</sub> includes probe and jig capacitance.
- All diodes are 1N3064 or equivalent.

**Figure 1. Test Circuit and Voltage Waveforms**

# **TYPICAL CHARACTERISTICS<sup>(1)</sup>**



- (1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

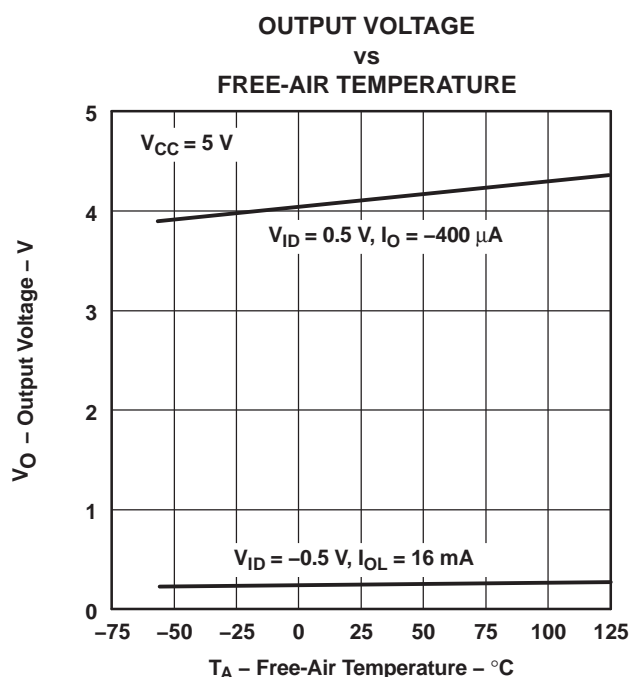
TYPICAL CHARACTERISTICS<sup>(1)</sup>

Figure 5.

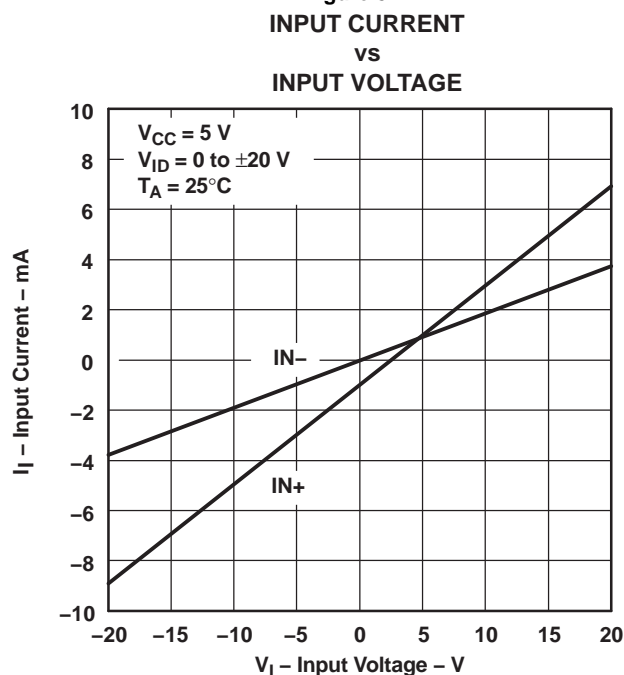


Figure 7.

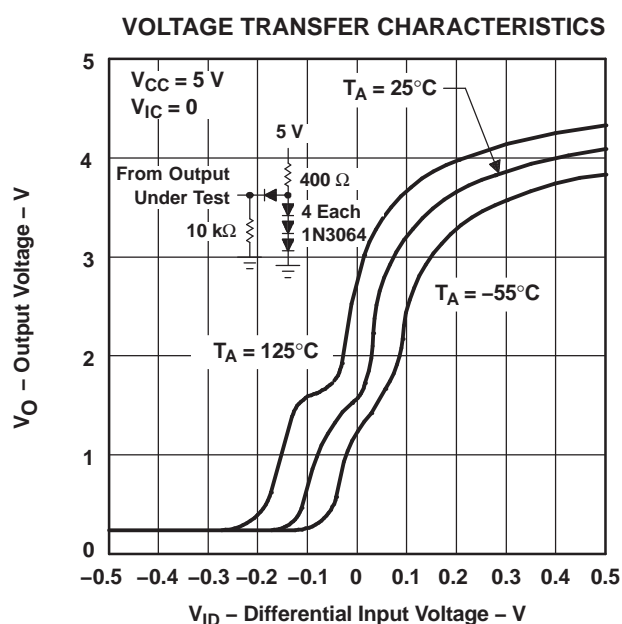


Figure 6.

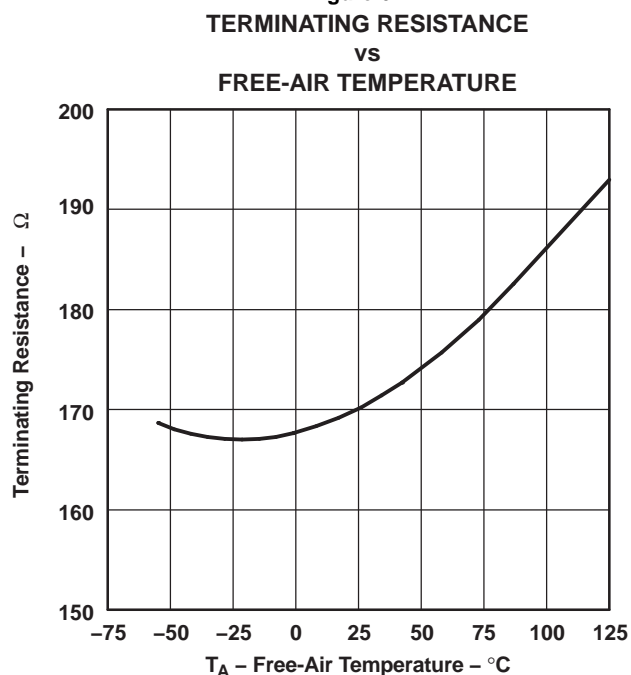


Figure 8.

- (1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.



# TYPICAL CHARACTERISTICS<sup>(1)</sup>

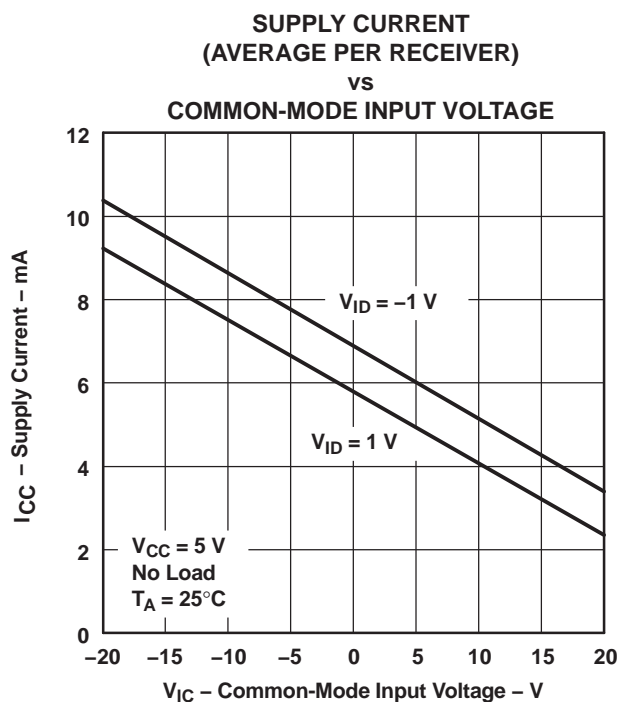


Figure 9.

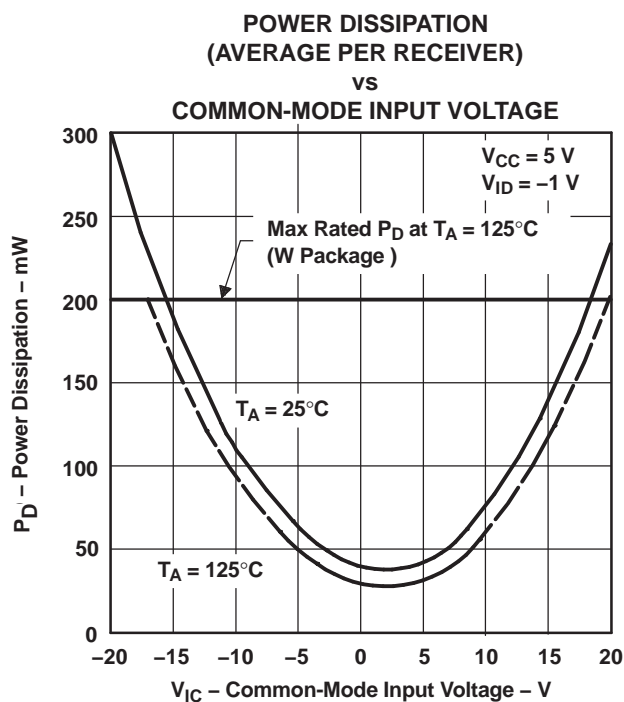
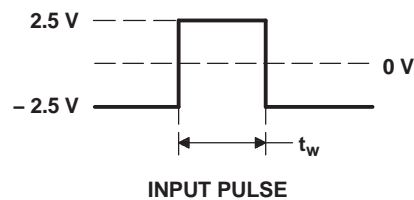
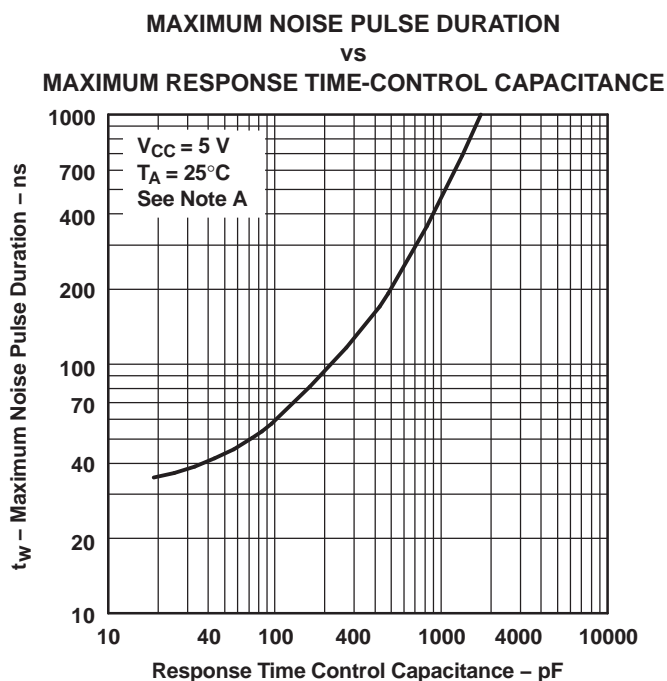


Figure 10.

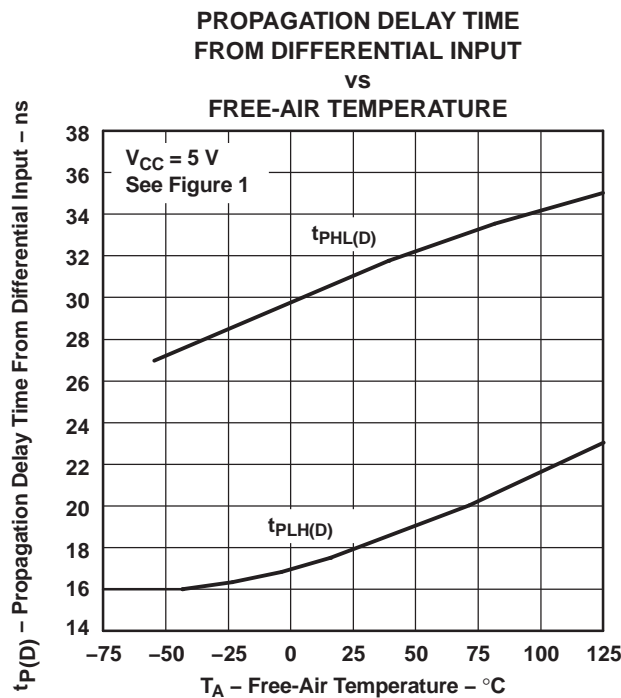


- A. Figure 11 shows the maximum duration of the illustrated pulse that can be applied differentially without the output changing from the low to high level.

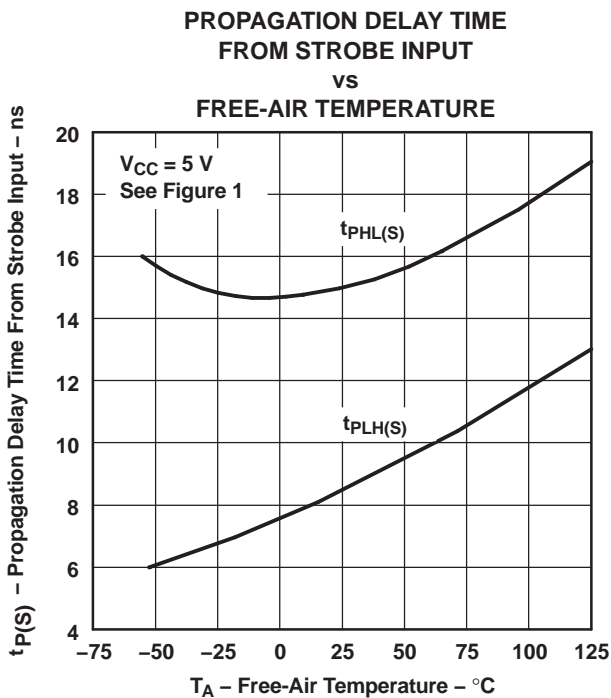
Figure 11.

- (1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

**TYPICAL CHARACTERISTICS<sup>(1)</sup>**



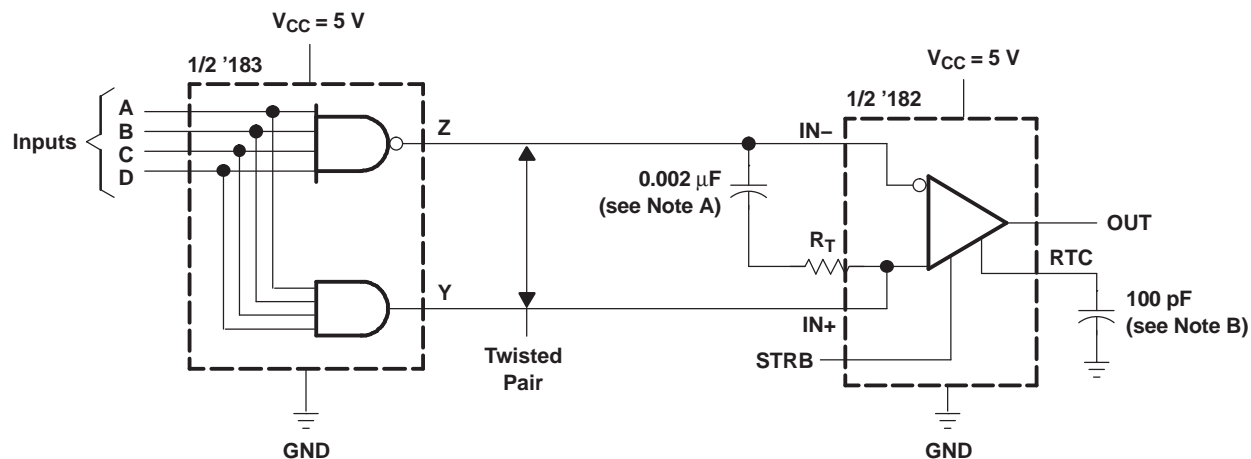
**Figure 12.**



**Figure 13.**

- (1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

## APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let  $f = 5 \text{ MHz}$   
 $C = 0.002 \mu\text{F}$

$$Z_{(C)} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(C)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

**Figure 14. Transmission of Digital Data Over Twisted-Pair Line**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7900801VCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7900801VC A SNV55182J	<a href="#">Samples</a>
5962-7900801VDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7900801VD A SNV55182W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

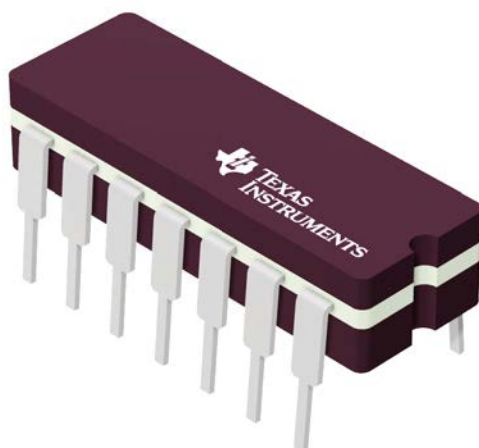
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

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