采用超小型封装的 ISO1500 3kV$_{RMS}$ 基础型隔离式 RS-485/RS-422 收发器

1 特性

- 符合或超出 TIA/EIA-485-A 要求
- 半双工收发器
- 低 EMI 1Mbps 数据速率
- 总线 I/O 保护
  - ±16kV HBM ESD
- 1.71V 至 5.5V 逻辑侧电源 (V_{CC1})，4.5V 至 5.5V 总线侧电源 (V_{CC2})
- 1/8 单位负载：多达 256 个总线节点
- 失效防护接收器（总线开路、短路和空闲）
- 100kV/μs（典型值）高共模瞬态抗扰度
- 扩展温度范围为 -40°C 至 +125°C
- 适用于热插拔功能的无干扰加电和断电
- 超小型 SSOP (DBQ-16) 封装
- 安全相关认证：
  - 符合 DIN VDE V 0884-11:2017-01 标准的 4242V$_{PK}$ V_{IOTM} 和 566V$_{PK}$ V_{IORM}
  - 符合 UL 1577 标准且长达 1 分钟的 3000 V_{RMS} 隔离
  - IEC 60950-1、IEC 62368-1 和 IEC 61010-1 认证
  - CQC、TUV 和 CSA 认证
  - VDE、UL、CQC 和 TUV 认证完成；等待 CSA 审批

2 应用

- 电表
- 保护继电器
- 工厂自动化与控制
- HVAC 系统和楼宇自动化
- 电机驱动器

3 说明

ISO1500 器件是适用于 TIA/EIA RS-485 和 RS-422 应用的电隔离差动线路 收发器。该器件采用超小型 16 引脚 SSOP 封装，具有一个 3 通道数字隔离器和一个 RS-485 收发器。该收发器的总线引脚受到 IEC ESD 接触放电和 IEC EFT 事件保护。接收器输出具有针对总线开路、短路和空闲情况的失效防护。与其他集成的隔离式 RS-485 解决方案或采用光耦合器和非隔离式 RS-485 收发器的分立式实施相比，ISO1500 的小解决方案尺寸可极大地减少所需的布板空间。

该器件用于长距离通信。隔离会破坏通信节点之间的接地回路，从而获得更大的共模电压范围。经测试，每个器件的对称隔离层可在总线收发器和逻辑电平接口之间按照 UL 1577 标准提供为时 1 分钟的 3000V$_{RMS}$ 隔离。

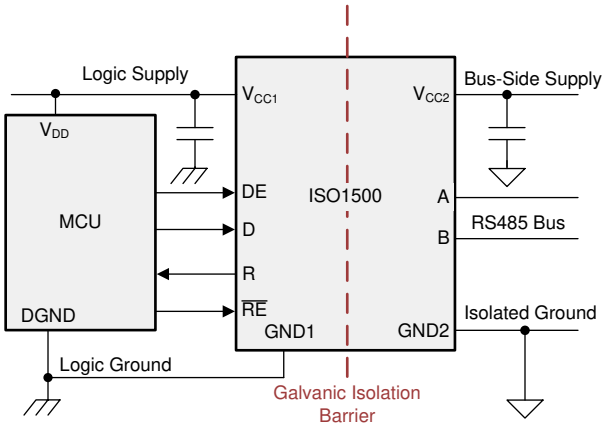
ISO1500 器件可由 1 侧的 1.71V 至 5.5V 电压供电，从而使器件可与低压 FPGA 和 ASIC 相连接。2 侧的电源电压范围为 4.5V 至 5.5V。该器件支持 -40°C 至 +125°C 的宽工作环境温度范围。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO1500	SSOP (16)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (May 2019) to Revision C **Page**

- 已更改 证书相关信息 特性 部分中的 VDE 和 CSA 安全相关认证说明 ... 1
- Added footnote to Pin function table for NC pin ... 3
- Changed Insulation Specifications table with test condition for VIOSM and qPD (Partial discharge) ... 6
- Changed certificate related info in Safety-Related Certifications section ... 7

Changes from Revision A (December 2018) to Revision B **Page**

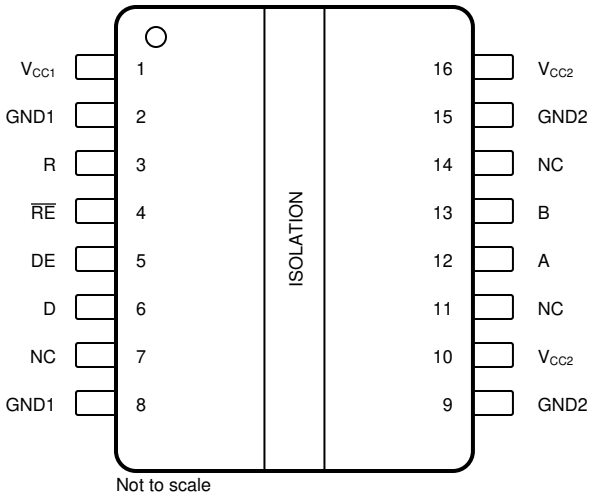
- 已添加 向特性列表中添加了 HBM ESD ... 1

Changes from Original (September 2018) to Revision A **Page**

- 已更改 将器件状态从“预告信息”更改为“生产数据” ... 1

5 Pin Configuration and Functions

DBQ Package
16-Pin SSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	12	I/O	Transceiver noninverting input or output (I/O) on the bus side
B	13	I/O	Transceiver inverting input or output (I/O) on the bus side
D	6	I	Driver input
DE	5	I	Driver enable. This pin enables the driver output when high and disables the driver output when low or open.
GND1	2	—	Ground connection for V_{CC1}
	8		
GND2	9	—	Ground connection for V_{CC2}
	15		
NC(1)	7	—	No internal connection
	11		
	14		
R	3	O	Receiver output
$\overline{RE}$	4	I	Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low.
V_{CC1}	1	—	Logic-side power supply
V_{CC2}	10	—	Transceiver-side power supply. These pins are not connected internally and must be shorted externally on PCB.
	16		

(1) Device functionality is not affected if NC pins are connected to supply or ground on PCB

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC1}	Supply voltage, side 1	-0.5	6	V
V_{CC2}	Supply voltage, side 2	-0.5	6	V
V_{IO}	Logic voltage level (D, DE, $\overline{RE}$, R)	-0.5	V_{CC1}+0.5(3)	V
I_O	Output current on R pin	-15	15	mA
V_{BUS}	Voltage on bus pins (A, B, Y, Z w.r.t GND2)	-18	18	V
T_J	Junction temperature	-40	150	℃
T_{STG}	Storage temperature	-65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except bus pins(1)	±4000	V
		Bus terminals to GND2(1)	±16000	V
	Electrostatic discharge Charged device model (CDM), per JEDEC specification JESD22-C101	All pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC1}	Supply Voltage, Side 1, 1.8-V operation	1.71	1.89	V
	Supply Voltage, Side 1, 2.5-V, 3.3-V and 5.5-V operation	2.25	5.5	V
V_{CC2}	Supply Voltage, Side 2	4.5	5.5	V
V_I	Common mode voltage at any bus terminal: A or B	-7	12	V
V_{IH}	High-level input voltage (D, DE, $\overline{RE}$ inputs)	0.7*V_{CC1}	V_{CC1}	V
V_{IL}	Low-level input voltage (D, DE, $\overline{RE}$ inputs)	0	0.3*V_{CC1}	V
V_{ID}	Differential input voltage	-12	12	V
I_O	Output current, Driver	-60	60	mA
I_{OR}	Output current, Receiver	-4	4	mA
R_L	Differential load resistance	54		Ω
$1/t_{UI}$	Signaling rate		1	Mbps
T_A	Operating ambient temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ISO1500 DBQ (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Thermal Information (continued)

THERMAL METRIC(1)		ISO1500 DBQ (SSOP) 16 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	64.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	63.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	--	°C/W

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_A=125°C, T_J = 150°C, A-B load = 54 Ω ||50pF, Load on R=15pF Input a 500kHz 50% duty cycle square wave to D pin with V_{DE}=V_{CC1}, $V_{\overline{RE}}$=GND1			278	mW
P_{D1}	Maximum power dissipation (side-1)				28	mW
P_{D2}	Maximum power dissipation (side-2)				250	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
			DBQ-16	
IEC 60664-1				
CLR	External clearance (1)	Side 1 to side 2 distance through air	>3.7	mm
CPG	External creepage (1)	Side 1 to side 2 distance across package surface	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01 (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISO1500 (3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 10000\ V_{PK}$ (qualification)	4000	V_{PK}
q_{pd}	Apparent charge (4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output (5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 150°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) ISO1500 is suitable for safe *electrical insulation* within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017- 01	Plan to certify according to IEC 60950-1, IEC 62368-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010/A1:2019, EN 60950-1:2006/A2:2013 and EN 62368-1:2014
Maximum transient isolation voltage, 4242 V_{PK}; Maximum repetitive peak isolation voltage, 566 V_{PK}; Maximum surge isolation voltage, 4000 V_{PK}	CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., for pollution degree 2, material group I: 370 V_{RMS}	Single protection, 3000 V_{RMS}	Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage	EN 61010-1:2010/A1:2019, 300 VRMS basic isolation ---------- EN 60950-1:2006/A2:2013 and EN 62368-1:2014, 400 VRMS basic isolation
Certificate number: 40040142	Certificate planned	File number: E181974	Certificate number: CQC18001199097	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DBQ-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 67.9°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 图 1			201	mA
		$R_{\theta JA}$ = 67.9°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 图 1			308	
		$R_{\theta JA}$ = 67.9°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 图 1			403	
		$R_{\theta JA}$ = 67.9°C/W, V_I = 1.89 V, T_J = 150°C, T_A = 25°C, see 图 1			586	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 67.9°C/W, T_J = 150°C, T_A = 25°C, see 图 2			1105	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics: Driver

Typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27℃ (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential-output voltage magnitude	Open circuit voltage, unloaded bus, 4.5 V ≤ V_{CC2} ≤ 5.5 V	1.5	4.3	V_{CC2}	V
		R_L = 60 Ω, –7 V ≤ V_{TEST} ≤ 12 V, 4.5 V < V_{CC2} < 5.5 V (see 图 19)	1.5	2.5		V
		R_L = 100 Ω (see 图 20), RS-422 load	2	2.9		V
		R_L = 54 Ω (see 图 20), RS-485 load, 4.5 V < V_{CC2} < 5.5 V	1.5	2.5		V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states	R_L = 54 Ω or R_L = 100 Ω, see 图 20	–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or R_L = 100 Ω, see 图 20		0.5 × V_{CC2}	3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	R_L = 54 Ω or R_L = 100 Ω, see 图 20	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	R_L = 54 Ω or R_L = 100 Ω, see 图 20		300		mV
I_{OS}	Short-circuit output current	V_D = V_{CC1} or V_D = V_{GND1}, V_{DE} = V_{CC1}, –7 V ≤ V_O ≤ 12 V, see 图 28	–175		175	mA
I_i	Input current	V_D and V_{DE} = 0 V or V_D and V_{DE} = V_{CC1}	–10		10	µA
CMTI	Common-mode transient immunity	V_D= V_{CC1} or GND1, V_{CM} = 1200V, See 图 22	85	100		kV/µs

6.10 Electrical Characteristics: Receiver

Typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27℃ (Min/Max are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{i1}	Bus input current	V_{DE} = 0 V, V_{CC2} = 0 V or V_{CC2} = 5.5 V, One bus input at –7 V or 12 V, other input at 0 V	–100		100	µA
V_{TH+}	Positive-going input threshold voltage	–7 V ≤ Common mode voltage on bus terminals ≤ 12 V	See (1)	–100	–50	mV
$V_{TH–}$	Negative-going input threshold voltage	–7 V ≤ Common mode voltage on bus terminals ≤ 12 V	–200	–145	See (1)	mV
V_{hys}	Input hysteresis (V_{TH+} – $V_{TH–}$)	–7 V ≤ Common mode voltage on bus terminals ≤ 12 V	20	45		mV
V_{OH}	Output high voltage on the R pin	V_{CC1}=5V+/-10%, I_{OH} = –4 mA, V_{ID} = 200 mV	V_{CC1} – 0.4			V
		V_{CC1}=3.3V+/-10%, I_{OH} = –2 mA, V_{ID} = 200 mV	V_{CC1} – 0.3			V
		V_{CC1}=2.5V+/-10%, 1.8V+/-5%, I_{OH} = –1 mA, V_{ID} = 200 mV	V_{CC1} – 0.2			V
V_{OL}	Output low voltage on the R pin	V_{CC1}=5V+/-10%, I_{OL} = 4 mA, V_{ID} = –200 mV			0.4	V
		V_{CC1}=3.3V+/-10%, I_{OL} = 2 mA, V_{ID} = –200 mV			0.3	V
		V_{CC1}=2.5V+/-10%, 1.8V+/-5%, I_{OL} = 1 mA, V_{ID} = –200 mV			0.2	V
I_{OZ}	Output high-impedance current on the R pin	V_R = 0 V or V_R = V_{CC1}, $V_{\overline{RE}}$ = V_{CC1}	–1		1	µA
I_i	Input current on the $\overline{RE}$ pin	$V_{\overline{RE}}$ = 0 V or $V_{\overline{RE}}$ = V_{CC1}	–10		10	µA
CMTI	Common-mode transient immunity	V_{ID} = 1.5 V or -1.5 V, V_{CM}= 1200 V , See 图 22	85	100		kV/µs

(1) Under any specific conditions, V_{TH+} is ensured to be at least V_{hys} higher than $V_{TH–}$.

6.11 Supply Current Characteristics: Side 1(I_{CC1})

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, RECEIVER DISABLED					
Logic-side supply current	$V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		2.6	4.4	mA
Logic-side supply current	$V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		2.6	4.4	mA
Logic-side supply current	D = 1Mbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%		3.2	5.1	mA
Logic-side supply current	D = 1Mbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%		3.2	5.1	mA
DRIVER ENABLED, RECEIVER ENABLED					
Logic-side supply current	$V_{\overline{RE}} = V_{GND1}$, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		2.6	4.4	mA
Logic-side supply current	$V_{\overline{RE}} = V_{GND1}$, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		2.6	4.4	mA
Logic-side supply current	$V_{\overline{RE}} = V_{GND1}$, D = 1Mbps square wave with 50% duty cycle, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		3.4	5.2	mA
Logic-side supply current	$V_{\overline{RE}} = V_{GND1}$, D= 1Mbps square wave with 50% duty cycle, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		3.2	5.2	mA
DRIVER DISABLED, RECEIVER ENABLED					
Logic-side supply current	$V_{(A-B)} \geq$ 200 mV, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		1.5	3.1	mA
Logic-side supply current	$V_{(A-B)} \geq$ 200 mV, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		1.5	3.1	mA
Logic-side supply current	(A-B) =1Mbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%, $C_{L(R)}$ (1) = 15 pF		1.7	3.2	mA
Logic-side supply current	(A-B) = 1Mbps square wave with 50% duty cycle, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%, $C_{L(R)}$ (1) = 15 pF		1.7	3.2	mA
DRIVER DISABLED, RECEIVER DISABLED					
Logic-side supply current	$V_{DE} = V_{GND1}$, $V_D = V_{CC1}$, V_{CC1} = 5 V ± 10%		1.5	3.1	mA
Logic-side supply current	$V_{DE} = V_{GND1}$, $V_D = V_{CC1}$, V_{CC1} = 3.3 V ± 10%		1.5	3.1	mA

(1) $C_{L(R)}$ is the load capacitance on the R pin.

6.12 Supply Current Characteristics: Side 2(I_{CC2})

$V_{\overline{RE}} = V_{GND1}$ or $V_{\overline{RE}} = V_{CC1}$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, BUS UNLOADED					
Bus-side supply current	$V_D = V_{CC1}$, V_{CC2} = 5 V ± 10%		2.5	4.4	mA
DRIVER ENABLED, BUS LOADED					
Bus-side supply current	$V_D = V_{CC1}$, R_L = 54 Ω, V_{CC2} = 5 V ± 10%		52	70	mA
Bus-side supply current	D =1Mbps square wave with 50% duty cycle, R_L = 54 Ω, C_L = 50 pF, V_{CC2} = 5 V ± 10%		60	80	mA
DRIVER DISABLED, BUS LOADED OR UNLOADED					
Bus-side supply current	$V_D = V_{CC1}$, V_{CC2} = 5 V ± 10%		2.4	3.9	mA

6.13 Switching Characteristics: Driver

Typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27℃ (Min/Max specs over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1Mbps DEVICE						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see 图 21		210	300	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 21		210	300	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see 图 21		3	30	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 23, and 图 24		160	250	ns
t_{PZH}, t_{PZL}	Enable time	See 图 23, and 图 24		200	400	ns

(1) Also known as pulse skew.

6.14 Switching Characteristics: Receiver

Typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27℃ (Min/Max are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1Mbps DEVICE						
t_r, t_f	Differential output rise time and fall time	C_L = 15 pF, see 图 25		2.4	4	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see 图 25		120	180	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see 图 25		5	20	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 26 and 图 27		11	30	ns
t_{PZH}, t_{PZL}	Enable time	See 图 26 and 图 27		7	20	ns

(1) Also known as pulse skew.

6.15 Insulation Characteristics Curves

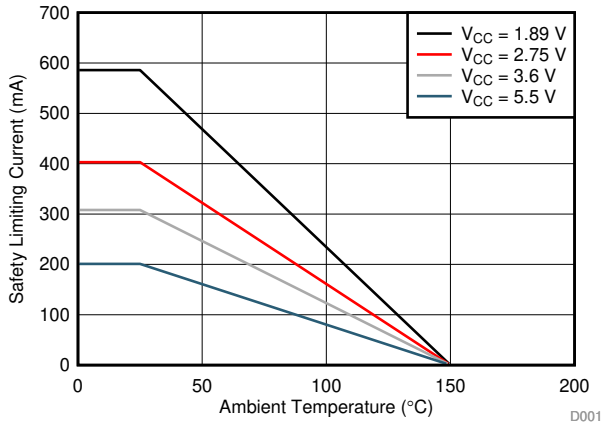


图 1. Thermal Derating Curve for Limiting Current per VDE

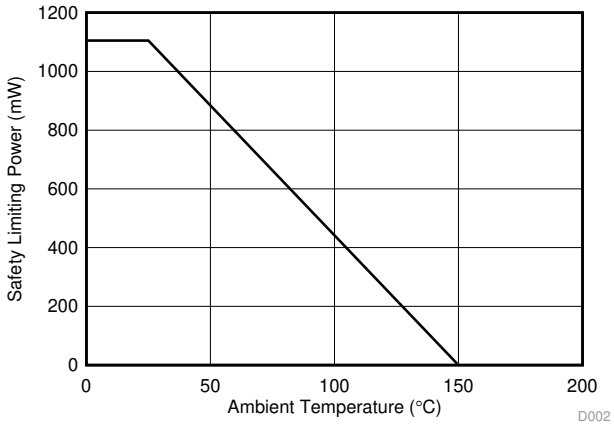
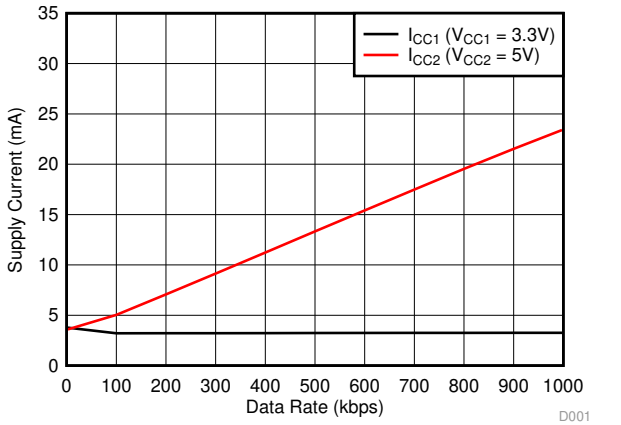


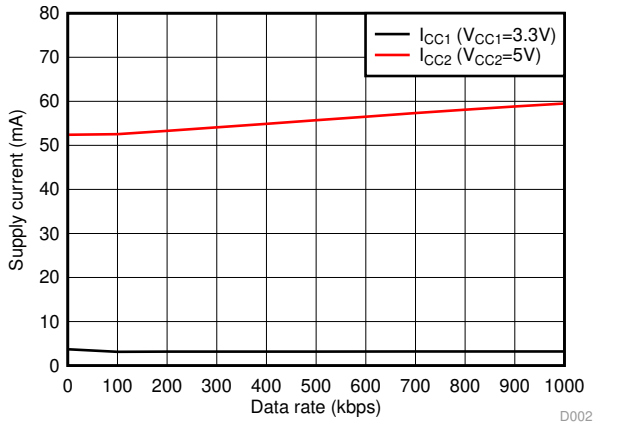
图 2. Thermal Derating Curve for Limiting Power per VDE

6.16 Typical Characteristics



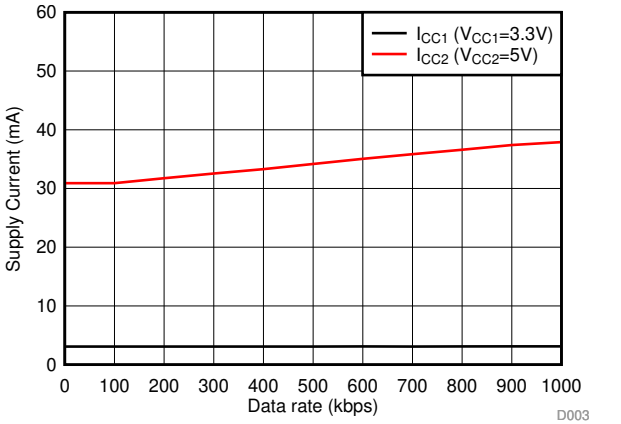
T_A = 25°C　　DE = V_{CC1}　　$\overline{RE}$ = GND1

图 3. Supply Current Vs Data Rate- No Load



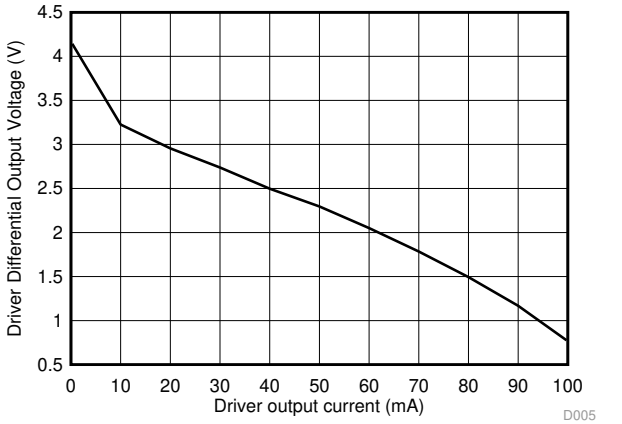
T_A = 25°C　　DE = V_{CC1}　　$\overline{RE}$ = GND1
Driver load = 54 ohm || 50 pF　　Load on R = 15 pF

图 4. Supply Current Vs Data Rate- with 54 Ω || 50 pf Load



T_A = 25°C　　DE = V_{CC1}　　$\overline{RE}$ = GND1
Driver load = 120 ohm || 50 pF　　Load on R = 15 pF

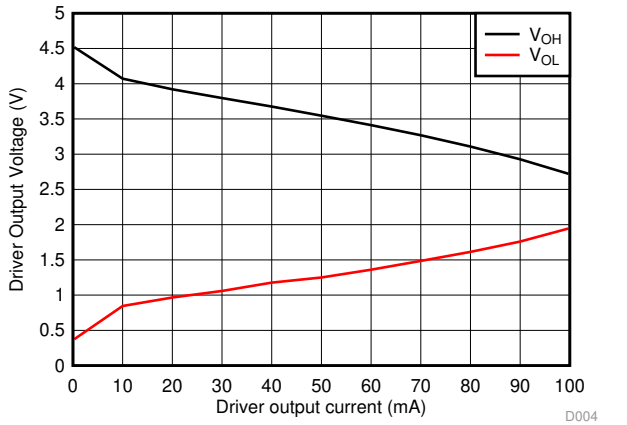
图 5. Supply Current Vs Data Rate - with 120 Ω || 50 pf Load



DE = V_{CC1}　　D = GND1　　V_{CC1} = 3.3 V
V_{CC2} = 5 V　　T_A = 25°C

图 6. Driver Differential Output Voltage Vs Driver Output Current

Typical Characteristics (接下页)



DE = V_{CC1} D = GND1 V_{CC1} = 3.3 V
V_{CC2} = 5 V T_A = 25°C

图 7. Driver Output Voltage Vs Driver Output Current

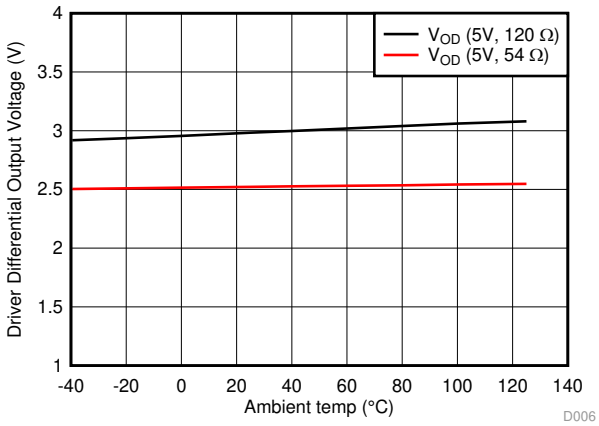
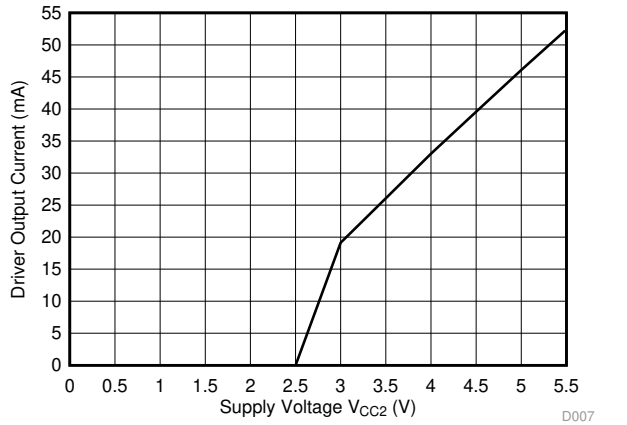
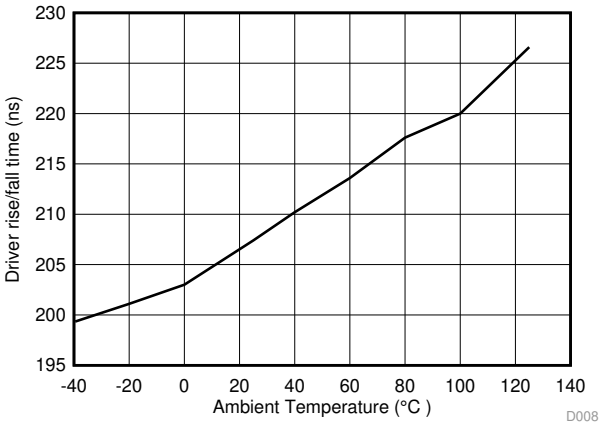


图 8. Driver Differential Output Voltage Vs Temperature



T_A = 25°C R_L = 54 ohm DE = D = V_{CC1}

图 9. Driver Output Current Vs Supply Voltage (V_{CC2})



V_{CC1} = 3.3 V V_{CC2} = 5 V

图 10. Driver rise/fall time vs Temperature

Typical Characteristics (接下页)

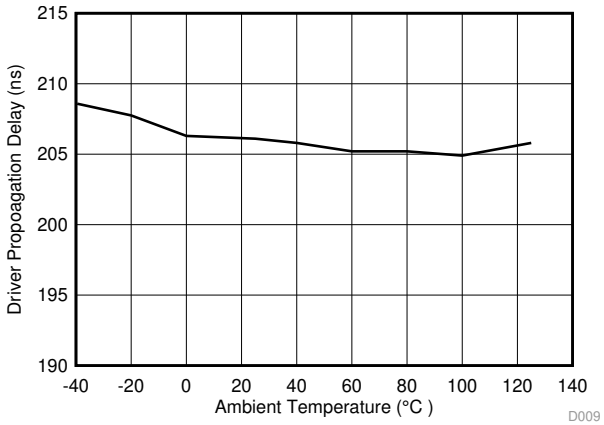


图 11. Driver Propagation Delay vs Temperature

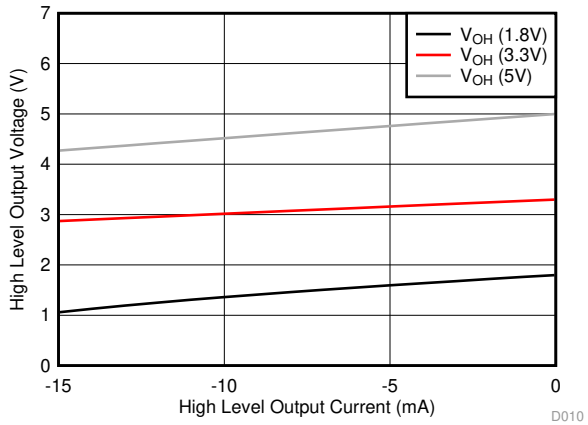


图 12. Receiver Buffer High Level Output Voltage Vs High Level Output Current

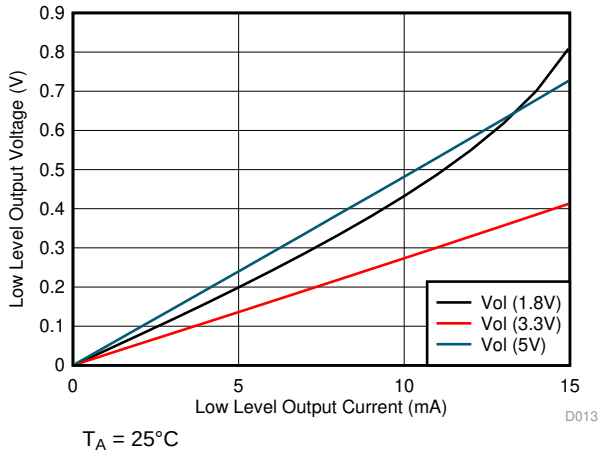


图 13. Receiver Buffer Low Level Output Voltage Vs Low Level Output Current

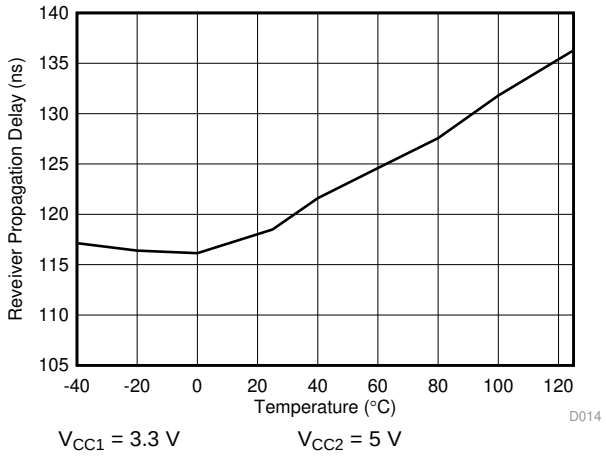


图 14. Receiver Propagation Delay Vs Temperature

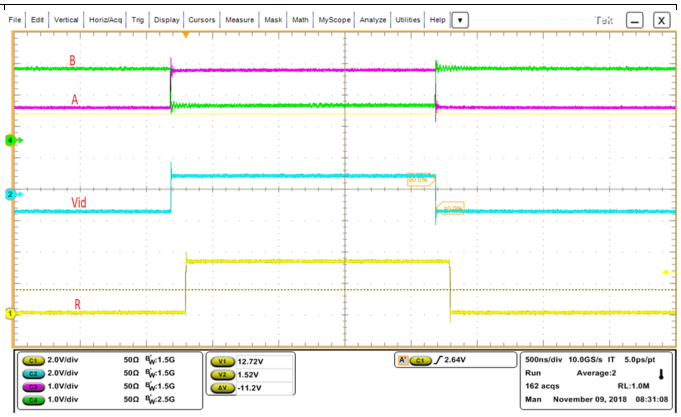
Typical Characteristics (接下页)

V_{CC1} = 3.3 V
T_A = 25°C

V_{CC2} = 5 V

DE = V_{CC1}

图 15. Driver Propagation delay



V_{CC1} = 3.3 V
DE = GND1

V_{CC2} = 5 V
$\overline{RE}$ = GND1

T_A = 25°C,

图 16. Receiver Propagation Delay

图 17. V_{CC1} Power Up / Power down- Glitch Free Behavior

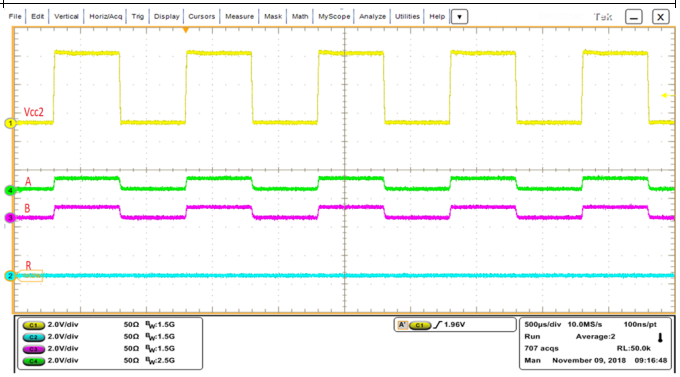


图 18. V_{CC2} Power Up / Power down- Glitch Free Behavior

7 Parameter Measurement Information

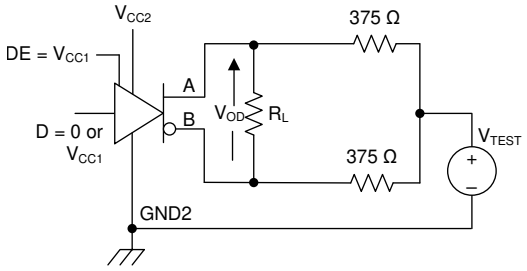
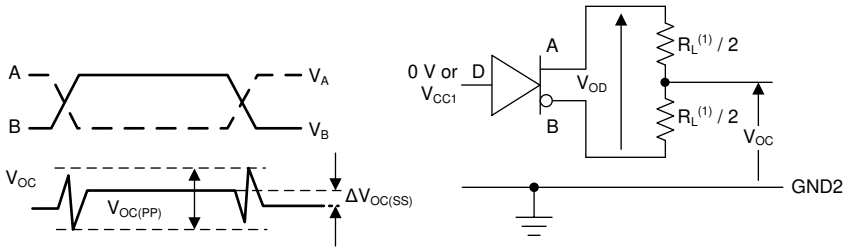
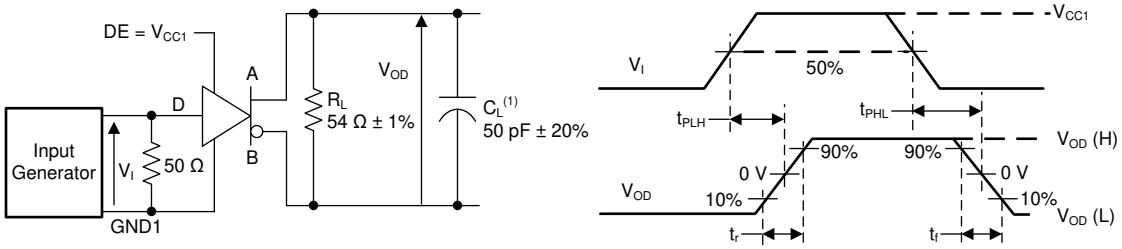


图 19. Driver Voltages



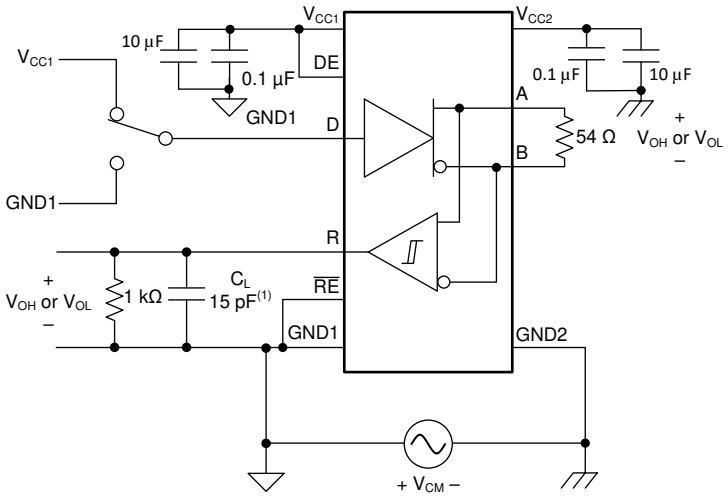
(1) R_L = 100 Ω for RS422, R_L = 54 Ω for RS-485

图 20. Driver Voltages



(1) C_L includes fixture and instrumentation capacitance.

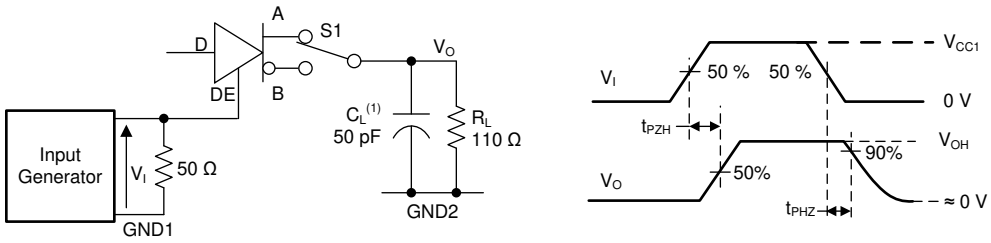
图 21. Driver Switching Specifications



(1) Includes probe and fixture capacitance.

图 22. Common Mode Transient Immunity (CMTI)—Half Duplex

Parameter Measurement Information (接下页)



(1) C_L includes fixture and instrumentation capacitance

图 23. Driver Enable and Disable Times

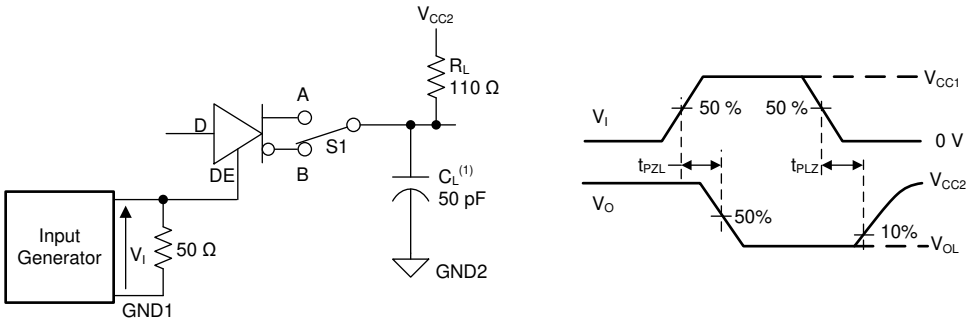
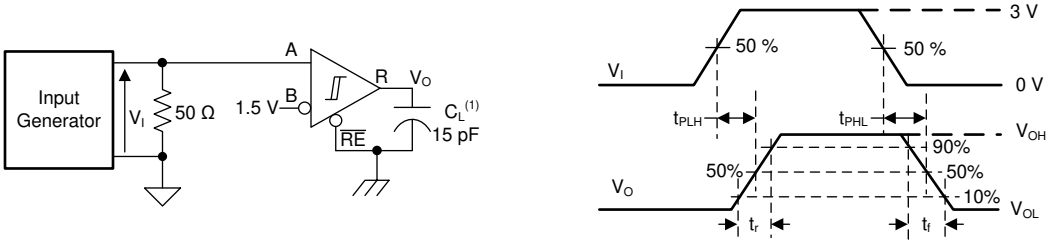


图 24. Driver Enable and Disable Times



(1) C_L includes fixture and instrumentation capacitance.

图 25. Receiver Switching Specifications

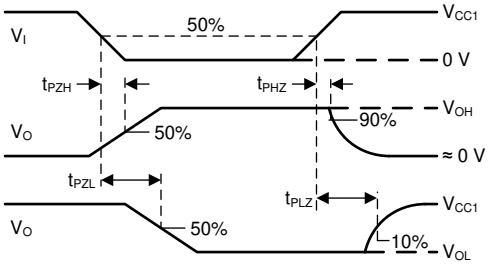


图 26. Receiver Enable and Disable Times

Parameter Measurement Information (接下页)

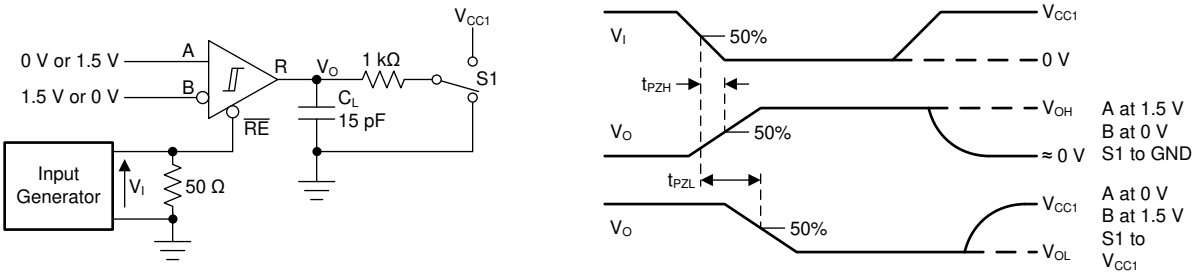
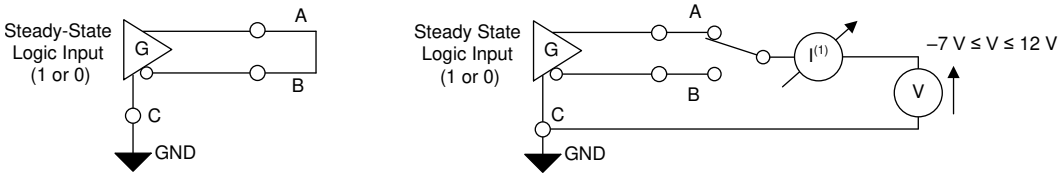


图 27. Receiver Enable and Disable Times



(1) The driver should not sustain any damage with this configuration.

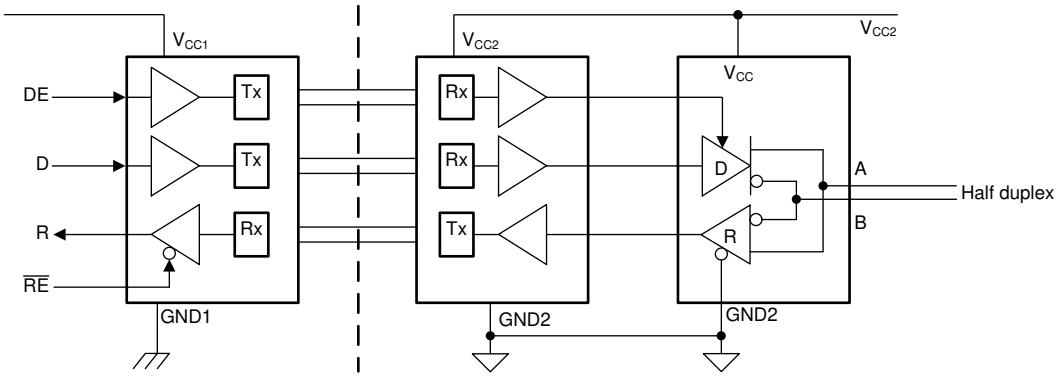
图 28. Short-Circuit Current Limiting

8 Detailed Description

8.1 Overview

The ISO1500 device is an isolated RS-485/RS-422 transceiver designed to operate in harsh industrial environments. This device supports data transmissions up to 1 Mbps. The ISO1500 device has a 3-channel digital isolator and an RS-485 transceiver in an ultra-small SSOP package. The silicon-dioxide based capacitive isolation barrier supports an isolation withstand voltage of 3 kV_{RMS} and an isolation working voltage of 566 V_{PK}. Isolation breaks the ground loop between the communicating nodes and lets data transfer in the presence of large ground potential differences. The wide logic supply of the device (V_{CC1}) supports interfacing with 1.8-V, 2.5-V, 3.3-V. and 5-V control logic. Functional Block Diagram shows the functional block diagram of the the half-duplex device.

8.2 Functional Block Diagram



8.3 Feature Description

表 1 shows an overview of the device features.

表 1. Device Features

PART NUMBER	ISOLATION	DUPLEX	DATA RATE	PACKAGE
ISO1500	Basic	Half	1 Mbps	16-pin SSOP

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO1500 device has dedicated circuitry to help protect the transceiver from Contact ESD per IEC61000-4-2.

8.3.2 Failsafe Receiver

The differential receiver of the ISO1500 device has failsafe protection from invalid bus states caused by:

- Open bus conditions such as a broken cable or a disconnected connector
- Shorted bus conditions such as insulation breakdown of a cable that shorts the twisted-pair
- Idle bus conditions that occur when no driver on the bus is actively driving

The differential input of the RS-485 receiver is 0 in any of these conditions for a terminated transmission line. The receiver outputs a failsafe logic-high state so that the output of the receiver is not indeterminate.

The receiver thresholds are offset in the receiver failsafe protection so that the indeterminate range of the input does not include a 0 V differential. The receiver output must generate a logic high when the differential input (V_{ID}) is greater than 200 mV to comply with the RS-485 standard. The receiver output must also generate a output a logic low when V_{ID} is less than –200 mV to comply with the RS-485 standard. The receiver parameters that determine the failsafe performance are V_{TH+}, V_{TH-}, and V_{HYS}. Differential signals less than –200 mV always cause a low receiver output as shown in the *Electrical Characteristics* table. Differential signals greater than 200 mV always cause a high receiver output. A differential input signal that is near zero is still greater than the V_{TH+} threshold which makes the receiver output logic high. The receiver output goes to a low state only when the differential input decreases by V_{HYS} to less than V_{TH+}.

The internal failsafe biasing feature removes the need for the two external resistors that are typically required with traditional isolated RS-485 transceivers as shown in 图 29.

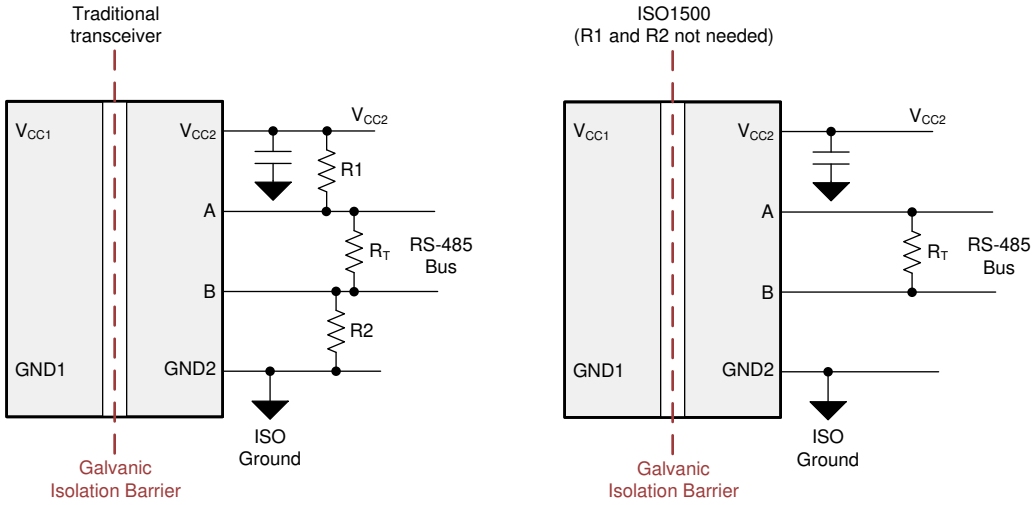


图 29. Failsafe Transceiver

8.3.3 Thermal Shutdown

The ISO1500 device has a thermal shutdown circuit to protect against damage when a fault condition occurs. A driver output short circuit or bus contention condition can cause the driver current to increase significantly which increases the power dissipation inside the device. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 170℃ (typical) which lets the device decrease the temperature. The device is enabled when the junction temperature becomes 163℃ (typical).

8.3.4 Glitch-Free Power Up and Power Down

Communication on the bus that already exist between a master node and slave node in an RS485 network must not be disturbed when a new node is swapped in or out of the network. No glitches on the bus occur when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and disabled state
- Powered up or powered down in a disabled state when already connected to the bus

The ISO1500 device does not cause any false data toggling on the bus when powered up or powered down in a disabled state with supply ramp rates from 100 µs to 10 ms.

8.4 Device Functional Modes

表 2 shows the driver functional modes.

表 2. Driver Functional Table(1)

V_{CC1}	V_{CC2}	INPUT D	DRIVER ENABLE DE	OUTPUTS	
				A	B
PU	PU	H	H	H	L
		L	H	L	H
		X	L	Hi-Z	Hi-Z
		X	Open	Hi-Z	Hi-Z
		Open	H	H	L
PD(2)	PU	X	X	Hi-Z	Hi-Z
X	PD	X	X	Hi-Z	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = High Level; L = Low level; X = Irrelevant, Hi-Z = High impedance state
(2) A strongly driven input signal can weakly power the floating V_{CC1} through an internal protection diode and cause an undetermined output.

When the driver enable pin, DE, is logic high, the differential outputs, A and B, follow the logic states at data input, D. A logic high at the D input causes the A output to go high and the B output to go low. Therefore the differential output voltage defined by 公式 1 is positive.

$$V_{OD} = V_A - V_B \quad (1)$$

A logic low at the D input causes the B output to go high and the A output to go low. Therefore the differential output voltage defined by 公式 1 is negative. A logic low at the DE input causes both outputs to go to the high-impedance (Hi-Z) state. The logic state at the D pin is irrelevant when the DE input is logic low. The DE pin has an internal pulldown resistor to ground. The driver is disabled (bus outputs are in the Hi-Z) by default when the DE pin is left open. The D pin has an internal pullup resistor. The A output goes high and the B output goes low when the D pin is left open while the driver enabled.

表 3 shows the receiver functional modes.

表 3. Receiver Functional Table(1)

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT	RECEIVER ENABLE $\overline{RE}$	OUTPUT R
		$V_{ID} = V_A - V_B$		
PU	PU	$-0.02\ V \le V_{ID}$	L	H
		$-0.2\ V < V_{ID} < 0.02\ V$	L	Indeterminate
		$V_{ID} \le -0.2\ V$	L	L
		X	H	Hi-Z
		X	Open	Hi-Z
		Open, Short, Idle	L	H
PD(2)	PU	X	X	Hi-Z
PU	PD	X	L	H
PD(2)	PD	X	X	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (OFF) state
(2) A strongly driven input signal can weakly power the floating V_{CC1} through an internal protection diode and cause an undetermined output.

The receiver is enabled when the receiver enable pin, $\overline{RE}$, is logic low. The receiver output, R, goes high when the differential input voltage defined by 公式 2 is greater than the positive input threshold, V_{TH+}.

$$V_{ID} = V_A - V_B \quad (2)$$

The receiver output, R, goes low when the differential input voltage defined by 公式 2 is less than the negative input threshold, V_{TH-}. If the V_{ID} voltage is between the V_{TH+} and V_{TH-} thresholds, the output is indeterminate. The receiver output is in the Hi-Z state and the magnitude and polarity of V_{ID} are irrelevant when the $\overline{RE}$ pin is logic high or left open. The internal biasing of the receiver inputs causes the output to go to a failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

8.4.1 Device I/O Schematics

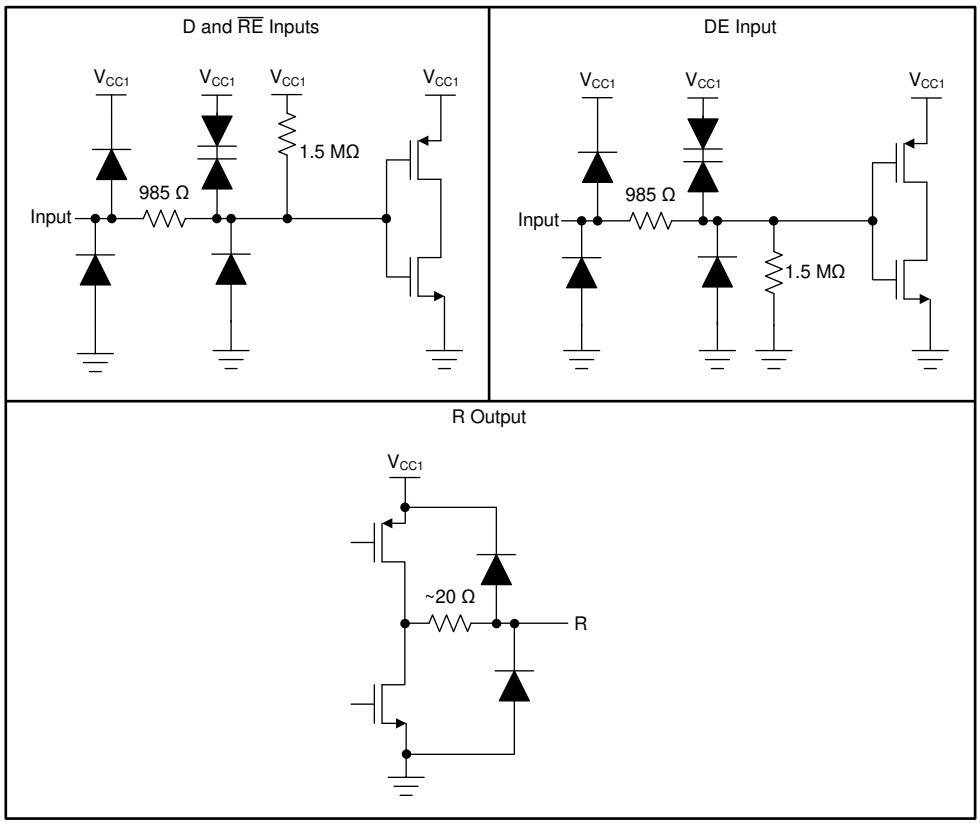


图 30. Device I/O Schematics

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO1500 device is designed for bidirectional data transfer on multipoint RS-485 networks. The design of each RS-485 node in the network requires an ISO1500 device and an isolated power supply as shown in 图 32.

An RS-485 bus has multiple transceivers that connect in parallel to a bus cable. Both cable ends are terminated with a termination resistor, R_T, to remove line reflections. The value of R_T matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, lets higher data rates be used over a longer cable length.

In half-duplex implementation, as shown in 图 31, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements.

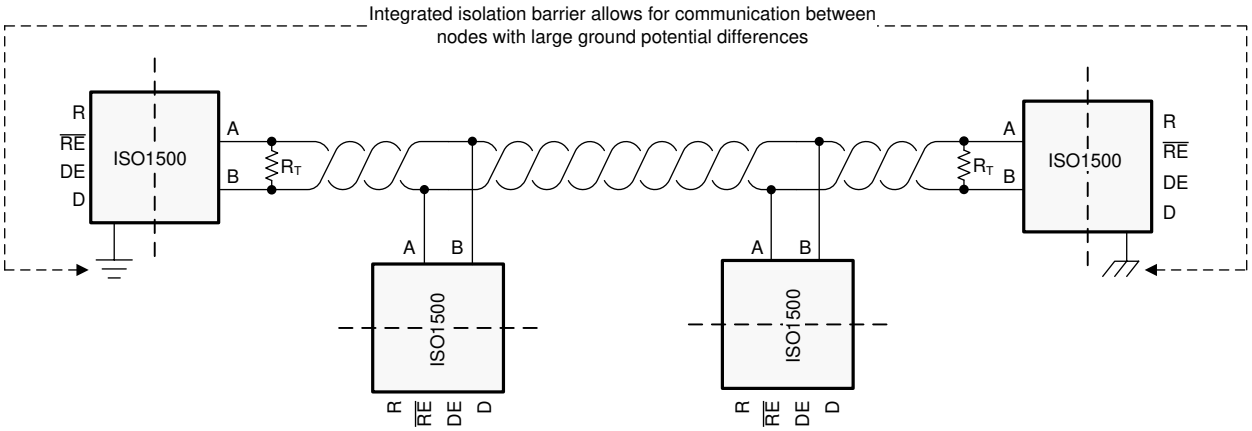


图 31. Half-Duplex Network Circuit

9.2 Typical Application

图 32 shows the application circuit of the ISO1500 device.

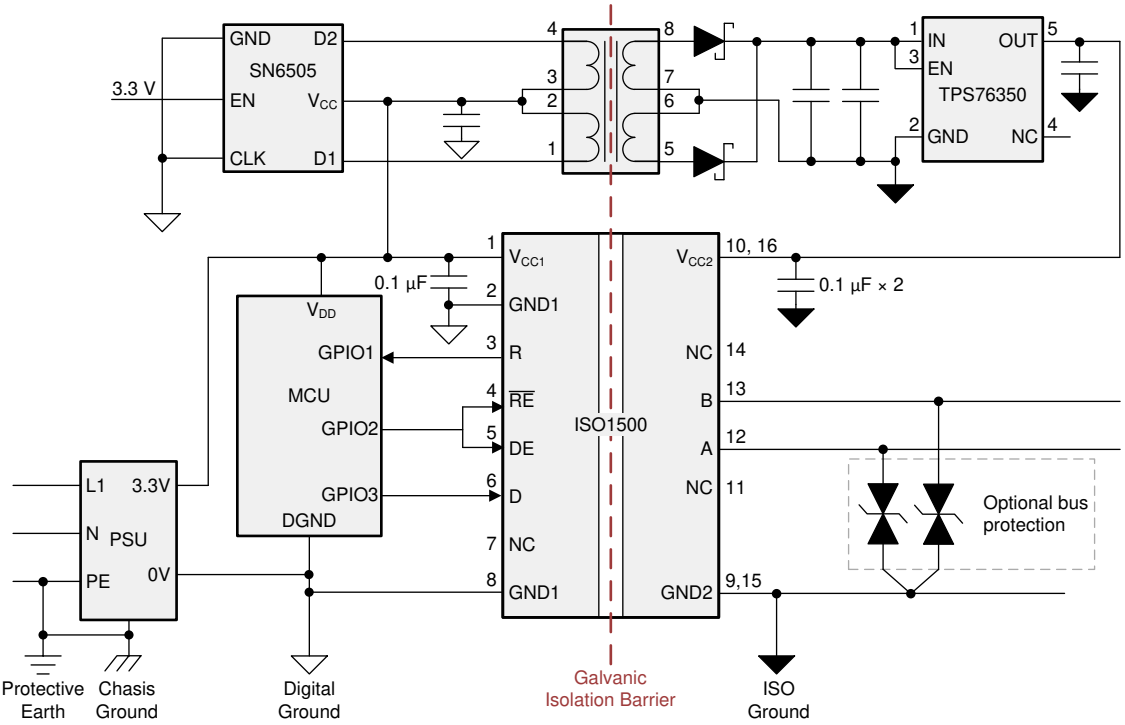


图 32. Typical Application

9.2.1 Design Requirements

Unlike an optocoupler-based solution, which requires several external components to improve performance, provide bias, or limit current, the ISO1500 device only requires external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

The RS-485 bus is a robust electrical interface suitable for long-distance communications. The RS-485 interface can be used in a wide range of applications with varying requirements of distance of communication, data rate, and number of nodes.

9.2.2.1 Data Rate and Bus Length

The RS-485 standard has typical curves similar to those shown in 图 33. These curves show the inverse relationship between signaling rate and cable length. If the data rate of the payload between two nodes is lower, the cable length between the nodes can be longer.

Typical Application (接下页)

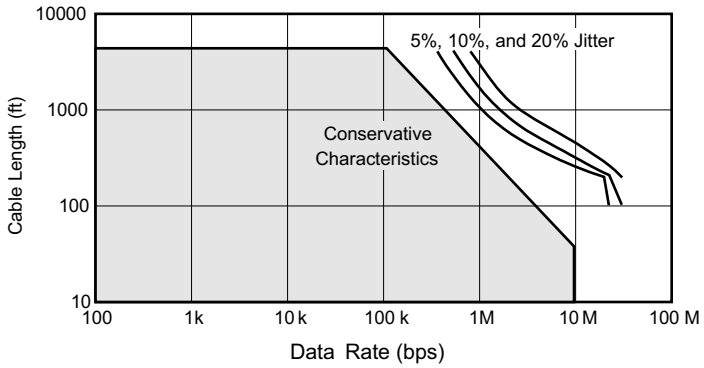


图 33. Cable Length vs Data Rate Characteristics

Applications can increase the cable length at slower data rates compared to what is shown in 图 33 by allowing for jitter of 5% or higher. Use 图 33 as a guideline for cable selection, data rate, cable length and subsequent jitter budgeting.

9.2.2.2 Stub Length

In an RS-485 network, the distance between the transceiver inputs and the cable trunk is known as the *stub*. The stub should be as short as possible when a node is connected to the bus. Stubs are a non-terminated piece of bus line that can introduce reflections of varying phase as the length of the stub increases. The electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver as a general guideline. Therefore, the maximum physical stub length ($L_{(STUB)}$) is calculated as shown in 公式 3.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (3)$$

where

- t_r is the 10/90 rise time of the driver.
- c is the speed of light (3×10^8 m/s).
- v is the signal velocity of the cable or trace as a factor of c.

9.2.2.3 Bus Loading

The current supplied by the driver must supply into a load because the output of the driver depends on this current. Add transceivers to the bus to increase the total bus loading. The RS-485 standard specifies a hypothetical term of a unit load (UL) to estimate the maximum number of possible bus loads. The UL represents a load impedance of approximately 12 kΩ. Standard-compliant drivers must be able to drive 32 of these ULs.

The ISO1500 device has 1/8 UL impedance transceiver and can connect up to 256 nodes to the bus.

10 Power Supply Recommendations

To make sure device operation is reliable at all data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the logic and transceiver supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as near to the supply pins as possible. Side 2 requires one V_{CC2} decoupling capacitor on each V_{CC2} pin. If only one primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6505B device. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 34). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

图 35 shows the recommended placement and routing of the device bypass capacitors and optional TVS diodes. Put the two V_{CC2} bypass capacitors on the top layer and as near to the device pins as possible. Do not use vias to complete the connection to the V_{CC2} and GND2 pins. If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

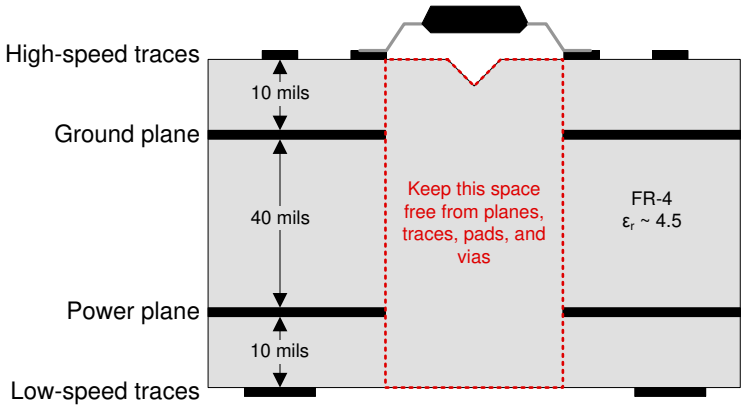


Figure 34. Recommended Layer Stack

Layout Example (接下页)

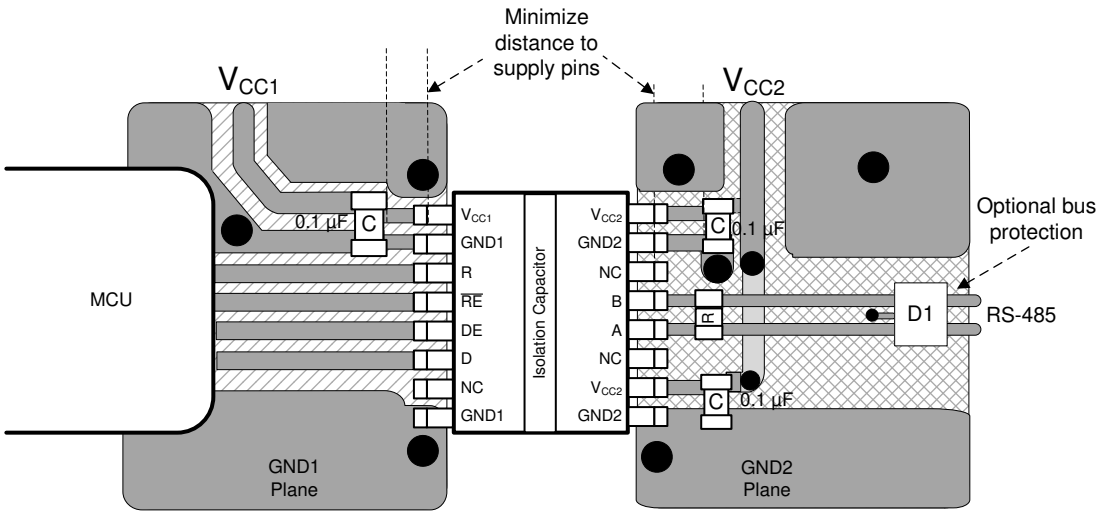


图 35. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《数字隔离器设计指南》*
- 德州仪器 (TI)，*《隔离相关术语》*
- 德州仪器 (TI)，*《ISO1500 隔离式 RS-485 半双工评估模块》*用户指南

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商标

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12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1500DBQ	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1500	Samples
ISO1500DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1500	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

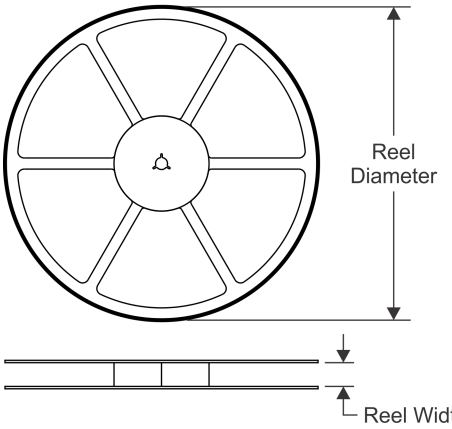
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

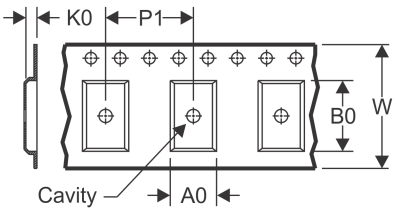
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

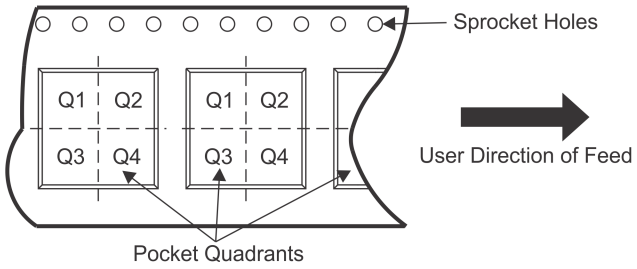


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

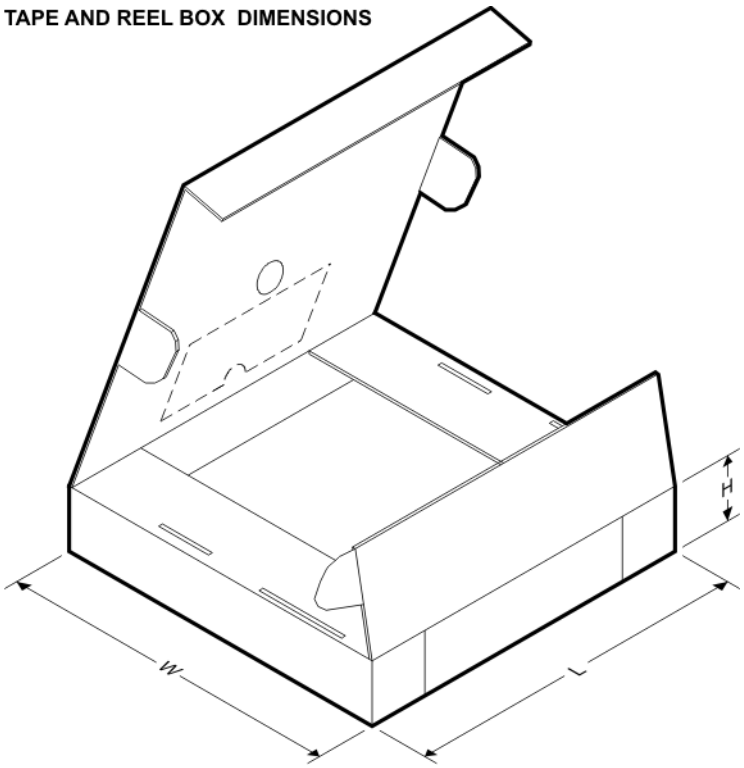
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

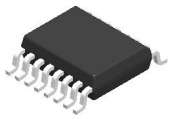
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1500DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1500DBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0

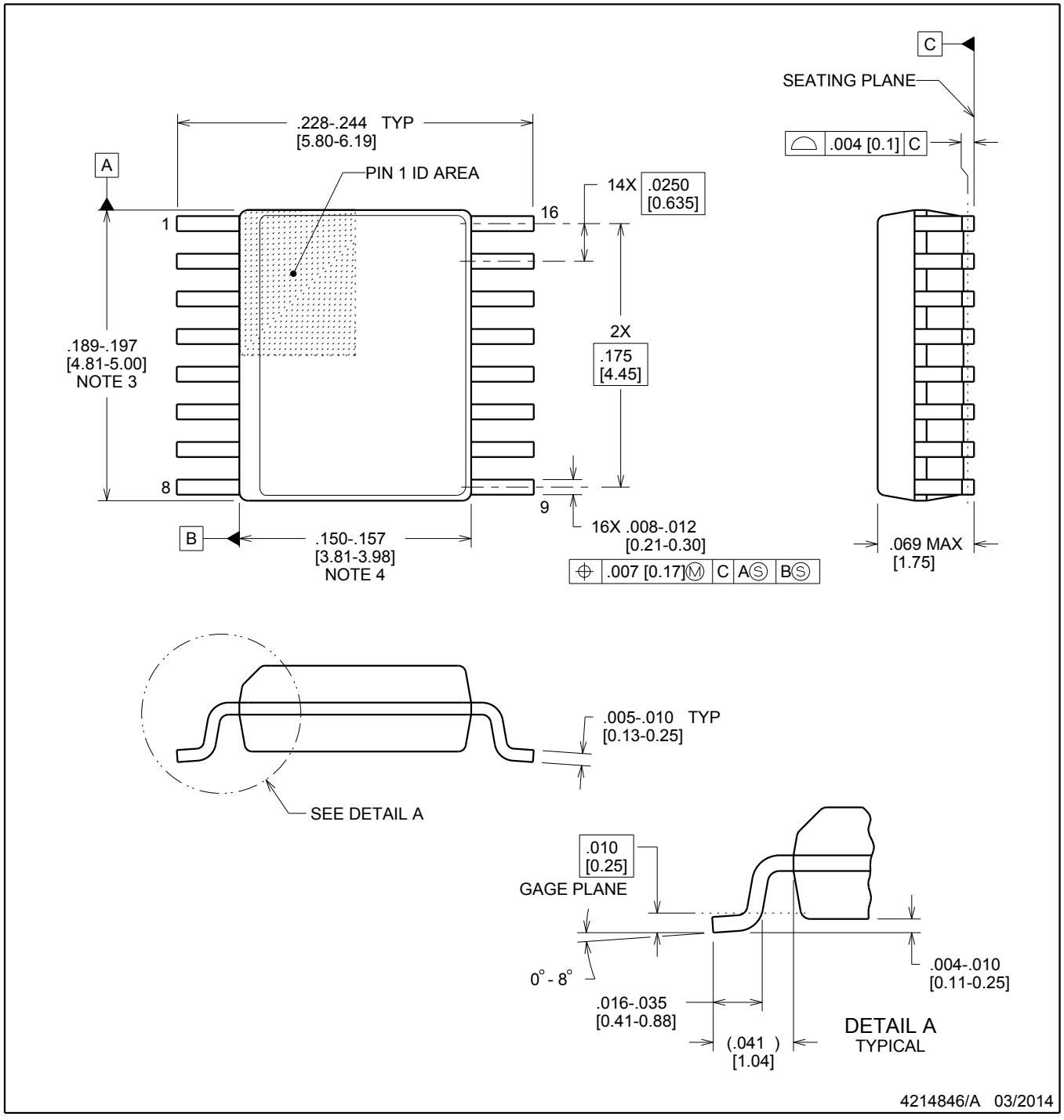


PACKAGE OUTLINE

DBQ0016A

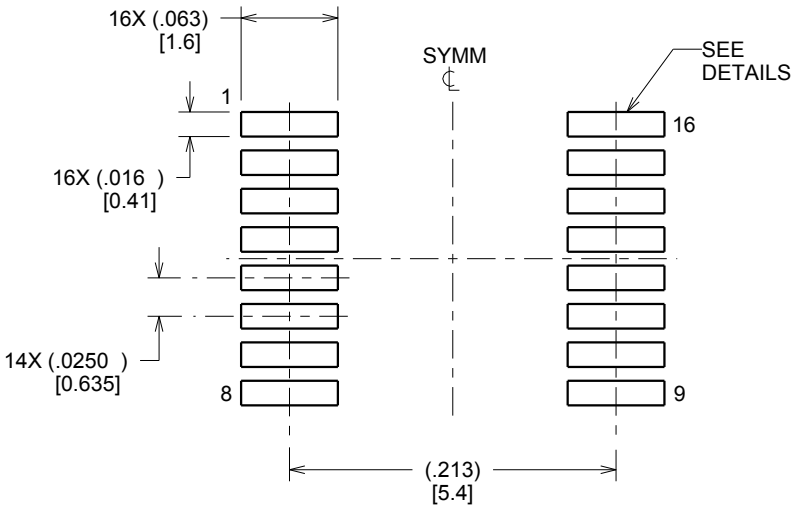
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

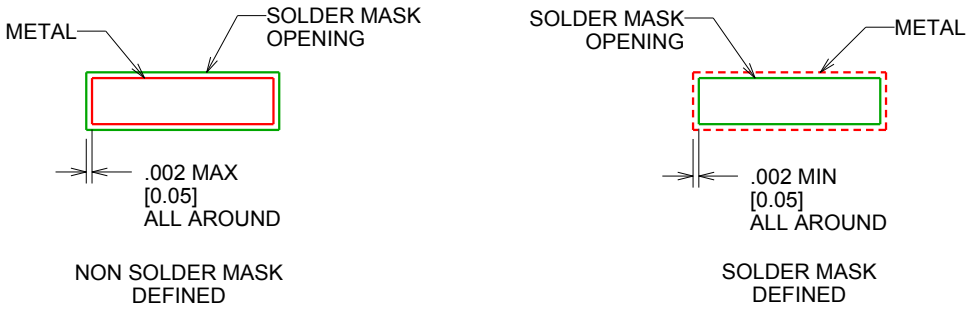


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

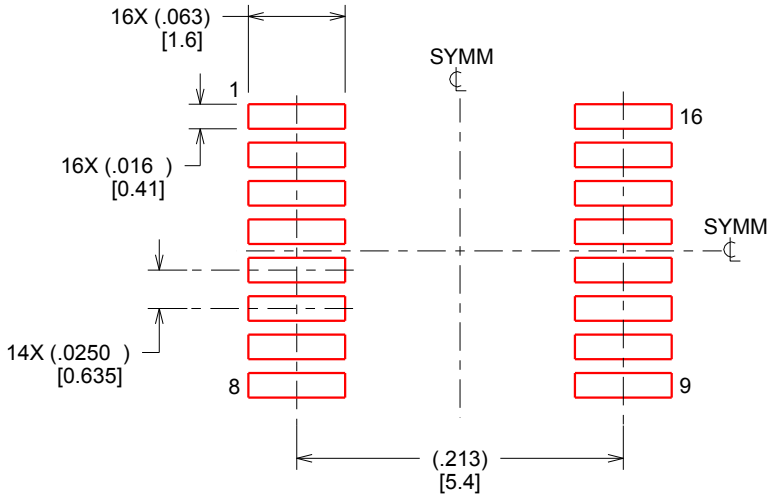
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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