DLPR410 配置 PROM

1 特性

- 预编程的 Xilinx®PROM 用于配置 DLPC410 DMD 数字控制器
- 兼容 1.8V 到 3.3V 的 I/O 引脚
- 1.8V 内核电源电压
- 工作温度范围：-40°C 至 +85°C

2 应用

- 直接成像平版印刷系统
- 3D 打印 [SLA 和 SLS]
- 3D 机器视觉
- 用于机器人和检测系统的 3D 扫描仪
- 动态灰度激光打标和编码
- 工业印刷
- 高速投影和高级成像
- 消融和修复系统
- 显微镜

3 说明

DLPR410 器件是一款经编程的 PROM，用于正确配置 DLPC410 控制器，从而运行五个 DMD 选件：DLP650LNIR、DLP7000、DLP7000UV、DLP9500 和 DLP9500UV。此器件中的固件使 DLPC410 控制器能够提供高达 48 千兆位/秒 (Gbps)的系统数据吞吐量，并提供随机行寻址和 Load4 功能选项。通常，此系列芯片设计用于高速 UV 和 NIR 光学系统，例如需要快速吞吐量和像素精确控制的直接成像平版印刷系统、3D 打印和激光打标设备。 中添加了 DLPR4101“Load 4”增强功能

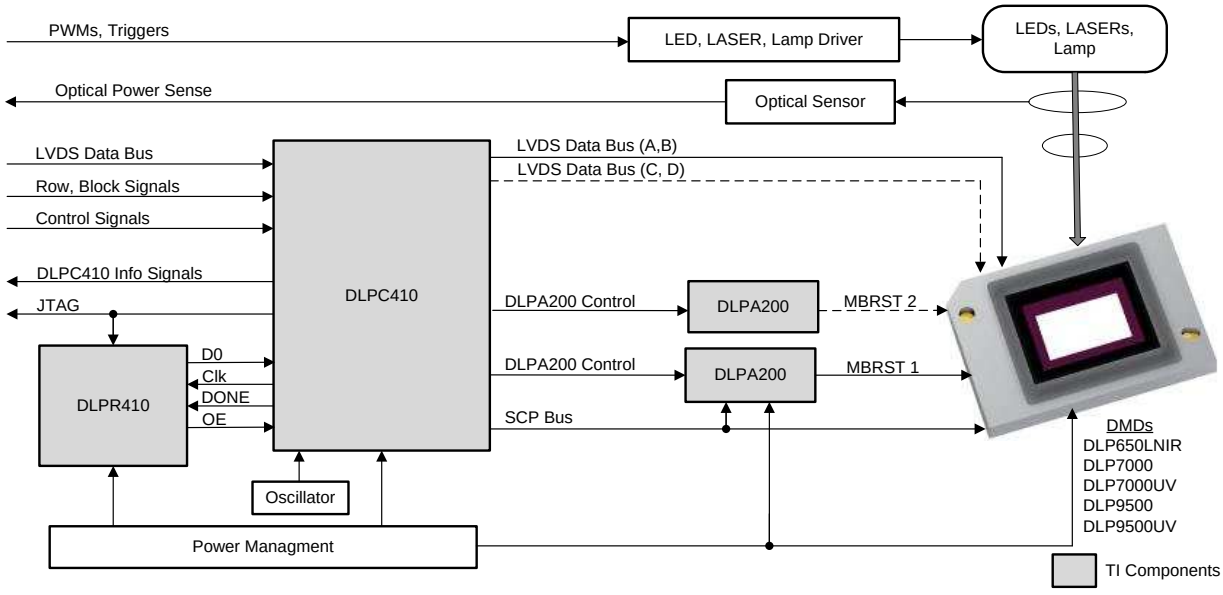
有关 DLPR410 的完整电气规格和机械规格，请参阅表 3 中列出的 XCF16P 产品规格。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLPR410	DSBGA (48)	8.00mm × 9.00mm × 1.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

4 简化应用



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

5 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (April 2015) to Revision E — **Page**

- 更新了*应用* 和*说明* 以包含新的 DLP650LNIR，删除了数据传输速率 ... 1
- 已更改 应用图以包含 DLP650LNIR DMD ... 1
- Corrected Min Tstorage per Xilinx data sheet ... 6
- Corrected Min VCCO per Xilinx data sheet ... 6
- Added support information for new DLP650LNIR DMD (multiple places) ... 8
- Updated Functional Block Diagram ... 8
- Corrected improper "DLPC910" reference to "DLPC410" ... 11
- Updated Figure 2 ... 11
- 添加了器件兼容性 表 ... 12
- 更新了器件命名规则 ... 12
- 更新了*器件标记* 部分 ... 13
- 已添加 向表 3 部分中添加 DLP650LNIR ... 14
- 已删除 表 3 中的 DLP Discovery 4100 芯片组参考 ... 14

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- 更新了*特性*、*应用*和*说明* ... 1
- 已删除 通篇删除了 DLPR4101（增强功能 PROM 器件型号） ... 1
- 添加了*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 将框图移至“典型应用”部分 ... 1
- Deleted 1.8 V and 3.3 V operation values from V_{CCO}, V_{IL}, and V_{IH} - this implementation is 2.5 V ... 6
- 已更改 器件标记图像 ... 13
- 已更改 器件标记图像 ... 13
- 已删除 *相关文档*中的 DLP® Discovery™ 4100 芯片组数据表 ... 14
- 已添加 链接至 xilinx.com 上的 XCF16P 数据表 ... 14

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- 已添加 器件俯视图 1
- 已添加 在 特性 1
- 已添加 通篇将 DLPR410 和 DLPR4101（增强功能 PROM 器件型号）更改为 DLPR410 1
- 添加了数据表链接 1
- Added the Version column to the *Ordering Information* table 4
- Updated DLPC and DLP7000 / DLP7000UV Embedded Example Block Diagram 11
- 已添加 DLPR4101YVA，等同于德州仪器 (TI) 器件型号 2510442-0006 12
- 已添加 “参考文献”至 DLPC410 数据表 12
- 已添加 DLPR410 至 图 4 12
- 已添加 “器件顶视图”至器件标记 12
- 已添加 DLP7000UV 相关文档 14
- 已添加 DLP9500UV 相关文档 14

Changes from Revision A (September 2012) to Revision B **Page**

- Changed the top-side marking in the *Ordering Information* table 4

Changes from Original (August 2012) to Revision A **Page**

- 将器件状态从“产品预览”更改成了“生产” 1

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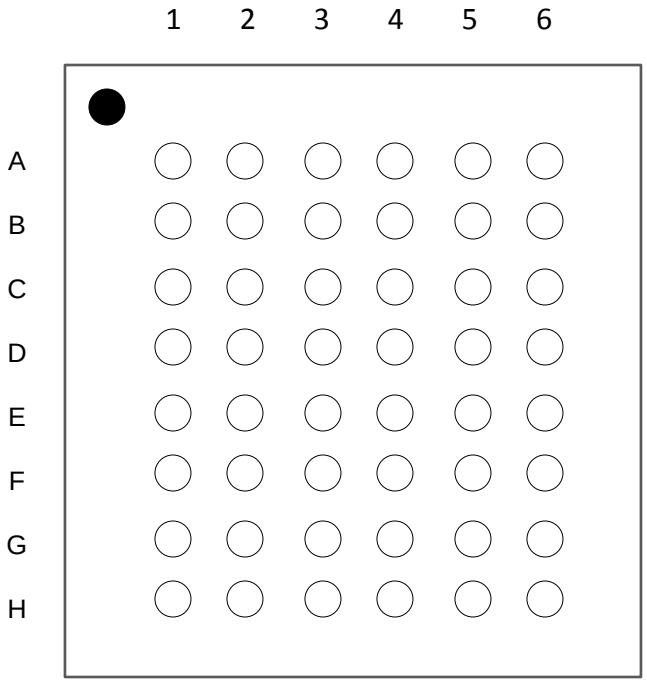
6 Pin Configuration and Functions

YVA Package
48-Pin DSBGA
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	A1	G	Ground
GND	A2	G	Ground
OE/$\overline{\text{RESET}}$	A3	I/O	Output Enable/$\overline{\text{RESET}}$ (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable. **Pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.**
DNC1	A4	—	Do Not Connect. Leave unconnected.
D6	A5	—	Do Not Connect. Leave unconnected.
D7	A6	—	Do Not Connect. Leave unconnected.
VCCINT1	B1	P	Positive 1.8-V supply voltage for internal logic.
VCCO1	B2	P	Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers.
CLK	B3	I	Do Not Connect. Leave unconnected.
$\overline{\text{CE}}$	B4	I	Chip Enable Input. When $\overline{\text{CE}}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high impedance state.
D5	B5	—	Do Not Connect. Leave unconnected.
GND	B6	G	Ground
BUSY	C1	—	Do Not Connect. Leave unconnected.
CLKOUT	C2	—	Configuration clock output. Each rising edge on the CLK input increments the internal address counter. **Pin must be pulled High and Low using an external 100-Ω pull-up to V_{CCO} and an external 100-Ω pull-down to Ground. Place resistors close to pin**.

(1) P = Power, G = Ground, I = Input, O = Output

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DNC2	C3	—	Do Not Connect. Leave unconnected.
DNC3	C4	—	Do Not Connect. Leave unconnected.
D4	C5	—	Do Not Connect. Leave unconnected.
VCCO2	C6	P	Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers.
$\overline{CF}$	D1	I	Configuration pin. **The $\overline{CF}$ pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}**. Selects serial mode configuration.
$\overline{CEO}$	D2	—	Do Not Connect. Leave unconnected.
DNC10	D3	—	Do Not Connect. Leave unconnected.
DNC11	D4	—	Do Not Connect. Leave unconnected.
D3	D5	—	Do Not Connect. Leave unconnected.
VCCO4	D6	P	Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers.
VCCINT2	E1	P	Positive 1.8-V supply voltage for internal logic.
TMS	E2	I	JTAG Mode Select Input. TMS has an internal 50-kΩ resistive pull-up to V_{CCJ}.
DNC4	E3	—	Do Not Connect. Leave unconnected.
DNC5	E4	—	Do Not Connect. Leave unconnected.
D2	E5	—	Do Not Connect. Leave unconnected.
TDO	E6	O	JTAG Serial Data Output. TDO has an internal 50-kΩ resistive pull-up to V_{CCJ}.
GND	F1	G	Ground
DNC6	F2	—	Do Not Connect. Leave unconnected.
DNC7	F3	—	Do Not Connect. Leave unconnected.
DNC8	F4	—	Do Not Connect. Leave unconnected.
GND	F5	G	Ground
GND	F6	G	Ground
TDI	G1	I	JTAG Serial Data Input. TDI has an internal 50k-Ω resistive pull-up to V_{CCJ}.
DNC9	G2	—	Do Not Connect. Leave unconnected.
REV_SEL0	G3	I	Revision Select [1:0] Inputs. When the $\overline{EN\_EXT\_SEL}$ is Low, the Revision Select pins are used to select the design revision to be enabled. The Revision Select [1:0] inputs have an internal 50-kΩ resistive pull-up to V_{CCO}. **The REV_SEL0 pin must be pulled Low using an external 10-kΩ pull-down to Ground**. **The REV_SEL1 pin must be connected to Ground**.
REV_SEL1	G4	I	
VCCO3	G5	P	Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers.
VCCINT3	G6	P	Positive 1.8-V supply voltage for internal logic.
GND	H1	G	Ground
VCCJ	H2	P	Positive 2.5-V JTAG I/O supply voltage connected to the TDO output voltage driver and TCK, TMS and TDI input buffers.
TCK	H3	I	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.
$\overline{EN\_EXT\_SEL}$	H4	I	External Selection Input. $\overline{EN\_EXT\_SEL}$ has an internal 50-kΩ resistive pull- up to V_{CCO}. **The $\overline{EN\_EXT\_SEL}$ pin must be connected to Ground**.
D1	H5	—	Do Not Connect. Leave unconnected.
D0	H6	O	DATA output pin to provide data for configuring the DLPC410 in serial mode.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see (1) (2))

			MIN	MAX	UNIT
V_{CCINT}	Internal supply voltage	Relative to ground	–0.5	2.7	V
V_{CCO}	I/O supply voltage	Relative to ground	–0.5	4.0	V
V_{IN}	Input voltage with respect to ground	V_{CCO} < 2.5 V	–0.5	3.6	V
		V_{CCO} ≥ 2.5 V	–0.5	3.6	V
V_{TS}	Voltage applied to high-impedance output	V_{CCO} < 2.5 V	–0.5	3.6	V
		V_{CCO} ≥ 2.5 V	–0.5	3.6	V
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature, ambient		–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA. During transitions, the device pins can undershoot to –2 V or overshoot to 7 V, provided this overshoot or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2) (3)	2000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC Standard JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CCINT}	Internal voltage supply		1.65	1.8	2.0	V
V_{CCO}	Supply voltage for output drivers	2.5-V operation	2.3	2.5	2.7	V
V_{IL}	Low-level input voltage	2.5-V operation	0		0.7	V
V_{IH}	High-level input voltage	2.5-V operation	1.7		3.6	V
V_O	Output voltage		0		V_{CCO}	V
t_{IN}	Input signal transition time (measured between 10% V_{CCO} and 90% V_{CCO})				500	ns
T_A	Operating ambient temperature		–40		85	°C

7.4 Thermal Information

Refer to the XCF16P product specifications at www.xilinx.com.

7.5 Electrical Characteristics

Refer to the XCF16P product specifications at www.xilinx.com.

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7.6 Supply Voltage Requirements for Power-On Reset and Power-Down

(see (1))

		MIN	MAX	UNIT
t_{VCC}	V_{CCINT} rise time from 0 V to nominal voltage (2)	0.2	50	ms
V_{CCPOR}	POR threshold for V_{CCINT} supply	0.5	–	V
t_{OER}	OE/$\overline{\text{RESET}}$ release delay following POR (3)	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply		0.5	V
t_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10		ms

(1) V_{CCINT}, V_{CCO}, and V_{CCJ} supplies can be applied in any order.
(2) At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 6, in the Xilinx XCF16P (v2.18) Product Specification for more information.
(3) If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

7.7 Timing Requirements

Refer to the XCF16P product specifications at www.xilinx.com.

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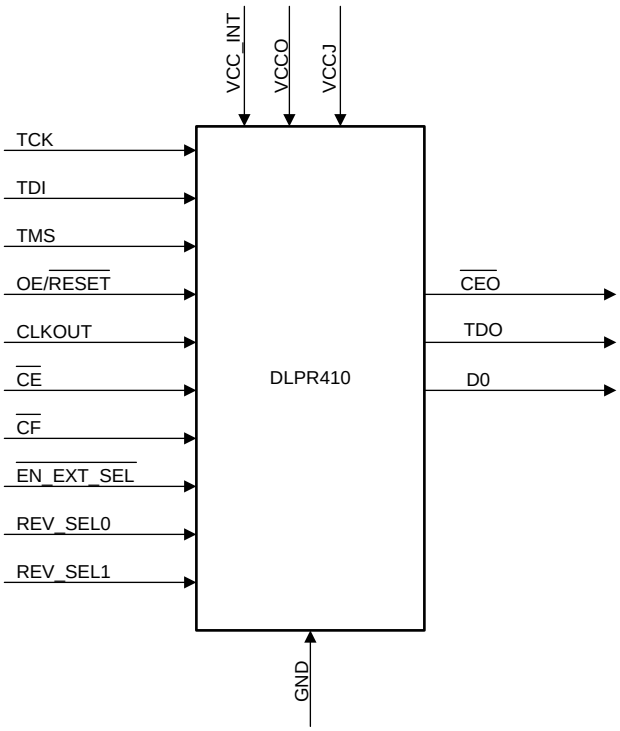
8 Detailed Description

8.1 Overview

The configuration bit stream stored in the DLPR410 device supports reliable operation of the DLPC410 device with the DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs. The DLPC410 digital controller loads this configuration bit stream from the DLPR410 device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Data Interface

8.3.1.1 Data Outputs

The DLPR410 device s configured for serial mode operation, where D0 is the data output pin. D0 output pin provides a serial connection to the DLPC410, where the configuration is read out by the DLPC410.

8.3.1.2 Configuration Clock Input

The configuration CLK is connected to the DLPC410 in Master Serial mode, where the DLPC410 provides the clock pulses to read the configuration from the DLPR410 device.

8.3.1.3 Output Enable and Reset

When the OE/$\overline{\text{RESET}}$ input is held low, the address counter is reset and the Data and CLKOUT outputs are placed in high-impedance state. **OE/$\overline{\text{RESET}}$ must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.**

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Feature Description (continued)

8.3.1.4 Chip Enable

The $\overline{CE}$ input is asserted by the DLPC410 to enable the Data and CLKOUT outputs. When $\overline{CE}$ is held high, the DLPR410 device address counter is reset, and the Data and CLKOUT outputs are placed in high-impedance states.

8.3.1.5 Configuration Pulse

The DLPR410 device is configured in serial mode when it holds configuration pulse pin, $\overline{CF}$, high and it enables the $\overline{CE}$ and OE pins. New data is available a short time after each rising clock edge.

8.3.1.6 Revision Selection

The device uses the REV_SEL_0, REV_SEL_1, and $\overline{EN\_EXT\_SEL}$ signals to select a revision to act as the default. Setting all three signals to GND defaults to revision 0 for simple DLPR410 device setup.

8.4 Device Functional Modes

To successfully program the DLPC410 upon power-up, the DLPR410 device must be configured and connected to the DLPC410 as shown in Figure 1.

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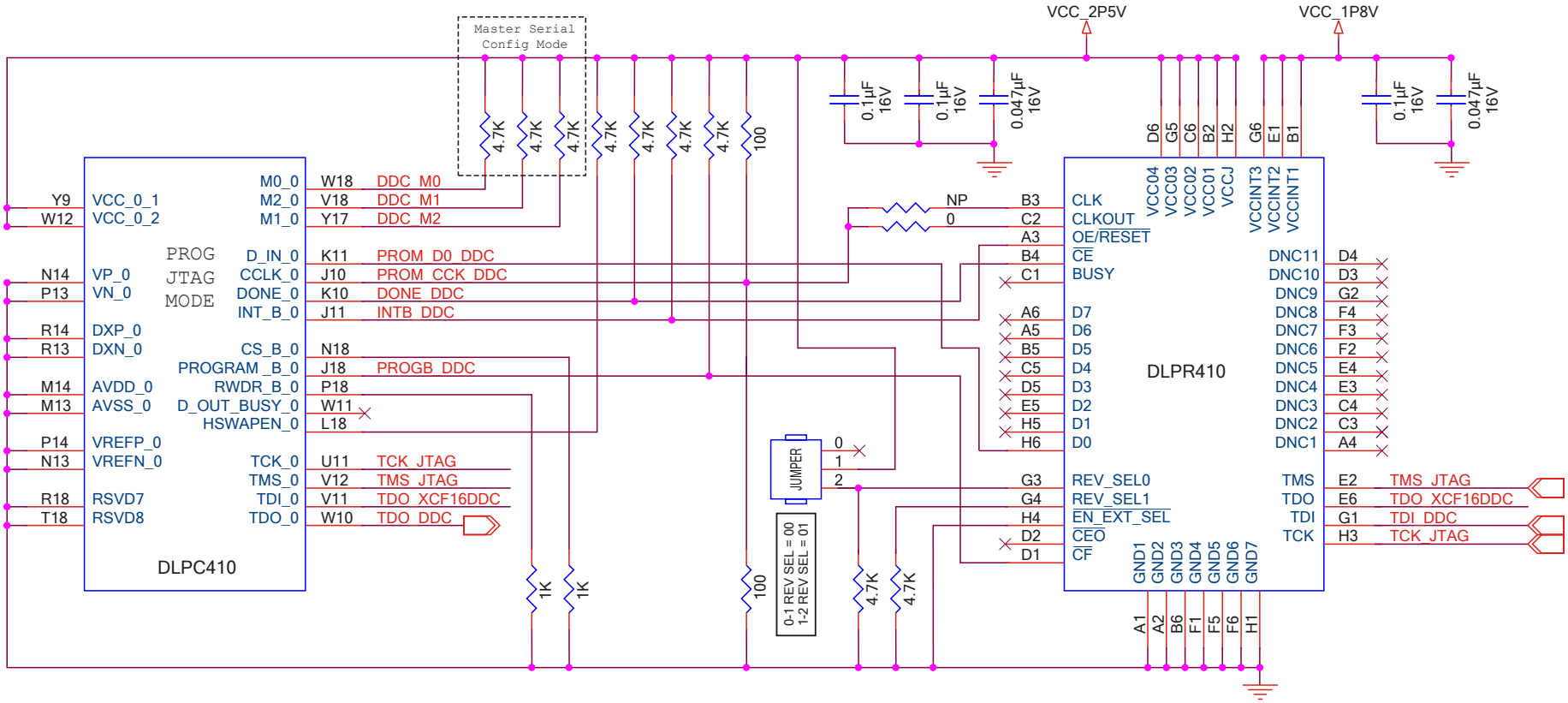

Figure 1. DLPC410 and DLPR410 Connection Schematic

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLPR410 device configuration PROM ships pre-programmed with configuration code for the DLPC410. Upon power-up, the DLPC410 and the DLPR410 device connect to enable configuration information to be sent from the DLPR410 device to the DLPC410, such that the DLPC410 can configure itself for proper operation within the application. Without the DLPR410 device properly connected to the DLPC410 in the application system, the DLPC410 does not boot and the system remains inoperable.

9.2 Typical Application

A typical embedded system application using the DLPR410 device to program the DLPC410 controller (to drive one of 5 different DMDs) is shown in Figure 2. For complete details of this typical application refer to the DLPC410 controller data sheet listed in 表 3.

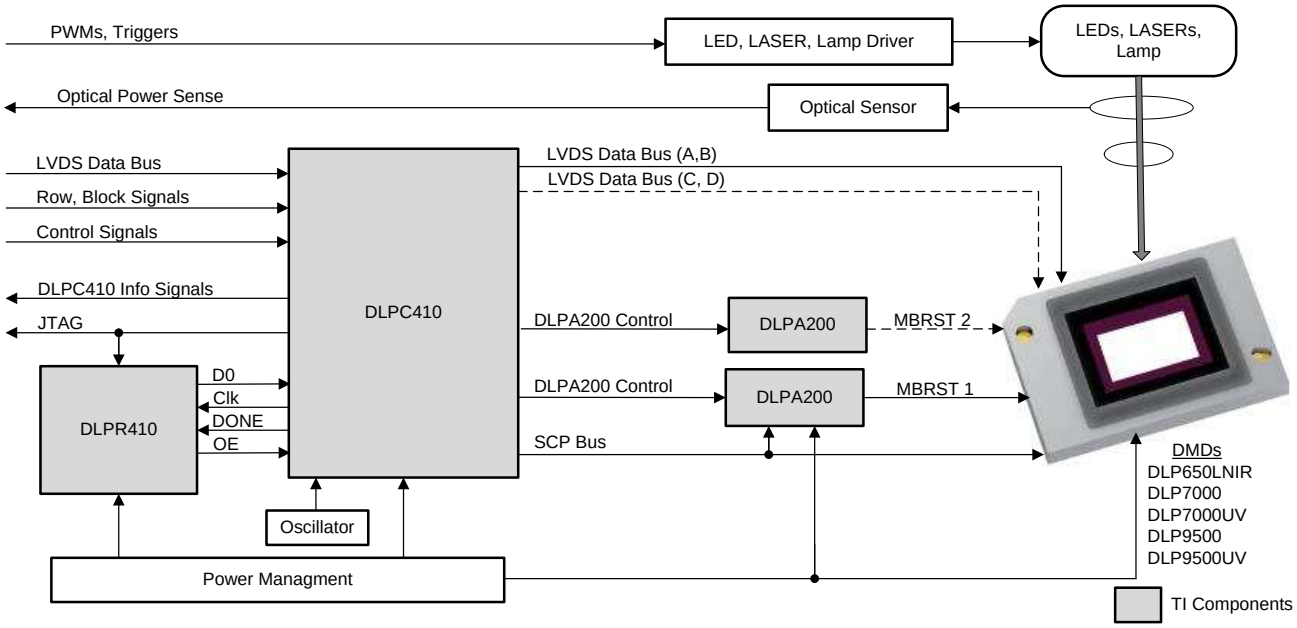

Figure 2. DLPR410 and DLPC410 with DMD Example Block Diagram

9.2.1 Design Requirements

The DLPR410 is part of a multi-chipset solution, and it is required to be coupled with the DLPC410 for reliable operation of the DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs. For more information, refer to the DLPC410 datasheet listed in 表 3.

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10 Power Supply Recommendations

The DLPR410 uses two power supply rails as shown in Table 1.

Table 1. DLPR410 Power Supply Rails

SUPPLY	POWER PINS	COMMENTS
1.8 V	V_{CCINT1}, V_{CCINT2}, and V_{CCINT3}	All V_{CCINT} pins must be connected with a 0.1-µF decoupling capacitor to GND.
2.5 V	V_{CCO1},V_{CCO2},V_{CCO3}, V_{CCO4}, and V_{CCJ}	All V_{CCO} and V_{CCJ} pins must be connected with a 0.1-µF decoupling capacitor to GND.

11 Layout

11.1 Layout Guidelines

The DLPR410 is part of a multi-chipset solution, and it is required to be coupled with the DLPC410 for reliable operation of the DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs. Refer to the DLPC410 datasheet listed in 表 3 for a layout example for this multi-chipset solution.

12 器件和文档支持

12.1 器件支持

12.1.1 器件兼容性

TI 器件型号	DDC_Version(3:0)(1)	兼容的 DMD (2)
DLPR410YVA	5	DLP7000BFLP、DLP7000UVFLP、DLP9500BFLN、DLP9500UVFLN
DLPR410AYVA	7	DLP650LNIRFYL、DLP7000BFLP、DLP7000UVFLP、DLP9500BFLN、DLP9500UVFLN

(1) 表示由此配置 PROM 进行配置后的 DLPC410 上的 DDC_Version(3:0) 输出引脚。请参阅 DLPC410 数据表 (DLPS024) 以了解更多信息。
(2) 请参阅“器件和文档支持”下每个单独的 DMD 数据表，了解更多 DMD 信息。

12.1.2 器件命名规则

器件命名规则如图 3 所示。以前和当前可用的器件型号的器件型号 说明 如表 2 所示。

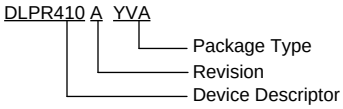

图 3. 器件命名规则

表 2. 器件型号 说明

TI 器件型号	说明	参考编号
DLPR410YVA	DLPR410 配置 PROM	2510442-0005
DLPR410AYVA	DLPR410A 配置 PROM（添加了与 DLP650LNIR 的兼容性）	DLPR410AYVA

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12.1.3 器件标记

图 4 展示了 DLPR410 器件以前的器件标记。对于 DLPR410A，此器件标记命名规则已更新为使用 DLPR410A 器件型号而不是以前的 2510442 标记，如图 5 所示。

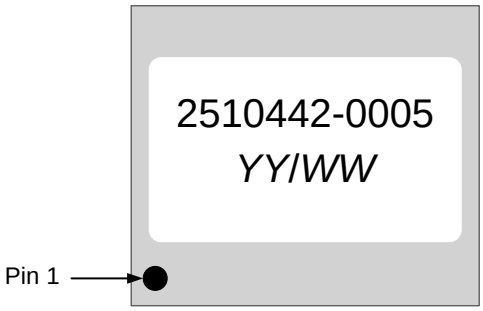

图 4. DLPR410 器件标记

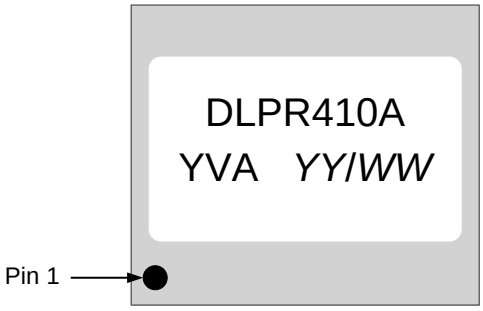

图 5. DLPR410A 器件标记

其中的 *YY/WW* 表示通过编程设定的年/周。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

表 3. 相关文档

文档	TI 文献编号
DLP650LNIR 0.65 NIR WXGA S450 DMD 数据表	DLPS136
DLP7000 DLP 0.7 XGA 2xLVDS A 类 DMD	DLPS026
DLP7000UV DLP 0.7 UV XGA 2xLVDS A 类 DMD 数据表	DLPS061
DLP9500 DLP 0.95 1080p 2xLVDS A 类 DMD 数据表	DLPS025
DLP9500UV DLP 0.95 UV 1080p 2xLVDS A 类 DMD 数据表	DLPS033
《DLPA200 DMD 微镜驱动器数据表》	DLPS015
DLPC410 DMD 数字控制器数据表	DLPS024
XCF16P 数据表	可访问 www.xilinx.com 获取

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.4 商标

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12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPR410AYVA	ACTIVE	DSBGA	YVA	48	3	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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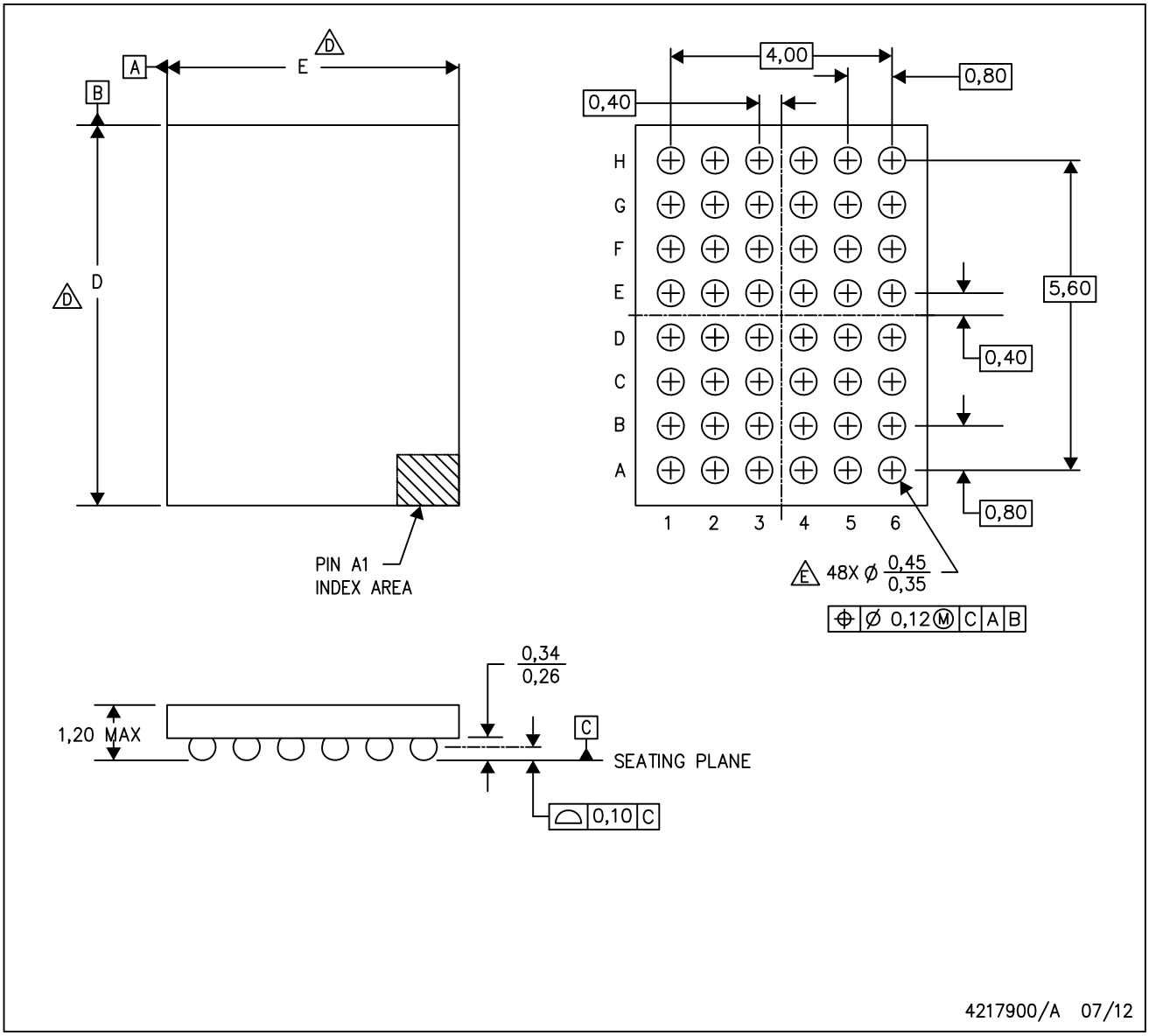
YVA (R–XBGA–N48) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
6 x 8 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

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