TEXAS INSTRUMENTS

UCC28710, UCC28711, UCC28712, UCC28713

ZHCSAH7C – NOVEMBER 2012 – REVISED JUNE 2017

具有初级侧调节功能的 UCC2871x 恒压、恒流控制器

1 特性

- 小于 10mW 空载功耗
- 采用初级侧调整 (PSR)，无需光耦合器
- 线路和负载具有 ±5% 电压调节和电流调节
- 700V 启动开关
- 100kHz 最大开关频率可实现高功率密度充电器设计
- 具有谐振谷底开关运行，可实现最高总体效率
- 频率抖动以简化电磁干扰 (EMI) 兼容性
- 宽 VDD 范围允许使用小型偏置电容器
- 针对金属氧化物半导体场效应晶体管 (MOSFET) 的已钳制栅极驱动输出
- 过压、低线路和过流保护功能
- 可编程电缆补偿 (UCC28710)
- 带有固定线缆补偿选项的负温度系数 (NTC) 电阻器接口（只适用于 UCC28711，UCC28712 和 UCC28713）
- 小外形尺寸集成电路 (SOIC)-7 封装
- 可使用 UCC28710 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 用于消费类电子产品的 USB 兼容适配器和充电器
  - 智能电话
  - 平板电脑
  - 摄像机
- 针对电视和台式机的待机电源
- 白色家电

3 说明

UCC2871x 系列反激式电源控制器在不使用光耦合器的情况下提供隔离式输出恒压 (CV) 和恒流 (CC) 输出调节。此器件可处理来自主要电源开关和辅助反激式绕组的信息，以对输出电压和电流进行精确控制。

一个内部 700V 启动开关、动态控制的工作状态和一个定制的调制配置文件在不牺牲启动时间或输出瞬态响应的同时支持超低待机功耗。

UCC28710 系列中的控制算法使得运行效率符合或者超过适用标准。输出驱动接至一个 MOSFET 电源开关。带有谷值开关的断续传导模式 (DCM) 减少了开关损耗。开关频率的调制和初级电流峰值振幅 (FM 和 AM) 在整个负载和线路范围内保持较高的转换效率。

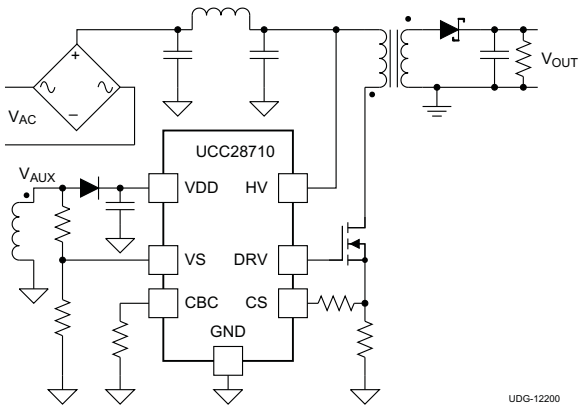
此控制器有一个 100kHz 的最大开关频率并且一直保持对变压器内初级峰值电流的控制。保护 功能 有助于抑制一次侧和二次侧应力分量。UCC28710 支持对线缆补偿进行编程。UCC28711、UCC28712 和 UCC28713 器件在提供固定线缆补偿电平的同时，可使用负温度系数 (NTC) 电阻器实现远程温度感测。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC28710	SOIC (7)	4.91mm × 3.90mm
UCC28711		
UCC28712		
UCC28713		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (July 2015) to Revision C — **Page**

- 已删除 针对 UCC28714、UCC28715 和 UCC28716 器件的所有参考 ... 1
- 已删除 “*准谐振*”中的“*准*” ... 1
- 已添加 *文档支持*、*接收文档更新通知*以及*社区资源* 部分 ... 26

Changes from Revision A (December 2014) to Revision B — **Page**

- Updated *Layout Guidelines* section ... 23

Changes from Original (November 2012) to Revision A — **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 说明* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

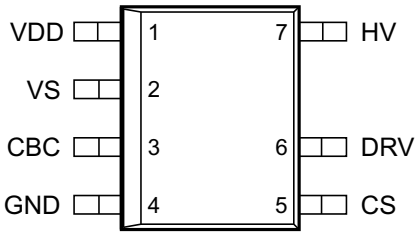
5 Device Comparison Table

PART NUMBER(1)	MINIMUM SWITCHING FREQUENCY	OPTIONS(2)
UCC28710	680 Hz	Programmable cable compensation
UCC28711		NTC option, 0-mV (at 5-V output) cable compensation
UCC28712		NTC option, 150-mV (at 5-V output) cable compensation
UCC28713		NTC option, 300-mV (at 5-V output) cable compensation

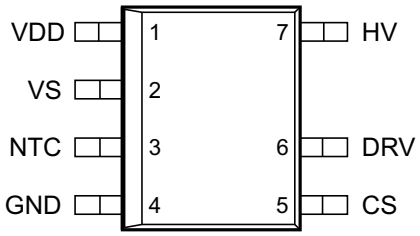
(1) See *机械、封装和可订购信息* section for specific device ordering information.
(2) For other fixed cable compensation options, call TI.

6 Pin Configuration and Functions

UCC28710 D Package
7-Pin SOIC
Top View



UCC28711, UCC28712, UCC28713 D Package
7-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	UCC28710	UCC28711 UCC28712 UCC28713		
CBC	3	—	I	Cable compensation is a programming pin for compensation of cable voltage drop. Cable compensation is programmed with a resistor to GND.
CS	5	5	I	Current sense input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the AC-mains input varies.
DRV	6	6	O	Drive is an output used to drive the gate of an external high voltage MOSFET switching transistor.
GND	4	4	—	The ground pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
HV	7	7	I	The high-voltage pin connects directly to the rectified bulk voltage and provides charge to the VDD capacitor for start-up of the power supply.
NTC	—	3	I	NTC an interface to an external negative temperature coefficient resistor for remote temperature sensing. Pulling this pin low shuts down PWM action.
VDD	1	1	I	VDD is the bias supply input pin to the controller. A carefully-placed bypass capacitor to GND is required on this pin.
VS	2	2	I	Voltage sense is an input used to provide voltage and timing feedback to the controller. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program the AC-mains run and stop thresholds and line compensation at the CS pin.

7 Specifications

7.1 Absolute Maximum Ratings

See (1).

			MIN	MAX	UNIT
V_{HV}	Start-up pin voltage, HV			700	V
V_{VDD}	Bias supply voltage, VDD			38	V
I_{DRV}	Continuous gate current sink			50	mA
I_{DRV}	Continuous gate current source			Self-limiting	mA
I_{VS}	Peak current, VS			−1.2	mA
V_{DRV}	Gate drive voltage at DRV		−0.5	Self-limiting	V
	Voltage	VS	−0.75	7	V
		CS, CBC, NTC	−0.5	5	V
T_J	Operating junction temperature		−55	150	°C
	Lead temperature 0.6 mm from case for 10 s			260	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Bias supply operating voltage	9		35	V
C_{VDD}	VDD bypass capacitor	0.047		1	µF
R_{CBC}	Cable-compensation resistance	10			kΩ
I_{VS}	VS pin current	−1			mA
T_J	Operating junction temperature	−40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCC2871x D (SOIC) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, $R_{CBC(NTC)}$ = open, T_A = –40 °C to 125 °C, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-VOLTAGE START UP						
I_{HV}	Start-up current out of VDD	V_{HV} = 100 V, V_{VDD} = 0 V, start state	100	250	500	µA
I_{HVLKG}	Leakage current at HV	V_{HV} = 400 V, run state		0.1	1	µA
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		95	120	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state, I_{HV} = 0		18	30	µA
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		95	125	µA
UNDERVOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turnon threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turnoff threshold	V_{VDD} high to low	7.7	8.1	8.5	V
VS INPUT						
V_{VSR}	Regulating level	Measured at no-load condition, T_J = 25 °C(1)	4.01	4.05	4.09	V
V_{VSNC}	Negative clamp level	I_{VS} = –300 µA, volts below ground	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
CS INPUT						
$V_{CST(max)}$	Maximum CS threshold voltage	V_{VS} = 3.7 V	738	780	810	mV
$V_{CST(min)}$	Minimum CS threshold voltage	V_{VS} = 4.35 V	175	195	215	mV
K_{AM}	AM control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	3.6	4	4.4	V/V
V_{CCR}	Constant current regulating level	CC regulation constant	318	330	343	mV
K_{LC}	Line compensation current ratio	I_{VSLS} = –300 µA, I_{VSLS} / current out of CS pin	24	25	28.6	A/A
T_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	180	235	280	ns
DRIVERS						
I_{DRS}	DRV source current	V_{DRV} = 8 V, V_{VDD} = 9 V	20	25		mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		6	12	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V		14	16	V
R_{DRVSS}	DRV pulldown in start state		150	190	230	kΩ

(1) The regulating level at VS decreases with temperature by 0.8 mV/°C. This compensation is included to reduce the power supply output voltage variance over temperature.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, $R_{CBC(NTC)}$ = open, T_A = –40 °C to 125 °C, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TIMING							
$f_{SW(max)}$	Maximum switching frequency	V_{VS} = 3.7 V		92	100	106	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{VS} = 4.35 V	UCC28710 UCC28711 UCC28712 UCC28713	600	680	755	Hz
t_{ZTO}	Zero-crossing timeout delay			1.8	2.1	2.55	µs
PROTECTION							
V_{OVP}	Overvoltage threshold	At VS input, T_J = 25 °C (1)		4.55	4.6	4.71	V
V_{OCP}	Overcurrent threshold	At CS input		1.4	1.5	1.6	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin increasing		190	225	275	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin decreasing		70	80	100	µA
K_{VSL}	VS line sense ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$		2.45	2.8	3.05	A/A
$T_{J(stop)}$	Thermal shut-down temperature	Internal junction temperature			165		°C
CABLE COMPENSATION							
$V_{CBC(max)}$	Cable compensation maximum voltage	Voltage at CBC at full load	UCC28710	2.9	3.2	3.5	V
$V_{CVS(min)}$	Compensation at VS	V_{CBC} = open, change in VS regulating level at full load	UCC28710	–55	–15	25	mV
$V_{CVS(max)}$	Maximum compensation at VS	V_{CBC} = 0 V, change in VS regulating level at full load	UCC28710	275	320	375	mV
V_{CVS}	Compensation at VS	Change in VS regulating level at full load	UCC28711	–55	–15	25	mV
			UCC28712		103		
			UCC28713		206		
NTC INPUT							
V_{NTCTH}	NTC shut-down threshold	Fault UVLO cycle when below this threshold	UCC28711 UCC28712 UCC28713	0.9	0.95	1	V
I_{NTC}	NTC pullup current	Current out of pin	UCC28711 UCC28712 UCC28713	90	105	125	µA

7.6 Typical Characteristics

VDD = 25 V, unless otherwise noted.

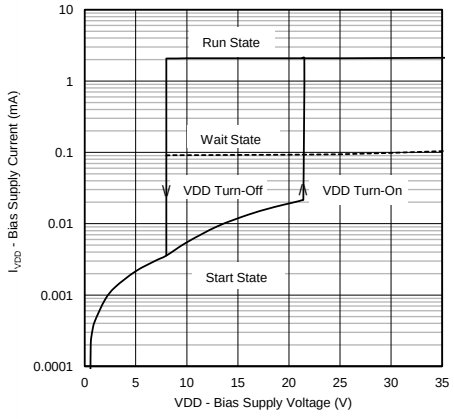


Figure 1. Bias Supply Current vs. Bias Supply Voltage

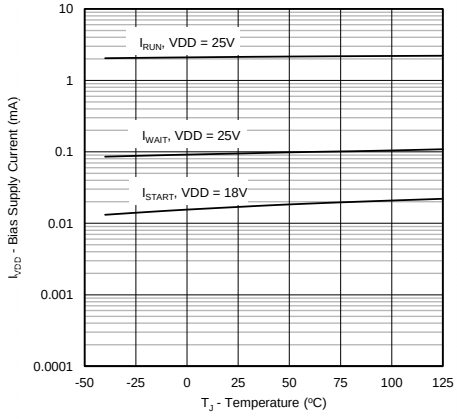


Figure 2. Bias Supply Current vs. Temperature

Typical Characteristics (continued)

VDD = 25 V, unless otherwise noted.

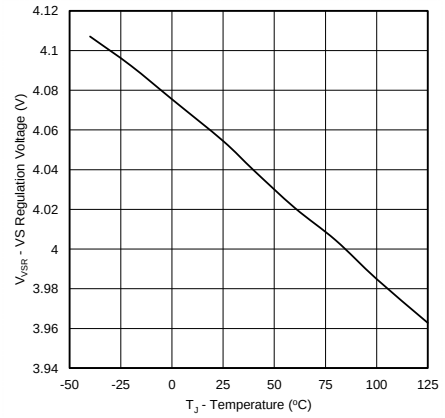


Figure 3. VS Regulation Voltage vs. Temperature

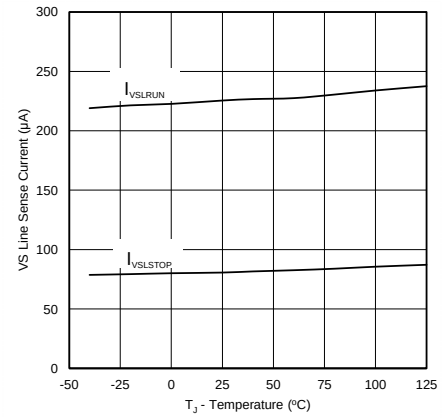


Figure 4. VS Line Sense Current vs. Temperature

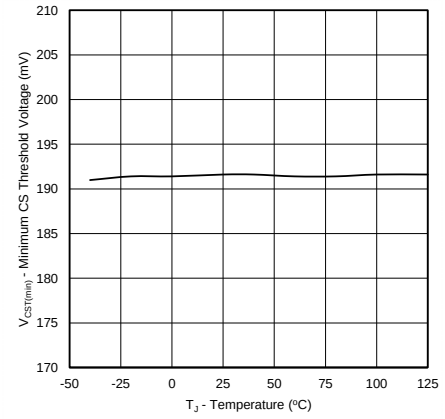


Figure 5. Minimum CS Threshold vs. Temperature

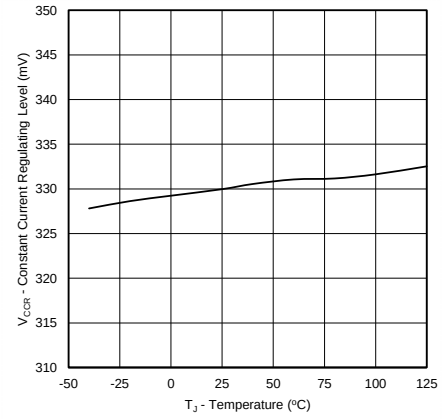


Figure 6. Constant Current Regulating Level vs. Temperature

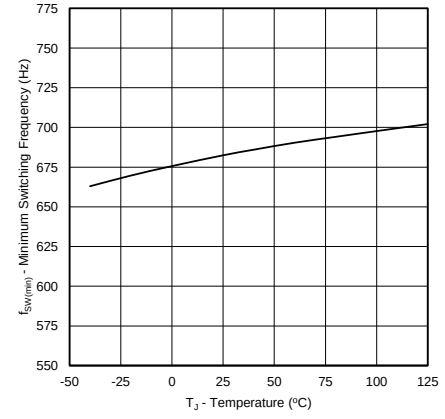
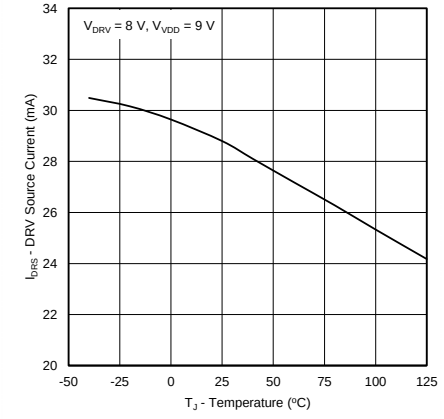


Figure 7. Minimum Switching Frequency vs. Temperature



V_{DRV} = 8 V V_{VDD} = 9 V

Figure 8. DRV Source Current vs. Temperature

Typical Characteristics (continued)

VDD = 25 V, unless otherwise noted.

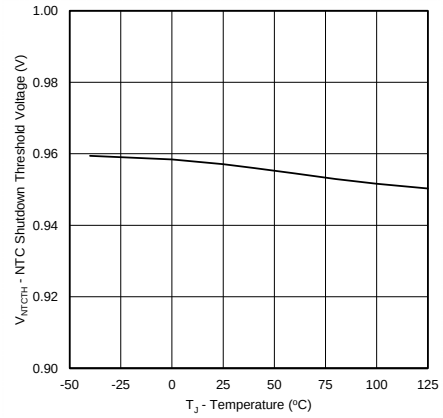


Figure 9. NTC Shutdown Threshold Voltage vs. Temperature

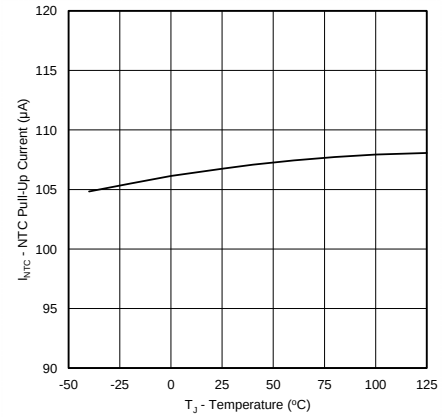


Figure 10. NTC Pull-Up Current vs. Temperature

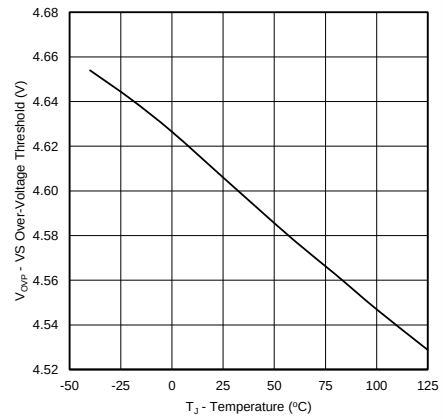


Figure 11. VS Overvoltage Threshold vs. Temperature

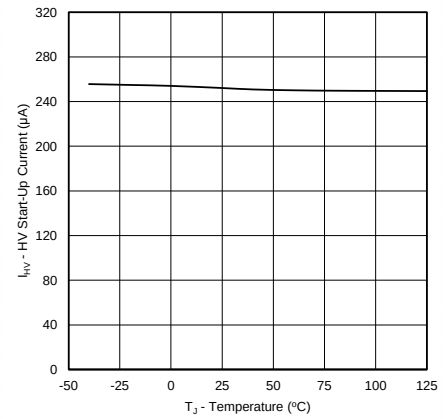


Figure 12. HV Start-Up Current vs. Temperature

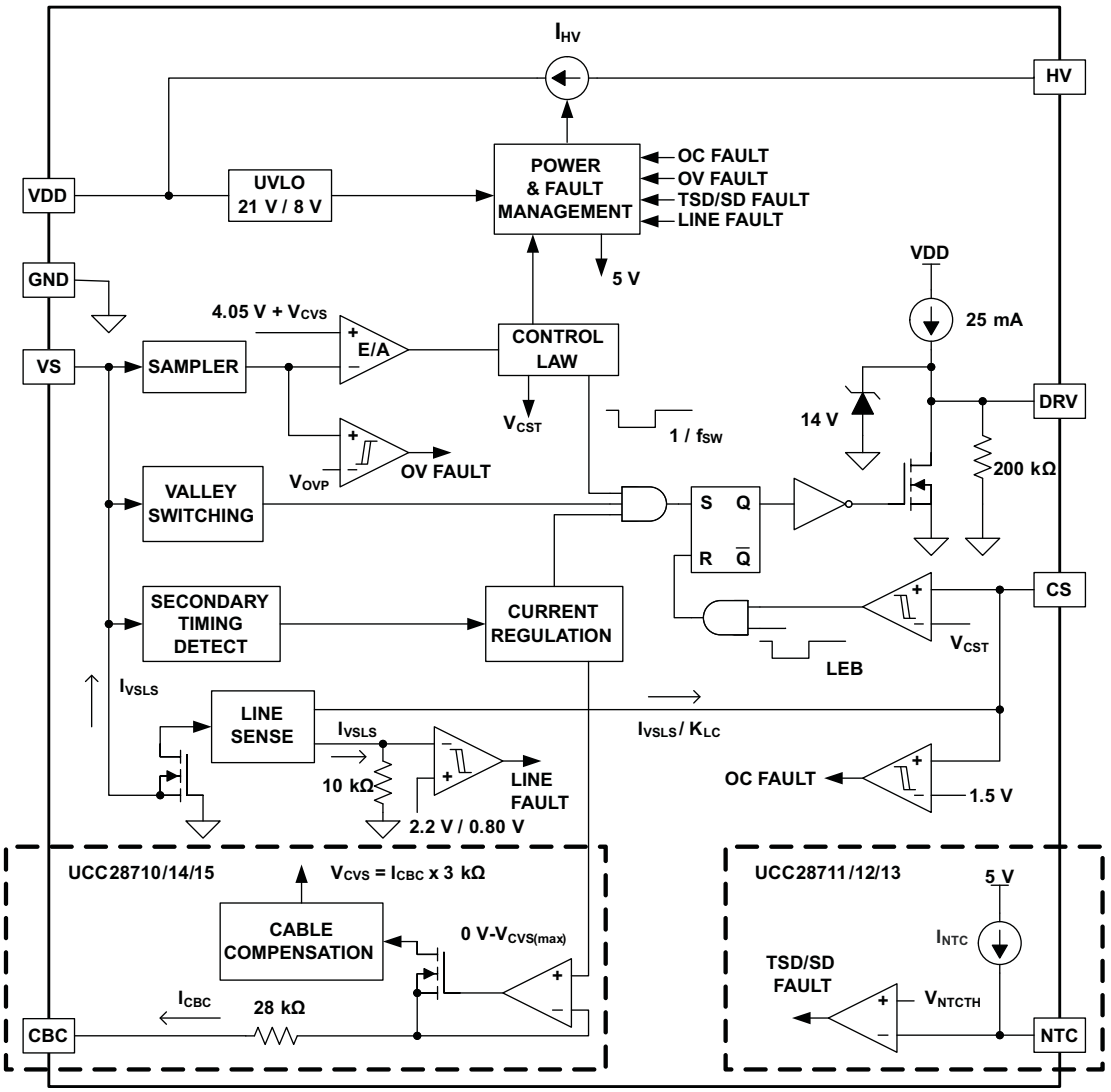
8 Detailed Description

8.1 Overview

The UCC2871x family is a flyback power supply controller which provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley-switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range. The control law provides a wide-dynamic operating range of output power which allows the power designer to achieve the <10-mW stand-by power requirement.

During low-power operating ranges the device has power management features to reduce the device operating current at operating frequencies below 33 kHz. The UCC2871x family includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete charger solution can be realized with a straightforward design process, low cost and low component count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Detailed Pin Description

8.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor (+) terminal. The VDD turnon UVLO threshold is 21 V and turnoff UVLO threshold is 8.1 V, with an available operating range up to 35 V. The USB charging specification requires the output current to operate in constant-current mode from 5 V to a minimum of 2 V; this is easily achieved with a nominal VDD of approximately 25 V. The additional VDD headroom up to 35 V allows for VDD to rise due to the leakage energy delivered to the VDD capacitor in high-load conditions. Also, the wide VDD range provides the advantage of selecting a relatively small VDD capacitor and high-value start-up resistance to minimize no-load stand-by power loss in the start-up resistor.

8.3.1.2 GND (Ground)

This is a single ground reference external to the device for the gate drive current and analog signal reference. Place the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

8.3.1.3 VS (Voltage-Sense)

The VS pin is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Avoid placing a filter capacitor on this input which would interfere with accurate sensing of this waveform.

The VS pin also senses the bulk capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. This information is sensed during the MOSFET on-time. For the AC-input run/stop function, the run threshold on VS is 220 µA and the stop threshold is 80 µA. The values for the auxilliary voltage divider upper-resistor R_{S1} and lower-resistor R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$ is the AC RMS voltage to enable turnon of the controller (run),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the MOSFET on-time. (see the *Electrical Characteristics* table)

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (2)$$

where

- V_{OCV} is the converter regulated output voltage,
- V_F is the output rectifier forward drop at near-zero current,
- N_{AS} is the transformer auxiliary to secondary turns ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{VSR} is the CV regulating level at the VS input (see the *Electrical Characteristics* table).

Feature Description (continued)

8.3.1.4 DRV (Gate Drive)

The DRV pin is connected to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turnon characteristic of the driver is a 25-mA current source which limits the turnon dv/dt of the MOSFET drain and reduces the leading-edge current spike, but still provides gate-drive current to overcome the Miller plateau. The gate-drive turnoff current is determined by the low-side driver $R_{DS(on)}$ and any external gate-drive resistance. The user can reduce the turnoff MOSFET drain dv/dt by adding external gate resistance.

8.3.1.5 CS (Current Sense)

The current-sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The current-sense threshold is 0.75 V for $I_{PP(max)}$ and 0.25 V for $I_{PP(min)}$. The series resistor R_{LC} provides the function of feed-forward line compensation to eliminate change in I_{PP} due to change in di/dt and the propagation delay of the internal comparator and MOSFET turnoff time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turnon current spike. It should not be necessary to place a bypass capacitor on the CS pin. The value of R_{CS} is determined by the target output current in constant-current (CC) regulation. The values of R_{CS} and R_{LC} can be determined by the equations below. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example: With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 1.5%. The η_{XFMR} value is approximately: 1 - 0.05 - 0.035 - 0.015 = 0.9.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}}$$

where

- V_{CCR} is a current regulation constant (see the *Electrical Characteristics* table),
- N_{PS} is the transformer primary-to-secondary turns ratio (a ratio of 13 to 15 is recommended for 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency. (3)

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P}$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- T_D is the current-sense delay including MOSFET turnoff delay, add ~50 ns to MOSFET delay,
- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant (see the *Electrical Characteristics* table). (4)

8.3.1.6 CBC (Cable Compensation), Pin 1 UCC28700

The cable compensation pin is connected to a resistor to ground to program the amount of output voltage compensation to offset cable resistance. The cable compensation block provides a 0-V to 3-V voltage level on the CBC pin corresponding to 0 to I_{OCC} output current. The resistance selected on the CBC pin programs a current mirror that is summed into the VS feedback divider therefore increasing the output voltage as I_{OUT} increases. There is an internal series resistance of 28 kΩ to the CBC pin which sets a maximum cable compensation of a 5-V output to 400 mV when CBC is shorted to ground. The CBC resistance value can be determined by the equation below.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\ k\Omega \times (V_{OCV} + V_F)}{V_{VSR} \times V_{OCBC}} - 28\ k\Omega$$

Feature Description (continued)

where

- V_O is the output voltage,
- V_F is the diode forward voltage,
- V_{OCBC} is the target cable compensation voltage at the output terminals,
- $V_{CBC(max)}$ is the maximum voltage at the cable compensation pin at the maximum converter output current (see the *Electrical Characteristics* table),
- V_{VSR} is the CV regulating level at the VS input (see the *Electrical Characteristics* table). (5)

8.3.1.7 NTC (NTC Thermistor Shut-down), Pin 1 UCC28701/2/3

These versions of the UCC28700 family utilize pin 1 for an external NTC thermistor to allow user-programmable external thermal shut-down. The shut-down threshold is 0.95 V with an internal 105-µA current source which results in a 9.05-kΩ thermistor shut-down threshold. These controllers have either zero or fixed internal cable compensation.

8.3.2 Fault Protection

There is comprehensive fault protection. Protection functions include:

- Output overvoltage fault
- Input undervoltage fault
- Internal overtemperature fault
- Primary overcurrent fault
- CS pin fault
- VS pin fault

A UVLO reset and restart sequence applies for all fault protection events.

The output overvoltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 115% of the nominal V_{OUT}, the device stops switching and the internal current consumption is I_{FAULT} which discharges the VDD capacitor to the UVLO turnoff threshold. After that, the device returns to the start state and a start-up sequence ensues.

The UCC2871x family always operates with cycle-by-cycle primary peak current control. The normal operating range of the CS pin is 0.78 V to 0.195 V. There is additional protection if the CS pin reaches 1.5 V. This results in a UVLO reset and restart sequence.

The line input run and stop thresholds are determined by current information at the VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through R_{S1} is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. The run current threshold is 225 µA and the stop current threshold is 80 µA.

The internal over-temperature protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

8.4 Device Functional Modes

8.4.1 Primary-Side Voltage Regulation

Figure 13 illustrates a simplified flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control.

Device Functional Modes (continued)

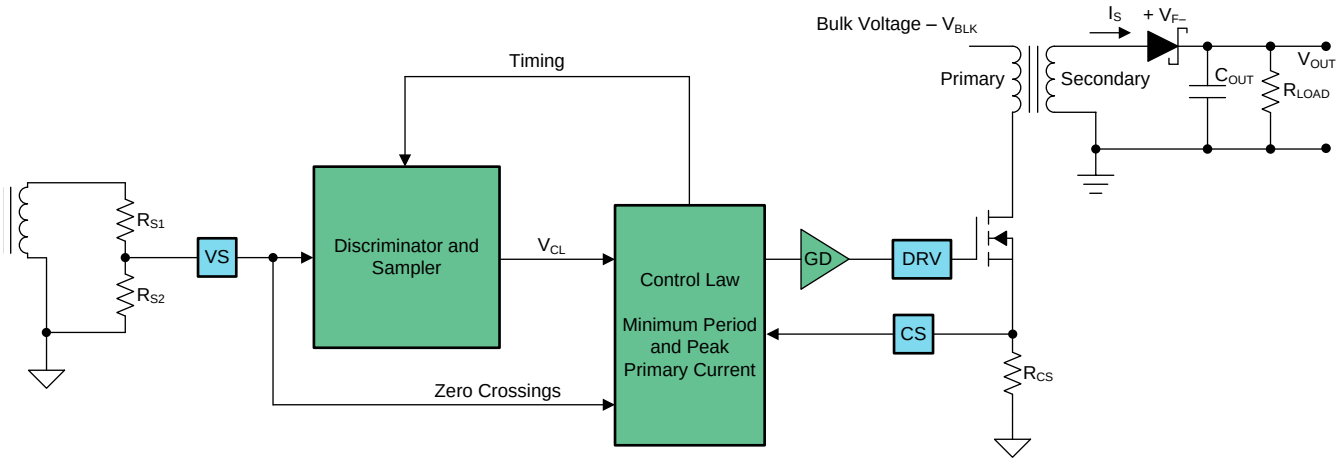


Figure 13. Simplified Flyback Convertor (With the Main Voltage Regulation Blocks)

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in Figure 14 it is clear there is a down slope representing a decreasing total rectifier V_F and resistance voltage drop ($I_S R_S$) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V. Temperature compensation on the VS reference voltage of -0.8-mV/°C offsets the change in the output rectifier forward voltage with temperature. The resistor divider is selected as outlined in the VS pin description.

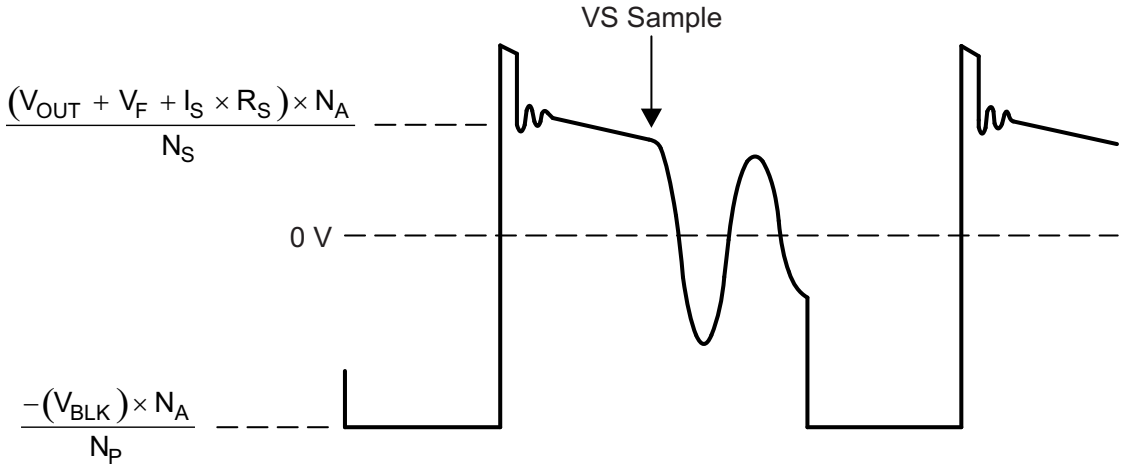


Figure 14. Auxiliary Winding Voltage

The UCC2871x family includes a VS signal sampler that signals discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 15 below for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, t_{LK_RESET} in Figure 15. Because this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time less than 600 ns for I_{PRI} minimum, and less

Device Functional Modes (continued)

than 2.2 µs for I_{PRI} maximum. The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 100 mV_{p-p} at least 200 ns before the end of the demagnetization time, t_{DM}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary winding voltage by R_{S1} and R_{S2}, and is equal to 100 mV x (R_{S1} + R_{S2}) / R_{S2}.

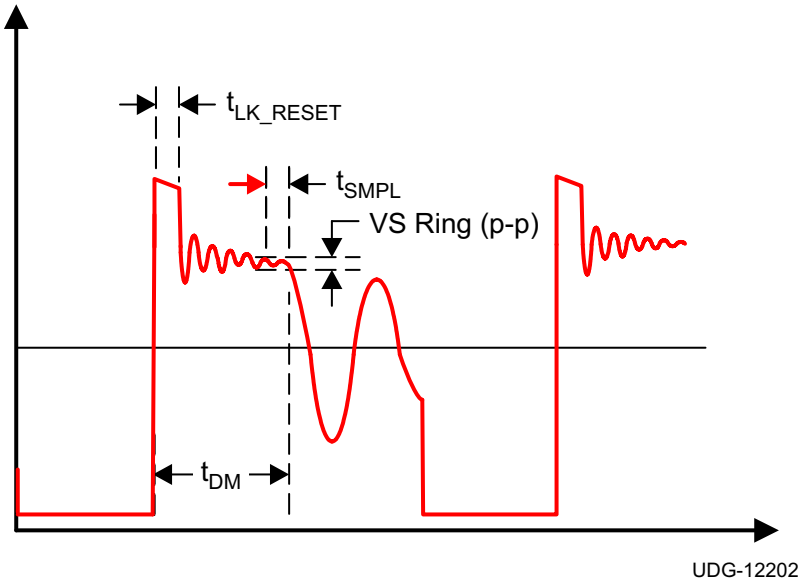


Figure 15. Auxiliary Waveform Details

During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode as illustrated in Figure 16 below. The internal operating frequency limits of the device are 100 kHz maximum and $f_{SW(min)}$. The transformer primary inductance and primary peak current chosen sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no stability compensation required for the UCC2871x family.

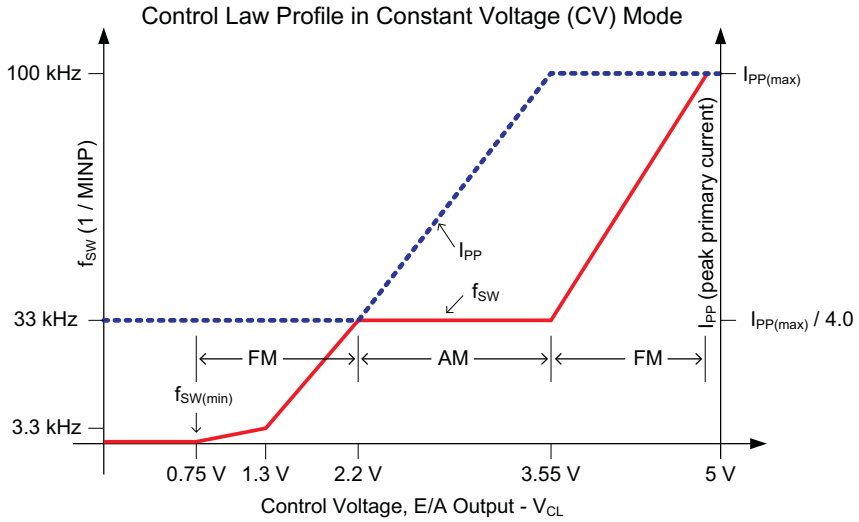


Figure 16. Frequency and Amplitude Modulation Modes (During Voltage Regulation)

Device Functional Modes (continued)

8.4.2 Primary-Side Current Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at $I_{PP(max)}$. Referring to Figure 17 below, the primary-peak current, turns ratio, secondary demagnetization time (t_{DM}), and switching period (t_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by Equation 6. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turnoff threshold.

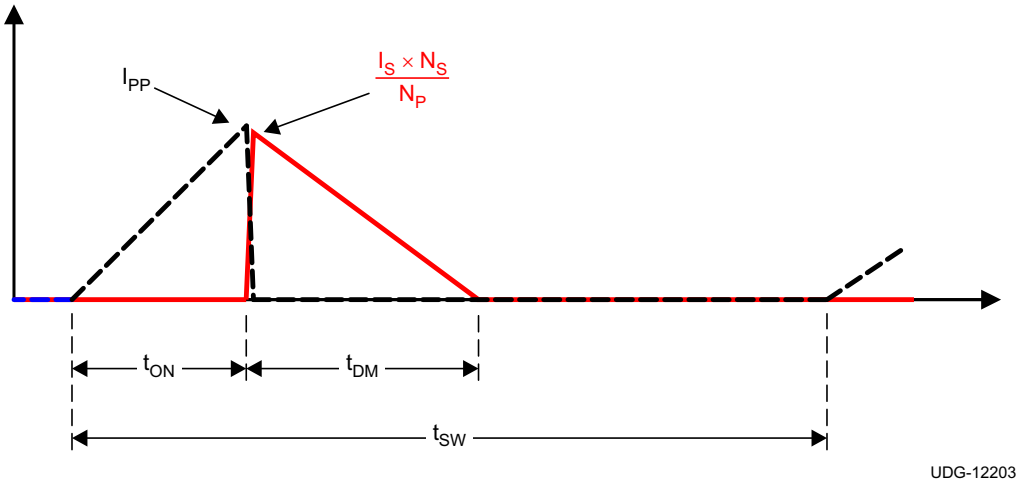


Figure 17. Transformer Currents

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (6)$$

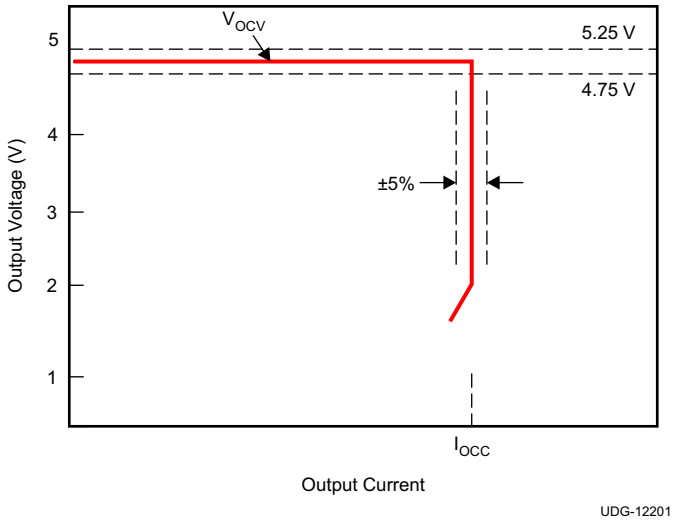


Figure 18. Typical Target Output V-I Characteristic

8.4.3 Valley Switching

The UCC2871x family utilizes valley switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turnon current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing has diminished.

Device Functional Modes (continued)

Referring to Figure 19 below, the UCC2871x family operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

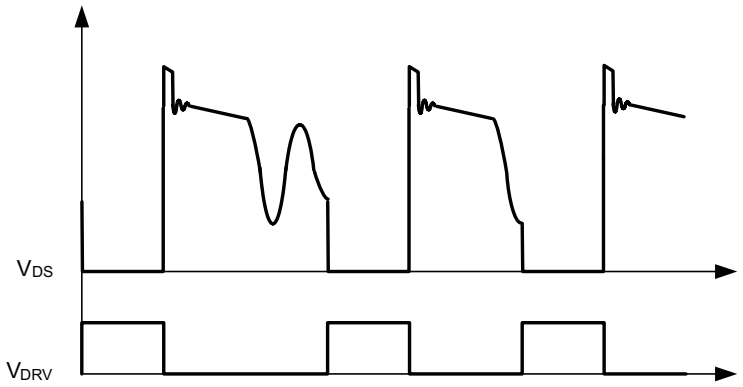


Figure 19. Valley-Skipping Mode

8.4.4 Start-Up Operation

The internal high-voltage start-up switch connected to the bulk capacitor voltage (V_{BLK}) through the HV pin charges the VDD capacitor. During start up there is typically 300 µA available to charge the VDD capacitor. When VDD reaches the 21-V UVLO turnon threshold, the controller is enabled, the converter starts switching and the start-up switch is turned off. The initial three cycles are limited to $I_{PP(min)}$. After the initial three cycles at minimum $I_{PP(min)}$, the controller responds to the condition dictated by the control law. The converter will remain in discontinuous mode during charging of the output capacitor(s), maintaining a constant output current until the output voltage is in regulation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC2871x family of flyback power supply controllers provides constant voltage (CV) and constant current (CC) output regulation to help meet USB-compliant adaptors and charger requirements. These devices use the information obtained from auxiliary winding sensing (VS) to control the output voltage and do not require optocoupler/TL431 feedback circuitry. Eliminating the optocoupler feedback reduces component count and makes the design more cost effective. Refer to Figure 20 for details.

9.2 Typical Application

The procedure in the *Detailed Design Procedure* section outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC2871x family of controllers. Refer to the typical application schematic for component location (Figure 20) and the *器件命名规则* section for variable definitions.

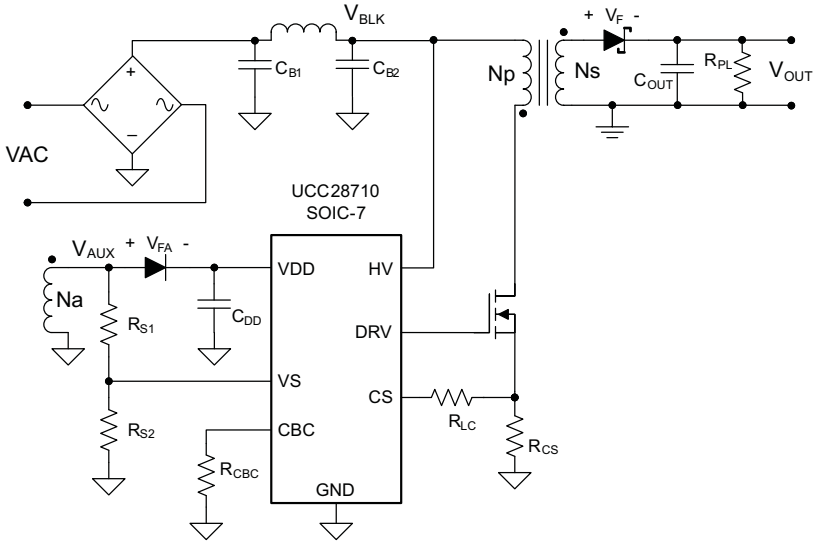


Figure 20. Design Procedure Application Example

9.2.1 Design Requirements

Table 1. Design Parameters

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input Voltage		100	115/230	240	V
f_{LINE}	Line Frequency		47	50/60	64	Hz
P_{SB_CONV}	No Load Input Power	V_{IN} = Nom, I_O = 0 A			10	mW
$V_{IN(RUN)}$	Brownout Voltage	I_O = Nom		70		V
OUTPUT CHARACTERISTICS						
V_O	Output Voltage	V_{IN} = Nom, I_O = Nom	4.75	5	5.25	V
V_{RIPPLE}	Output Voltage Ripple	V_{IN} = Nom, I_O = Max			0.1	V
I_O	Output Current	V_{IN} = Min to Max		1	1.05	A

Typical Application (continued)

Table 1. Design Parameters (continued)

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
V_{OVP}	Output OVP	I_{OUT} = Min to Max		5.75		V
	Transient Response					
$V_{O\Delta}$	Load Step (V_O = 4.1 V to 6 V)	(0.1 to 0.6 A) or (0.6 to 0.1 A) $V_{O\Delta}$ = 0.9 V for C_{OUT} calculation in applications section	4.1	5	6	A
SYSTEMS CHARACTERISTICS						
	Switching Frequency				90	kHz
η	Full Load Efficiency (115/230 V RMS Input)	I_O = 1 A	74%		76%	

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28710 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Stand-by Power Estimate

Assuming no-load stand-by power is a critical design parameter, determine estimated no-load power based on target converter maximum switching frequency and output power rating.

The following equation estimates the stand-by power of the converter.

$$P_{SB\_CONV} = \frac{P_{OUT} \times f_{MIN}}{\eta_{SB} \times K_{AM}^{2} \times f_{MAX}} \quad (7)$$

For a typical USB charger application, the bias power during no-load is approximately 2.5 mW. This is based on 25-V VDD and 100-µA bias current. The output preload resistor can be estimated by V_{OCV} and the difference in the converter stand-by power and the bias power. The equation for output preload resistance accounts for bias power estimated at 2.5 mW.

$$R_{PL} = \frac{V_{OCV}^{2}}{P_{SB\_CONV} - 2.5\,mW} \quad (8)$$

The capacitor bulk voltage for the loss estimation is the highest voltage for the stand-by power measurement, typically 325 V_{DC}.

For the total stand-by power estimation add an estimated 2.5 mW for snubber loss to the converter stand-by power loss.

$$P_{SB} = P_{SB\_CONV} + 2.5\,mW \quad (9)$$

9.2.2.3 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np to Ns turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV}, I_{OCC}, and the full-load efficiency target.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \tag{10}$$

The below equation provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\Pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^{2} - V_{BULK(min)}^{2}\right) \times f_{LINE}} \tag{11}$$

9.2.2.4 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period, or 1 µs assuming 500-kHz resonant frequency. D_{MAX} can be determined using the equation below.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX}\right) - D_{MAGCC} \tag{12}$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current, CC, operation. It is set internally by the UCC2871x family at 0.425. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV}, the secondary rectifier V_F, and the cable compensation voltage (V_{OCBC}). For the 5-V USB charger applications, a turns ratio range of 13 to 15 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_F + V_{OCBC}\right)} \tag{13}$$

Once an optimum turns ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC2871x family constant-current regulation is achieved by maintaining a maximum D_{MAG} duty cycle of 0.425 at the maximum primary current setting. The transformer turns ratio and constant-current regulating voltage determine the current sense resistor for a target constant current.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. For a 5-V, 1-A charger example, bias power of 1.5% is a good estimate. An overall transformer efficiency of 0.9 is a good estimate to include 3.5% leakage inductance, 5% core and winding loss, and 1.5% bias power.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{14}$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output and transformer power losses are included in the equation below. Initially determine transformer primary current.

Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (15)$$

$$L_P = \frac{2\left(V_{OCV} + V_F + V_{OCBC}\right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \quad (16)$$

The secondary winding to auxiliary winding transformer turns ratio (N_{AS}) is determined by the lowest target operating output voltage in constant-current regulation and the VDD UVLO of the UCC2871x family. There is additional energy supplied to VDD from the transformer leakage inductance energy which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \quad (17)$$

9.2.2.5 Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage so these should be reviewed. The UCC2871x family does require a minimum on time of the MOSFET (t_{ON}) and minimum D_{MAG} time (t_{DMAG}) of the secondary rectifier in the high line, minimum load condition. The selection of f_{MAX}, L_P and R_{CS} affects the minimum t_{ON} and t_{DMAG}.

The secondary rectifier and MOSFET voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \quad (18)$$

For the MOSFET V_{DS} voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \quad (19)$$

Equation 20 and Equation 21 are used to determine if the minimum t_{ON} target of 300 ns and minimum t_{DMAG} target of 1.2 µs is achieved.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)} \times V_{CST(min)}}{V_{CST(max)}} \quad (20)$$

$$t_{DMAG(min)} = \frac{t_{ON} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \quad (21)$$

9.2.2.6 Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no-load. For example, in some USB charger applications there is a requirement to maintain a minimum V_O of 4.1 V with a load-step transient of 0 mA to 500 mA . The equation below assumes that the switching frequency can be at the UCC2871x family's minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN}\left(\frac{1}{f_{SW(min)}} + 150\ \mu s\right)}{V_{O\Delta}} \quad (22)$$

Another consideration of the output capacitor(s) is the ripple voltage requirement which is reviewed based on secondary peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in the equation below.

$$R_{ESR} = \frac{V_{RIPPLE} \times 0.8}{I_{PP(max)} \times N_{PS}} \quad (23)$$

9.2.2.7 VDD Capacitance, C_{DD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the voltage to the UCC2871x family. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. There is an estimated 1 mA of gate-drive current in the equation and 1 V of margin added to VDD.

$$C_{DD} = \frac{\left(I_{RUN} + 1\,mA\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{\left(V_{DD(on)} - V_{DD(off)}\right) - 1\,V} \tag{24}$$

9.2.2.8 VS Resistor Divider, Line Compensation, and Cable Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary to primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \tag{25}$$

The low-side VS pin resistor is selected based on desired V_O regulation voltage.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times \left(V_{OCV} + V_F\right) - V_{VSR}} \tag{26}$$

The UCC2871x family can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and expected gate drive and MOSFET turnoff delay. Assume a 50-ns internal delay in the UCC2871x family.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \tag{27}$$

On the UCC28710, which has adjustable cable compensation, the resistance for the desired compensation level at the output terminals can be determined using Equation 28.

$$R_{CBC} = \frac{V_{CBC(max)} \times 3\,k\Omega \times \left(V_{OCV} + V_F\right)}{V_{VSR} \times V_{OCBC}} - 28\,k\Omega \tag{28}$$

9.2.3 Application Curves

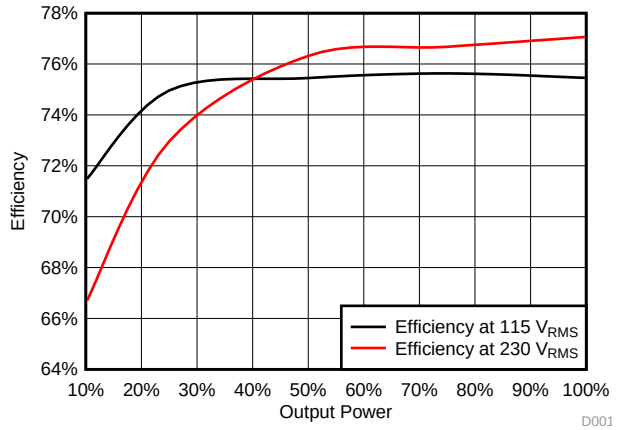


Figure 21. Efficiency

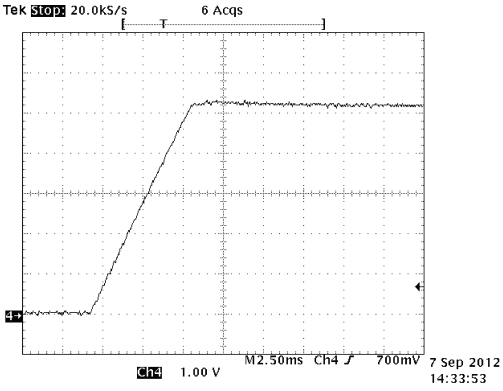


Figure 22. Output at Startup at 115-V RMS (No Load)

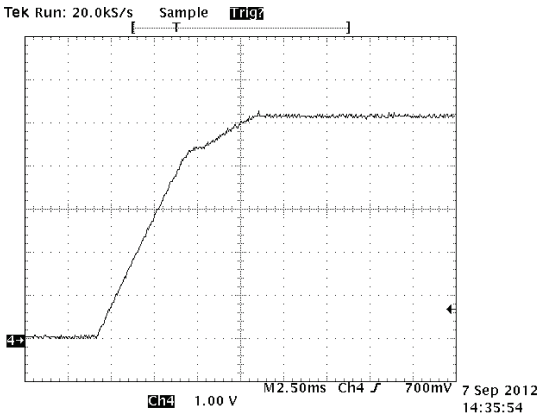


Figure 23. Output at Startup at 115-V RMS (5-Ω Load)

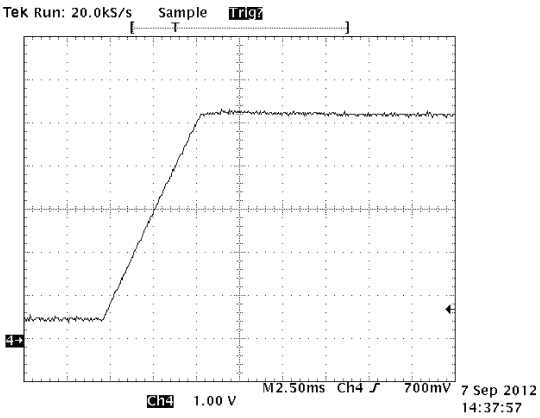


Figure 24. Output at Startup at 230-V RMS (No Load)

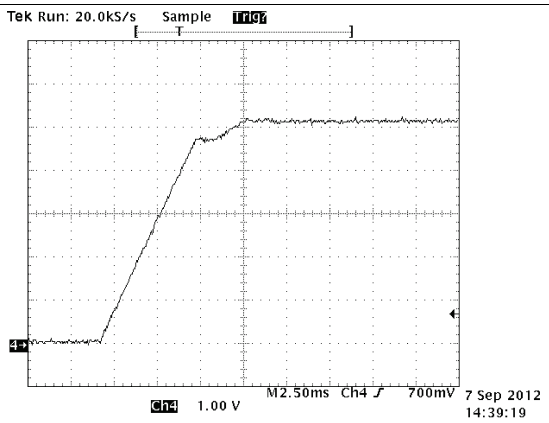
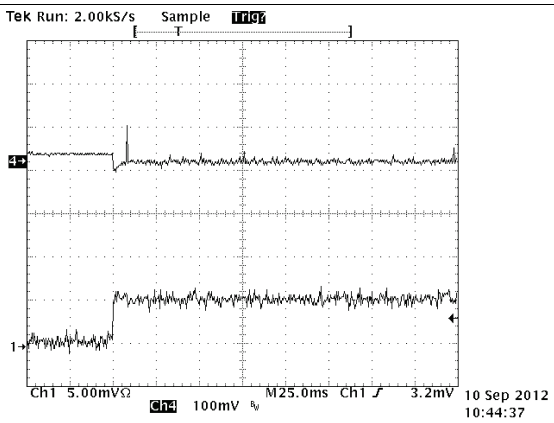
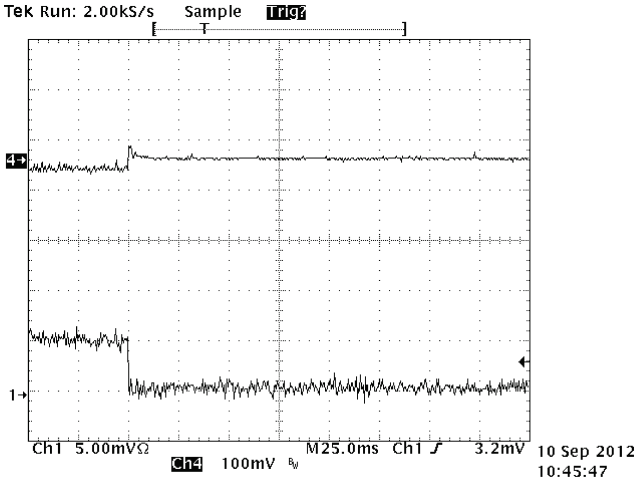


Figure 25. Output at Startup at 230-V RMS (5-Ω Load)



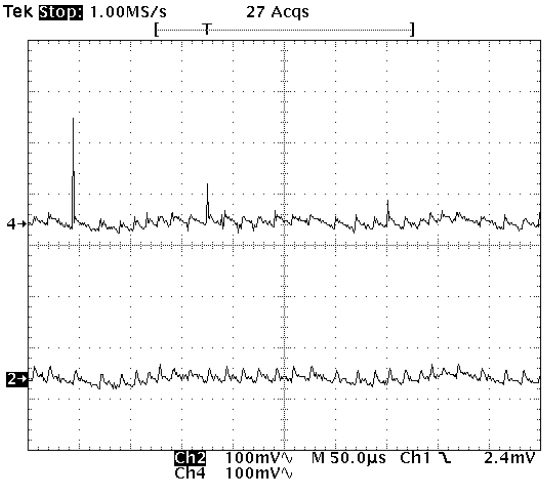
CH1 = I_O, CH4 = V_O With a 5-V Offset

Figure 26. Load Transients: (0.1-A to 0.6-A Load Step)



CH1 = I_O, CH4 = V_O With a 5-V Offset

Figure 27. Load Transients: (0.6-A to 0.1-A Load Step)



CH4 = V_O, Output voltage at EVM output

CH2 = V_O, Output voltage measured at the end of the 3M of cable in parallel with a 1-uF capacitor. The output voltage has less than 50 mV of output ripple at the end of the cable.

Figure 28. Output Ripple Voltage at Full Load

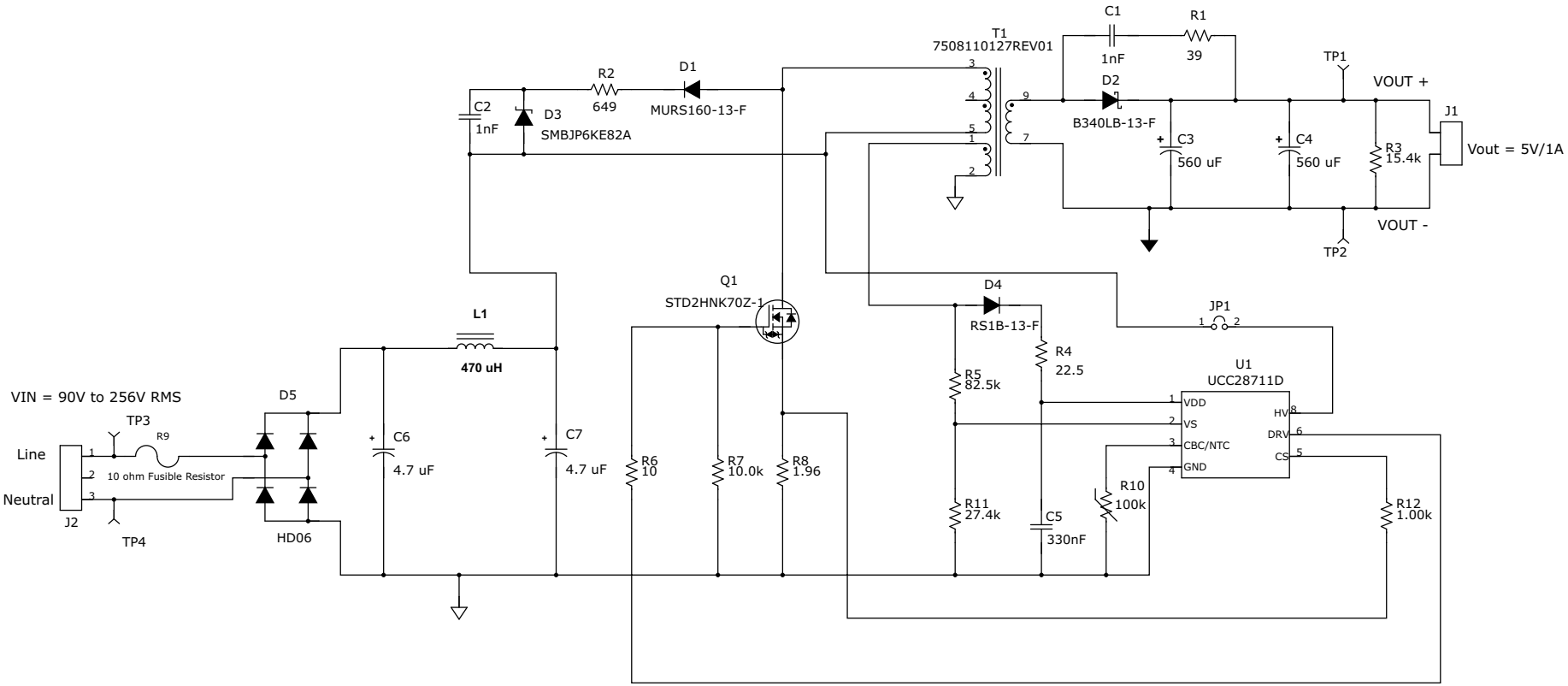
10 Power Supply Recommendations

The UCC2871x family is intended for AC/DC adapters and chargers with input voltage range of 85 $V_{AC(rms)}$ to 265 $V_{AC(rms)}$ using Flyback topology. It can be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device. To maintain output current regulation over the entire input voltage range, design the converter to operate close to f_{MAX} when in full-load conditions. To improve thermal performance increase the copper area connected to GND pins.

11 Layout

11.1 Layout Guidelines

- High frequency bypass Capacitor C5 should be placed across Pin 1 and 4 as close as you can get it to the pins.
- Resistor R4 and C5 form a low pass filter and the connection of R4 and C5 should be as close to the VDD pin as possible.
- The VS pin controls the output voltage through the transformer turns ratio and the voltage divider of R5 and R11. Note the trace length between the R5, R11 and VS pin should be as short as possible to reduce or eliminate possible EMI coupling.
- Note the IC ground and power ground should meet at the bulk capacitor's (C6 and C7) return. Try to ensure that high frequency/high current from the power stage does not go through the signal ground.
  - The high frequency/high current path that you need to be cautious of on the primary is C7 +, T1 (P5, P3), Q1d, Q1s, R8 to the return of C6 and C7. Try to keep all high current loops as short as possible.
- Try to keep all high current loops as short as possible.
- Keep all high current/high frequency traces away from or perpendicular to other traces in the design.
- Traces on the voltage clamp formed by D1, R2, D3 and C2 as short as possible.
- C6 return needs to be as close to the bulk capacitor supply as possible. This reduces the magnitude of dv/dt caused by large di/dt.
- Avoid mounting semiconductors under magnetics.



No value means not populated.

Figure 29. 5-W USB Adapter Schematic

11.2 Layout Example

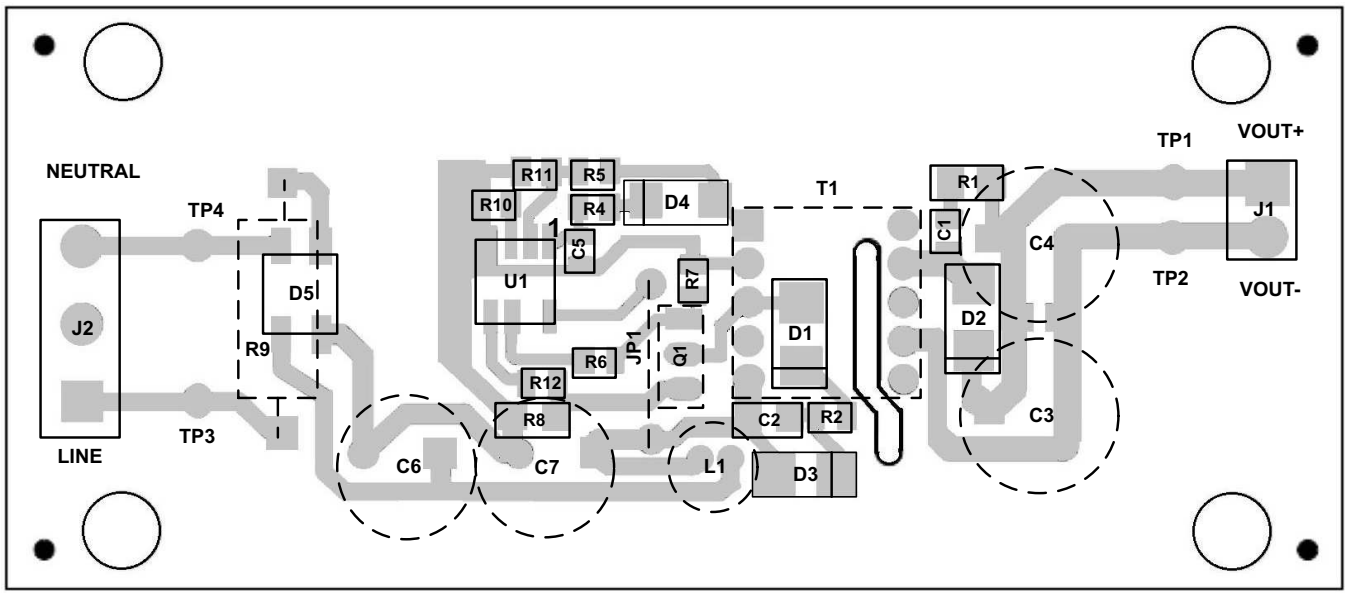


Figure 30. Layout Example Schematic

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

有关设计工具，请参阅 UCC2871x 计算器、UCC2871x PSpice 瞬态模型、UCC2871x TINA-TI 瞬态 Spice 模型和 UCC2871x TINA-TI 瞬态参考设计。

12.1.1.1 使用 WEBENCH® 工具创建定制设计方案

请单击此处，通过 WEBENCH® 电源设计器使用 UCC28710 器件创建定制的设计方案。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

12.1.2 器件命名规则

12.1.2.1 电容术语（以法拉为单位）

- **C_{BULK}**：CB1 和 CB2 的总输入电容。
- **C_{DD}**：VDD 引脚上所需的最小电容。
- **C_{OUT}**：所需的最小输出电容。

12.1.2.2 占空比术语

- **D_{MAGCC}**：CC 中的二次侧二极管导通占空比，0.425。
- **D_{MAX}**：MOSFET 导通时间占空比。

12.1.2.3 频率术语（以赫兹为单位）

- **f_{LINE}**：最小线路频率。
- **f_{MAX}**：转换器的目标满载最大开关频率。
- **f_{MIN}**：转换器的最小开关频率，为器件的 $f_{SW(min)}$ 限值增加 15% 裕度。
- **$f_{SW(min)}$**：最小开关频率（请参阅*Electrical Characteristics*）。

12.1.2.4 电流术语（以安培为单位）

- **I_{OCC}**：转换器目标恒流输出。
- **$I_{PP(max)}$**：变压器一次侧最大电流。
- **I_{START}**：启动偏置电源电流（请参阅*Electrical Characteristics*）。
- **I_{TRAN}**：所需的正负载阶跃电流。
- **$I_{VSL(run)}$**：VS 引脚运行电流（请参阅*Electrical Characteristics*）。

12.1.2.5 电流和电压调节术语

- **K_{AM}**：最大/最小峰值初级电流比率（请参阅*Electrical Characteristics*）。
- **K_{LC}**：电流调节常量（请参阅*Electrical Characteristics*）。

12.1.2.6 变压器术语

- **L_P**：变压器一次侧电感。

器件支持 (接下页)

- N_{AS}：变压器辅助侧与二次侧的匝数比。
- N_{PA}：变压器一次侧与辅助侧的匝数比。
- N_{PS}：变压器一次侧与二次侧的匝数比。

12.1.2.7 功率术语（以瓦特为单位）

- P_{IN}：转换器的最大输入功率。
- P_{OUT}：转换器的满载输出功率。
- P_{RSTR}：VDD 启动电阻的功耗。
- P_{SB}：总待机功耗。
- P_{SB_CONV}：P_{SB}与启动电阻和缓冲器损耗的差值。

12.1.2.8 电阻术语（以 Ω 为单位）

- R_{CS}：一次侧电流编程电阻。
- R_{ESR}：输出电容器的总 ESR。
- R_{PL}：转换器输出端的预载电阻。
- R_{S1}：高侧 VS 引脚电阻。
- R_{S2}：低侧 VS 引脚电阻。

12.1.2.9 时间术语（以秒为单位）

- t_D：包括 MOSFET 关断延迟在内的电流感测延迟；在 MOSFET 延迟基础上增加 50ns。
- $T_{DMAG(min)}$：次级整流器的最短导通时间。
- $t_{ON(min)}$：最短 MOSFET 导通时间。
- t_R：DCM（断续导通模式）期间的谐振频率。

12.1.2.10 电压术语（以伏特为单位）

- V_{BLK}：用于待机功耗测量的大容量电容最高电压。
- $V_{BULK（最小值）}$：满功率条件下 C_{B1} 和 C_{B2} 的最低电压。
- V_{OCBC}：输出引脚的目标电缆补偿电压。
- $V_{CBC(max)}$：最大转换器输出电流条件下 CBC 引脚的最大电压（请参阅*Electrical Characteristics*）。
- V_{CCR}：恒流调节电压（请参阅*Electrical Characteristics*）。
- $V_{CST(max)}$：CS 引脚最大电流感测阈值（请参阅*Electrical Characteristics*）。
- $V_{CST(min)}$：CS 引脚最小电流感测阈值（请参阅*Electrical Characteristics*）。
- $V_{DD(off)}$：UVLO 关断电压（请参阅*Electrical Characteristics*）。
- $V_{DD(on)}$：UVLO 开启电压（请参阅*Electrical Characteristics*）。
- $V_{O\Delta}$：负载阶跃瞬态期间允许的输出压降。
- V_{DSPK}：高压线路中的峰值 MOSFET 漏极-源极电压。
- V_F：电流接近零时的二次侧整流器正向压降。
- V_{FA}：辅助整流器正向压降。
- V_{LK}：估计的漏感能量复位电压。
- V_{OCV}：经稳压的转换器输出电压。
- V_{OCC}：恒流稳压条件下的最低目标转换器输出电压。
- V_{REV}：二次侧整流器的峰值反向电压。
- V_{RIPPLE}：满载条件下的输出峰峰值纹波电压。
- V_{VSR}：VS 输入处的 CV 调节电平（请参阅*Electrical Characteristics*）。

12.1.2.11 交流电压术语（以 V_{RMS} 为单位）

- $V_{IN(max)}$：转换器的最大输入电压。
- $V_{IN(min)}$：转换器的最小输入电压。
- $V_{IN(min)}$：转换器的输入启动（运行）电压。

器件支持 (接下页)

12.1.2.12 效率术语

- η_{SB}：无载条件下估算的转换器效率，其中不包括启动电阻或偏置损耗。对于 5V USB 充电器应用而言，60% 到 65% 是很好的初步估算值。
- η：转换器总体效率。
- η_{XFMR}：变压器一次侧与二次侧之间的功率传输效率。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- *《在缓冲电路中选择使用标准恢复二极管或超快恢复二极管》*
- *《低功率交流/直流转换器面临的控制挑战》*
- *《TI PSR 控制器疑难解答》*
- *《采用 UCC28711 EVM-160 的评估模块》*
- *《用于确定绝缘电阻的泄漏电流测量参考设计》*
- *《用于伺服驱动器的 100V/200V 交流输入 30W 反激式隔离型电源参考设计》*

12.2.2 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **2.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
UCC28710	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC28711	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC28712	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC28713	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我*进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28710D	ACTIVE	SOIC	D	7	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28710	Samples
UCC28710DR	ACTIVE	SOIC	D	7	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28710	Samples
UCC28711D	ACTIVE	SOIC	D	7	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28711	Samples
UCC28711DR	ACTIVE	SOIC	D	7	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28711	Samples
UCC28712D	ACTIVE	SOIC	D	7	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28712	Samples
UCC28712DR	ACTIVE	SOIC	D	7	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28712	Samples
UCC28713D	ACTIVE	SOIC	D	7	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28713	Samples
UCC28713DR	ACTIVE	SOIC	D	7	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28713	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

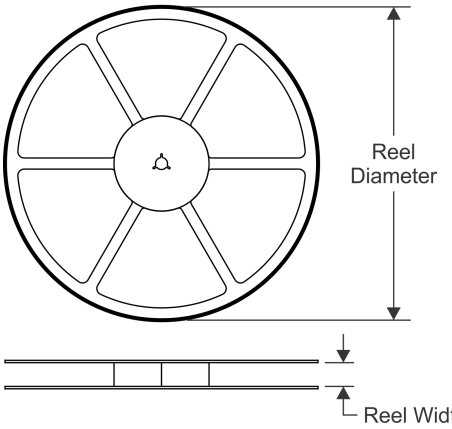
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

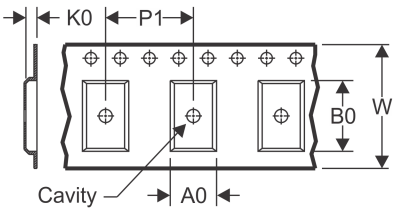
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

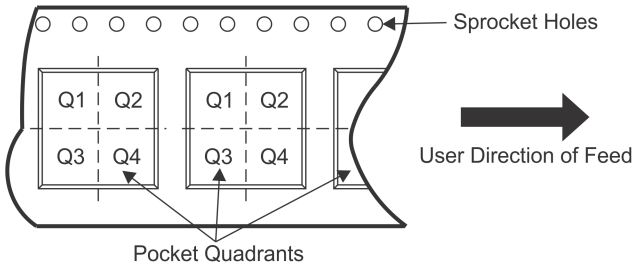


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

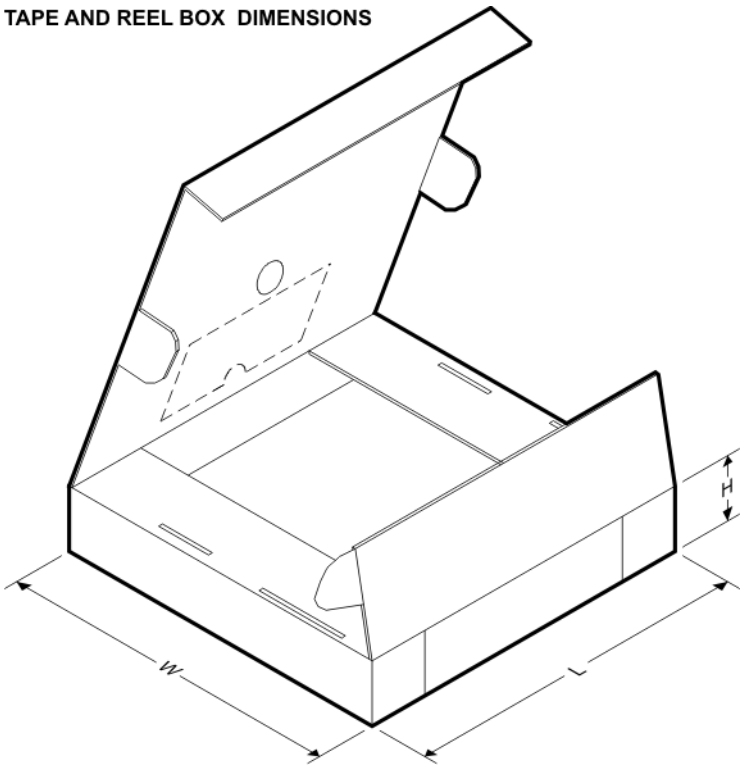
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

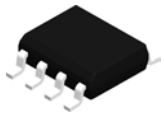
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28710DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28711DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28712DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28713DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28710DR	SOIC	D	7	2500	853.0	449.0	35.0
UCC28711DR	SOIC	D	7	2500	853.0	449.0	35.0
UCC28712DR	SOIC	D	7	2500	853.0	449.0	35.0
UCC28713DR	SOIC	D	7	2500	853.0	449.0	35.0

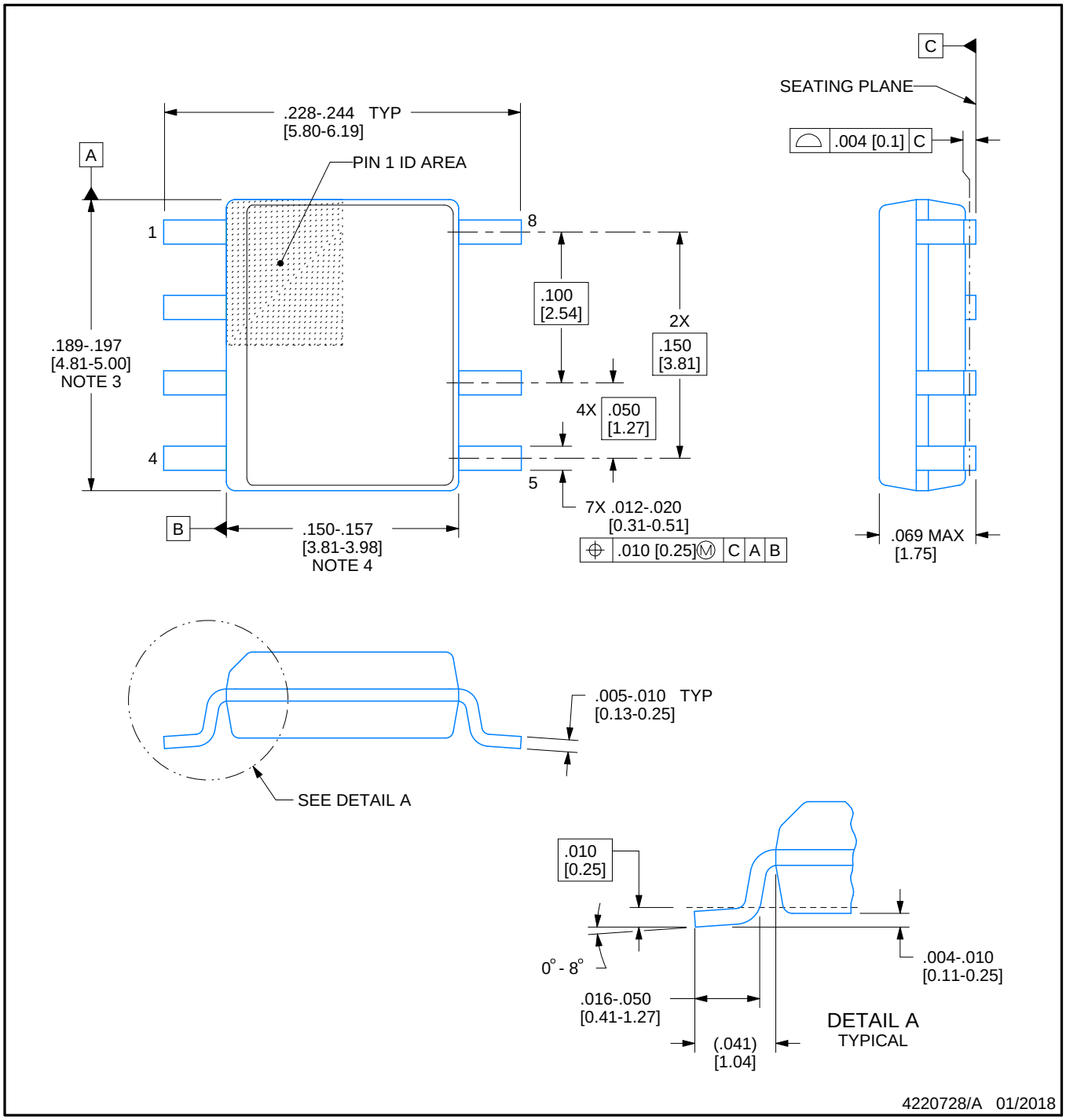


PACKAGE OUTLINE

D0007A

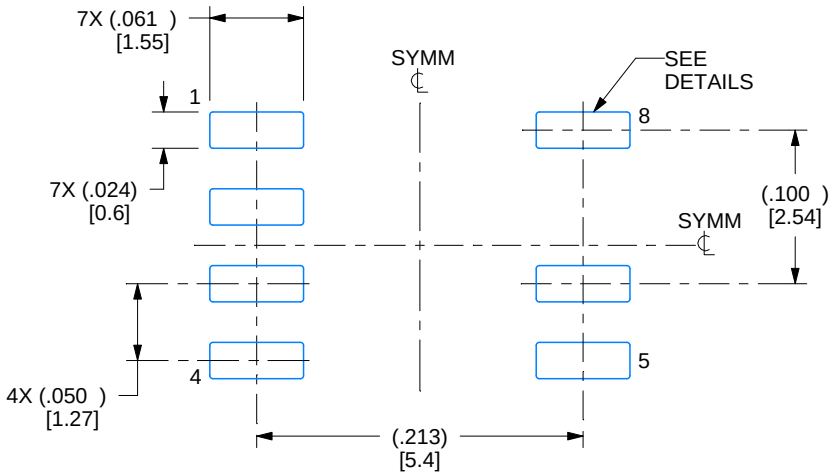
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

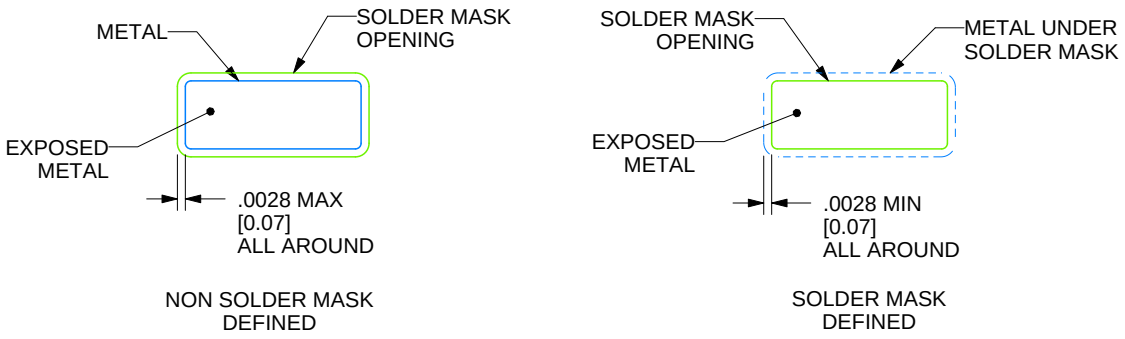


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

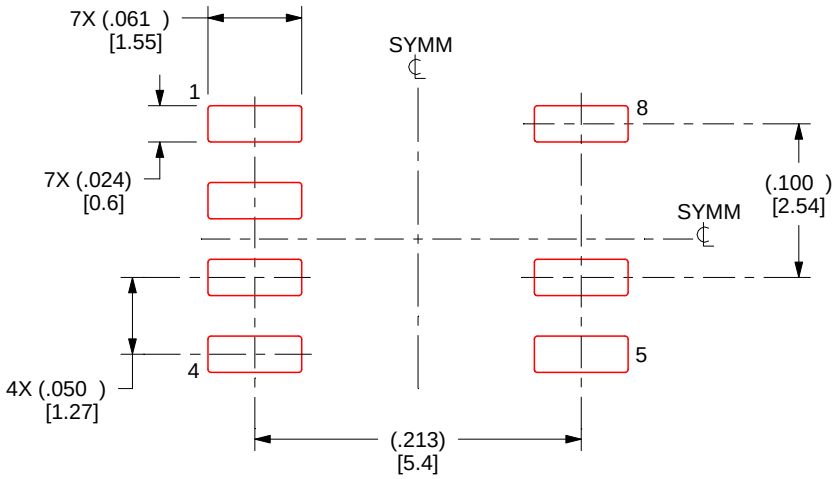
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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