TPS37x (65 V & 2 µA) Over & Undervoltage Detector with Delay Function

1 Features

- VDD: 2.7 V to 65 V (V_{POR} = 1.4 V)
- SENSE and RESET pins are 65 V graded
- Low supply current: 1 µA (Typ.)
- Flexible voltage options Table 14-2
  - 2.7 V to 36 V (1.5% max accuracy)
  - 800 mV option (1% max accuracy)
- Built-in hysteresis (V_{HYS})
  - Percentage options: 2% to 13% (1% steps)
  - Fixed options: VTH < 8 V = 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V
- Programmable reset time delay
  - 10 nF = 12.8 ms, 10 µF = 12.8 s
- Programmable sense time delay
  - 10 nF = 1.28 ms, 10 µF = 1.28 s
- Manual reset feature
- Output reset latching feature
- Output topology:
  - Channel 1: Open-Drain or Push-Pull topologies
  - Channel 2: Open-Drain

2 Applications

- Gateway
- PLC
- I/O Module
- Servo/AC Motor Control
- Factory Automation
- Power Tools

3 Description

The TPS37x is a 65 V-input voltage detector with 1 µA I_{DD}, 1% accuracy, and 10 µs detection time in a 6.25 mm^2 package. This device can be connected directly to 12 V / 24 V to monitor for overvoltage (OV) and undervoltage (UV); with its internal resistor divider, the TPS37x offers the smallest total solution size. This combination of features is ideal for Factory/Building Automation and Motor Drives. Built-in hysteresis on the SENSE pins prevents false reset signals when the monitored a supply voltage rail.

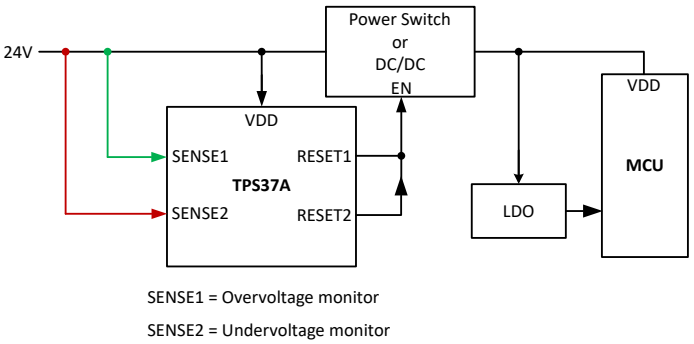
The separate VDD and SENSE pins allow for the redundancy sought by high-reliability systems. SENSE is decoupled from VDD and can monitor higher and lower voltages than VDD. Optional use of external resistors are supported by the high impedance input of the SENSE pins. Both CTSx and CTRx provide delay adjustability on the rising and falling edges of the RESET signals. Also, CTSx functions as a debouncer by ignoring voltage glitches on the monitored voltage rails; CTRx operates as a manual reset ($\overline{MR}$) that can be used to force a system reset.

The TPS37x is available in a small 2.5-mm×2.5-mm×0.1-mm WSON 10-pin wettable flanks package. The central pad is non-conductive to increase the creepage between VDD and GND per guidelines in IEC60664. TPS37x operates over –40°C to +125°C (T_A).

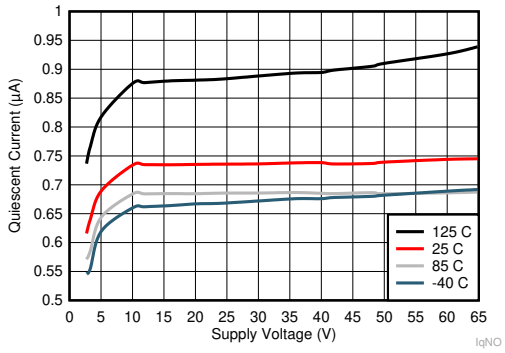
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPS37x	WSON (10) (DSK)	2.5 mm × 2.5 mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.



Typical Application Circuit



Typical Supply Current vs VDD

ADVANCE INFORMATION

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4 Revision History

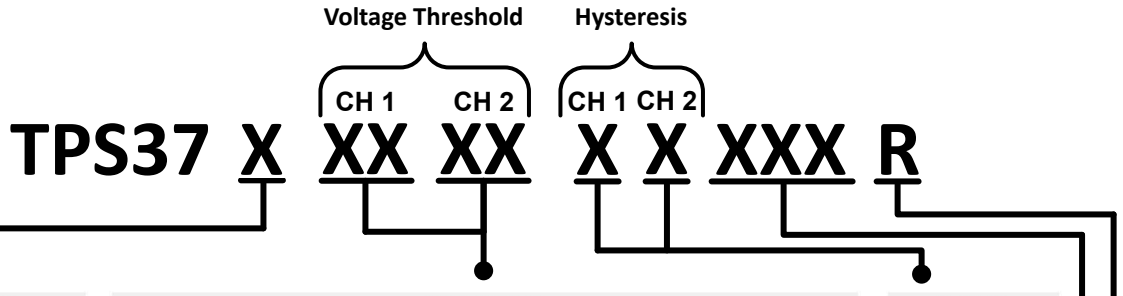
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2020) to Revision B (January 2021)	Page
• APL Update	1
• Edited both Power Cycle figures (SENSE Outside and Within Nominal Voltage)	12
• Corrected the Hysteresis titles for both Undervoltage figures	14
• Corrected Channel 1 of TPS37E from Open-Drain Low to Open-Drain High in Output Logic table	15
• Added reset time delay discharge guideline	16
• Added reset time delay discharge guideline	16
• Added Device Functional Modes tables	18
• Added correct Package Outline figure	26

Changes from Revision * (October 2020) to Revision A (November 2020)	Page
• Updated typical application circuit	1

5 Device Comparison

Contact TI sales representatives or consult TI's E2E forum for details and availability; minimum order quantities may apply.



Topology

Suffix	CH1	CH2
A	OV OD L	UV OD L
B	OV PP H	UV OD L
C	OV OD L	UV OD H
D	OV PP H	UV OD H
E	OV OD H	UV OD H
F	OV OD H	UV OD L
G	OV PP L	UV OD H
H	OV PP L	UV OD L

Threshold Voltage

100mV steps				400mV steps		500mV steps		1V steps	
Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT
01	800mV	70	7.0V	A0	10.4V	D0	20.5V	F0	31.0V
27	2.7V	71	7.1V	A1	10.8V	D1	21.0V	F1	32.0V
28	2.8V	72	7.2V	A2	11.2V	D2	21.5V	F2	33.0V
29	2.9V	73	7.3V	A3	11.6V	D3	22.0V	F3	34.0V
30	3.0V	74	7.4V	A4	12.0V	D4	22.5V	F4	35.0V
31	3.1V	75	7.5V	A5	12.4V	D5	23.0V	F5	36.0V
32	3.2V	76	7.6V	A6	12.8V	D6	23.5V		
33	3.3V	77	7.7V	A7	13.2V	D7	24.0V		
34	3.4V	78	7.8V	A8	13.6V	D8	24.5V		
35	3.5V	79	7.9V	A9	14.0V	D9	25.0V		
36	3.6V	80	8.0V	B0	14.4V	E0	25.5V		
37	3.7V	81	8.1V	B1	14.8V	E1	26.0V		
38	3.8V	82	8.2V	B2	15.2V	E2	26.5V		
39	3.9V	83	8.3V	B3	15.6V	E3	27.0V		
40	4.0V	84	8.4V	B4	16.0V	E4	27.5V		
41	4.1V	85	8.5V	B5	16.4V	E5	28.0V		
42	4.2V	86	8.6V	B6	16.8V	E6	28.5V		
43	4.3V	87	8.7V	B7	17.2V	E7	29.0V		
44	4.4V	88	8.8V	B8	17.6V	E8	29.5V		
45	4.5V	89	8.9V	B9	18.0V	E9	30.0V		
46	4.6V	90	9.0V	C0	18.4V				
47	4.7V	91	9.1V	C1	18.8V				
48	4.8V	92	9.2V	C2	19.2V				
49	4.9V	93	9.3V	C3	19.6V				
50	5.0V	94	9.4V	C4	20.0V				
51	5.1V	95	9.5V						
52	5.2V	96	9.6V						
53	5.3V	97	9.7V						
54	5.4V	98	9.8V						
55	5.5V	99	9.9V						
56	5.6V	00	10.0V						
57	5.7V								
58	5.8V								
59	5.9V								
60	6.0V								
61	6.1V								
62	6.2V								
63	6.3V								
64	6.4V								
65	6.5V								
66	6.6V								
67	6.7V								
68	6.8V								
69	6.9V								

Hysteresis

Suffix	CH1
2	2%
3	3%
4	4%
5	5%
6	6%
7	7%
8	8%
9	9%
A	10%
B	11%
C	12%
D	13%
E	0.5V
F	1V
G	1.5V
H	2V
I	2.5V

Package

Suffix	Name
DSK	WSON
DDF	SOT-23

Reel

Suffix	Name
R	Large

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1. Sense logic: OV = Over-Voltage; UV = Under-Voltage
2. Reset topology: PP = Push-Pull; OD = Open-Drain
3. Reset logic: L = Active-Low; H = Active-High
4. A to I hysteresis options are only available for 2.9 V to 9 V threshold options

ADVANCE INFORMATION

6 Pin Configuration and Functions

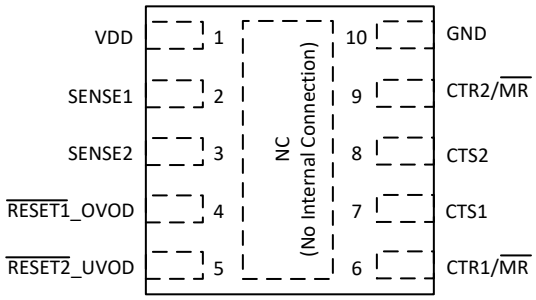

Figure 6-1. DSK Package, 10-Pin WSON, TPS37A (Top View)

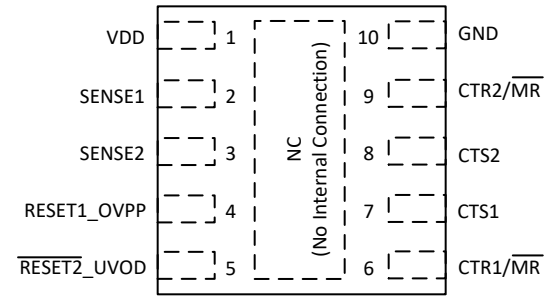

Figure 6-2. DSK Package, 10-Pin WSON, TPS37B (Top View)

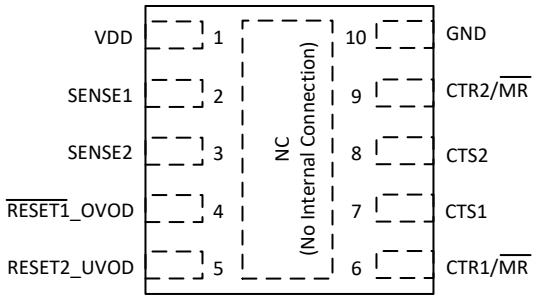

Figure 6-3. DSK Package, 10-Pin WSON, TPS37C (Top View)

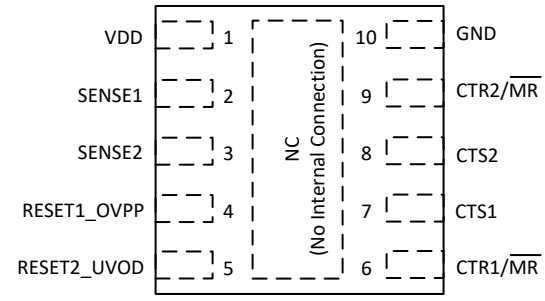

Figure 6-4. DSK Package, 10-Pin WSON, TPS37D (Top View)

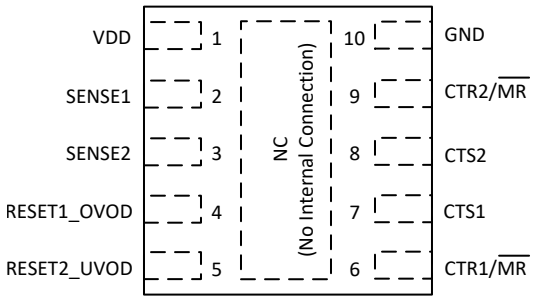

Figure 6-5. DSK Package, 10-Pin WSON, TPS37E (Top View)

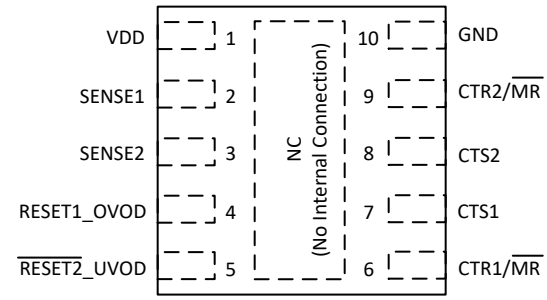

Figure 6-6. DSK Package, 10-Pin WSON, TPS37F (Top View)

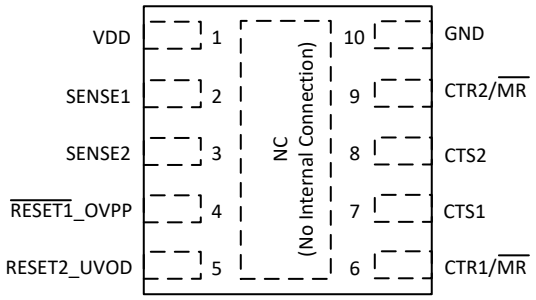

Figure 6-7. DSK Package, 10-Pin WSON, TPS37G (Top View)

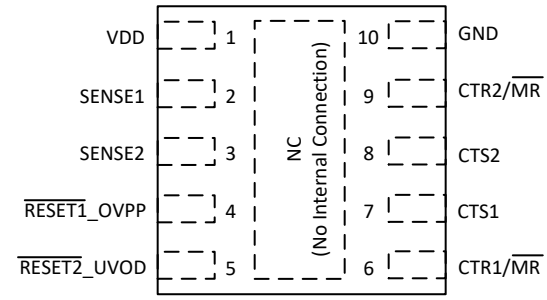

Figure 6-8. DSK Package, 10-Pin WSON, TPS37H (Top View)

Table 6-1. Pin Functions Generic

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	**Input Supply Voltage.**
SENSE1	2	I	Input for the monitored supply voltage rail channel 1
SENSE2	3	I	Input for the monitored supply voltage rail channel 2
RESET1/$\overline{\text{RESET1}}$	4	O	**Output Reset Signal For Channel 1**: See Section 14.1
RESET2/$\overline{\text{RESET2}}$	5	O	**Output Reset Signal For Channel 2**: See Section 14.1
CTR1/ $\overline{\text{MR}}$	6	_	**Capacitor Time Delay Reset 1**: User-programmable reset release delay for Reset 1. Connect an external capacitor for adjustable time delay or leave floating for fastest delay. **Manual Reset:** If this pin is driven low the RESET1 output will reset, leave pin floating or connected to a cap to release reset. This pin should not be driven high.
CTR2/ $\overline{\text{MR}}$	9	_	**Capacitor Time Delay Reset 2**: User-programmable reset release delay for Reset 2. Connect an external capacitor for adjustable time delay or leave floating for fastest delay. **Manual Reset:** If this pin is driven low the RESET2 output will reset, leave pin floating or connected to a cap to release reset. This pin should not be driven high.
GND	10	_	**Ground**
NC	PAD	-	Not internally connected, the PAD can be connected to VDD, GND or be left floating.
CTS1	7	_	**Capacitor Time Delay Sense 1**: User-programmable sense delay for Sense 1. Connect an external capacitor for adjustable time delay or leave floating for fastest delay.
CTS2	8	_	**Capacitor Time Delay Sense 2**: User-programmable sense delay for Sense 2. Connect an external capacitor for adjustable time delay or leave floating for fastest delay.
TPS37A			
$\overline{\text{RESET1}}$_OVOD	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Open Drain, Active Low topology.
$\overline{\text{RESET2}}$_UVOD	5	O	Reset output signal for Sense 2. Topology: Undervoltage, Open Drain, Active Low topology.
TPS37B			
RESET1_OVPP	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Push Pull, Active High topology.
$\overline{\text{RESET2}}$_UVOD	5	O	Reset output signal for Sense 2. Topology: Undervoltage, Open Drain, Active Low topology.
TPS37C			
$\overline{\text{RESET1}}$_OVOD	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Open Drain, Active Low topology.
RESET2_UVOD	5	O	Reset output signal for Sense 2. Topology: Undervoltage, Open Drain, Active High topology.
TPS37D			
RESET1_OVPP	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Push Pull, Active High topology.
RESET2_UVOD	5	O	Reset output signal for Sense 2. Topology: Undervoltage, Open Drain, Active High topology.
TPS37E			
RESET1_OVOD	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Open Drain, Active High topology.
RESET2_UVOD	5	O	Reset output signal for Sense 2. Topology: Undervoltage, Open Drain, Active High topology.
TPS37F			
RESET1_OVOD	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Open Drain, Active High topology.
$\overline{\text{RESET2}}$_UVPP	5	O	Reset output signal for Sense 2. Topology: Undervoltage, Push Pull, Active Low topology.
TPS37G			
$\overline{\text{RESET1}}$_OVPP	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Push Pull, Active Low topology.
RESET2_UVOD	5	O	Reset output signal for Sense 2. Topology: Undervoltage, Open Drain, Active High topology.
TPS37H			
$\overline{\text{RESET1}}$_OVPP	4	O	Reset output signal for Sense 1. Topology: Overvoltage, Push Pull, Active Low topology.
$\overline{\text{RESET2}}$_UVOD	5	O	Reset output signal for Sense 2. Topology: Overvoltage, Open Drain, Active Low topology.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD, V_{SENSE1},V_{SENSE2}, V_{RESET1}, V_{RESET2}, $V_{\overline{RESET1}}$, $V_{\overline{RESET2}}$	–0.3	70	
Voltage	V_{CTS1}, V_{CTS2}, V_{CTR1}, V_{CTR2}	–0.3	6	
Current	I_{RESET1}, I_{RESET2}, $I_{\overline{RESET1}}$, $I_{\overline{RESET2}}$		10	mA
Temperature(2)	Operating junction temperature, T_J	–40	150	°C
Temperature(2)	Operating Ambient temperature, T_A	–40	150	°C
Temperature(2)	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	2.7		65	V
Voltage	V_{SENSE1},V_{SENSE2}, V_{RESET1}, V_{RESET2}, $V_{\overline{RESET1}}$, $V_{\overline{RESET2}}$	0		65	V
Voltage	V_{CTS1}, V_{CTS2}, V_{CTR1}, V_{CTR2}	0		5.5	V
Current	I_{RESET1}, I_{RESET2}, $I_{\overline{RESET1}}$, $I_{\overline{RESET2}}$	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DSK 10-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	34.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR1 / $\overline{MR}$ = CTR2 / $\overline{MR}$ = CTS1 = CTS2 = Open, Output reset Pullup Resistor (R_{PULLUP}) = 10 kΩ, Output reset Pullup Voltage (V_{PULLUP}) = 5.5 V, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 16 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
V_{DD}	Supply Voltage		2.7		65	V
UVLO [2]	Under Voltage Lockout	V_{DD} Falling below $V_{DD\ (MIN)}$			2.7	V
V_{POR}	Power on Reset Voltage[5] $\overline{RESET}$, Active Low (Open-Drain, Push-Pull)	$V_{OL(max)}$ = 300 mV $I_{OUT\ (Sink)}$ = 15 µA			1.4	V
V_{POR}	Power on Reset Voltage[5] RESET, Active High (Push-Pull)	$V_{OH(min)}$ = 0.8 x V_{DD} $I_{OUT\ (Source)}$ = 15 µA			1.4	V
I_{DD}	Supply current into VDD pin	V_{IT} = 800 mV $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$		1	2.6	µA
		V_{IT} = 2.7 V to 36 V $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$		1	2	µA
SENSE (Input)						
I_{SENSE}	Input current (SENSE1, SENSE2)	V_{IT} = 800 mV			100	nA
I_{SENSE}	Input current (SENSE1, SENSE2)	V_{IT} < 10 V			0.8	uA
I_{SENSE}	Input current (SENSE1, SENSE2)	10 V < V_{IT} < 26 V			1.2	uA
I_{SENSE}	Input current (SENSE1, SENSE2)	V_{IT} > 26 V			2	uA
V_{ITN}	Input Threshold Negative (Under-Voltage)	V_{IT} = 2.7 V to 36 V	-1.5		1.5	%
		V_{IT} = 800 mV[3]	0.792	0.800	0.808	V
V_{ITP}	Input Threshold Positive (Over-Voltage)	V_{IT} = 2.7 V to 36 V	-1.5		1.5	%
		V_{IT} = 800 mV[3]	0.792	0.800	0.808	V
V_{HYS}	Hysteresis Accuracy[1]	V_{IT} = 0.8 V and 2.7 V to 36 V V_{HYS} Range = 2% to 13% (1% step)	-1.5		1.5	%
		V_{IT} = 2.7 V to 8 V V_{HYS} = 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V V_{IT}-V_{HYS} ≥ 2.4 V	-1.5		1.5	%
RESET (output)						
$I_{lkg(OD)}$	Open-Drain leakage (RESET1, RESET2)	V_{RESET} = 5.5 V V_{ITN} < V_{SENSE} < V_{ITP}			300	nA
		V_{RESET} = 65 V V_{ITN} < V_{SENSE} < V_{ITP}			300	nA
V_{OL} [4]	Low level output voltage	2.7 V ≤ VDD ≤ 65 V I_{RESET} = 5 mA			300	mV
V_{OH_DO}	High level output voltage dropout (V_{DD} - V_{OH} = V_{OH_DO}) (Push-Pull only)	2.7 V ≤ VDD ≤ 65 V I_{RESET} = 500 uA			43	mV
V_{OH} [4]	High level output voltage (Push-Pull only)	2.7 V ≤ VDD ≤ 65 V I_{RESET} = 5 mA	0.8V_{DD}			V

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7.5 Electrical Characteristics (continued)

At $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR1 / $\overline{MR}$ = CTR2 / $\overline{MR}$ = CTS1 = CTS2 = Open, Output reset Pullup Resistor (R_{PULLUP}) = 10 kΩ, Output reset Pullup Voltage (V_{PULLUP}) = 5.5 V, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 16 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR1 / $\overline{MR}$, CTR2 / $\overline{MR}$)		877	1000	1147	Kohms
R_{CTS}	Internal resistance ($C_{TS1,}$ C_{TS2})		88	100	122	Kohms
Manual Reset (MR)						
$V_{\overline{MR}\_IH}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic high input	VDD = 2.7 V	2000			mV
$V_{\overline{MR}\_IH}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic high input	VDD = 65 V	2500			mV
$V_{\overline{MR}\_IL}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic low input	VDD = 2.7 V			1300	mV
$V_{\overline{MR}\_IL}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic low input	VDD = 65 V			1300	mV

(1) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.
(2) When V_{DD} voltage falls below UVLO, reset is asserted for Output 1 and Output 2. V_{DD} slew rate ≤ 100mV/µs
(3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
(4) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**
(5) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below VPOR, the output cannot be determined. V_{DD} dv/dt ≤ 100mV/µs

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7.6 Timing Requirements

At $V_{DD\_(MIN)} \le V_{DD} \le V_{DD\_(MAX)}$, CTR1/$\overline{MR}$ = CTR2/$\overline{MR}$ = CTS1 = CTS2 = Open (1), Output reset Pullup Resistor (R_{PULLUP}) = 10 kΩ, Output reset Pullup Voltage (V_{PULLUP}) = 5.5V, output reset load (C_{LOAD}) = 10 pF, VDD and SENSE slew rate = 1V/us, over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C and VDD=16 V and VIT = 6.5 V (VIT refers to either V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters						
t_{CTR}	Reset release time delay (CTR1/$\overline{MR}$, CTR2/$\overline{MR}$)(3)	VIT = 2.7 V to 36 V C_{TR1} = C_{TR2} = Open 20% Overdrive from Hysteresis			100	us
		VIT = 800 mV C_{TR1} = C_{TR2} = Open 20% Overdrive from Hysteresis			40	us
t_{CTS}	Sense detect time delay (CTS1, CTS2)(4)	VIT = 2.7 V to 36 V C_{TS1} = C_{TS2} = Open 20% Overdrive from V_{IT}		34	90	us
		VIT = 800 mV C_{TS1} = C_{TS2} = Open 20% Overdrive from V_{IT}	8		11	us
t_{SD}	Startup Delay(2)	$C_{TR1/MR}$ = C_{TR2} = Open			2	ms

(1) C_{TR1} = Reset delay channel 1, C_{TR2} = Reset delay channel 2,
C_{TS1} = Sense delay channel 1, C_{TS2} = Sense delay channel 2

(2) During the power-on sequence,VDD mustbe at or above VDD (MIN) for at least t_{SD} before the output is in the correct state based on V_{SENSE}.
t_{SD} time includes the propagation delay (C_{TR1} = C_{TR2} = Open). Capaicitor in C_{TR1} or C_{TR2} will add time to t_{SD}.

(3) **CTR Reset detect time delay:**
OVER-voltage active-LOW output is measure from $V_{ITP\ -\ HYS}$ to V_{OH}
UNDER-voltage active-LOW output is measure from $V_{ITN\ +\ HYS}$ to V_{OH}
OVER-voltage active-HIGH output is measure from $V_{ITP\ -\ HYS}$ to V_{OL}
UNDER-voltage active-HIGH output is measure from $V_{ITN\ +\ HYS}$ to V_{OL}

(4) **CTS Sense detect time delay:**
Active-low output is measure from V_{IT} to V_{OL} (or V_{Pullup})
Active-high output is measured from V_{IT} to V_{OH}
V_{IT} refers to either V_{ITN} or V_{ITP}

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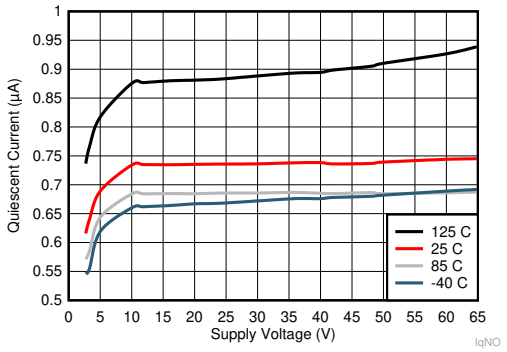
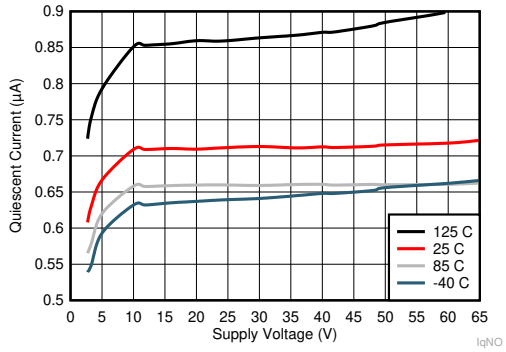
8 Typical Characteristics

Typical characteristics show the typical performance of the TPS37x device. Test conditions are T_J = 25°C, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.



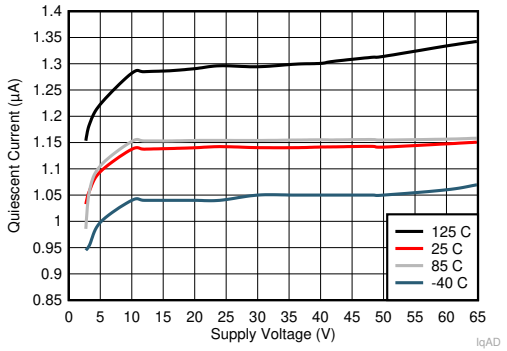
$\overline{RESET}$ = high, V_{IT} = 2.7V

Figure 8-1. Supply Voltage (V_{DD}) vs Supply Voltage (I_{DD}) over Temperature



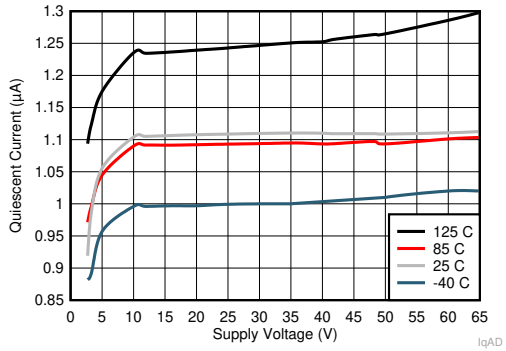
$\overline{RESET}$ = low, V_{IT} = 2.7V

Figure 8-2. Supply Voltage (V_{DD}) vs Supply Current (I_{DD}) over Temperature



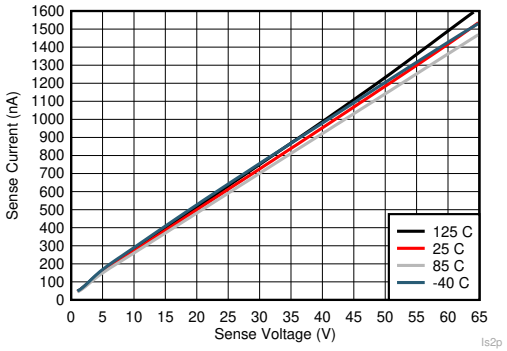
$\overline{RESET}$ = high, V_{IT} = 0.8V

Figure 8-3. Supply Voltage (V_{DD}) vs Supply Current (I_{DD}) over Temperature



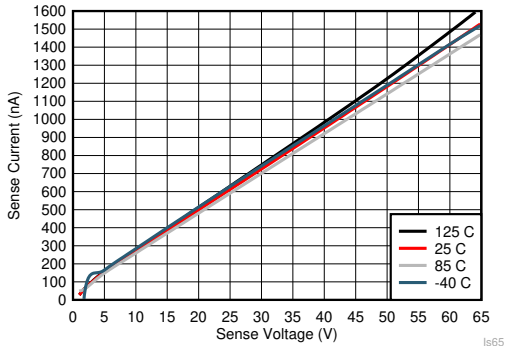
$\overline{RESET}$ = low, V_{IT} = 0.8V

Figure 8-4. Supply Voltage (V_{DD}) vs Supply Current (I_{DD}) over Temperature



V_{DD} = 2.7V

Figure 8-5. Sense Voltage (V_{SENSE}) vs Sense Current (I_{SENSE}) over Temperature



V_{DD} = 65V

Figure 8-6. Sense Voltage (V_{SENSE}) vs Sense Current (I_{SENSE}) over Temperature

9 Detailed Description

9.1 Overview

The TPS37x is a family of high voltage and low quiescent current reset IC with fixed threshold voltage. Voltage divider is integrated to eliminate the need for external resistors and eliminate leakage current that comes with resistor dividers. However, it can also support external resistor if required by application, the lowest threshold 800 mV (bypass internal resistor ladder) is recommenced for external resistors use case to take advantage of faster detection time and lower I_{SENSE} current.

VDD, SENSE and RESET pins can support 65 V continuos operation; both VDD and SENSE voltage levels can be independent of each other, meaning VDD pin can be connected at 2.7 V while SENSE pins are connected to a higher voltage.

Additional features include programable sense time delay (CTS1, CTS2) and reset delay time and manual reset (CTR1/MR, CTR2/MR).

9.2 Functional Block Diagram

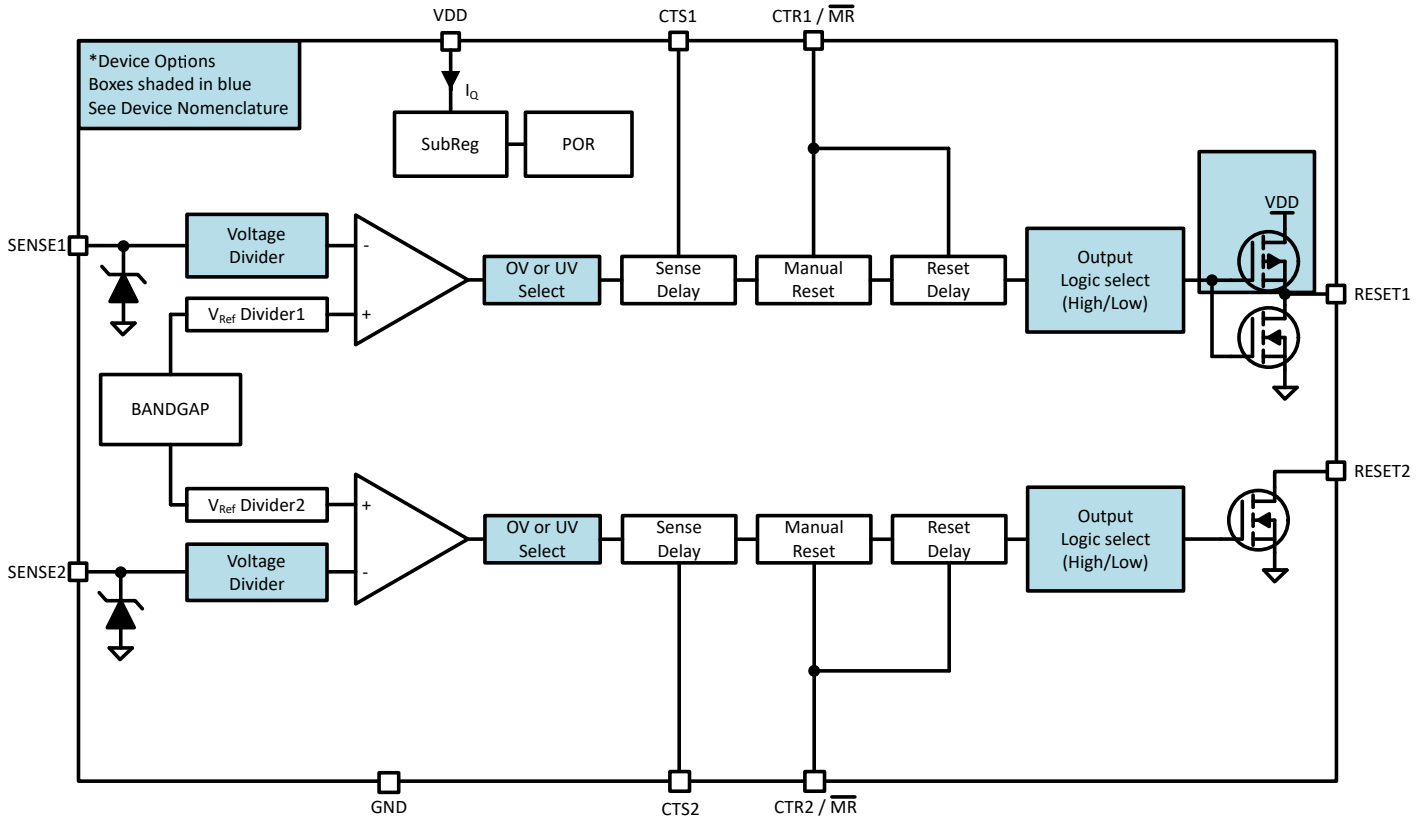


Figure 9-1. Functional Block Diagram [1]

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[1] Refer to Section 14.1 for complete list of topologies and output logic combination

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9.3 Feature Description

9.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1-µF capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET}, meaning that VDD can be higher or lower than the other pins.

9.3.1.1 Undervoltage Lockout (V_{POR} < V_{DD} < UVLO)

When the voltage on VDD is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the output pins will be in reset, regardless of the voltage at SENSE pins.

9.3.1.2 Power-On Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

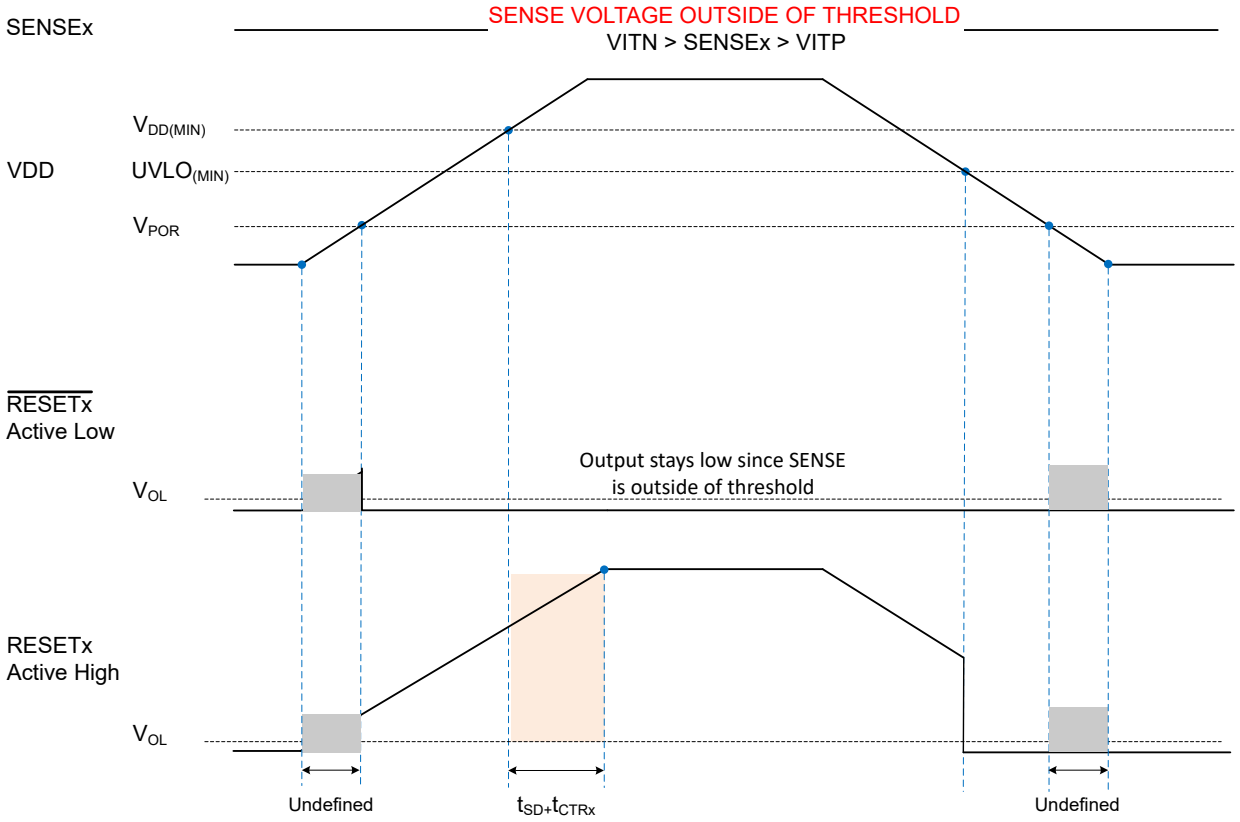

Figure 9-2. Power Cycle (SENSE Outside of Nominal voltage) [2]

[2] Figure assume Pull-up resistor connected to VDD

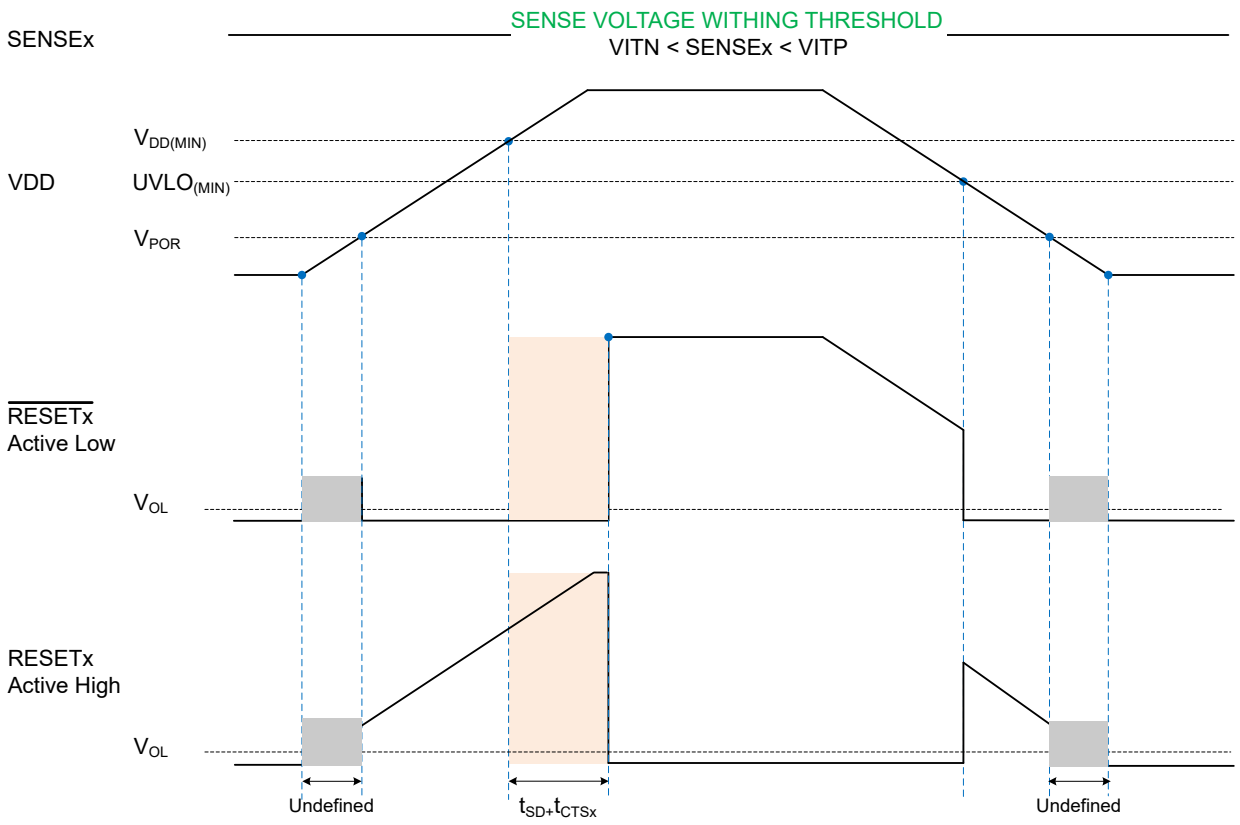

Figure 9-3. Power Cycle (SENSE Within Nominal voltage) [3]

[3] Figure assume Pull-up resistor connected to VDD

9.3.2 SENSE

The TPS37x high voltage family integrates two voltage comparators, a precision reference voltage and trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Device also has built-in hysteresis that provides noise immunity and ensures stable operation.

Channels are independent of each other, meaning that SENSE1 and SENSE2 and respective outputs can be connected to different voltage rails.

9.3.2.1 SENSE Hysteresis

Built-in hysteresis to avoid erroneous output reset release. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

For all the hysteresis options possible see Table 14-1.

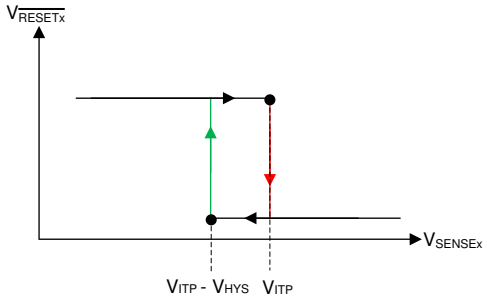

Figure 9-4. Hysteresis (Overvoltage Active-Low)

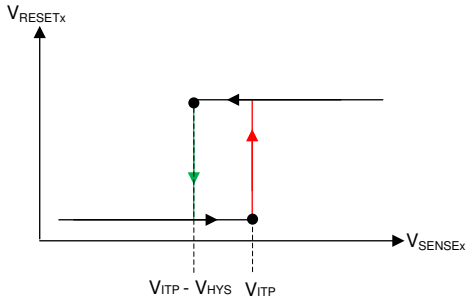

Figure 9-5. Hysteresis (Overvoltage Active-High)

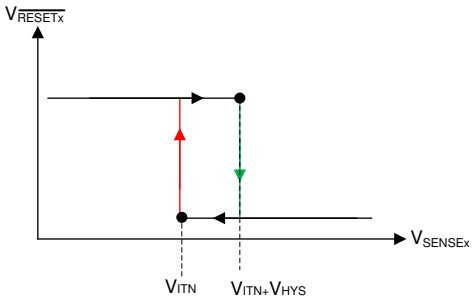

Figure 9-6. Hysteresis (Undervoltage Active-High)

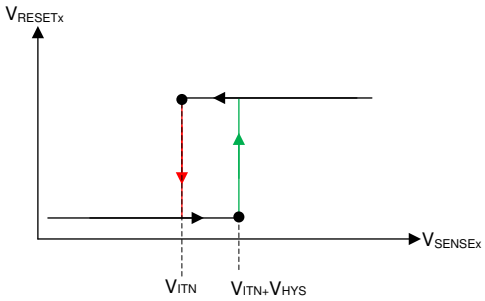

Figure 9-7. Hysteresis (Undervoltage Active-Low)

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9.3.3 Output Logic Configurations

TPS37x has two channels with separate sense pins and reset pins that can be configured independently of each other. Channel 1 is available as Open-Drain and Push-Pull while channel 2 is only available as Open-Drain topology.

The available output logic configuration combinations are shown in Table 9-1.

Table 9-1. TPS37x Output Logic

DESCRIPTION	NOMENCLATURE	VALUE	
GPN	**TPS37 (+ topology)**	**CHANNEL 1**	**CHANNEL 2**
Topology (OV and UV only) both channels are either OV or UV • UV = Undervoltage • OV = Overvoltage • PP = Push Pull • OD = Open Drain • L = Active low • H = Active high	TPS37A	OV OD L	UV OD L
	TPS37B	OV PP H	UV OD L
	TPS37C	OV OD L	UV OD H
	TPS37D	OV PP H	UV OD H
	TPS37E	OV OD H	UV OD H
	TPS37F	OV PP H	UV OD L
	TPS37G	OV OD L	UV OD H
	TPS37H	OV OD H	UV OD L
	TPS37I	OV PP L	UV PP L
	TPS37J	OV PP H	UV PP L

9.3.3.1 Open-Drain

Open drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system V_{OH} and the (I_{lkg}) current provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS37X open-drain output pin.

9.3.3.2 Push-Pull

Push-Pull output does not require an external resistor since is the output is internally pulled-up to V_{DD} during V_{OH} condition and output will be connected to GND during V_{OH} condition.

9.3.3.3 Active-High (RESET)

RESET (active-high), denoted with no bar above the pin label. RESET remains low (V_{OL}, deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

9.3.3.4 Active-Low ($\overline{RESET}$)

$\overline{RESET}$ (active low) denoted with a bar above the pin label. $\overline{RESET}$ remains high voltage (V_{OH}, deasserted) (open drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

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9.3.4 User-Programmable Reset Time Delay

TPS37X has adjustable reset release time delay with external capacitors. Channel timing are independent of each other.

- A capacitor in CTR1/$\overline{MR}$ program the reset time delay of Output 1.
- A capacitor in CTR2/$\overline{MR}$ program the reset time delay of Output 2.
- No capacitor on this pins gives the fastest reset delay time indicated in the Section 7.6.

9.3.4.1 Reset Time Delay Configuration

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR1 pin and GND, CTR2 for channel 2. In this section CTRx represent either channel 1 or channel 2.

The relationship between external capacitor C_{CTRx_EXT} and the time delay (t_{CTRx}) is given by Equation 1.

$$t_{CTRx} = 1.28 \times R_{CTRx} \times C_{CTRx\_EXT} \quad (1)$$

R_{CTRx} = is in kilo ohms (kOhms)

C_{CTRX_EXT} = is given in microfarads (µF)

t_{CTRx} = is in milliseconds (ms)

The recommended maximum reset delay capacitor for the TPS37x is limited to a percentage of the period or duration of the programmed reset time delay to ensure enough time for the capacitor to fully discharge when a voltage fault occurs. When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 5% of the programmed reset time delay.

9.3.5 User-Programmable Sense Delay

TPS37X has adjustable sense release time delay with external capacitors. Channel timing are independent of each other. Sense delay is used as a de-glitcher or ignoring known transients.

- A capacitor in CTS1 program the excursion detection on sense 1.
- A capacitor in CTS2 program the excursion detection on sense 2.
- No capacitor on this pins gives the fastest detection time indicated in the Section 7.6.

9.3.5.1 Sense Time Delay Configuration

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTR1 pin and GND, CTS2 for channel 2. In this section CTRx represent either channel 1 or channel 2

The relationship between external capacitor C_{CTSx_EXT} and the time delay (t_{CTSx}) is given by Equation 2.

$$t_{CTSx} = 1.28 \times R_{CTSx} \times C_{CTSx\_EXT} \quad (2)$$

R_{CTSx} = is in kilo ohms (kOhms)

C_{CTSX_EXT} = is given in microfarads (µF)

t_{CTSx} = is in milliseconds (ms)

The recommended maximum sense delay capacitor for the TPS37x is limited to a percentage of the period or duration of the programmed sense time delay to ensure enough time for the capacitor to fully discharge when a voltage fault occurs. When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time

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to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed sense time delay.

9.3.6 Manual RESET (CTR1/ $\overline{MR}$) and (CTR2/ $\overline{MR}$) Input

The manual reset input allows a processor or other logic circuits to initiate a reset. In this section $\overline{MR}$ is a generic reference to (CTR1/ $\overline{MR}$) and (CTR2/ $\overline{MR}$). A logic low on $\overline{MR}$ causes $\overline{RESET1}$ to assert on reset output. After $\overline{MR}$ is left floating, $\overline{RESET1}$ will release the reset if the voltage at SENSE1 pin is at nominal voltage. $\overline{MR}$ should not be driven high, this pin should be left floating or connected to a capacitor to GND, this pin can be left unconnected if is not used.

If the logic driving the $\overline{MR}$ cannot tri-state (floating and GND) then a logic-level FET should be used as illustrated in Figure 9-8.

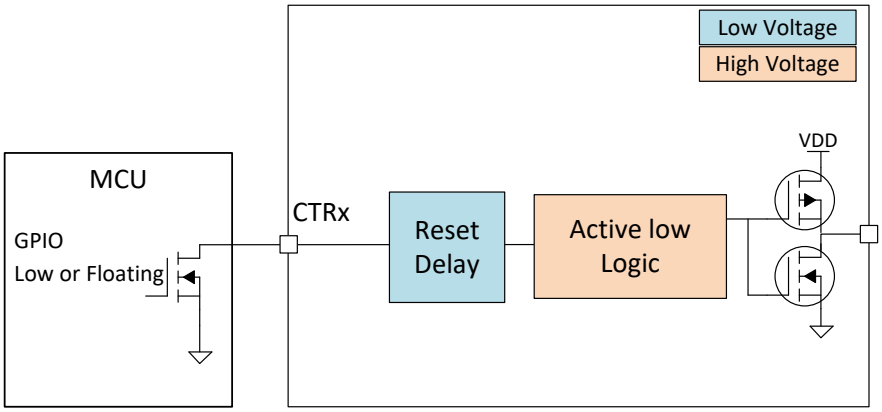

Figure 9-8. Manual Reset Implementation

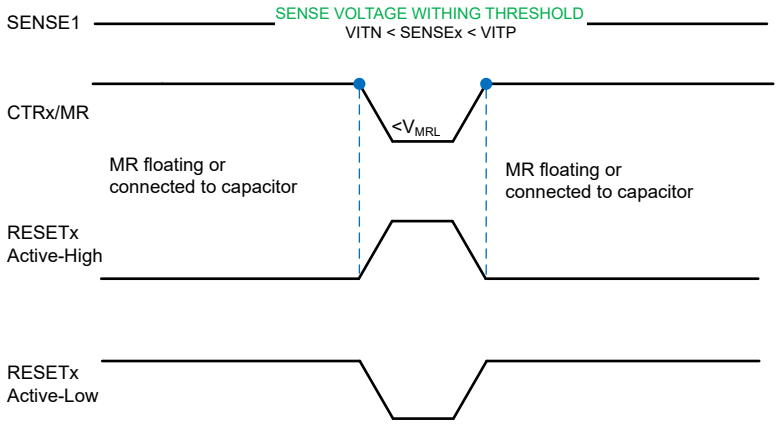

Figure 9-9. Manual Rest Timing Diagram

Table 9-2. $\overline{MR}$ Functional Table

$\overline{MR}$	SENSE ON NOMINAL VOLTAGE	RESET STATUS
Low	Yes	Reset asserted
Floating	Yes	Fast reset release when SENSE voltage goes back to nominal voltage
Capacitor	Yes	Programable reset time delay
High	Yes	NOT Recommended

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10 Device Functional Modes

Table 10-1. Undervoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR(1) / $\overline{MR}$ PIN	VDD PIN	OUTPUT(2) ($\overline{RESET}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Undervoltage Detection	SENSE > $V_{ITN(UV)}$	SENSE < $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Undervoltage Detection	SENSE < $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Normal Operation	SENSE < $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$ + HYS	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Manual Reset	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Low	V_{DD} > $V_{DD(MIN)}$	Low
UVLO Engaged	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{POR} < V_{DD} < $V_{DD(MIN)}$	Low
Below V_{POR}, Undefined Output	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} < V_{POR}	Undefined

1. Reset time delay is ignored in the truth table
2. Open-drain active low output. External pull-up resistor to high voltage

Table 10-2. Overvoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR(1) / $\overline{MR}$ PIN	VDD PIN	OUTPUT(2) ($\overline{RESET}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Undervoltage Detection	SENSE < $V_{ITN(OV)}$	SENSE > $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Undervoltage Detection	SENSE > $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Normal Operation	SENSE > $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$ - HYS	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Manual Reset	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Low	V_{DD} > $V_{DD(MIN)}$	Low
UVLO Engaged	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{POR} < V_{DD} < UVLO	Low
Below V_{POR}, Undefined Output	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} < V_{POR}	Undefined

1. Reset time delay is ignored in the truth table
2. Open-drain active low output. External pull-up resistor to high voltage

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Adjustable Voltage Thresholds

Equation 3 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 2.0 V rail being monitored (V_{MON}) using. Using Equation 3, R1 = 15 kΩ given that R2 = 10 kΩ, V_{MON} = 2 V, and V_{SENSE} = 0.8 V. Using Equation 3, V_{MON} = 1.94 V when $V_{SENSE} = V_{IT-(UV)}$. This can be denoted as V_{MON-}, the monitored undervoltage threshold where the device will assert a reset signal.

$$V_{SENSE} = V_{MON} \times (R_2 \div (R_1 + R_2)) \quad (3)$$

Aside from the tolerance of the resistor divider, the SENSE pin leakage current affects the accuracy of the resistor divider. The sense leakage, I_{SENSE}, is given in Section 7.5. The actual input threshold due to the leakage SENSE current can be calculated with Equation 4

$$I_{VIT\_Actual} = V_{MON} + R_1 ((V_{REF} \div R_2) + I_{SENSE}) \quad (4)$$

11.2 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

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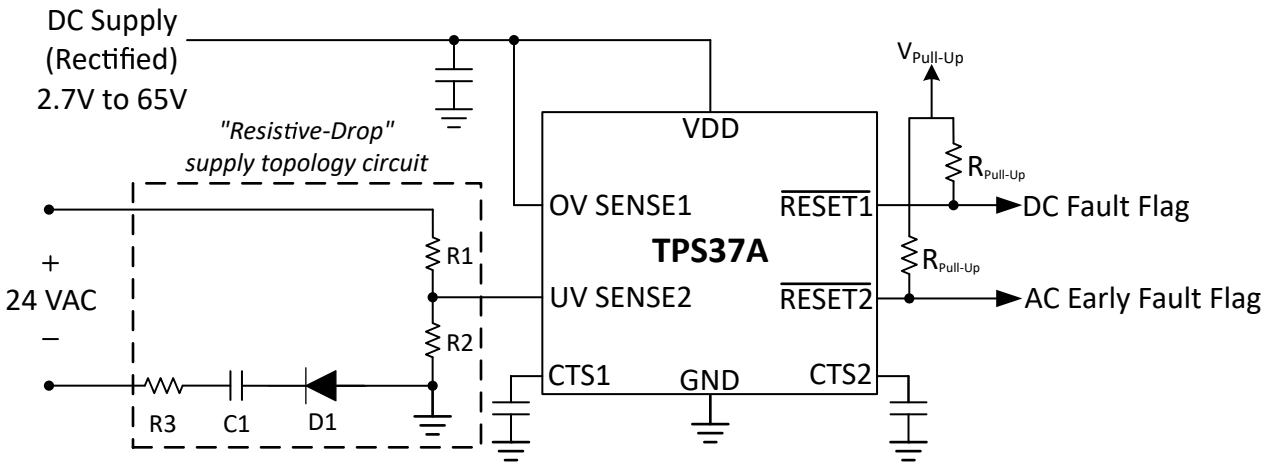
11.2.1 Typical Application

11.2.1.1 Design 1: High Voltage – Fast AC Signal Monitoring For Power Fault Detection

In many industrial and factory automation applications, there are multiple power rails that power various subsystems within the application. Some of these power rails include 24 / 48 VAC AC sources with a known operating frequency that requires a full-bridge rectifier and capacitors to convert its signal to a DC voltage where it can be monitored by a voltage supervisor. One drawback with the described conversion is the response time of the DC voltage when the AC power rail experiences a change of operating frequency or voltage amplitude. Due to the output filter of the full-bridge rectifier, the detection in the change of voltage or operating frequency may require several AC cycles before the voltage supervisor outputs a fault condition. The direct monitoring of the AC source by using a “Resistive-Drop” supply topology circuit provides the user a fast transient fault detection. In this design example, the TPS37A is being highlighted with the ability to offer a unique “window operating” solution by monitoring the output of the AC source for over or undervoltage operation.



* The circuit solution is not isolated and one must take into account when planning to use in high power systems.

Figure 11-1. Sensing an AC Signal for Power Fault Detection

11.2.1.1.1 Design Requirements

This design requires voltage supervision on an AC, with a known operating frequency, power supply rail. The overvoltage fault sensing is achieved by monitoring the DC output of a full bridge rectifier while the undervoltage fault is detected by inputting a half wave signal and its voltage frequency and magnitude are being monitored. The target output of this TPS37A application is for 5 V reset logic.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 24 VAC 800 Hz power supply for undervoltage and overvoltage conditions. Trigger undervoltage fault at 5 V and overvoltage fault at 24 V.	TPS37A provides voltage monitoring with 1.5% max accuracy with adjustable/non-adjustable variations.
Maximum Input Voltage	Operate with power supply input up to 34 V.	The TPS37A can support a VDD of up to 65 V.
Output logic voltage	Open-Drain Output Topology	An open-drain output is recommended to provide the a 5 V reset signal.
SENSE Delay when a fault is detected	$\overline{\text{RESET}}$ delay of at least 0.625 ms which is the time between half wave cycles	C_{CTS2} = 5.6 nF sets 717 µs delay
Voltage Monitor Accuracy	Maximum voltage monitor accuracy of 1.5%.	The TPS37A has 1.5% maximum voltage monitor accuracy.

11.2.1.1.2 Detailed Design Procedure

The main advantage of this unique application is being able to monitor a single AC source with a known operating frequency AC source rail. Because the TPS37A is an over and undervoltage detector with delay

function, detecting faults either from a change of operating frequency range or voltage amplitude of the AC source is achievable.

Figure 11-1 illustrates an example of how the TPS37A is monitoring an AC source. Input to SENSE1 of TPS37A is monitoring a full wave rectifier DC signal. The DC signal is the result from the rectification of the 24 VAC source and monitors the AC source for overvoltage events due to a change of voltage amplitude or an increase to operating frequency. Input to SENSE2 of TPS37A will monitor the AC source by using a "resistive-drop" supply topology circuit. The unique circuit resistively divides the AC voltage signal and provides only the positive half wave Figure 11-2 into SENSE2 input. The half wave signal does not go through any output filter and hence any change to the AC voltage or operating frequency can be rapidly detected. Knowing the operating frequency of the AC source and converting to the time domain, the TPS37A SENSE2 delay can be programmed, by the capacitor on CTS2 pin, to equal or be greater than one-half of the operating period (the frequency of the half wave rectification signal) or the half cycle shown in Figure 11-2. When the half wave voltage amplitude falls below the SENSE2 threshold voltage, the SENSE2 time delay counter begins to increment. If the next half wave voltage amplitude exceeds the SENSE2 threshold voltage, the SENSE2 time delay counter will reset and the TPS37A $\overline{\text{RESET2}}$ pin will indicate no fault was detected. Conversely, if the voltage amplitude of the half wave does not reach the SENSE2 threshold voltage within the programmed time delay of t_{CTS}, a fault will occur. Also, a fault can occur if the operating frequency from the AC source decreases, resulting in lower AC voltage amplitude at the programmed time delay t_{CTS}.

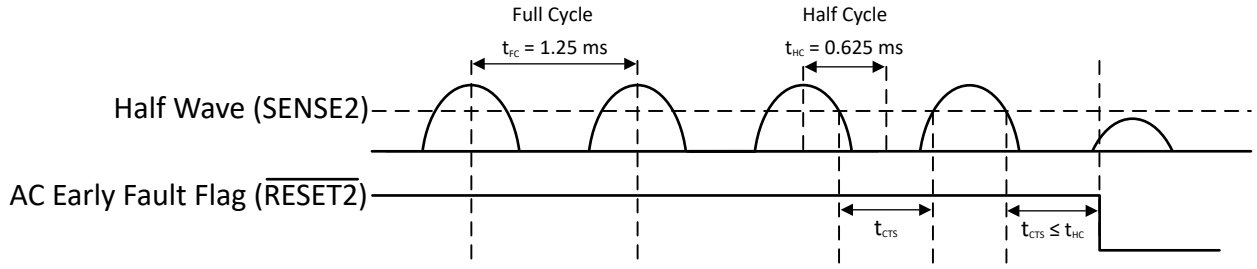


Figure 11-2. Design 2 Timing Diagram

The TPS37A, with its ability of having a wide VDD range from 2.7 V to 65 V and under and overvoltage detection, offers a unique “window operating” AC power rail monitoring solution. Combining SENSE delay feature with the "resistive-drop" supply circuitry, detecting an undervoltage event on the half cycle of the AC power rail provides a fast power fault response. Likewise, the TPS37A provides an overvoltage monitoring and SENSE delay fault detection for the same AC power rail. With under and overvoltage supervision of the AC power rail, applications needing a specific operating DC range to protect its subsystems is achieve through TPS37A. Good design practice recommends using a 0.1-µF capacitor on the VDD pin and this capacitance may need to increase if using an adjustable version with a resistor divider.

Note that this design solution is not isolated and one must take into account when planning to use in high power systems.

ADVANCE INFORMATION

12 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.4 V (V_{POR}) to 65 V (max operation). Good analog design practice recommends placing a minimum 0.1-µF ceramic capacitor as near as possible to the VDD pin.

12.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuos allowable power dissipation for the device in a given package can be calculated using Equation 5:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} – T_A) / R_{\theta JA}) \quad (5)$$

The actual power being dissipated in the device can be represented by Equation 6:

$$P_D = V_{DD} \times I_{DD} + p_{RESET} \quad (6)$$

p_{RESET} is calculated by Equation 7 or Equation 8

$$p_{RESET\ (PUSHPULL)} = VDD - V_{RESET} \times I_{RESET} \quad (7)$$

$$p_{RESET\ (OPEN\text{-}DRAIN)} = V_{RESET} \times I_{RESET} \quad (8)$$

Equation 5 and Equation 6 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 9:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (9)$$

13 Layout

13.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a capacitor is used on CTS1, CTS2, CTR1, or CTR2, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- Place the pull-up resistors on $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ pins as close to the pins as possible.

13.2 Layout Example

The layout example in Figure 13-1 shows how the TPS37x is laid out on a printed circuit board (PCB) with user-defined delays.

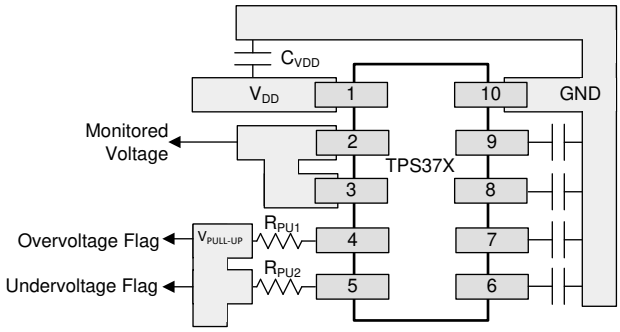


Figure 13-1. TPS37x Recommended Layout

13.3 Creepage Distance

Per IEC 60664 Creepage is the shortest distance between two conductive parts or as shown in Figure 13-2 the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

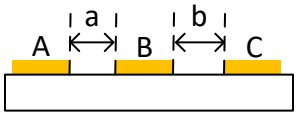


Figure 13-2. Creepage Distance

Figure 13-2 details

- A = Left pins (high voltage)
- B = Central pad (conductive not internally connected
- C = Right pins (low voltages)
- Creepage distance = a + b

ADVANCE INFORMATION

14 Device and Documentation Support

14.1 Device Nomenclature

Section 5 shows how to decode the function of the device based on its part number

Table 14-2 shows TPS37x possible voltage options per channel. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

Table 14-1 shows TPS37x common hysteresis and voltage options.

Table 14-1. Common Hysteresis Lookup Table

TARGET			DEVICE ACTUAL HYSTERESIS OPTION
DETECT THRESHOLD	TOPOLOGY	RELEASE VOLTAGE (V)	
18.0 V	Overvoltage	17.5 V	-3%
18.0 V	Overvoltage	16.0 V	-11%
17.0 V	Overvoltage	16.5 V	-3%
16.0 V	Overvoltage	15.0 V	-6%
15.0 V	Overvoltage	14.0 V	-7%
6.0 V	Undervoltage	6.5 V	0.5 V
5.5 V	Undervoltage	6 V	0.5 V
8 V	Undervoltage	9 V	1 V
5 V	Undervoltage	7.5 V	2.5 V

ADVANCE INFORMATION

Table 14-2. Voltage Options

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS
08	800 mV (divider bypass)	**70**	7.0 V	**A0**	10.4 V	**D0**	20.5 V	**F0**	31.0 V
27	2.7 V	**71**	7.1 V	**A1**	10.8 V	**D1**	21.0 V	**F1**	32.0 V
28	2.8 V	**72**	7.2 V	**A2**	11.2 V	**D2**	21.5 V	**F2**	33.0 V
29	2.9 V	**73**	7.3 V	**A3**	11.6 V	**D3**	22.0 V	**F3**	34.0 V
30	3.0 V	**74**	7.4 V	**A4**	12.0 V	**D4**	22.5 V	**F4**	35.0 V
31	3.1 V	**75**	7.5 V	**A5**	12.4 V	**D5**	23.0 V	**F5**	36.0 V
32	3.2 V	**76**	7.6 V	**A6**	12.8 V	**D6**	23.5 V		
33	3.3 V	**77**	7.7 V	**A7**	13.2 V	**D7**	24.0 V		
34	3.4 V	**78**	7.8 V	**A8**	13.6 V	**D8**	24.5 V		
35	3.5 V	**79**	7.9 V	**A9**	14.0 V	**D9**	25.0 V		
36	3.6 V	**80**	8.0 V	**B0**	14.4 V	**E0**	25.5 V		
37	3.7 V	**81**	8.1 V	**B1**	14.8 V	**E1**	26.0 V		
38	3.8 V	**82**	8.2 V	**B2**	15.2 V	**E2**	26.5 V		
39	3.9 V	**83**	8.3 V	**B3**	15.6 V	**E3**	27.0 V		
40	4.0 V	**84**	8.4 V	**B4**	16.0 V	**E4**	27.5 V		
41	4.1 V	**85**	8.5 V	**B5**	16.4 V	**E5**	28.0 V		
42	4.2 V	**86**	8.6 V	**B6**	16.8 V	**E6**	28.5 V		
43	4.3 V	**87**	8.7 V	**B7**	17.2 V	**E7**	29.0 V		
44	4.4 V	**88**	8.8 V	**B8**	17.6 V	**E8**	29.5 V		
45	4.5 V	**89**	8.9 V	**B9**	18.0 V	**E9**	30.0 V		
46	4.6 V	**90**	9.0 V	**C0**	18.4 V				
47	4.7 V	**91**	9.1 V	**C1**	18.8 V				
48	4.8 V	**92**	9.2 V	**C2**	19.2 V				
49	4.9 V	**93**	9.3 V	**C3**	19.6 V				
50	5.0 V	**94**	9.4 V	**C4**	20.0 V				
51	5.1 V	**95**	9.5 V						
52	5.2 V	**96**	9.6 V						
53	5.3 V	**97**	9.7 V						
54	5.4 V	**98**	9.8 V						
55	5.5 V	**99**	9.9 V						
56	5.6 V	**00**	10.0 V						
57	5.7 V								
58	5.8 V								
59	5.9 V								
60	6.0 V								
61	6.1 V								
62	6.2 V								
63	6.3 V								
64	6.4 V								
65	6.5 V								
66	6.6 V								
67	6.7 V								

ADVANCE INFORMATION

Table 14-2. Voltage Options (continued)

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS
68	6.8 V								
69	6.9 V								

14.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

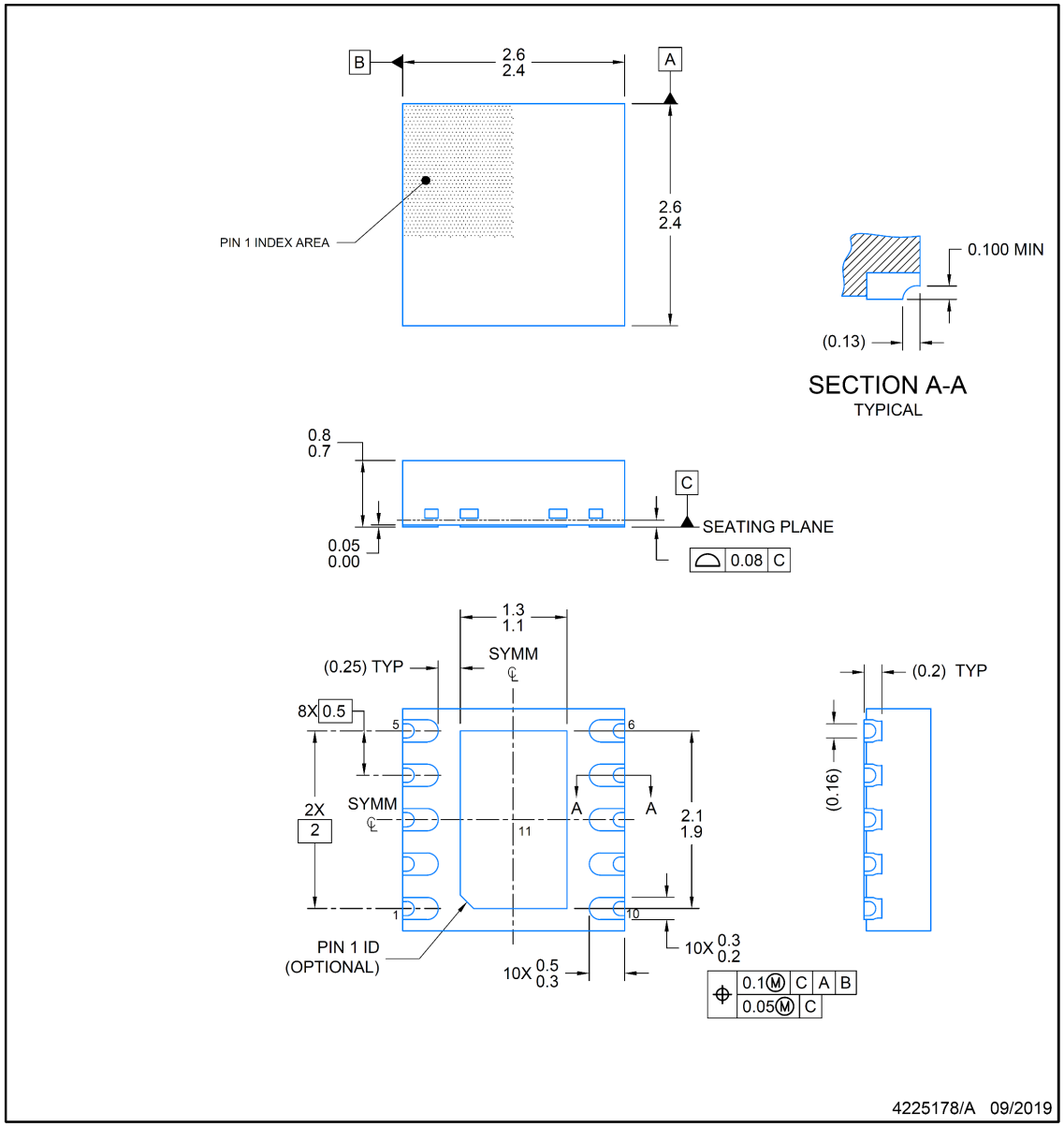
ADVANCE INFORMATION

PACKAGE OUTLINE

DSK0010C

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

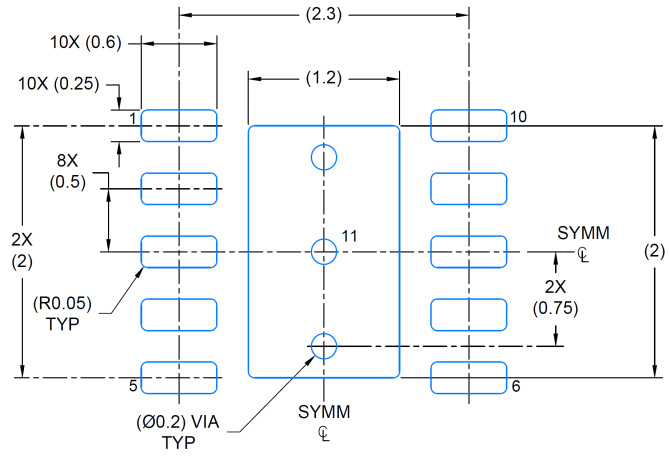
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

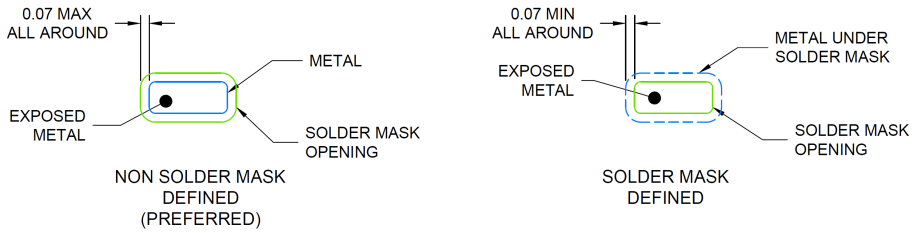
DSK0010C

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4225178/A 09/2019

NOTES: (continued)

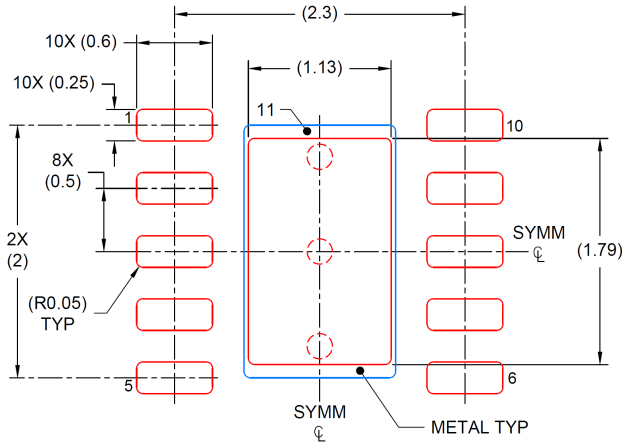
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSK0010C

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED COVERAGE BY AREA
SCALE: 20X

4225178/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PS37B010122DSKR	ACTIVE	SON	DSK	10	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples
PS37F010122DSKR	ACTIVE	SON	DSK	10	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

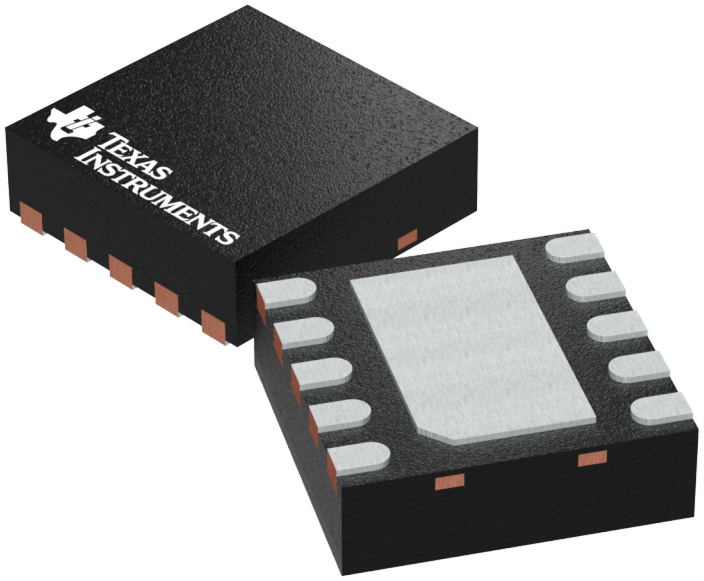
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DSK 10 WSON - 0.8 mm max height

2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265