TLV8xxE 低功耗 250nA I_Q 电源电压监控器

1 特性

- 当 VDD = 0.7V 至 6V 时，确保执行 $\overline{\text{RESET}}$ 输出
- 固定延时时间：40µs、10ms、50ms、100ms、200ms、400ms
- 电源电流 (IDD)：250nA（典型值）
  - 1µA（VDD = 3.3V 时的最大值）
- 输出拓扑：
  - TLV809E：推挽，低电平有效
  - TLV803E：开漏，低电平有效
  - TLV810E，推挽，高电平有效
- 欠压检测：
  - 高精度：±0.5%（典型值）
  - 标称电压监控器：3V、3.3V、5V
  - (V_{IT-})：1.7V、1.8V、1.9V、2.4V、2.64V、2.93V、3.08V、4.38V、4.63V
- 封装：
  - SOT23-3 (DBZ)（引脚 1 = GND）
  - SOT23-3 (DBZ)（引脚 1 = RESET）
  - SC-70 (DCK)
- 温度范围：-40°C 至 +125°C
- 与 MAX803/809/810、APX803/809/810 引脚对引脚兼容

2 应用

- 使用 DSP、微控制器或微处理器的 应用
- 电表
- 便携式、电池供电类设备
- 机顶盒和电视
- 楼宇自动化
- 笔记本电脑/台式机、服务器

3 说明

TLV803E、TLV809E 和 TLV810E 是 TLV803、TLV853、TLV809、LM809、TPS3809 和 TLV810 的增强替代品。TLV803E、TLV809E 和 TLV810E 为使用电池供电的 应用提供更低的电源电流，并具有更高精度、更宽的温度范围和更低的上电复位电压 (V_{POR})，可提高系统可靠性。

TLV80xE 和 TLV81xE 系列是具有低 I_Q（250nA 典型值、1µA 最大值）的电压监控电路（复位 IC），可监控 VDD 电压电平。每当电源电压 VDD 下降到出厂编程下降阈值电压 V_{IT-} 以下时，这些器件都会启动一个复位信号。当 VDD 电压高于上升阈值电压 (V_{IT+})（与下降阈值电压 (V_{IT-})）和迟滞电压 (V_{HYS}) 等效）时，复位输出会保持低电平以保持固定的复位延时时间 t_D。

这些器件具有集成的毛刺抑制功能，可忽略 VDD 引脚上的快速瞬变。这些电压监控器具有低电流消耗和高精度（±0.5% 典型值），因此非常适用于低功耗和便携式 应用。对于低至 V_{POR} = 0.7V 的电源电压，TLV80xE 和 TLV81xE 器件具有指定的输出逻辑状态。TLV80xE 和 TLV81xE 器件可采用业界通用的 3 引脚 SOT23 (DBZ) 封装和 3 引脚 SC70 (DCK) 封装。

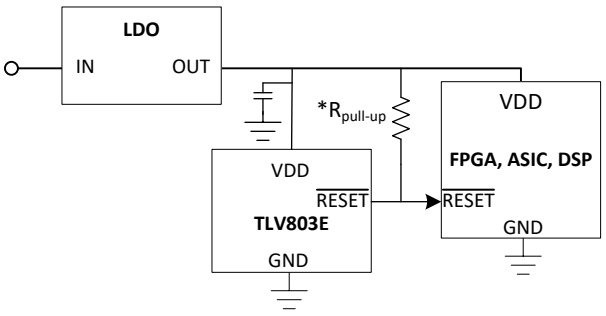
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV803E、TLV809E、TLV810E(2)	SOT-23 (3)	2.90mm × 1.30mm
	SC-70 (3)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 预发布封装

典型应用



*Pull-up resistor not required for TLV809E

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (November 2019) to Revision D — **Page**

- 已添加 添加了 TLV810E 特性、 说明和器件信息 ... 1
- Added device nomenclature figure ... 3
- Added RESET pin function for TLV810E ... 4
- Added TLV810E section to the Electrical Characteristics table as preview for APL release ... 6
- Added reset delay rows for delay variants B and C in the Timing Requirements table as preview for APL release ... 7
- 已添加 timing diagram for TLV810E ... 8
- 已添加 Figure 6, Figure 23, Figure 24 ... 9
- 已更改 block diagram and description to include TLV810E ... 14
- 已添加 typical application for TLV810E ... 19

Changes from Revision B (July 2019) to Revision C — **Page**

- 将器件状态从“预告信息”更改为“生产数据” ... 1

5 Device Comparison

Figure 1 shows the device naming nomenclature to compare the difference device variants. See 表 1 for a more detailed explanation.

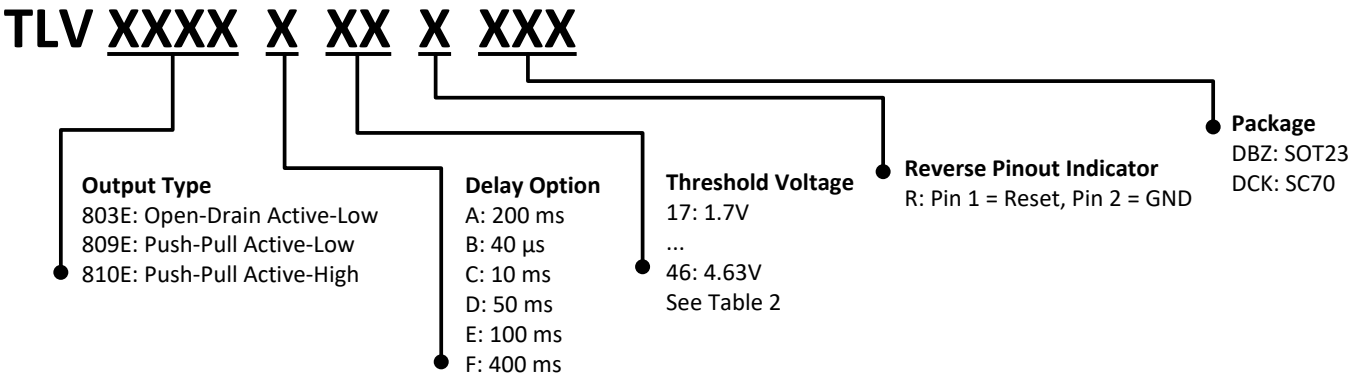
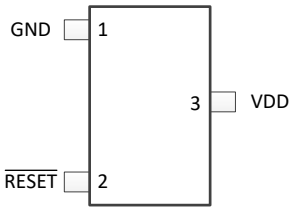


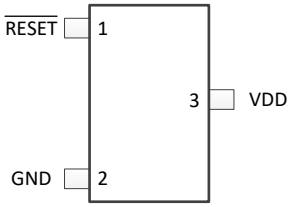
Figure 1. Device Naming Nomenclature

6 Pin Configuration and Functions

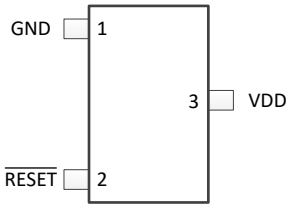
DBZ Package (Pin 1 = GND)
3-Pin SOT-23
Top View



DBZ Package (Pin 1 = RESET, reverse pinout)
3-Pin SOT-23
Top View



DCK Package
3-Pin SC-70
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DCK, DBZ	DBZ (Reverse Pinout)		
GND	1	2	—	Ground
$\overline{\text{RESET}}$	2	1	O	**Active low output reset signal:** This pin is driven low logic when VDD voltage falls below the negative voltage threshold (V_{IT-}). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period (t_D) after VDD voltage rise above V_{IT+}.
RESET	2	1	O	**Active High output reset signal (TLV810E only):** This pin is driven high logic when VDD voltage falls below the negative voltage threshold (V_{IT-}). RESET remains high (asserted) for the delay time period (t_D) after VDD voltage rise above V_{IT+}.
VDD	3	3	I	**Input supply voltage.** TLV80xE and TLV81xE monitors VDD voltage.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD pin	–0.3	6.5	V
	$\overline{\text{RESET}}$ (TLV809E), RESET(TLV810E)	–0.3	V_{DD} + 0.3 (2)	V
	$\overline{\text{RESET}}$ (TLV803E)	–0.3	6.5	V
Current	Output sink and source current	-20	20	mA
Temperature(3)	Operating ambient, T_A	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions (above the Recommended Operating Conditions) for extended periods may affect device reliability.
(2) The absolute maximum rating is (V_{DD} + 0.3) V or 6.5 V, whichever is smaller.
(3) As a result of the low dissipated power in this device, the junction temperature is assumed to be equal to the ambient temperature.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	1.7		6	V
$V_{\overline{\text{RESET}}}$, V_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin voltage	0		6	V
$I_{\overline{\text{RESET}}}$, I_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin current	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV8XXE		UNIT
		DCK (SC70-3)	DBZ (SOT23-3)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	300.5	254.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	178.2	150.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	166.5	140.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	70	48.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	165.2	139.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

over operating range (T_A = -40°C to 125°C), 1.7 V < V_{DD} < 6 V, R_{UP} = 10 kΩ to 6 V, 10 pF load at RESET pin, unless otherwise noted. Typical values are at 25°C, VDD = 3.3V and V_{IT-} = 2.93 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage		1.7		6	V
V_{IT-}	Input threshold voltage accuracy	T_A= -40 °C to125 °C	-2	0.5	2	%
V_{HYS}	Hysteresis voltage	Hysteresis from V_{IT-}	0.9	1.2	1.5	%
I_{DD}	Supply current into VDD pin	V_{DD}=3.3 V; V_{DD}>V_{IT+} (1)		0.25	1	µA
		V_{DD}=6 V		0.4	1.2	µA
TLV809E (Push-Pull Active-Low)						
V_{POR}	Power on reset voltage (2)	V_{OL}<= 300mV, $I_{OUT\ (Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} =1.7V, V_{DD} < V_{IT-}, $I_{OUT\ (Sink)}$ = 500 µA			300	mV
		V_{DD}= 3.3V, V_{DD} < V_{IT-}, $I_{OUT\ (Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	V_{DD} = 6V, V_{DD} > V_{IT+}, $I_{OUT\ (source)}$ = 4 mA	0.8V_{DD}			V
		V_{DD}= 3.3V, V_{DD} > V_{IT+}, $I_{OUT\ (source)}$ = 2 mA	0.8V_{DD}			V
TLV803E (Open-Drain Active-Low)						
V_{POR}	Power on reset voltage (2)	V_{OL} <= 300 mV, $I_{OUT\ (Sink)}$ = 15 uA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 1.7 V, V_{DD} < V_{IT-}, I_{OUT} = 500 µA			300	mV
		V_{DD} = 3.3 V, V_{DD} < V_{IT-}, I_{OUT} = 2 mA			300	mV
$I_{lkg(OD)}$	Open drain output leakage current	V_{DD} = V_{PULLUP} = 6 V, V_{DD} > V_{IT+}		100	350	nA
TLV810E (Push-Pull Active-High) (3)						
V_{OH}	High level output voltage	V_{DD}= 3.3V, V_{DD} < V_{IT-}, $I_{OUT\ (source)}$ = 2 mA	0.8V_{DD}			V
		V_{DD} = 1.7V, V_{DD} < V_{IT-}, $I_{OUT\ (source)}$ = 500 uA	0.8V_{DD}			V
V_{POR}	Power on Reset Voltage	V_{OH} >= 720 mV, $I_{OUT\ (Source)}$ = 15 uA			900	mV
V_{OL}	Low level output voltage	V_{DD} = 6V, V_{DD} > V_{IT+}, $I_{OUT\ (Sink)}$ = 2 mA			300	mV
		V_{DD}= 3.3V, V_{DD} > V_{IT+}, $I_{OUT\ (Sink)}$ = 500 µA			300	mV

(1) V_{IT+} = V_{IT-} + V_{HYS}
(2) Minimum VDD voltage for a controlled output state. Below V_{POR}, the output cannot be determined.
(3) Product Preview

7.6 Timing Requirements

over operating range (T_A = -40°C to 125°C), 1.7 V < V_{DD} < 6 V, Open-Drain-only: R_{UP} = 10 kΩ to 6 V (Open Drain only), 10 pF load at RESET pin, Overdrive = 10%, unless otherwise noted. Typical values are at 25°C, VDD = 3.3V and V_{IT-} = 2.93.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{GI}	Glitch immunity	5% Overdrive (1)		10		µs
t_{PD_HL}	Propagation delay from VDD falling below V_{IT-} to RESET	V_{DD} = (V_{IT+} + 30%) to (V_{IT-} - 10%)		30	50	µs
t_D	Release time or reset timeout period	Reset time delay variant A (2)	130	200	270	ms
		Reset time delay variant B (2) (3); R_{UP}=100 kΩ, C_L = 100 pF (4)		45	90	µs
		Reset time delay variant B (2) (3)		40	80	µs
		Reset time delay variant C (2) (3)	6.5	10	13.5	ms

(1) Overdrive = [(V_{DD}/ V_{IT-}) - 1] × 100%. Refer to Section 8.3.3 on VDD glitch immunity.
(2) Refer to device nomenclature table in Section 12.1.1. VDD: (V_{IT-}-10%) to (V_{IT+} + 10%)
(3) Product Preview
(4) Specified by design

7.7 Timing Diagram

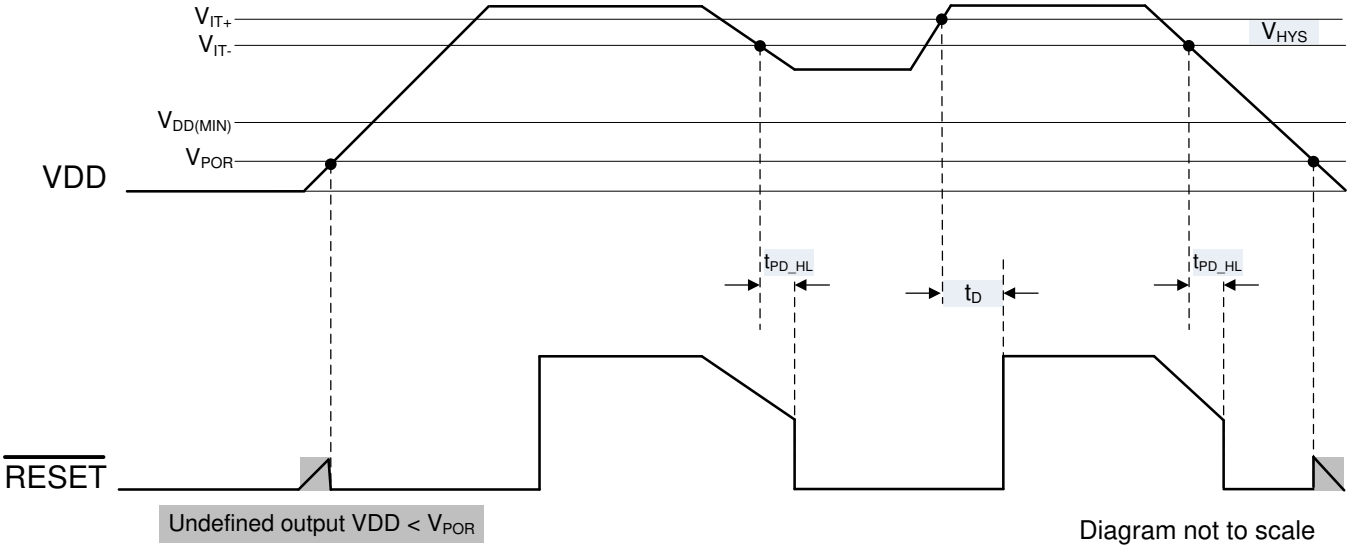


图 2. TLV803E, TLV809E Timing Diagram

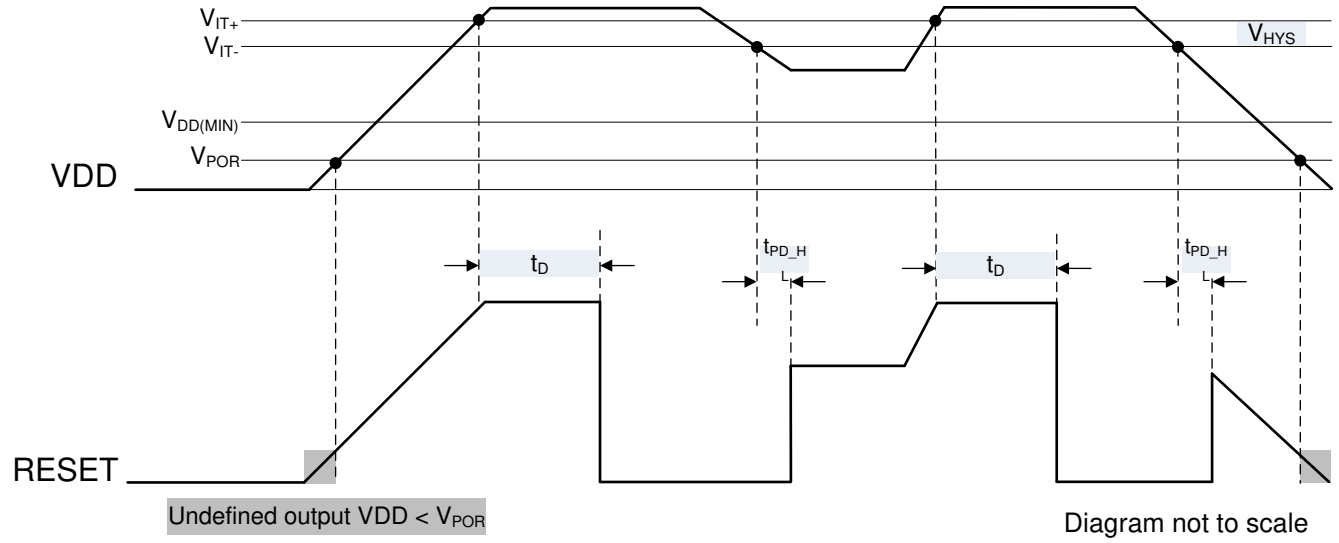


图 3. TLV810E Timing Diagram

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TLV803E and TLV809E devices. Test conditions are T_J = 25°C, VDD = 3.3 V, V_{IT-} = 2.93 V, $R_{pull-up}$ = 10 kΩ to 6 V, C_{Load} = 50 pF, unless otherwise noted.

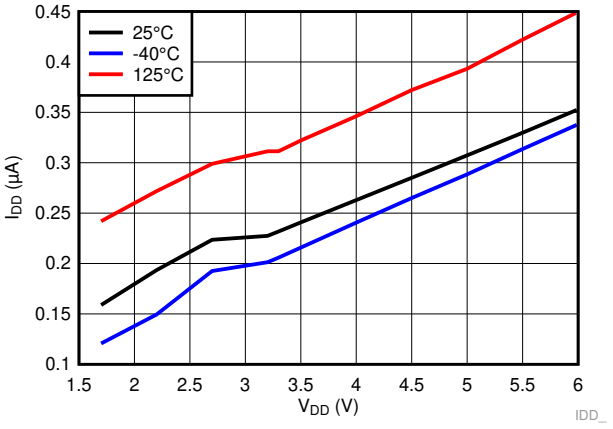


图 4. Supply Current Versus Supply Voltage for TLV803EA29

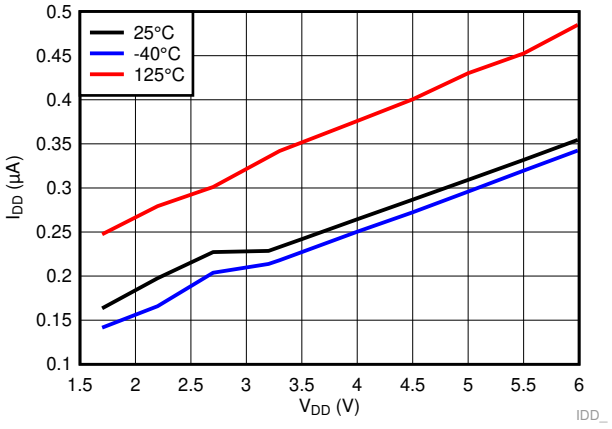


图 5. Supply Current Versus Supply Voltage for TLV809EA29

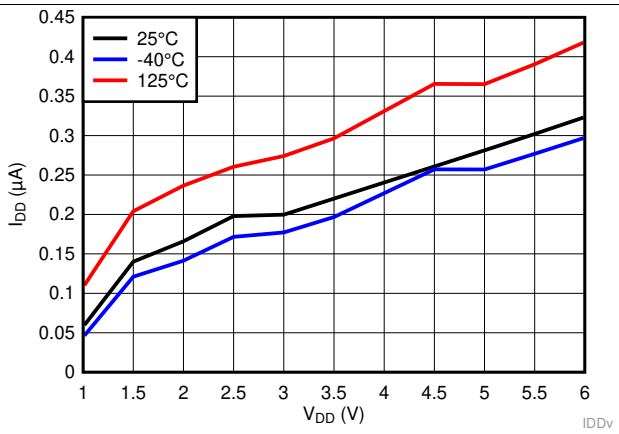


图 6. Supply Current Versus Supply Voltage for TLV810EA29

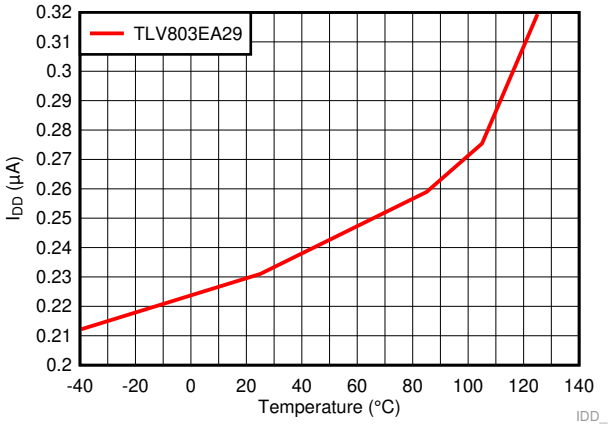


图 7. Supply Current Over Temperature for TLV803EA29, VDD = 3.3 V

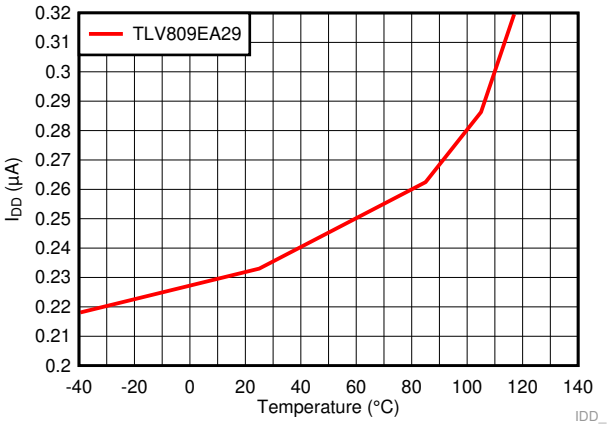


图 8. Supply Current Over Temperature for TLV809EA29, VDD = 3.3 V

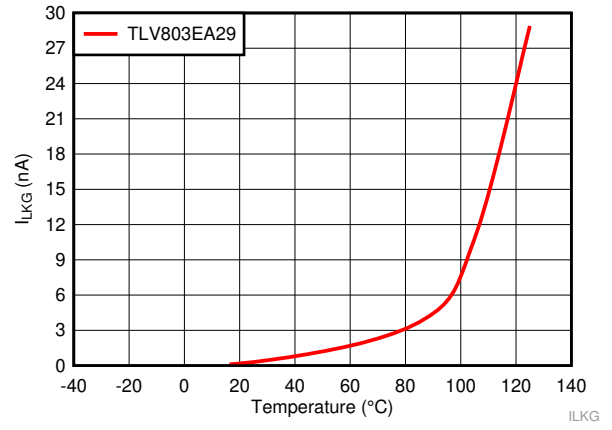


图 9. Leakage Current Over Temperature for TLV803EA29

Typical Characteristics (接下页)

Typical characteristics show the typical performance of the TLV803E and TLV809E devices. Test conditions are T_J = 25°C, VDD = 3.3 V, V_{IT-} = 2.93 V, $R_{pull-up}$ = 10 kΩ to 6 V, C_{Load} = 50 pF, unless otherwise noted.

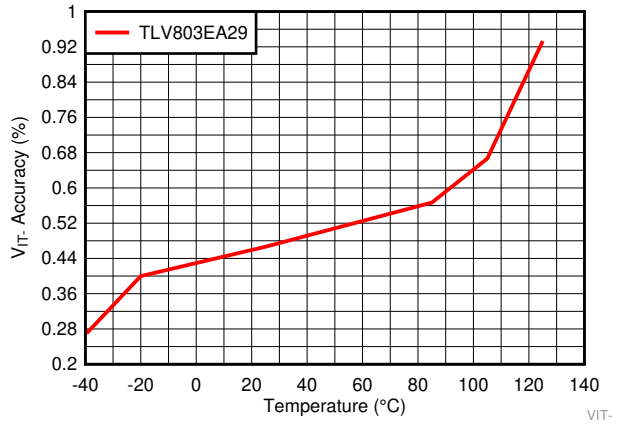


图 10. Voltage Threshold Accuracy Over Temperature for TLV803EA29

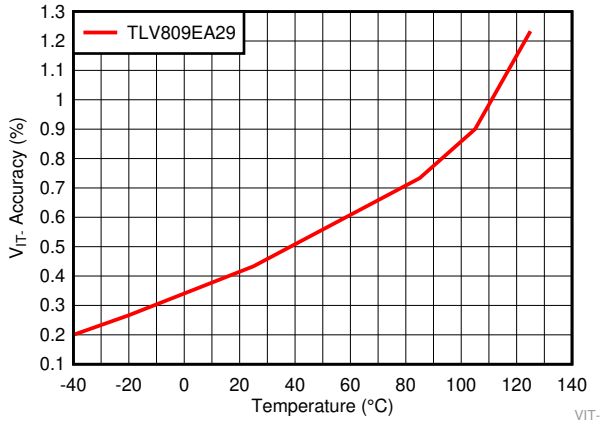


图 11. Voltage Threshold Accuracy Over Temperature for TLV809EA29

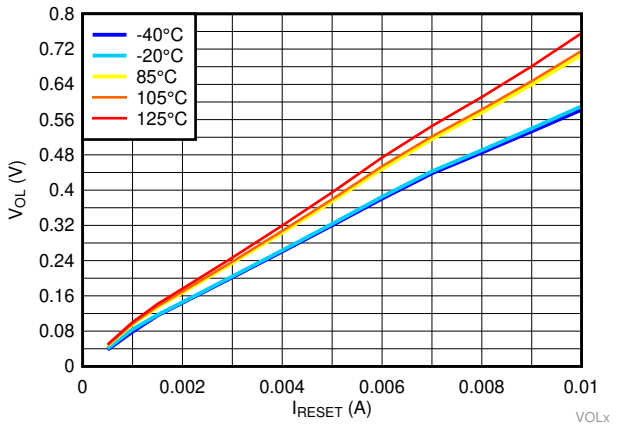


图 12. Low Voltage Output Versus Output Current for TLV803EA29, VDD = 1.7 V

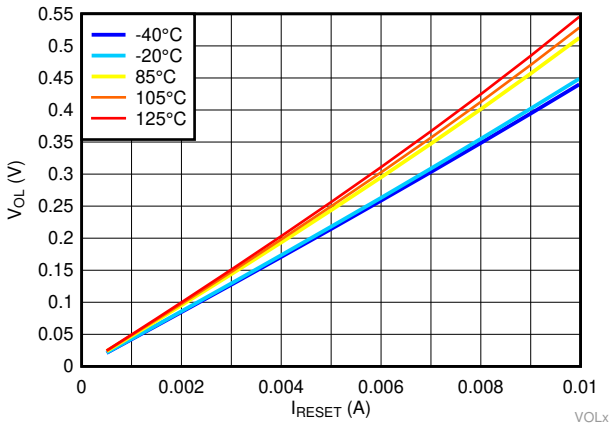


图 13. Low Voltage Output Versus Output Current for TLV809EA29, VDD = 1.7 V

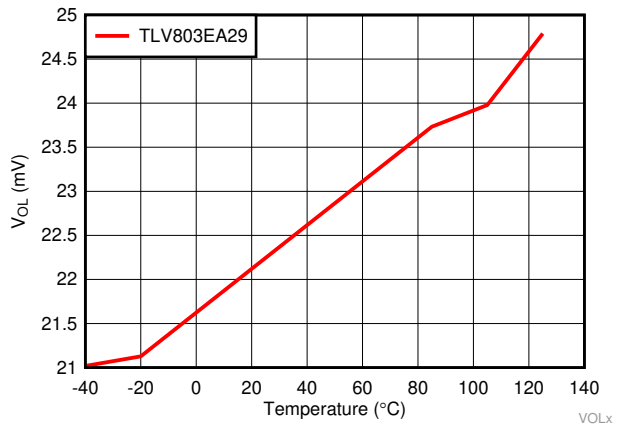


图 14. Low Voltage Output Over Temperature for TLV803EA29, VDD = 1.7 V

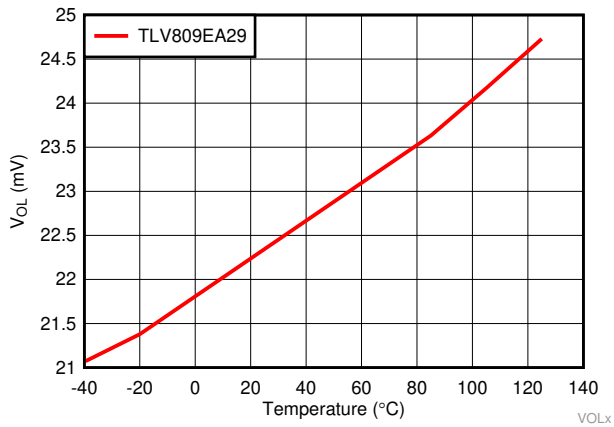


图 15. Low Voltage Output Over Temperature for TLV809EA29, VDD = 1.7 V

Typical Characteristics (接下页)

Typical characteristics show the typical performance of the TLV803E and TLV809E devices. Test conditions are T_J = 25°C, VDD = 3.3 V, V_{IT-} = 2.93 V, $R_{pull-up}$ = 10 kΩ to 6 V, C_{Load} = 50 pF, unless otherwise noted.

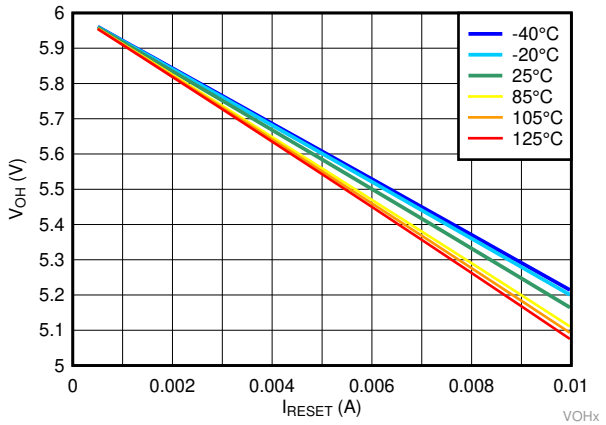


图 16. High Voltage Output Versus Output Current for TLV809EA29, VDD = 6 V

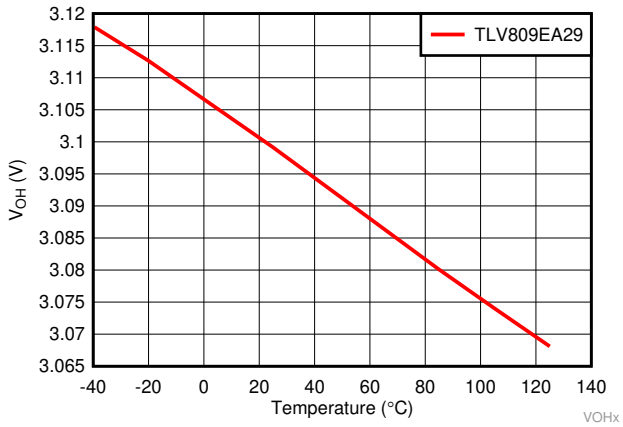


图 17. High Voltage Output Over Temperature for TLV809EA29, VDD = 3.3 V

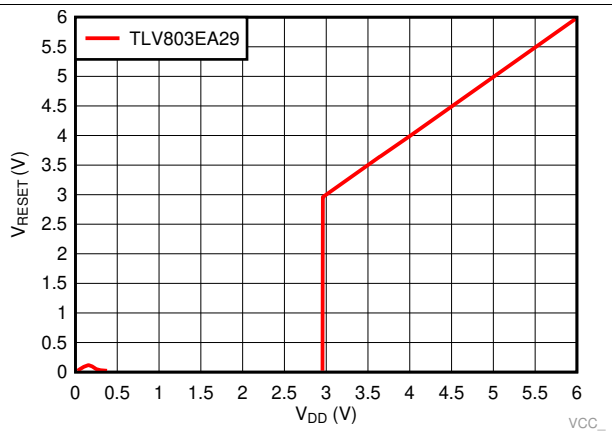


图 18. Reset Voltage Output Versus Voltage Input for TLV803EA29, $V_{pull-up}$ = VDD, $R_{pull-up}$ = 10 kΩ

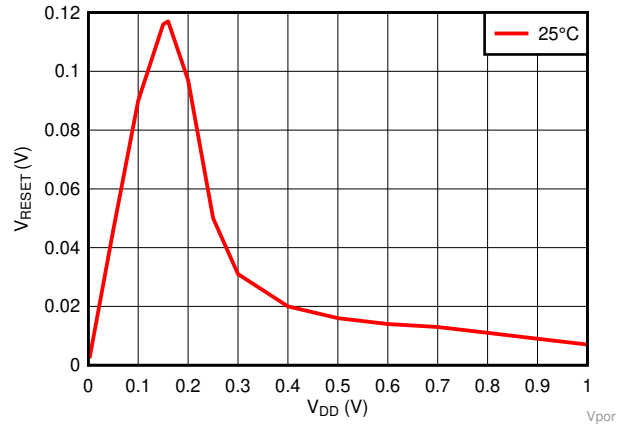


图 19. Reset Voltage Output Versus Voltage Input for TLV803EA29, $R_{pull-up}$ = 10 kΩ

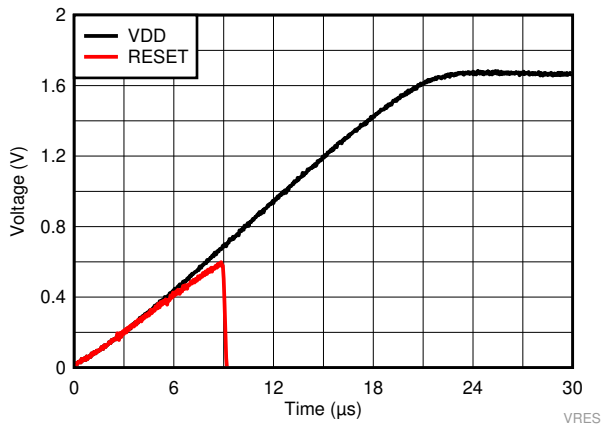


图 20. Transient Power-on-Reset Voltage for TLV809EA30, I_{RESET} = 15 µA

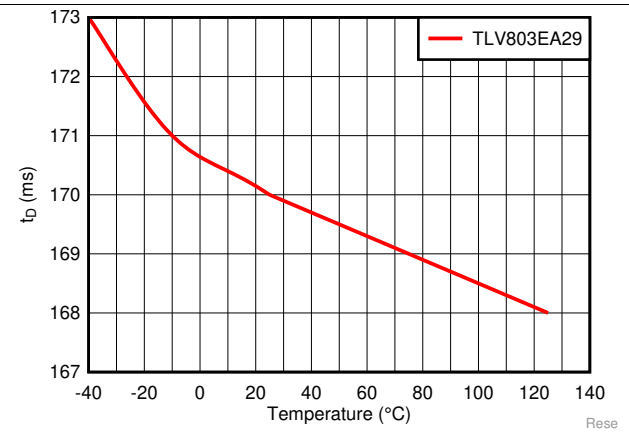


图 21. Reset Delay Time Over Temperature for TLV803EA29

Typical Characteristics (接下页)

Typical characteristics show the typical performance of the TLV803E and TLV809E devices. Test conditions are T_J = 25°C, VDD = 3.3 V, V_{IT-} = 2.93 V, $R_{pull-up}$ = 10 kΩ to 6 V, C_{Load} = 50 pF, unless otherwise noted.

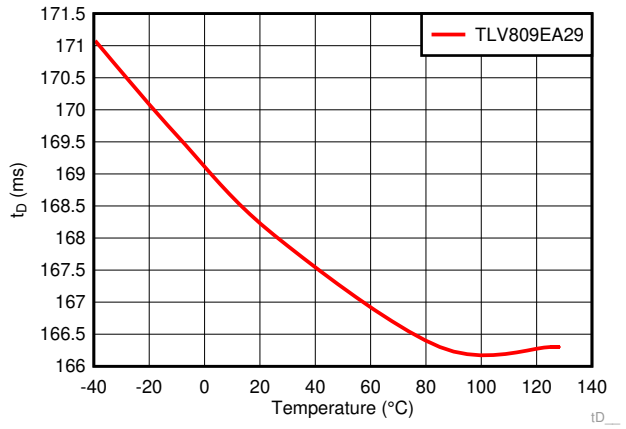


图 22. Reset Delay Time Over Temperature for TLV809EA29

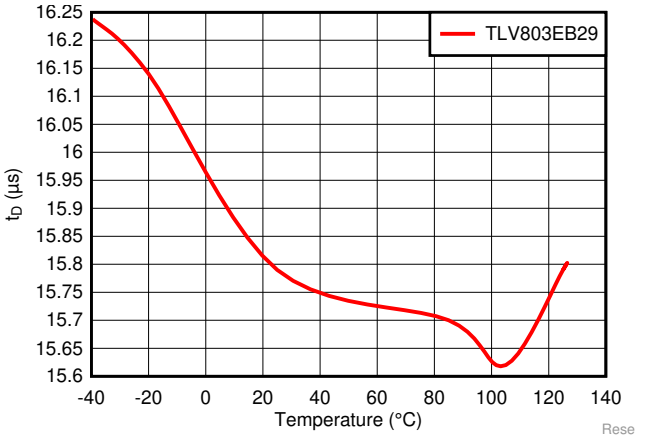


图 23. Reset Delay Time Over Temperature for TLV803EB29

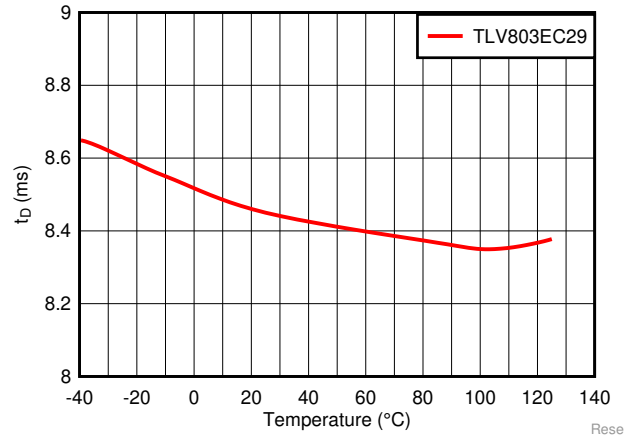


图 24. Reset Delay Time Over Temperature for TLV803EC29

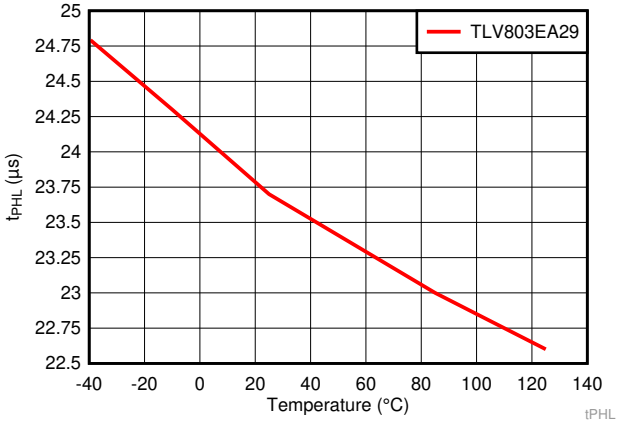


图 25. High-to-Low Propagation Delay Over Temperature for TLV803EA29

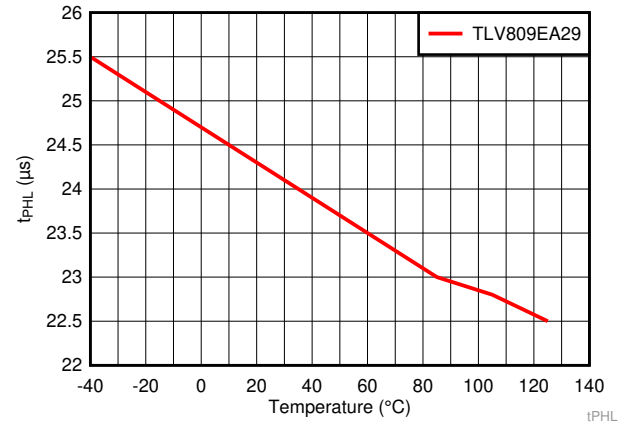


图 26. High-to-Low Propagation Delay Over Temperature for TLV809EA29

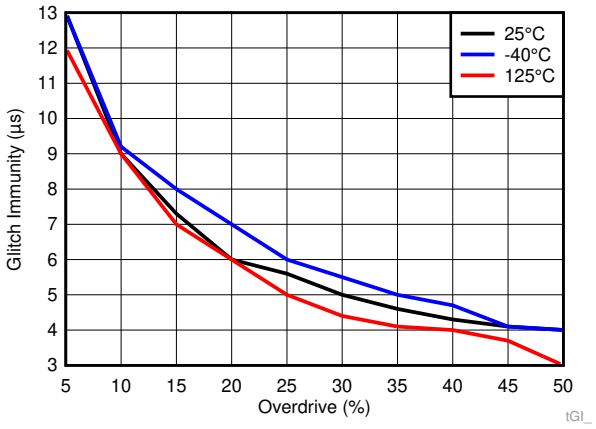


图 27. Glitch Immunity Versus Overdrive for TLV803EA29

Typical Characteristics (接下页)

Typical characteristics show the typical performance of the TLV803E and TLV809E devices. Test conditions are T_J = 25°C, VDD = 3.3 V, V_{IT-} = 2.93 V, $R_{pull-up}$ = 10 kΩ to 6 V, C_{Load} = 50 pF, unless otherwise noted.

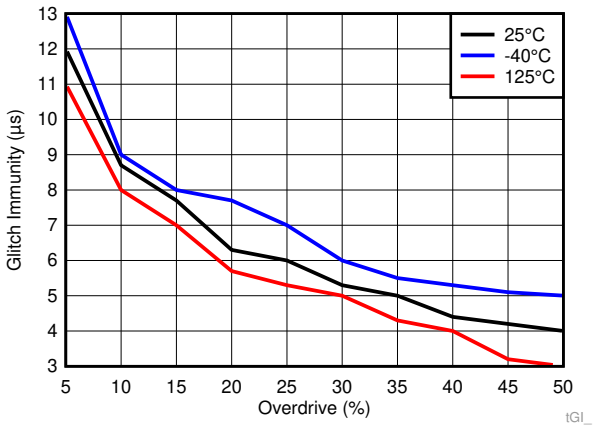


图 28. Glitch Immunity Versus Overdrive for TLV809EA29

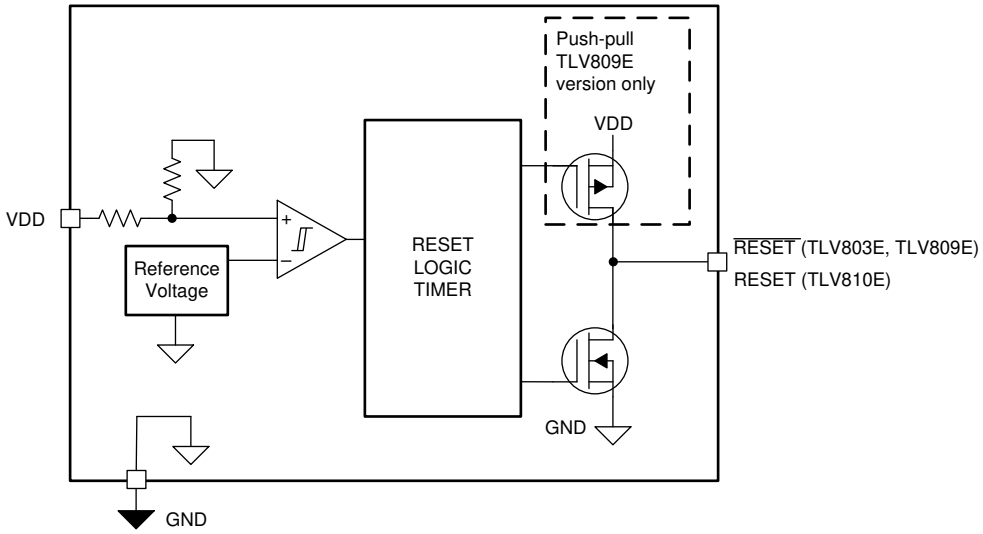
8 Detailed Description

8.1 Overview

The TLV8xxE is a family of easy to implement low power voltage supervisors (Reset ICs) with fixed threshold voltage and fixed reset delay. The TLV803E has open-drain active low output topology which requires a pull-up resistor, TLV809E has push-pull active low output topology and TLV810E has push-pull active high output topology. This family of devices features include integrated resistor divider threshold with hysteresis and a glitch immunity filter.

TLV8xxE is available in SOT-23 (3) and SC70 (3) industry standard package and pinout.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator with integrated reference to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the following:

- Internal bandgap (reference voltage)
- Internal regulator
- State machine
- Buffers
- Other control logic blocks

Good design practice involves placing a 0.1-µF to 1-µF bypass capacitor at VDD input for noisy applications and to ensure enough charge is available for the device to power up correctly. The reset output is undefined when VDD is below V_{POR}.

8.3.2 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below the falling voltage threshold $V_{IT–}$, the output reset is asserted. When the voltage at the VDD pin rises above the rising voltage threshold (V_{IT+}) equivalent to $V_{IT–}$ plus hysteresis (V_{HYS}), the output reset is deasserted after T_D time delay.

8.3.3 VDD Glitch Immunity

These devices are immune to quick voltage transient or excursion on VDD. Sensitivity to transients depends on both transient duration and transient overdrive. Overdrive is defined by how much VDD exceeds the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 1.

Feature Description (接下页)

Overdrive = | (VDD / V_{IT-} – 1) × 100% |

where

- V_{IT-} is the threshold voltage
- VDD is the input voltage crossing V_{IT-}

(1)

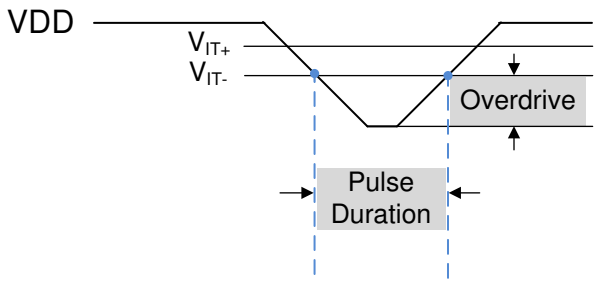


图 29. Overdrive Versus Pulse Duration

TLV80xE and TLV81xE devices have built-in glitch immunity (t_{GI}) of 10 µs typical as shown in *Timing Requirements*. 图 30 shows that VDD must fall below V_{IT-} for t_{GI}, otherwise the faling transistion is ignored. When VDD falls below V_{IT-} for t_{GI}, $\overline{\text{RESET}}$ transitions low to indicate a fault condition after the propagation delay high-to-low (t_{PDHL}). When VDD rises above V_{IT+}, $\overline{\text{RESET}}$ only deasserts to logic high indicating there is no more fault condition only if VDD remains above V_{IT+} for longer than the reset delay (t_D).

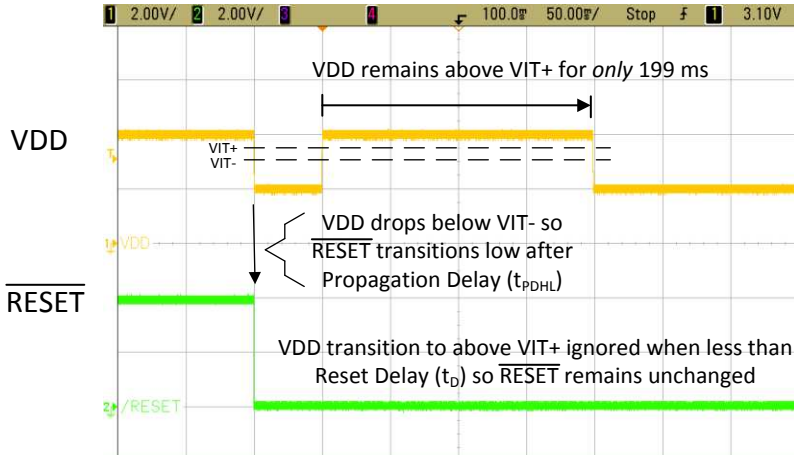


图 30. Glitch Immunity when VDD Rises Above V_{IT+} for Less than $\overline{\text{RESET}}$ Delay (TLV803EA29)

8.3.4 Output Logic

8.3.4.1 $\overline{\text{RESET}}$ Output, Active Low

$\overline{\text{RESET}}$ remains high (deasserted) as long as VDD is above the negative threshold (V_{IT-}). If VDD falls below the negative threshold (V_{IT-}), then reset is asserted and $\overline{\text{RESET}}$ goes to low impedance pulling output low V_{OL}.

When VDD rises above V_{IT+}, the delay circuit holds $\overline{\text{RESET}}$ low for the specified reset delay period (t_D). When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes back to high impedance and output goes high voltage (V_{OH}).

The open-drain version requires a pull-up resistor to hold the $\overline{\text{RESET}}$ pin high. Connect the pull-up resistor to the desired interface voltage logic. $\overline{\text{RESET}}$ can be pulled up to any voltage up to maximum voltage independent of the VDD voltage. To ensure proper voltage levels, take care when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$).

The push-pull variant does not require a pull-up resistor.

Feature Description (接下页)

8.3.4.2 RESET Output, Active High

RESET remains low (de-asserted) as long as VDD is above the positive threshold (V_{IT+}). If VDD falls below the negative threshold (V_{IT-}), then reset is asserted and RESET goes to logic high V_{OH}.

When VDD rise above V_{IT+}, the delay circuit holds RESET high for the specified reset delay period (t_D). When the reset delay has elapsed the RESET pin goes back to low logic and output goes to low voltage (V_{OL}).

The push-pull variant does not require a pull-up resistor.

8.4 Device Functional Modes

summarizes the various functional modes of the device.

V_{DD}	RESET (Active High)	$\overline{\text{RESET}}$(Active Low)
$V_{DD} < V_{POR}$	Undefined	Undefined
$V_{POR} < V_{DD} < V_{IT-}$	H	L
$V_{DD} \geq V_{IT-}$	L	H

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} voltage is greater than $V_{DD(min)}$, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-}).

8.4.2 V_{DD} Between VPOR and $V_{DD(min)}$

When the voltage on V_{DD} is less than the $V_{DD(min)}$ voltage and greater than the power-on-reset voltage (V_{POR}), the reset signal is asserted.

8.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than V_{POR}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV80xE and TLV81xE devices are used for voltage monitoring. These devices have only three pins: VDD, GND, and $\overline{\text{RESET}}$ (or RESET for TLV810E). There are at the most two external components: a capacitor on the VDD pin and a pull-up resistor on the $\overline{\text{RESET}}$ to VDD or another pull-up voltage for the open-drain variants. The design involves choosing the device with the desired voltage threshold and output topology and adding these components, if needed, as explained in the following sections.

9.2 Typical Application

A typical application for TLV80xE and TLV81xE devices is voltage rail monitoring. This rail can be the input power supply or the output of an LDO or DC/DC converter. 图 31 shows the TLV803EA29 monitoring the supply rail for a DSP, FPGA, or ASIC. This rail is at 3.3 V and generated by an LDO with an input power supply of 5 V. The supervisor is needed to make sure that the supply to the MCU/ASIC/FPGA/DSP is above a certain voltage threshold. If the supply voltage drops below a certain threshold, supervisor generates a reset output to indicate to the MCU that the supply is going down so that the MCU can take actions to save register data before supply enters brown-out conditions.

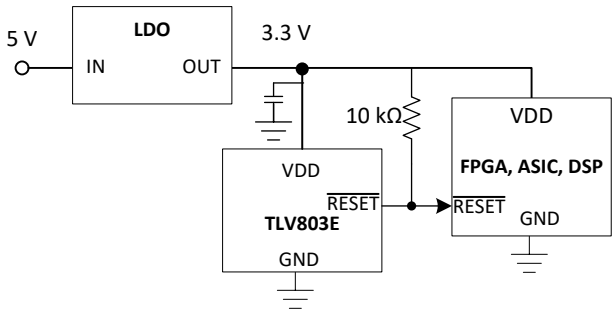


图 31. The Output of LDO Powering the MCU is Monitored by the TLV803EA29

9.2.1 Design Requirements

This design monitors a 3.3-V rail and flags an undervoltage fault at the $\overline{\text{RESET}}$ output when supply rail falls approximately 12% below the nominal rail voltage. The TLV803E device has an open-drain output topology so a pull-up resistor is required and chosen such that the $\overline{\text{RESET}}$ current (I_{RESET}) spec of ±5 mA is not violated. Pull-up resistors between 10 kΩ and 1 MΩ are recommended. If you are using the TLV809E device variant, no pull-up resistor is required because TLV809E has push-pull output topology.

9.2.2 Detailed Design Procedure

Select the TLV803EA29DBZR to satisfy the voltage threshold requirement for 3.3-V rail monitoring. As mentioned in 表 1, the TLV803EA29DBZR triggers an undervoltage fault at the $\overline{\text{RESET}}$ output when VDD falls below V_{IT-} which is 2.93 V for this device variant. Place a pull-up resistor on $\overline{\text{RESET}}$ to VDD to satisfy the output logic requirement while not violating the I_{RESET} recommended limit.

Typical Application (接下页)

9.2.3 Application Curves

图 32 and 图 33 show the TLV803EA29 functionality. In 图 32, the VDD supply voltage drops from 30% above V_{IT-} = 3.8 V to 10% below V_{IT-} = 2.6 V with a 0.1-µF capacitor on VDD. The RESET output is connected to VDD through the pull-up resistor so when the VDD supply voltage drops. The RESET output discharges down to the VDD supply voltage through the pull-up resistor and RESET pin capacitance. Once the high-to-low propagation delay t_{PD_HL} expires, the internal MOSFET turns on and asserts RESET to logic low. Note that t_{PD_HL} varies with VDD specifically on how much VDD drops and how quickly in addition to the VDD and RESET pin capacitances. In 图 33, VDD rises from 2 V to 4 V and the RESET output deasserts to logic high after the reset delay time (t_D) expires.

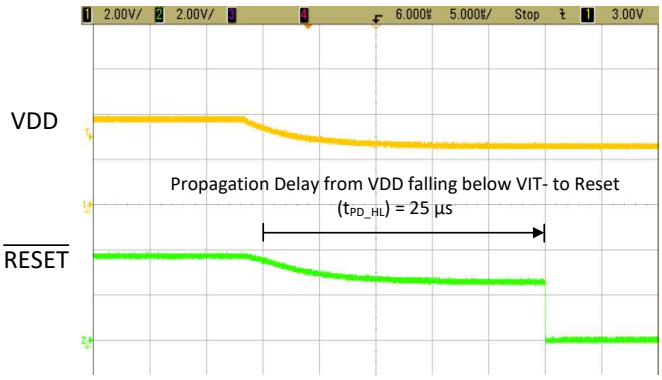


图 32. Propagation Delay when Fault Occurs after VDD Falls Below V_{IT-} (TLV803EA29 No Load) (1) (2)

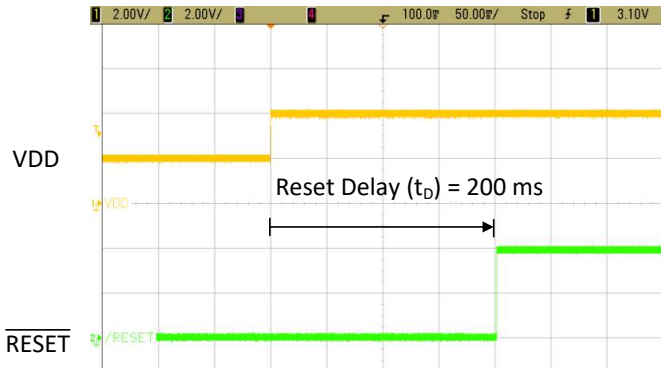


图 33. RESET Delay when Returning from Fault after VDD Rises Above V_{IT+} (TLV803EA29)

1. Typical t_{PD_HL}= 30 µs for VDD falling from (V_{IT+} + 30%) to (V_{IT-} - 10%).
2. VDD does not fall all the way to 0 V so RESET momentarily discharges to VDD until t_{PD_HL} expires.

9.3 Typical Application

A typical use case for the push-pull active high device variant TLV810E is overvoltage monitoring. The TLV810E can monitor a power supply, a MCU power rail, or a battery during charging for example. The VDD pin monitors the voltage rail and once VDD rises above VIT+, the RESET output deactivates to logic low after the reset delay time t_D. If VDD falls below V_{IT-}, the RESET output activates to logic high after the propagation delay (t_{PD_HL}). The voiltage thresholds and the reset delay time depends on the device variant. See Device Comparison for device variant naming nomenclature.

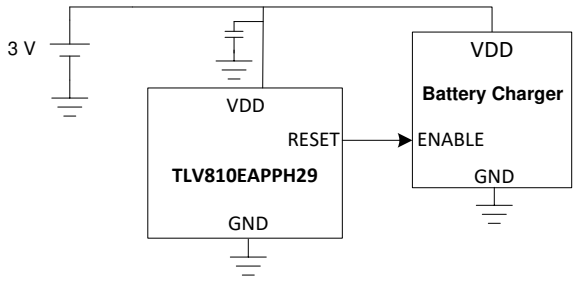


图 34. TLV810E Overvoltage Monitor Circuit for Battery Charger

9.3.1 Design Requirements

In this application design, the TLV810E device is monitoring a 3 V battery connected to a battery charger. The battery charger turns on when the battery voltage is below 2.9 V and turns off once the battery charges to 2.93 V and remains at 2.93 V for at least 200 ms. The design must be low power and not consume more than 500 nA typical.

9.3.2 Detailed Design Procedure

Select the TLV810EAPPH29 to accomplish this design. The TLV810EAPPH29 is a push-pull active high device with a V_{IT-} = 2.9 V and V_{IT+} = 2.9 + 1.2% = 2.93 V. Because the device is a push-pull output and the device threshold meets the design requirements, no external resistors are needed. The TLV810EAPPH29 device variant comes with 200 ms reset delay time meaning VDD must be above V_{IT+} for at least 200 ms for the RESET output to transistion to logic low to turn off the battery charger. This device meets the low power requirement because the TLV810E only consumes 250 nA typical.

10 Power Supply Recommendations

These devices are designed to operate from an input supply range of 1.7 V to 6 V. An input supply capacitor is recommended between the VDD pin and GND pin. If the voltage supply that provides power to VDD is susceptible to any large voltage transient that can exceed VDD maximum, the user must take additional precautions.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1-µF ceramic capacitor as close to the VDD pin as possible. A pull-up resistor is required for the open-drain output. Place the pull-up resistor on the $\overline{\text{RESET}}$ pin as close to the pin as possible.

11.2 Layout Example

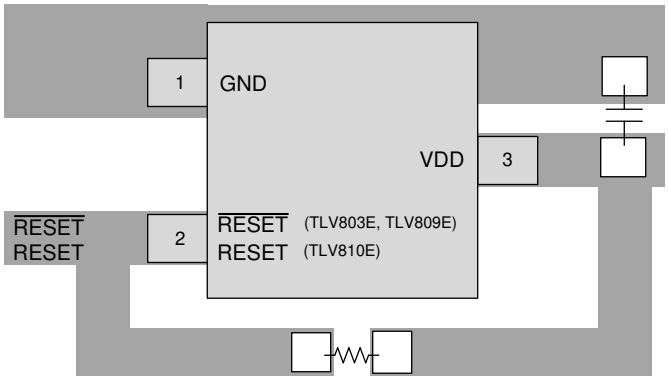


图 35. TLV803E, TLV809E, and TLV810E Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

表 1 显示了如何根据器件型号来解译器件的功能。例如：TLV803EA29DBZR 是一种开漏、低电平有效、200ms 复位延迟、2.93V 阈值电压、引脚 1 = GND、SOT23-3 引脚封装，并具有大卷带选项。

表 1 显示了 TLV80xE 和 TLV81xE 所有可能的型号。如需了解可订购选件，请参阅可订购器件信息表。如需了解可订购器件信息表以外器件的详细信息和供货情况，请联系德州仪器 (TI)。

表 1. 器件命名约定

说明	命名规则	值
器件型号	TLV803E	开漏，低电平有效
	TLV809E	推挽，低电平有效
	TLV810E	推挽，高电平有效
复位延时时间选项	A	200ms
	B	40us
	C	10ms
	D	50ms
	E	100ms
	F	400ms
阈值电压选项	17	1.7V
	18	1.8V
	19	1.9V
	24	2.4V
	26	2.64V
	29	2.93V
	30	3.08V
	43	4.38V
	46	4.63V
反向引脚指示器	R	引脚 1 = RESET、引脚 2 = GND
封装选项	DBZ	SOT23-3 引脚
	DCK	SC70-3 引脚
卷带	R	大卷带

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《TLV803EA29EVM 用户指南》*
- 德州仪器 (TI)，*《电压监控器（复位 IC）：常见问题解答 (FAQ)》*

12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV803E	单击此处	单击此处	单击此处	单击此处	单击此处
TLV809E	单击此处	单击此处	单击此处	单击此处	单击此处
TLV810E	单击此处	单击此处	单击此处	单击此处	单击此处

12.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV803EA17DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IT	Samples
TLV803EA18DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IV	Samples
TLV803EA22DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	322A	Samples
TLV803EA24DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	34A	Samples
TLV803EA26DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	326A	Samples
TLV803EA26DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	32A	Samples
TLV803EA26DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IW	Samples
TLV803EA26RDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	36AR	Samples
TLV803EA29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	329A	Samples
TLV803EA29DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	39A	Samples
TLV803EA29DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IX	Samples
TLV803EA29RDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	39AR	Samples
TLV803EA30DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	30A	Samples
TLV803EA42RDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DAR	Samples
TLV803EA43DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	343A	Samples
TLV803EA43RDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	34AR	Samples
TLV803EA43VDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	34AV	Samples
TLV803EB26RDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	36BR	Samples
TLV803EB29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	329B	Samples
TLV803EB33VDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3CBV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV803EB42VDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DBV	Samples
TLV803EB46DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	36B	Samples
TLV803EC29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	329C	Samples
TLV803EC30DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	330C	Samples
TLV803EC43DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	343C	Samples
TLV803ED17DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IS	Samples
TLV803ED18DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IU	Samples
TLV803ED29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	329D	Samples
TLV803EF26DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	326F	Samples
TLV803EF29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	329F	Samples
TLV809EA22DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	922A	Samples
TLV809EA26DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	926A	Samples
TLV809EA26DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IZ	Samples
TLV809EA29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	929A	Samples
TLV809EA29DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	99A	Samples
TLV809EA29DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	J1	Samples
TLV809EA30DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	930A	Samples
TLV809EA43DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	943A	Samples
TLV809EA45DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	945A	Samples
TLV809EA46DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	946A	Samples
TLV809EA46DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	J2	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV809EC26DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	926C	Samples
TLV809EC46DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	946C	Samples
TLV809ED29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	929D	Samples
TLV809EF30DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	930F	Samples
TLV810EA29DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	029A	Samples
TLV810EA29DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	J3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

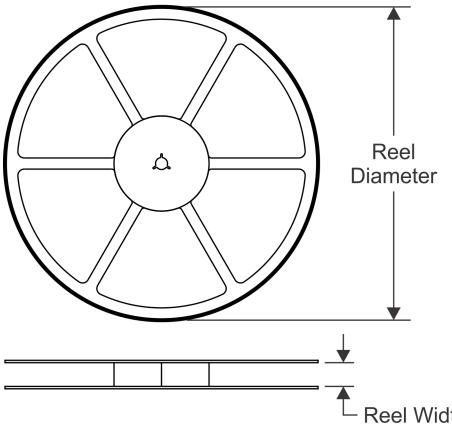
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

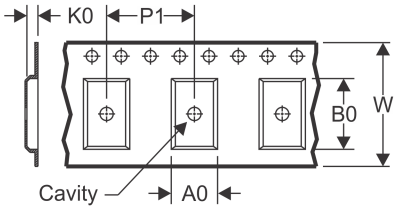
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

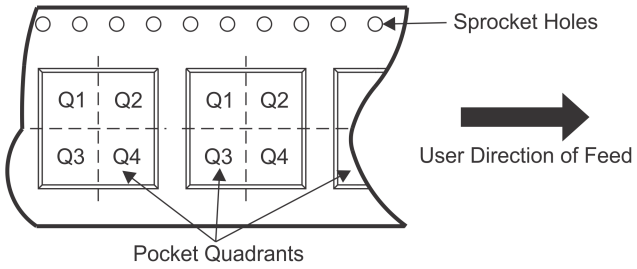


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

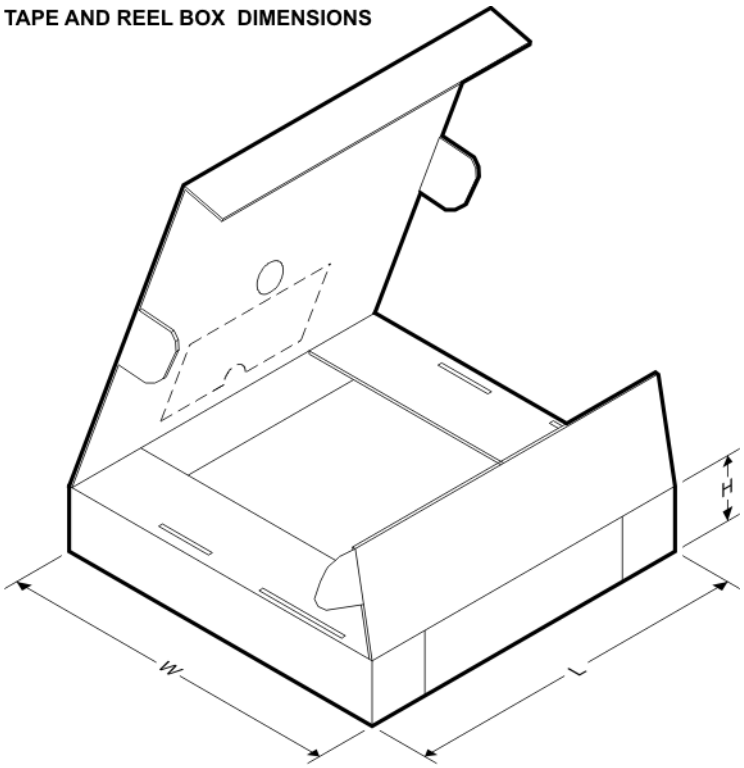


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV803EA17DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV803EA18DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV803EA22DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA24DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV803EA26DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA26DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV803EA26DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV803EA26RDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA29DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV803EA29DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV803EA29RDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA30DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV803EA42RDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA43DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA43RDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EA43VDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EB26RDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV803EB29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EB33VDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EB42VDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EB46DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV803EC29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EC30DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EC43DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803ED17DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV803ED18DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV803ED29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EF26DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803EF29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA22DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA26DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA26DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV809EA29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA29DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV809EA29DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV809EA30DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA43DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA45DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA46DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EA46DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV809EC26DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EC46DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809ED29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV809EF30DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV810EA29DBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV810EA29DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

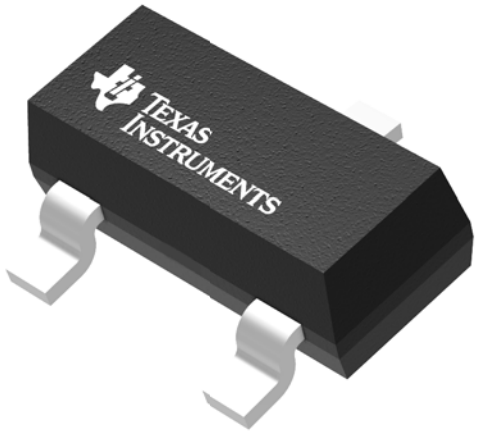
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV803EA17DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV803EA18DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV803EA22DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA24DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TLV803EA26DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA26DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TLV803EA26DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV803EA26RDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA29DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TLV803EA29DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV803EA29RDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA30DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TLV803EA42RDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA43DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA43RDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EA43VDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EB26RDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EB29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EB33VDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV803EB42VDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EB46DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TLV803EC29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EC30DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EC43DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803ED17DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV803ED18DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV803ED29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EF26DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803EF29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA22DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA26DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA26DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV809EA29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA29DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TLV809EA29DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV809EA30DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA43DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA45DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA46DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EA46DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV809EC26DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EC46DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809ED29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV809EF30DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV810EA29DBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV810EA29DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



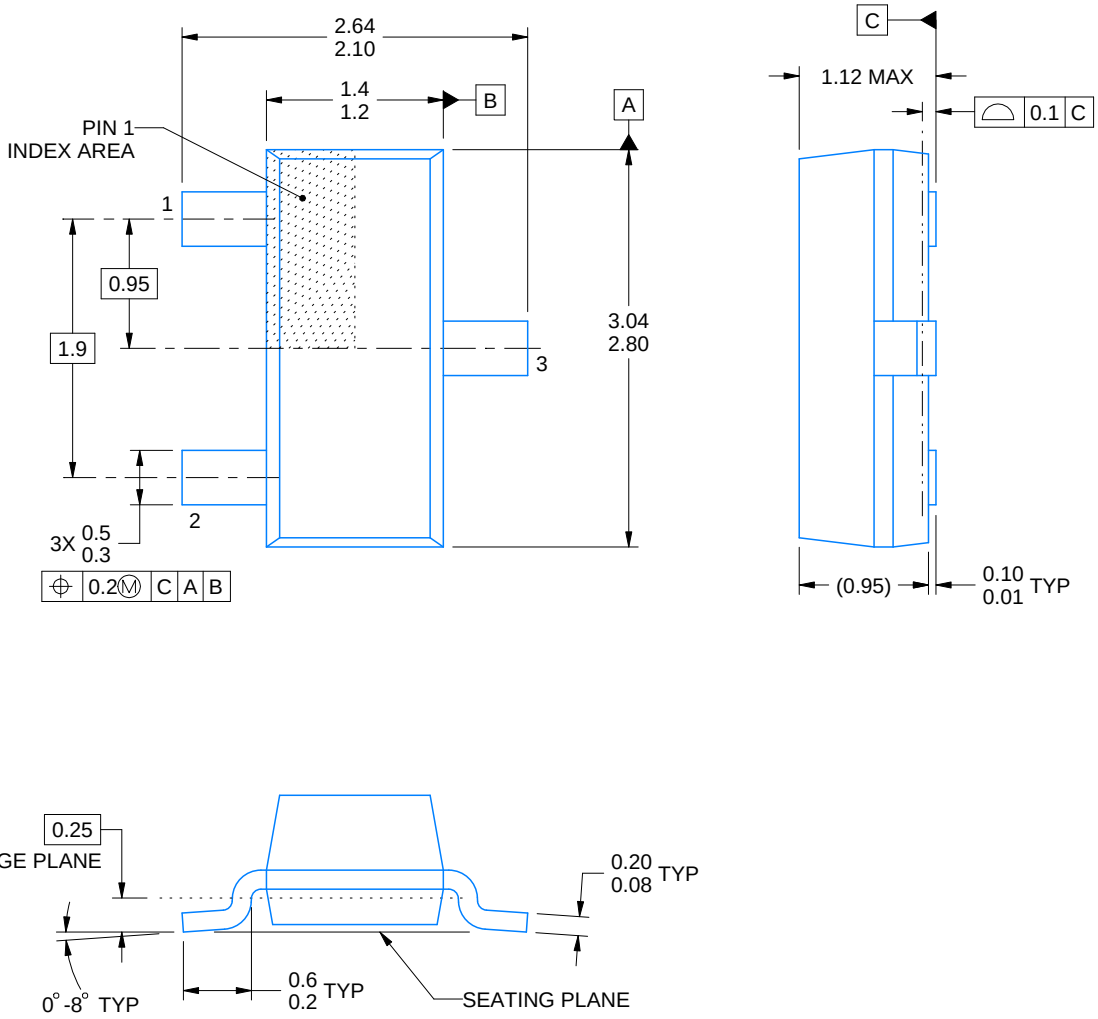
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

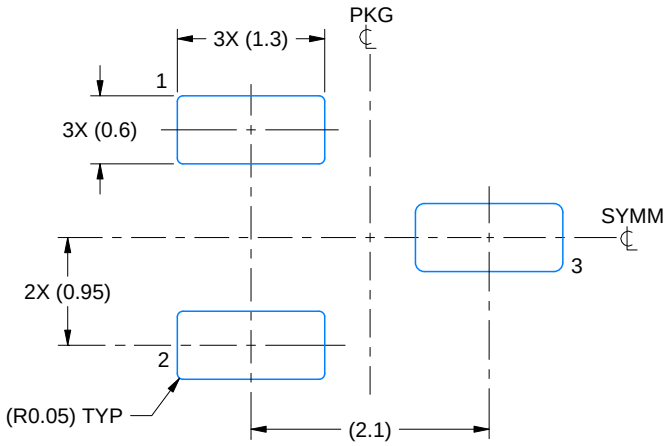
SMALL OUTLINE TRANSISTOR



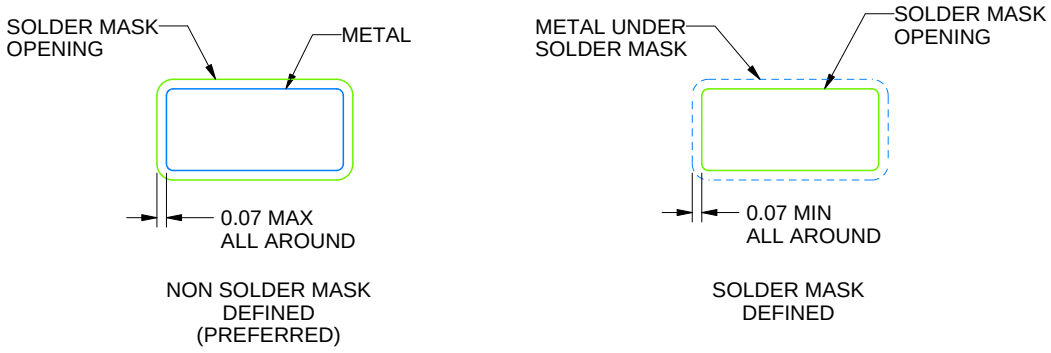
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

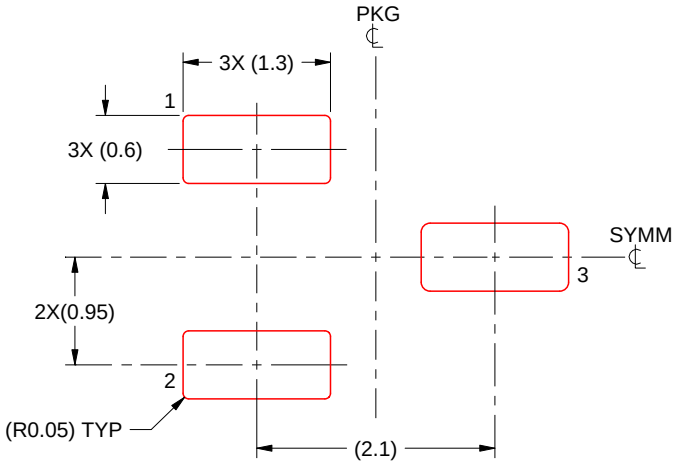


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

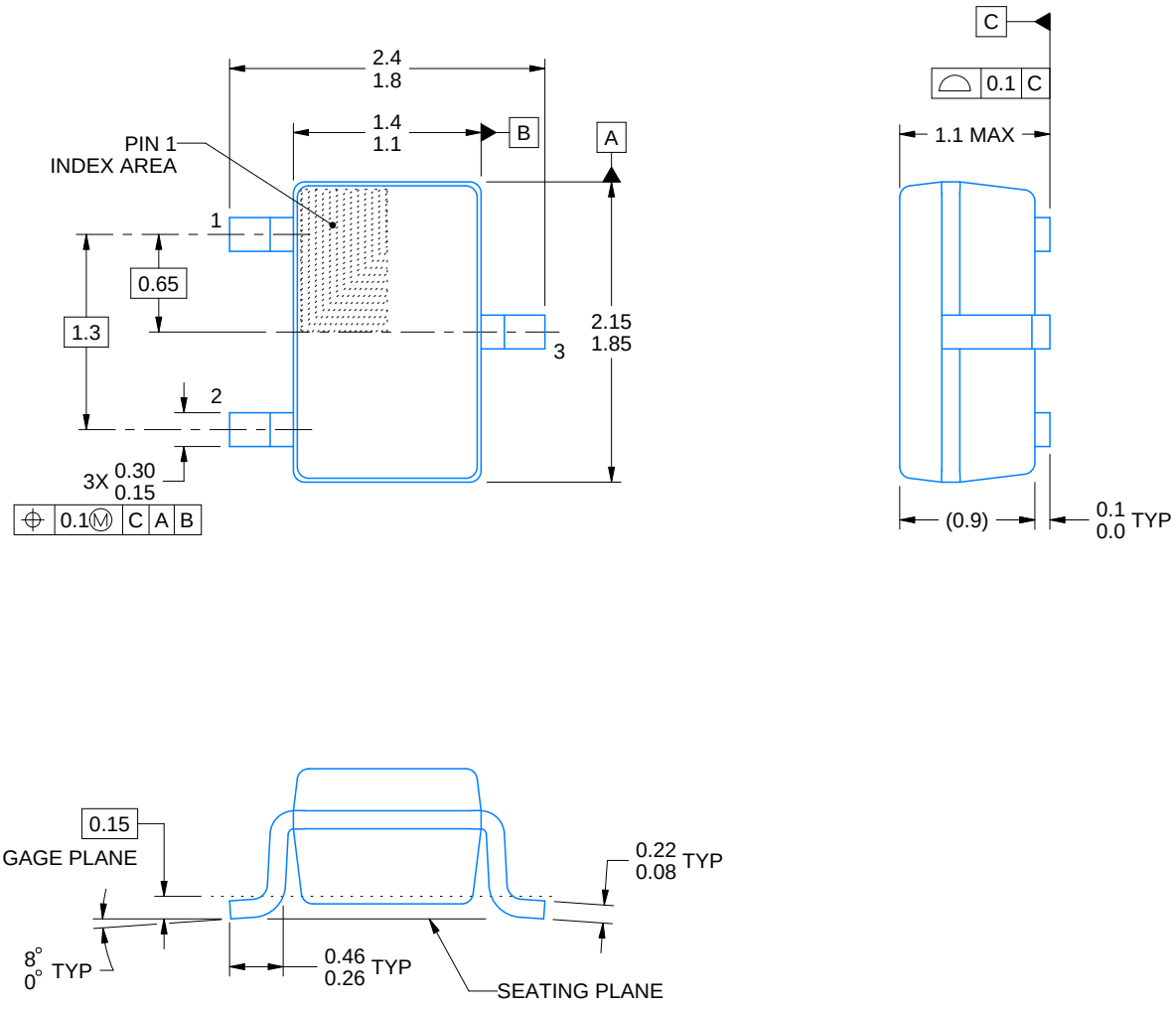
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DCK0003A

PACKAGE OUTLINE

SOT-SC70 - 1.1 max height

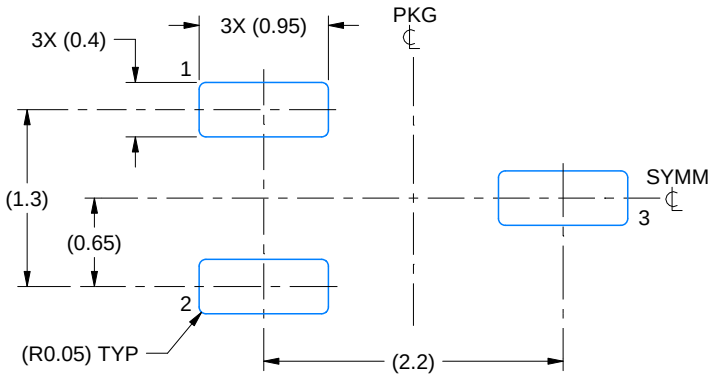
SMALL OUTLINE TRANSISTOR SC70



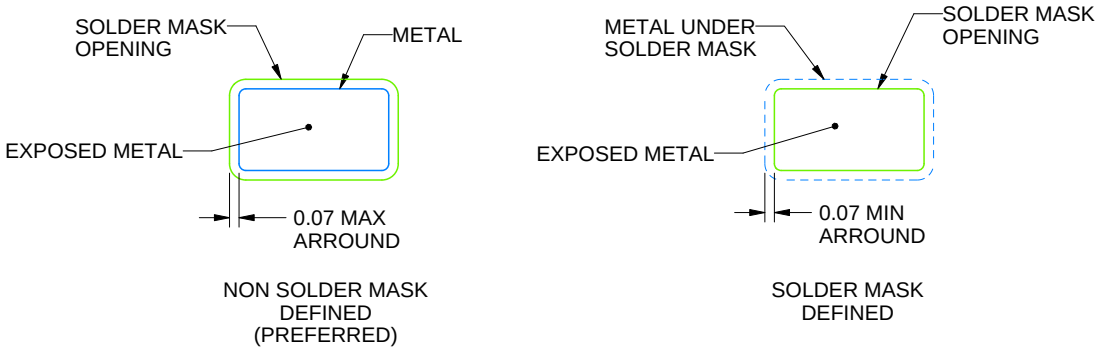
4220745/B 06/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

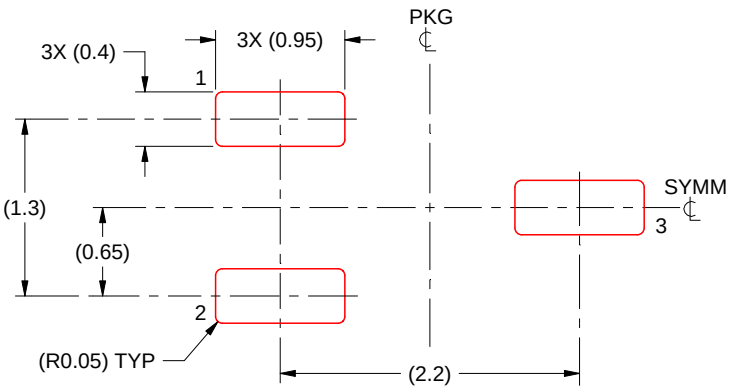


SOLDER MASK DETAILS

4220745/B 06/2020

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/B 06/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

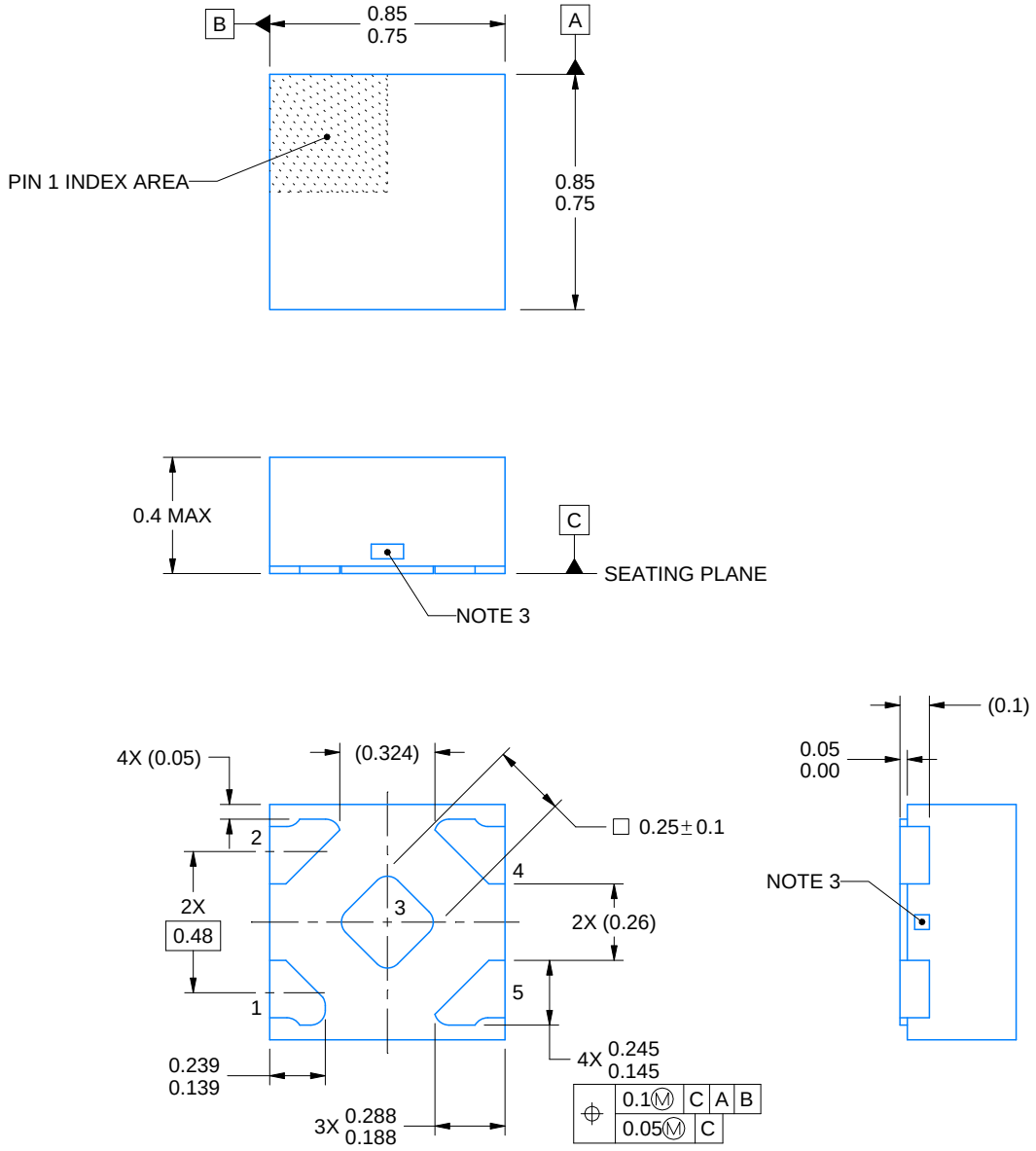
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

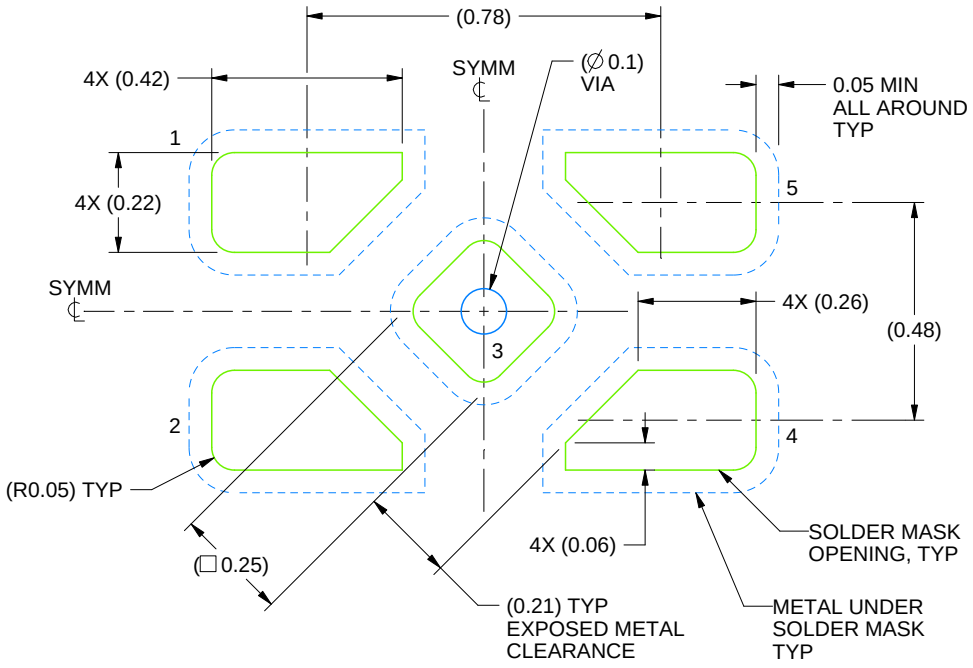
PLASTIC SMALL OUTLINE - NO LEAD



4223102/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/C 06/2021

NOTES: (continued)

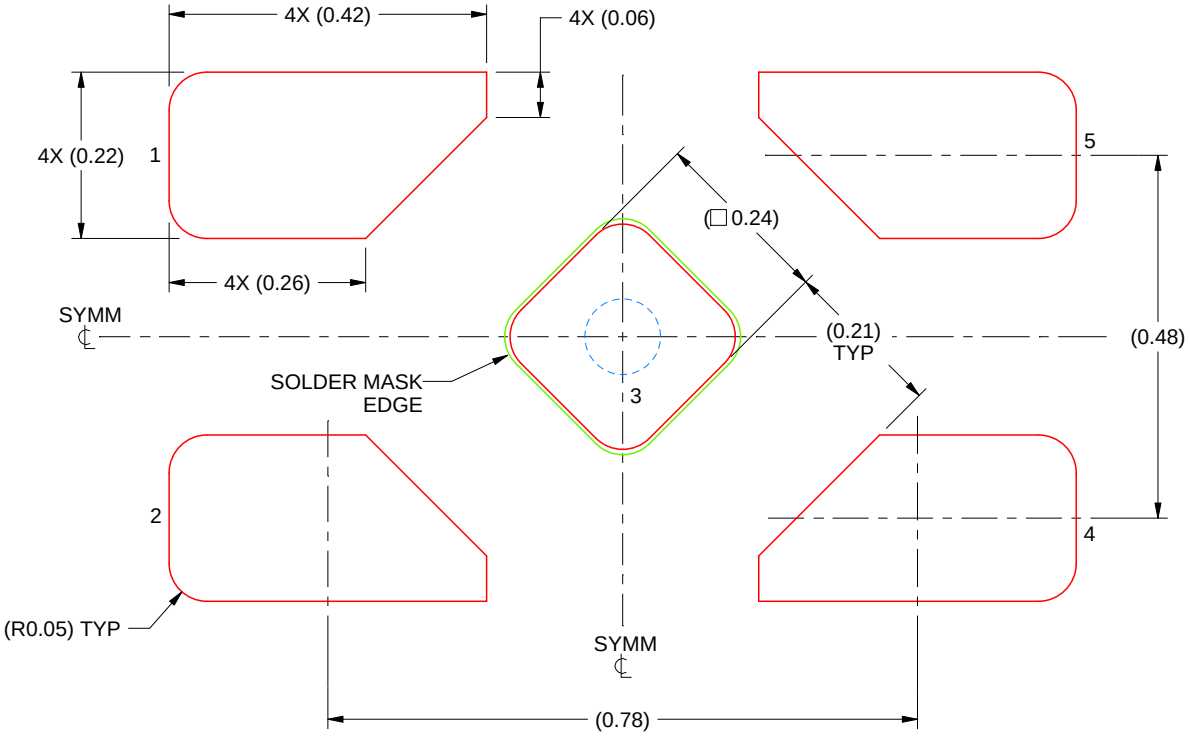
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/C 06/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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