ADJUSTABLE BATTERY-BACKUP SUPERVISOR FOR RAM RETENTION

FEATURES

- **Supply Current of 40 µA (Max)**
- **Battery Supply Current of 100 nA (Max)**
- **Supply Voltage Supervision Range:**
  - **Adjustable**
  - **Other Versions Available on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Power-On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Active-High and Active-Low Reset Output**
- **Chip-Enable Gating: 3 ns (at V_{DD} = 5 V) Max Propagation Delay**
- **10-Pin MSOP Package**
- **Temperature Range: −40°C to 85°C**

APPLICATIONS

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery-Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point-of-Sale Equipment**

DESCRIPTION

The TPS3613-01 supervisory circuit monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM.

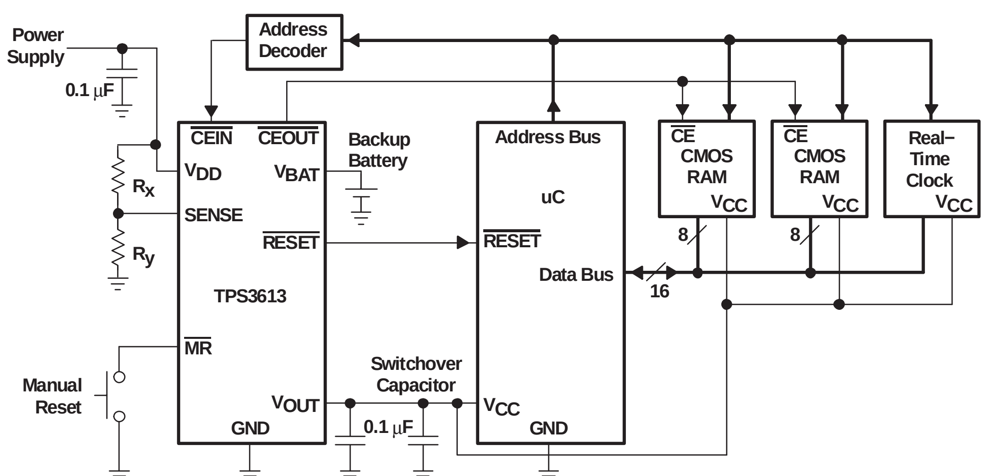
During power-on, reset (RESET and $\overline{\text{RESET}}$) is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V.

Thereafter, the supply voltage supervisor monitors V_{DD} at the SENSE pin through external feedback resistors and keeps reset active as long as SENSE remains below the threshold voltage, V_{IT}.

An internal timer delays the release of the reset state to ensure proper system reset. The delay time starts after SENSE rises above the threshold voltage, V_{IT}.

When SENSE drops below V_{IT}, reset becomes active again.

The TPS3613-01 is available in a 10-pin MSOP package and is characterized for operation over a temperature range of −40°C to +85°C.



PACKAGE INFORMATION

T_A	DEVICE NAME	MARKING
−40°C to +85°C	TPS3613−01DGSR†	AFK

† The DGSR passive indicates tape and reel of 2500 parts.

ordering information application specific versions

TPS361 3 − 01 DGS R

- TPS361 — **Family**
- 3 — **Functionality**
- 01 — **Nominal Supply Voltage**
- DGS — **Package**
- R — **Reel**

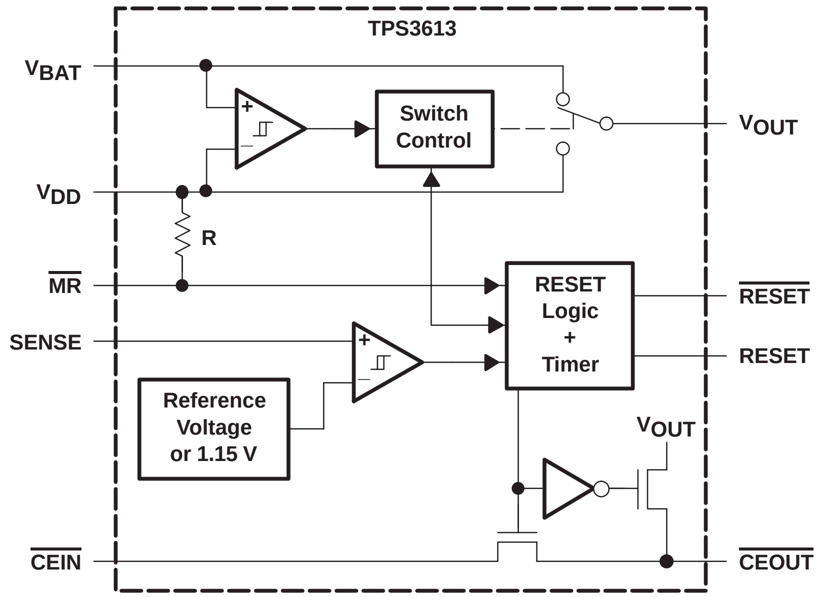
DEVICE NAME	NOMINAL VOLTAGE‡, V_{NOM}
TPS3613−01 DGS	Adjustable

‡ For other threshold voltages, contact the local TI sales office for availability and lead-time.

FUNCTION TABLE

SENSE > V_{IT}	V_{DD} > V_{BAT}	$\overline{MR}$	$\overline{CEIN}$	V_{OUT}	$\overline{RESET}$	RESET	$\overline{CEOUT}$
0	0	0	0	V_{BAT}	0	1	DIS
0	0	0	1	V_{BAT}	0	1	DIS
0	0	1	0	V_{BAT}	0	1	DIS
0	0	1	1	V_{BAT}	0	1	DIS
0	1	0	0	V_{DD}	0	1	DIS
0	1	0	1	V_{DD}	0	1	DIS
0	1	1	0	V_{DD}	0	1	DIS
0	1	1	1	V_{DD}	0	1	DIS
1	0	0	0	V_{DD}	0	1	DIS
1	0	0	1	V_{DD}	0	1	DIS
1	0	1	0	V_{DD}	1	0	0
1	0	1	1	V_{DD}	1	0	1
1	1	0	0	V_{DD}	0	1	DIS
1	1	0	1	V_{DD}	0	1	DIS
1	1	1	0	V_{DD}	1	0	0
1	1	1	1	V_{DD}	1	0	1

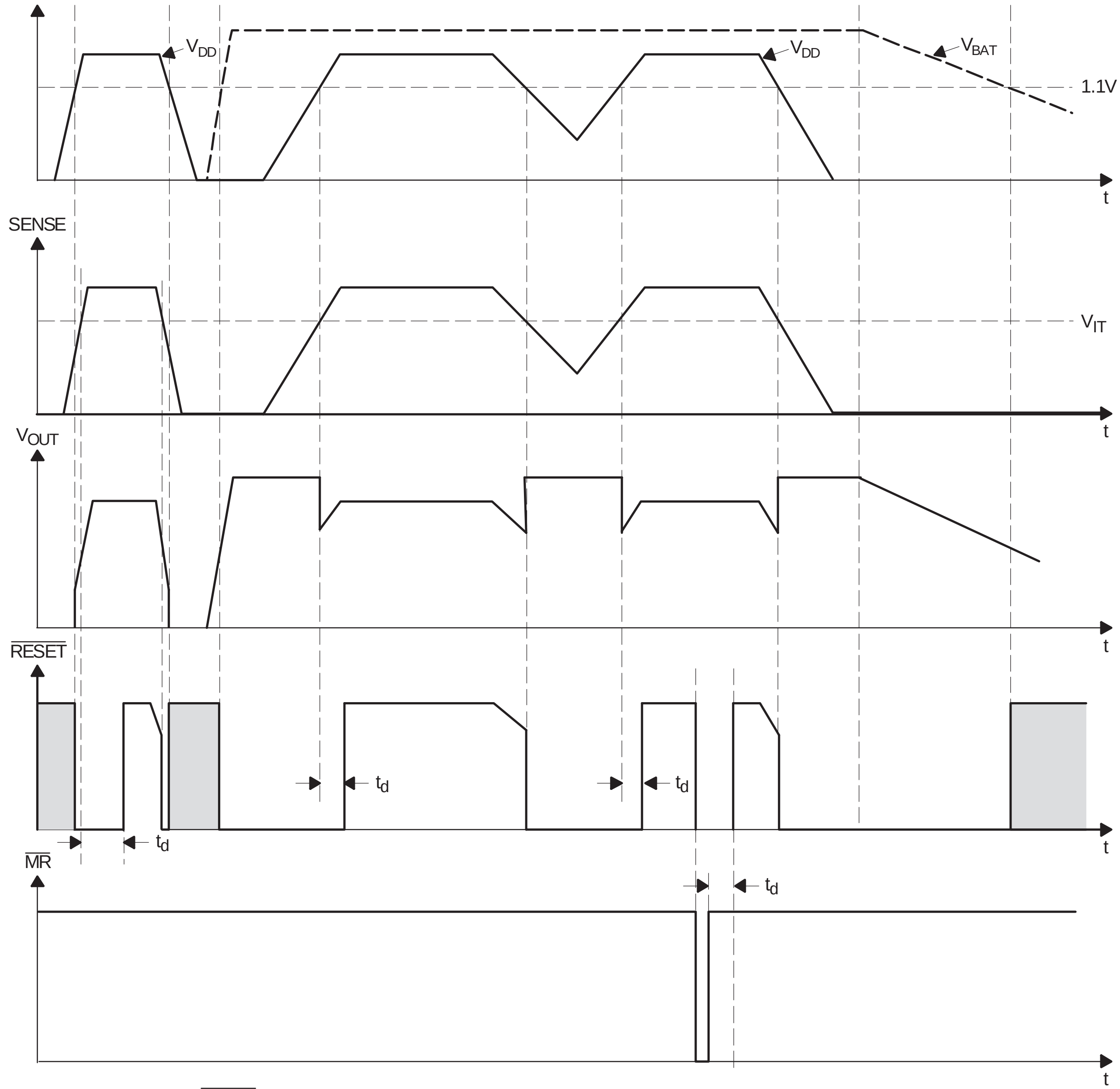
FUNCTIONAL SCHEMATIC



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{CEIN}$	5	I	Chip-enable input
$\overline{CEOUT}$	6	O	Chip-enable output
GND	3	I	Ground
$\overline{MR}$	4	I	Manual reset input
RESET	7	O	Active-high reset output
$\overline{RESET}$	9	O	Active-low reset output
SENSE	8	I	Adjustable sense input, assumed to be connect to V_{DD} throught feedback resistences. Call your local contacts for other application connections.
V_{BAT}	10	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output

TIMING DIAGRAM



NOTE: Shaded area in $\overline{RESET}$ is *undefined*.

detailed description

backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup battery (for example, 3.6-V lithium cells) to have a higher voltage than V_{DD}, these supervisors do not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or when V_{DD} rises above the reset threshold V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

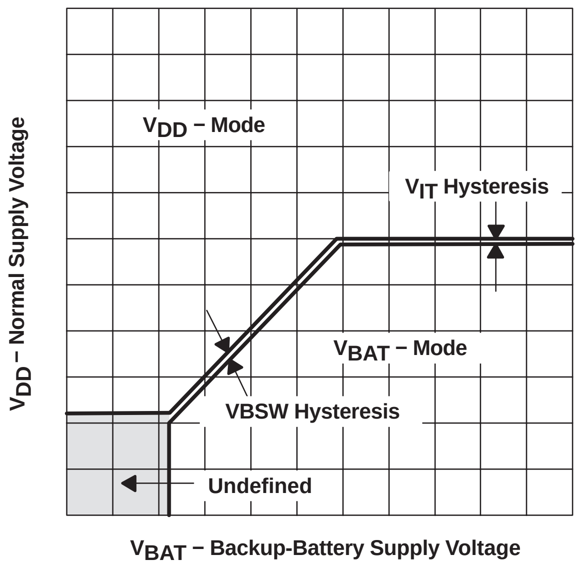


Figure 1. V_{DD} − V_{BAT} Switchover

detailed description (continued)

chip-enable signal gating

The internal gating of chip-enable ($\overline{CE}$) signals prevents erroneous data from corrupting CMOS RAM during an under-voltage condition. The TPS3613 uses a series transmission gate from $\overline{CEIN}$ to $\overline{CEOUT}$. During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{CEIN}$ to $\overline{CEOUT}$ enables the TPS3613 device to be used with most processors.

The CE transmission gate is disabled and $\overline{CEIN}$ is in high impedance (disable mode) while reset is asserted. During a power-down sequence when V_{DD} crosses the reset threshold, the CE transmission gate is disabled and $\overline{CEIN}$ immediately becomes high impedance if the voltage at $\overline{CEIN}$ is high. If $\overline{CEIN}$ is low when reset is asserted, the CE transmission gate is disabled when $\overline{CEIN}$ goes high, or 15 µs after reset asserts, whichever occurs first. This allows the current write cycle to complete during power down. When the CE transmission gate is enabled, the impedance of $\overline{CEIN}$ appears as a resistor in series with the load at $\overline{CEOUT}$. The overall device propagation delay through the CE transmission gate depends on V_{OUT}, the source impedance of the drive connected to $\overline{CEIN}$, and the load at $\overline{CEOUT}$. To achieve minimum propagation delay, the capacitive load at $\overline{CEOUT}$ should be minimized, and a low-output-impedance driver is used.

In the disabled mode, the transmission gate is off and an active pullup connects $\overline{CEOUT}$ to V_{OUT}. This pullup turns off when the transmission gate is enabled.

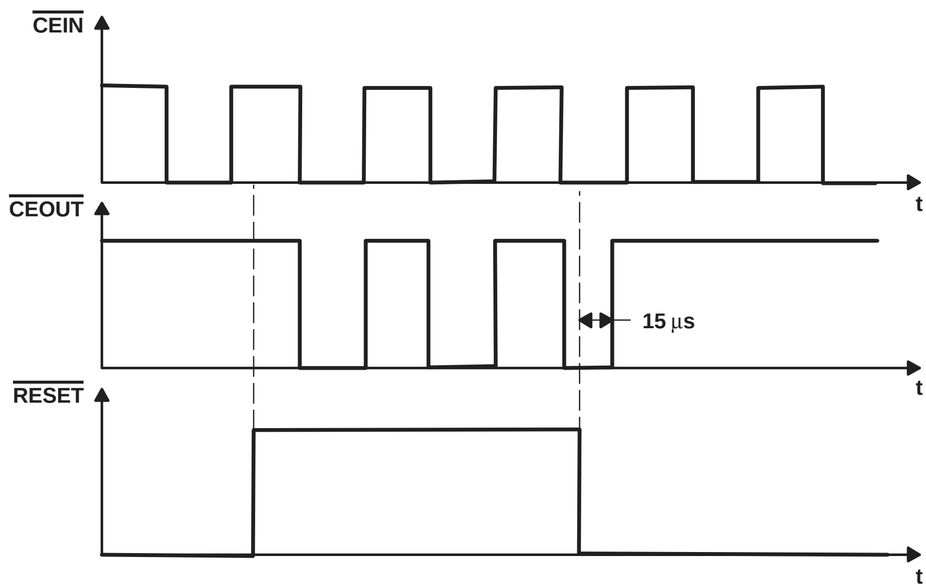


Figure 2. Chip-Enable Timing

ABSOLUTE MAXIMUM RATINGS
OVER OPERATING FREE-AIR TEMPERATURE (unless otherwise noted)(1)

Supply voltage: V_{DD}(2)	7 V
$\overline{MR}$ and SENSE pins(2)	−0.3 V to (V_{DD} + 0.3 V)
Continuous output current at V_{OUT}: I_O	400 mA
All other pins, I_O	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to +85°C
Storage temperature range, T_{stg}	−65°C to +150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	+260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device must not operate at 7 V for more than t = 1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le$ +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DGS	424 mW	3.4 mW/°C	271 mW	220 mW

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_{DD} + 0.3	V
High-level input voltage, V_{IH}	0.7 x V_{DD}		V
Low-level input voltage, V_{IL}		0.3 x V_{DD}	V
Continuous output current at V_{OUT}, I_O		300	mA
Input transition rise and fall rate at $\overline{MR}$, Δt/ΔV		100	ns/V
Slew rate at V_{DD} or V_{bat}		1	V/µs
Operating free-air temperature range, T_A	−40	+85	°C

ELECTRICAL CHARACTERISTICS
OVER RECOMMENDED OPERATING CONDITIONS (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 1.8 V I_{OH} = −400 µA	V_{DD} − 0.2 V			V
			V_{DD} = 3.3 V, I_{OH} = −2 mA V_{DD} = 5 V, I_{OH} = −3 mA	V_{DD} − 0.4 V			
		RESET	V_{DD} = 1.8 V, I_{OH} = −20 µA	V_{DD} − 0.3 V			
			V_{DD} = 3.3 V, I_{OH} = −80 µA V_{DD} = 5 V, I_{OH} = −120 µA	V_{DD} − 0.4 V			
		$\overline{CEOUT}$	V_{OUT} = 1.8 V, I_{OH} = −1 mA	V_{OUT} − 0.2 V			
		Enable mode $\overline{CEIN}$ = V_{OUT}	V_{OUT} = 3.3 V, I_{OH} = −2 mA V_{OUT} = 5 V, I_{OH} = −5 mA	V_{OUT} − 0.3 V			
		$\overline{CEOUT}$ Disable mode	V_{OUT} = 3.3 V, I_{OH} = −0.5 mA	V_{OUT} − 0.4 V			
V_{OL}	Low-level output voltage	$\overline{RESET}$	V_{DD} = 1.8 V, I_{OL} = 400 µA			0.2	V
		RESET	V_{DD} = 3.3 V, I_{OL} = 2 mA V_{DD} = 5 V, I_{OL} = 3 mA			0.4	
		$\overline{CEOUT}$	V_{OUT} = 1.8 V, I_{OL} = 1.0 mA			0.2	
		Enable mode $\overline{CEIN}$ = 0 V	V_{OUT} = 3.3 V, I_{OL} = 2 mA V_{OUT} = 5 V, I_{OL} = 5 mA			0.3	
		Power-up reset voltage (see Note 1)	V_{DD} > 1.1 V or V_{BAT} > 1.1 V, I_{OL} = 20 µA			0.4	V
V_{OUT}	Normal mode		I_O = 8.5 mA, V_{DD} = 1.8 V, V_{BAT} = 0 V	V_{DD} – 50 mV			V
			I_O = 125 mA, V_{DD} = 3.3 V, V_{BAT} = 0 V	V_{DD} − 150 mV			
			I_O = 200 mA, V_{DD} = 5 V, V_{BAT} = 0 V	V_{DD} – 200 mV			
	Battery-backup mode		I_O = 0.5 mA, V_{BAT} = 1.5 V, V_{DD} = 0 V	V_{BAT} − 20 mV			
			I_O = 7.5 mA, V_{BAT} = 3.3 V, V_{DD} = 0 V	V_{BAT} – 113 mV			
$R_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 5 V		0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{BAT} = 3.3 V		8	15	
V_{IT}	Negative-going input threshold voltage (see Note 2)			1.13	1.15	1.17	V
V_{hys}	Hysteresis	Sense	1.1 V < V_{IT} < 1.65 V		12		mV
		V_{BSW} (see Note 3)	V_{DD} = 1.8 V		55		
I_{IH}	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 x V_{DD}, V_{DD} = 5 V	−33		−76	µA
I_{IL}	Low-level input current		$\overline{MR}$ = 0 V, V_{DD} = 5 V	−110		−255	
I_I	Input current	SENSE	V_{DD} = 1.15 V	−25		25	nA
I_{DD}	V_{DD} supply current		V_{OUT} = V_{DD}			40	µA
			V_{OUT} = V_{BAT}			40	
I_{BAT}	V_{BAT} supply current		V_{OUT} = V_{DD}	−0.1		0.1	µA
			V_{OUT} = V_{BAT}			0.5	
I_{lkg}	$\overline{CEIN}$ leakage current		Disable mode, V_I < V_{DD}			±1	µA
C_i	Input capacitance		V_I = 0 V to 5 V		5		pF

(1) The lowest voltage at which $\overline{RESET}$ becomes active. $t_{r,(VDD)} \geq 15$ µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.
(3) For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}

TIMING REQUIREMENTS AT R_L = 1 MΩ, C_L = 50 PF, T_A = −40°C TO +85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_W	Pulse width	SENSE	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ − 0.2 V	6			µs

SWITCHING CHARACTERISTICS AT R_L = 1 MΩ, C_L= 50 PF, T_A = −40°C TO +85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{SENSE} \geq V_{IT}$ + 0.2 V, $\overline{MR} \geq$ 0.7 x V_{DD}, See timing diagram	60	100	140	ms
t_{PLH}	Propagation (delay) time, low-to-high-level output	50% $\overline{RESET}$ to 50% $\overline{CEOUT}$	$V_{OUT} = V_{IT}$		15		µs
t_{PHL}	Propagation (delay) time, high-to-low-level output	50% $\overline{CEIN}$ to 50% $\overline{CEOUT}$, C_L = 50 pF only (see Note 5)	V_{DD} = 1.8 V		5	15	ns
			V_{DD} = 3.3 V		1.6	5	ns
			V_{DD} = 5 V		1	3	ns
		SENSE to $\overline{RESET}$	$V_{IL} = V_{IT}$ − 0.2 V, $V_{IH} = V_{IT}$ + 0.2 V		2	5	µs
		$\overline{MR}$ to $\overline{RESET}$	$V_{SENSE} \geq V_{IT}$ + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}		0.1	1	µs
	Transition time	V_{DD} to V_{BAT}	$V_{IH} = V_{BAT}$ + 0.2 V, $V_{IL} = V_{BAT}$ − 0.2 V, $V_{BAT} < V_{IT}$			3	µs

(1) Assured by design

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance (V_{DD} to V_{OUT})	vs Output current	3
	Static drain-source on-state resistance (V_{BAT} to V_{OUT})	vs Output current	4
	Static drain-source on-state resistance ($\overline{CEIN}$ to $\overline{CEOUT}$)	vs Input voltage at $\overline{CEIN}$	5
I_{DD}	Supply current	vs Supply voltage	6
V_{IT}	Input threshold voltage at $\overline{RESET}$	vs Free-air temperature	7
V_{OH}	High-level output voltage at $\overline{RESET}$	vs High-level output current	8, 9
	High-level output voltage at $\overline{CEOUT}$		10, 11, 12, 13
V_{OL}	Low-level output voltage at $\overline{RESET}$	vs Low-level output current	14, 15
	Low-level output voltage at $\overline{CEOUT}$	vs Low-level output current	16, 17

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{DD} to V_{OUT}) vs OUTPUT CURRENT

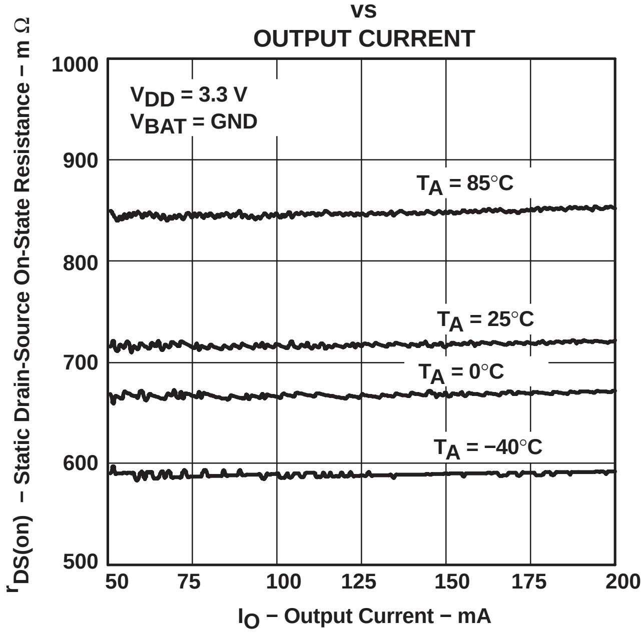


Figure 3

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{BAT} to V_{OUT}) vs OUTPUT CURRENT

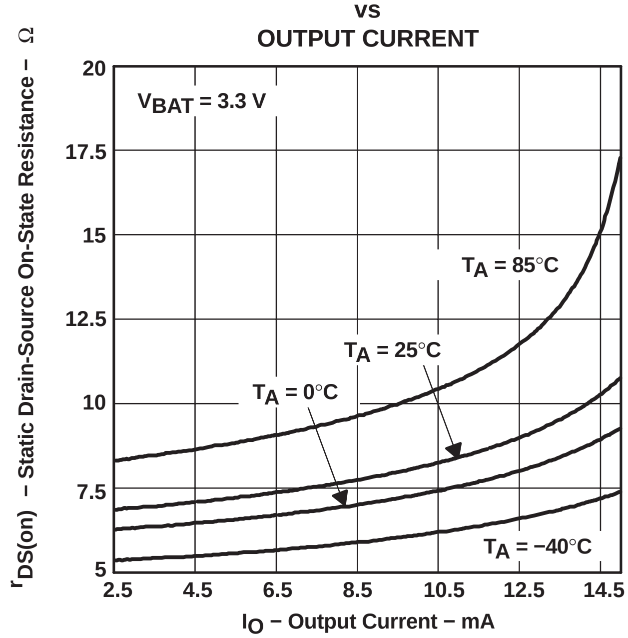


Figure 4

TYPICAL CHARACTERISTICS

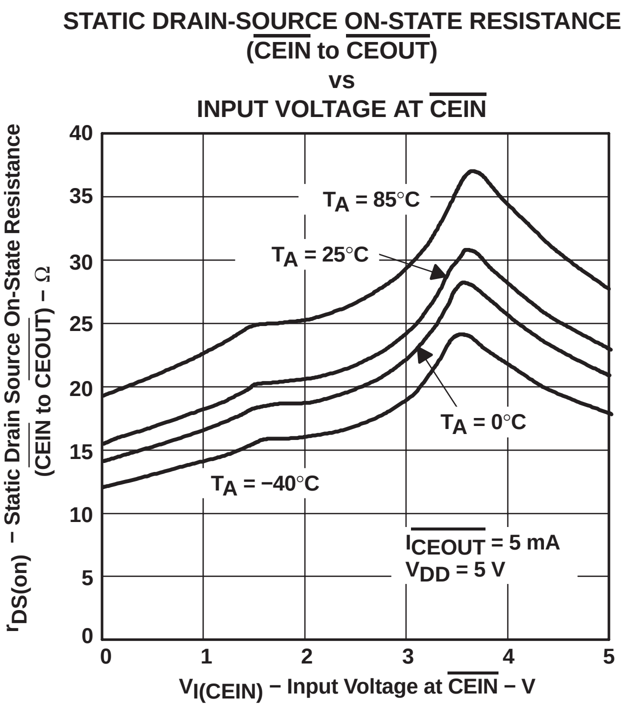


Figure 5

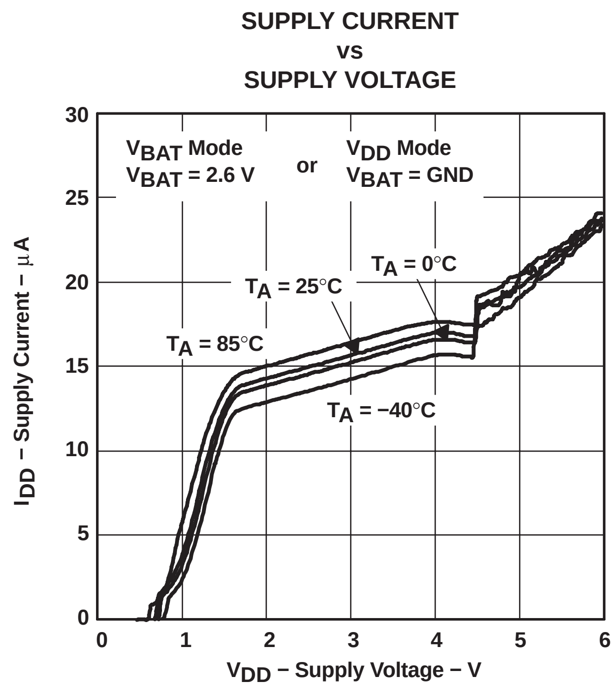


Figure 6

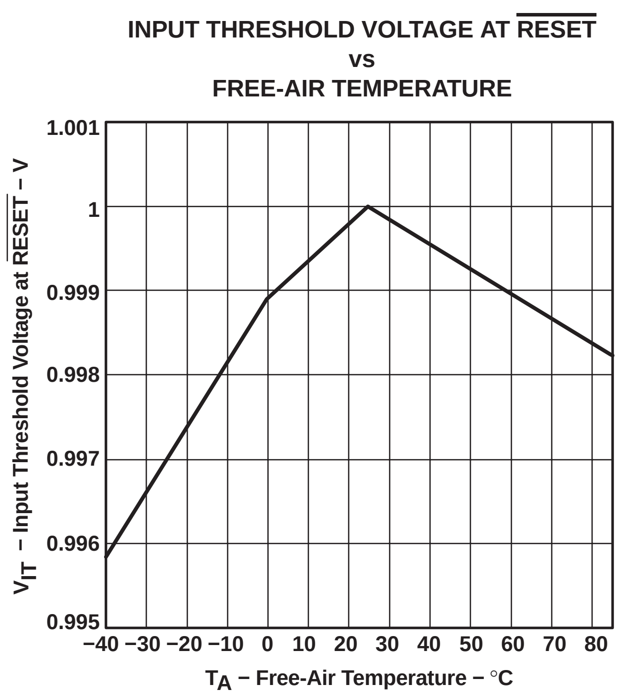


Figure 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE AT RESET
vs
HIGH-LEVEL OUTPUT CURRENT

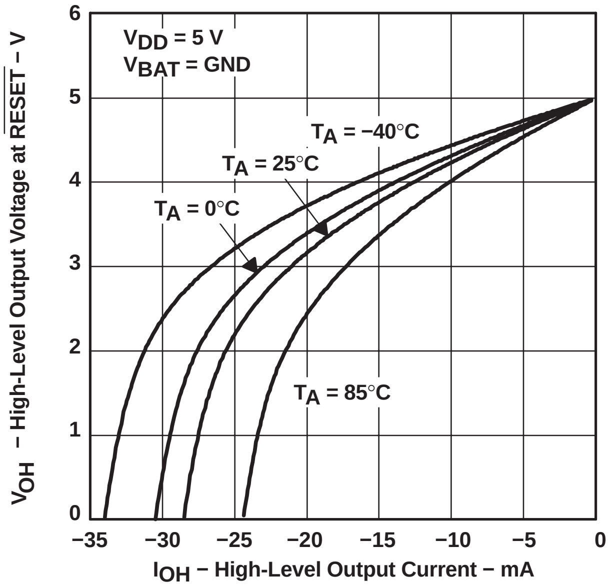


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE AT RESET
vs
HIGH-LEVEL OUTPUT CURRENT

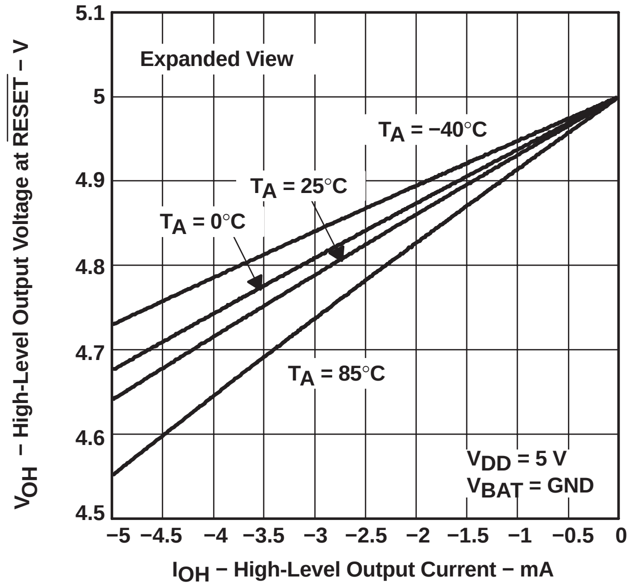


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE AT CEOUT
vs
HIGH-LEVEL OUTPUT CURRENT

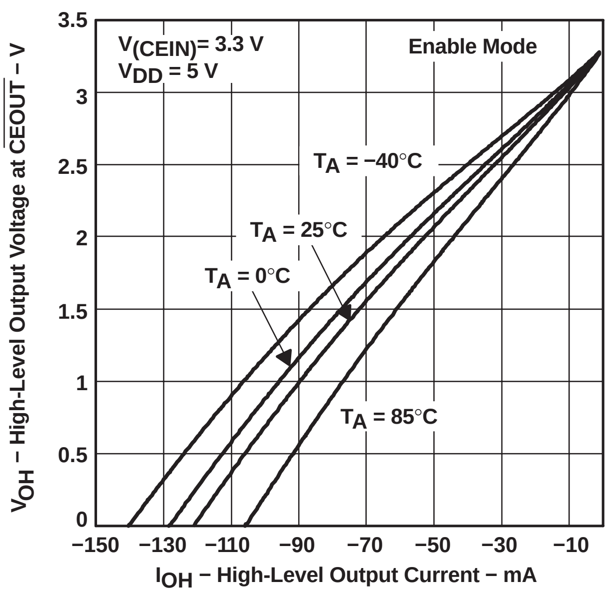


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE AT CEOUT
vs
HIGH-LEVEL OUTPUT CURRENT

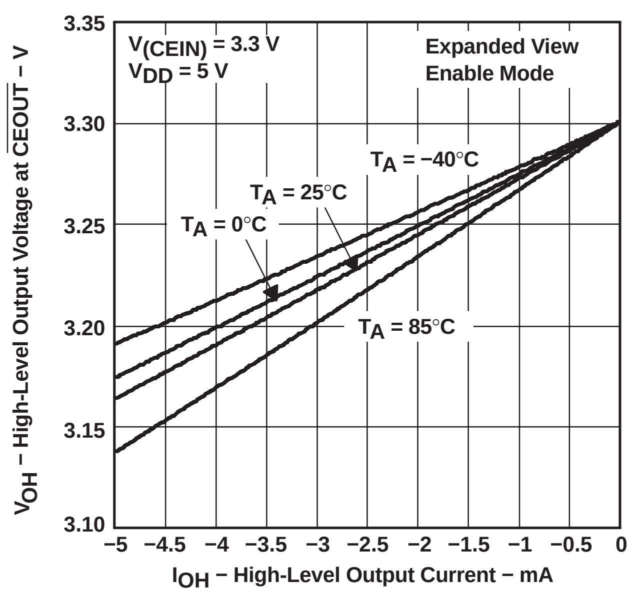


Figure 11

TYPICAL CHARACTERISTICS

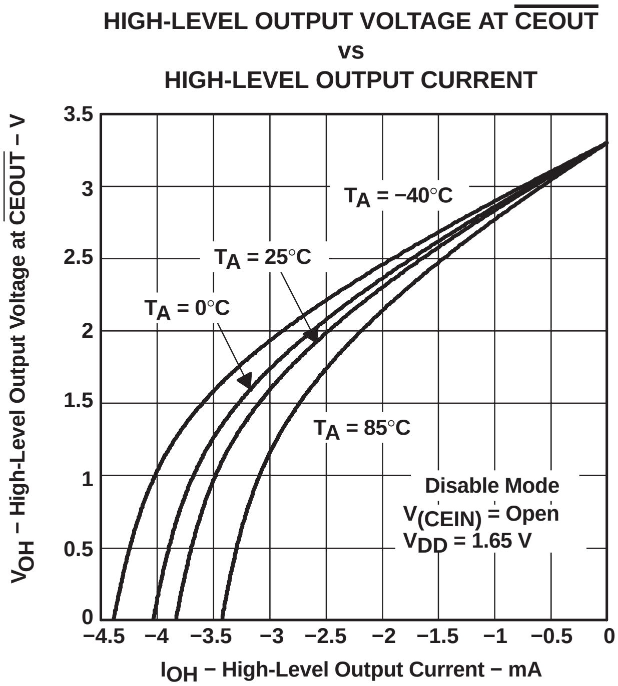


Figure 12

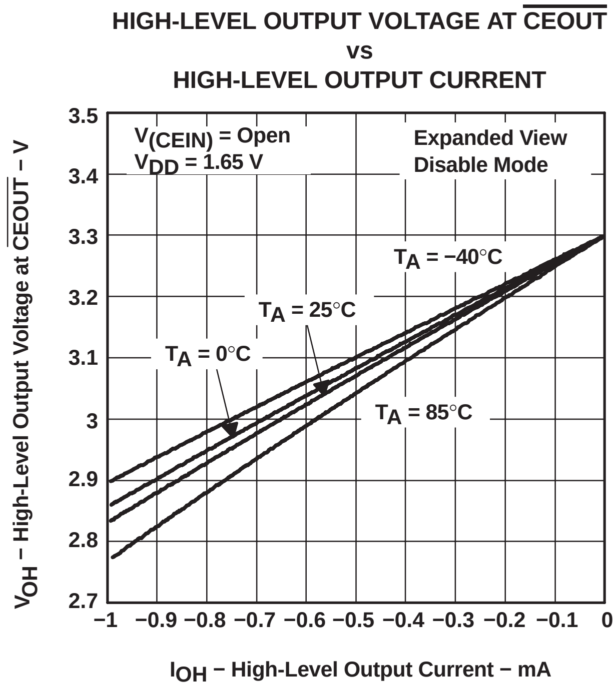


Figure 13

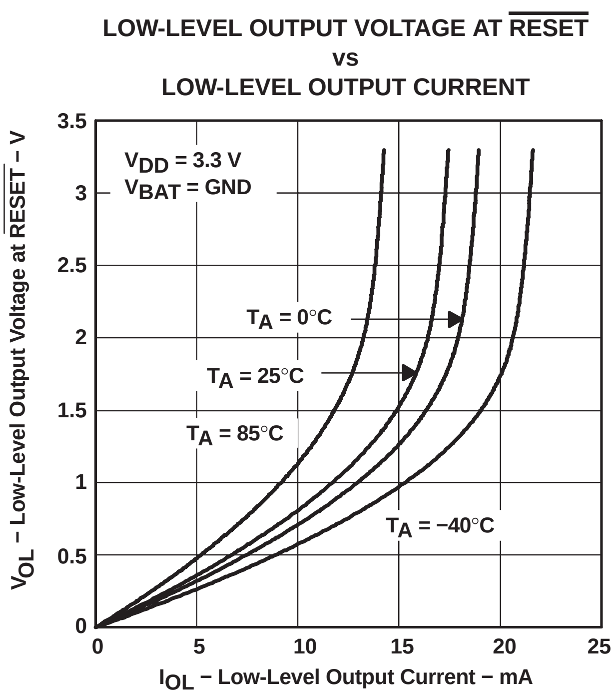


Figure 14

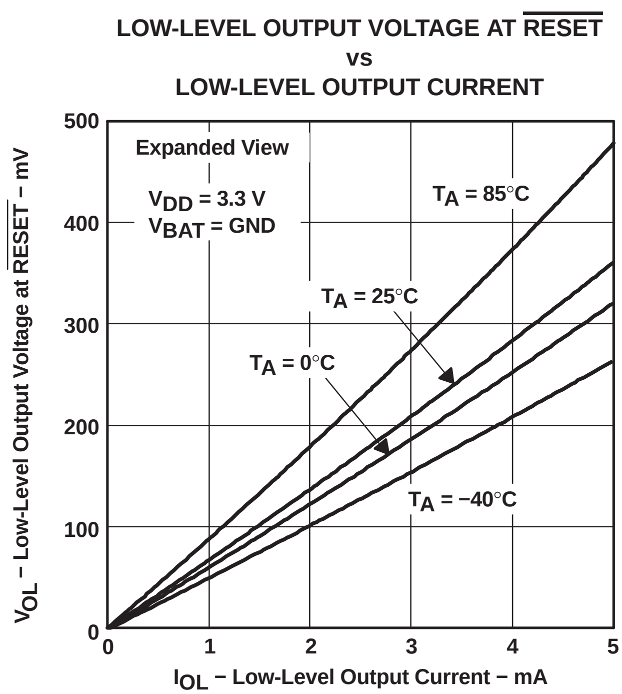


Figure 15

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{CEOUT}$ vs LOW-LEVEL OUTPUT CURRENT

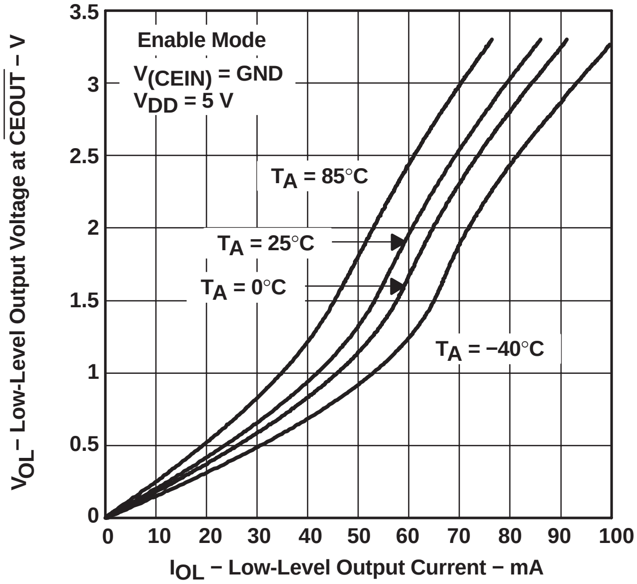


Figure 16

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{CEOUT}$ vs LOW-LEVEL OUTPUT CURRENT

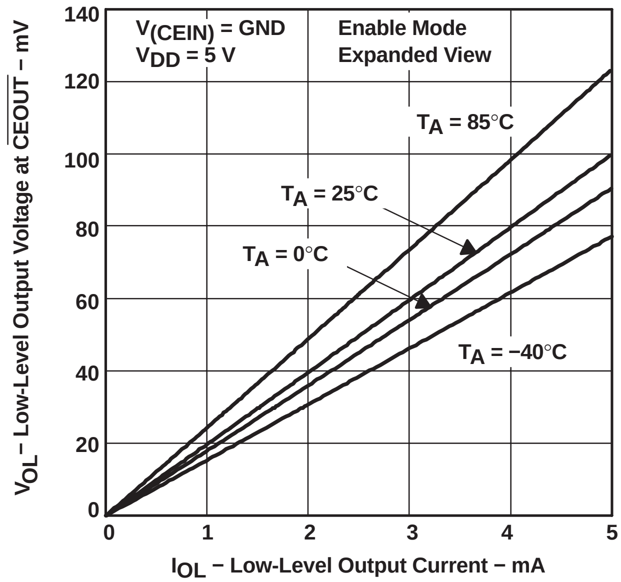


Figure 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3613-01DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFK	Samples
TPS3613-01DGSG4	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFK	Samples
TPS3613-01DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFK	Samples
TPS3613-01DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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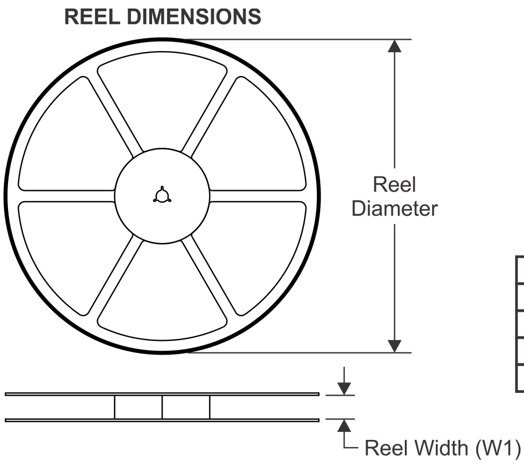
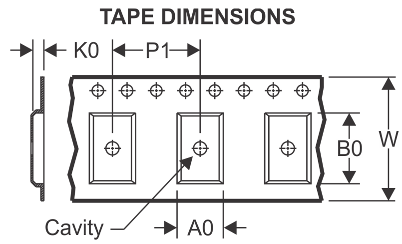
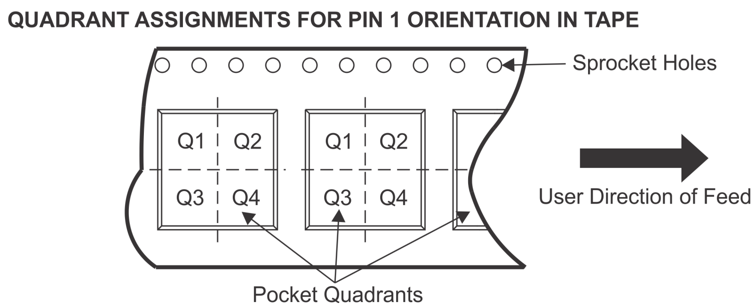
TAPE AND REEL INFORMATION





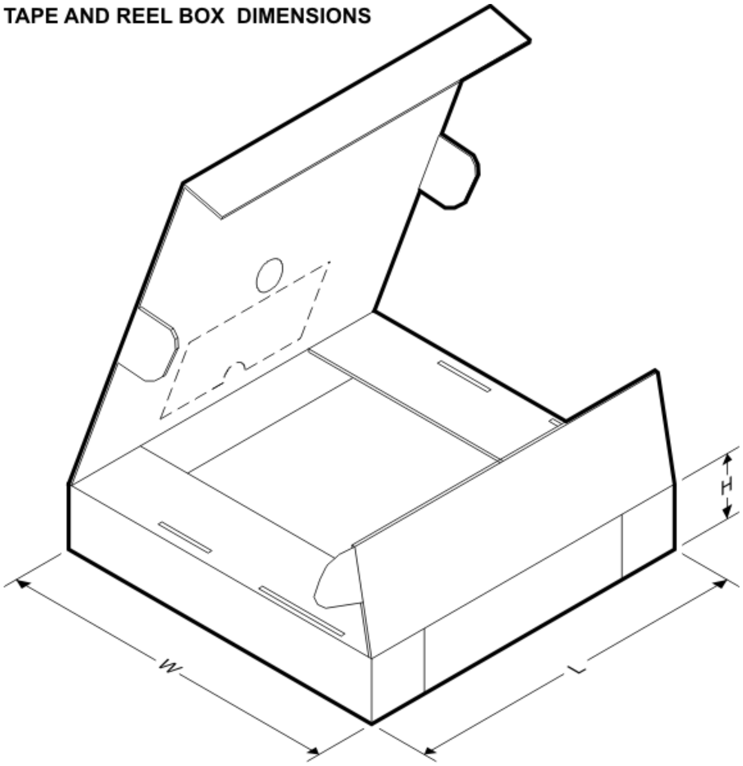
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

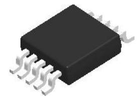
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3613-01DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

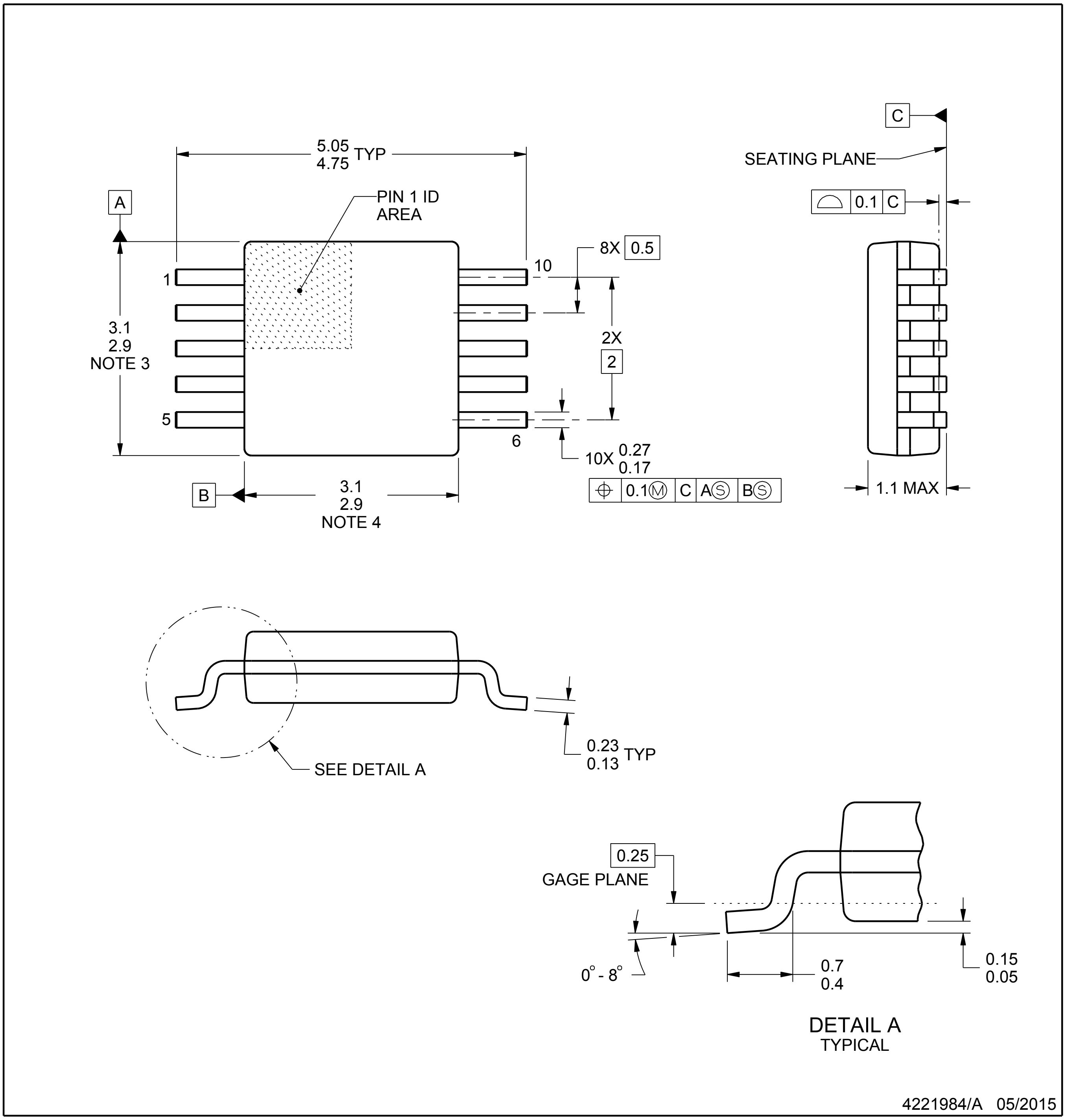
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3613-01DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0



PACKAGE OUTLINE

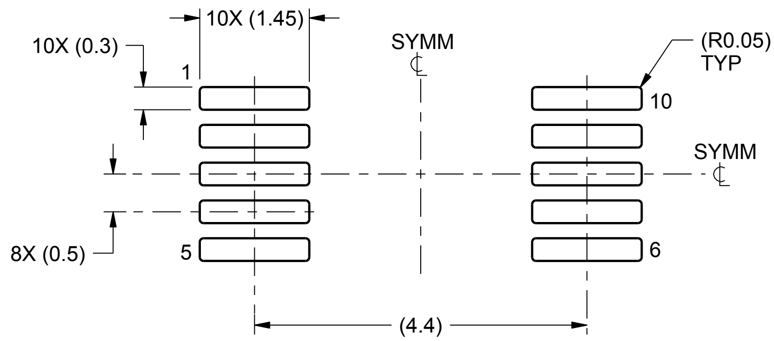
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

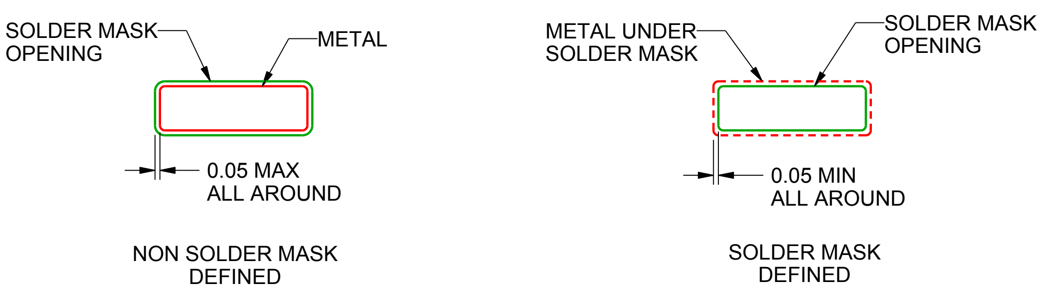


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

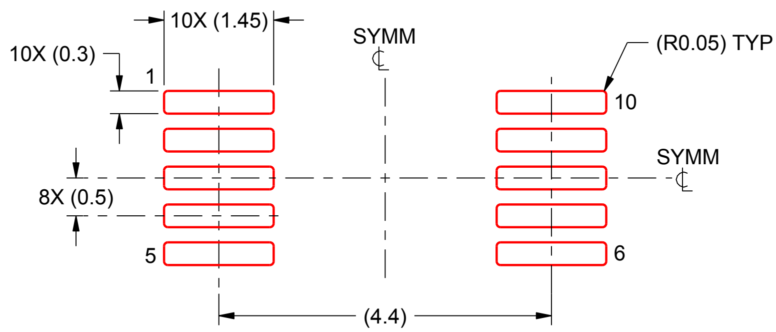


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.