低压电机驱动器集成电路 (IC)

查询样片: DRV8832-Q1

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果：
  - 器件温度 **1** 级：**-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C4B**
- **H** 桥压控电机驱动器
  - 驱动直流电机，一个步进电机的绕组，或其它致动器/负载
  - 高效脉宽调制 **(PWM)** 电压控制以实现变化电源电压时的恒定电机速度
  - 低金属氧化物半导体场效应晶体管 **(MOSFET)** 导通电阻：
    高侧 **(HS) +** 低侧 **(LS) 450mΩ**
- **1A** 最大直流/均方根 **(RMS)** 或峰值驱动电流
- **2.75V** 至 **6.8V** 运行电源电压范围
- **300nA**（典型值）睡眠模式电流
- 基准电压输出
- 电流限制电路
- 故障输出
- 耐热增强型表面贴装封装

应用范围

- 由电池供电的设备：
  - 打印机
  - 玩具
  - 机器人技术
  - 摄像机
  - 电话
- 小型致动器，泵等

说明

DRV8832-Q1 为电池供电类玩具、打印机和其它低电压或者电池供电的运动控制类应用提供了一个集成的电机驱动器解决方案。 此器件有一个 H 桥驱动器，并且能够驱动一个直流电机或者一个步进电机的绕组，以及其它诸如螺线管等的负载。 输出驱动器块包括配置为一个 H 桥的 N 通道和 P 通道功率 MOSFET 以驱动电机绕组。

由于提供了足够的印刷电路板 (PCB) 散热，DRV8832-Q1 能够提供高达 1A 的直流 / RMS 或峰值输出电流。 它可在 2.75V 至 6.8V 的电源电压下工作。

为了在变化的电池电压上保持恒定的电机速度，同时又保持较长电池使用寿命，提供了一个 PWM 电压调节方法。一个输入引脚可实现经稳压电压的设定。 还提供了一个内置电压基准输出。

提供了针对过流保护、短路保护、欠压锁定以及过热保护的内部保护功能。

DRV8832-Q1 还提供了一个电流限制功能来在诸如电机启动或停止转动的情况下调节电机电流，以及一个将故障情况发送给主机处理器的故障输出引脚。

DRV8832-Q1 采用具有 PowerPAD™ 的极小型 3mm x 3mm 10 引脚表面贴装小外形尺寸 (MSOP) 封装（环保型：符合 RoHS 标准且不含铅/溴）。

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	PowerPAD™ (MSOP) - DGQ	Reel of 250	DRV8832QDGQRQ1	8832Q
		Tube of 80	DRV8832QDGQQ1	8832Q

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

Functional Block Diagram

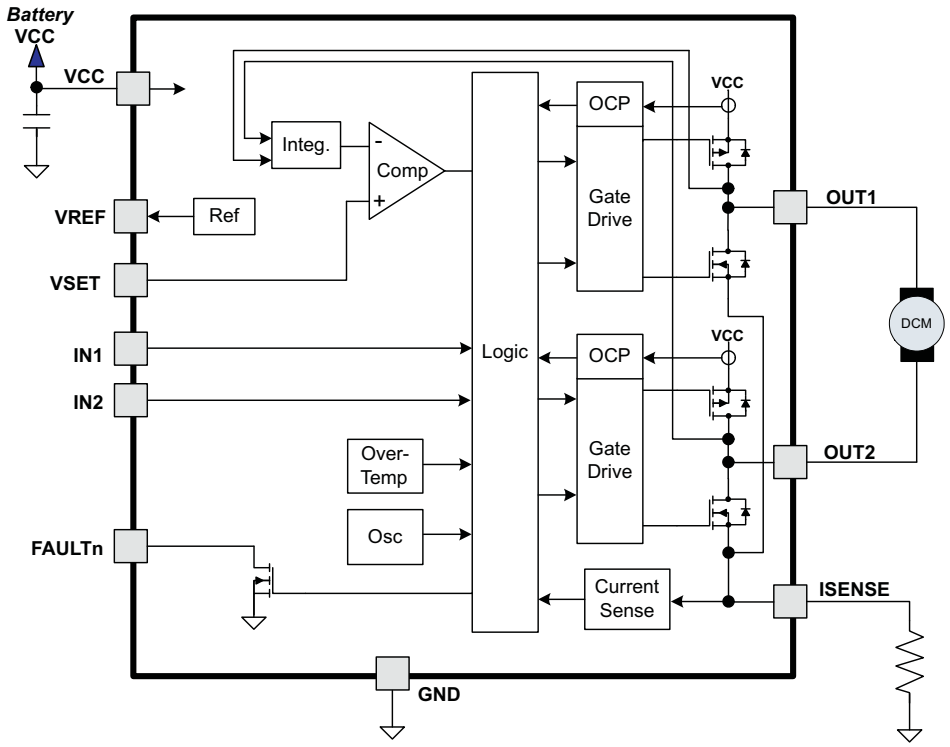
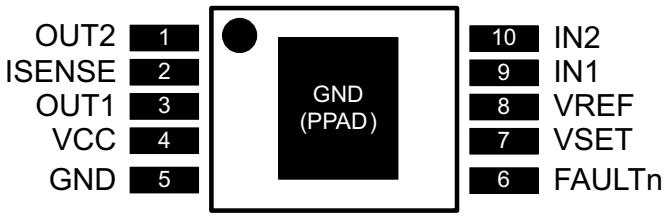


Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
GND	5	-	Device ground	
VCC	4	-	Device and motor supply	Bypass to GND with a 0.1-µF (minimum) ceramic capacitor.
IN1	9	I	Bridge A input 1	Logic high sets OUT1 high
IN2	10	I	Bridge A input 2	Logic high sets OUT2 high
VREF	8	O	Reference voltage output	Reference voltage output
VSET	7	I	Voltage set input	Input voltage sets output regulation voltage
FAULTn	6	OD	Fault output	Open-drain output driven low if fault condition present
OUT1	3	O	Bridge output 1	Connect to motor winding
OUT2	1	O	Bridge output 2	Connect to motor winding
ISENSE	2	IO	Current sense resistor	Connect current sense resistor to GND. Resistor value sets current limit level.

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

DGQ PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE	UNIT
VCC	Power supply voltage range	–0.3 to 7	V
	Input pin voltage range	–0.5 to 7	V
	Peak motor drive output current(3)	Internally limited	A
	Continuous motor drive output current(3)	1	A
	Continuous total power dissipation	See Dissipation Ratings table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8832-Q1 DGQ 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	69.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	63.5	
θ_{JB}	Junction-to-board thermal resistance(4)	51.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	23.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	9.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Motor power supply voltage range	2.75		6.8	V
I_{OUT}	Continuous or peak H-bridge output current(1)	0		1	A

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.75 V to 6.8 V, T_A = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VCC}	VCC operating supply current	V_{CC} = 5 V		1.4	2	mA
I_{VCCQ}	VCC sleep mode supply current	V_{CC} = 5 V, T_A = 25°C		0.3	1	µA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising		2.575	2.75	V
		V_{CC} falling		2.47		
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.25 x VCC	V
V_{IH}	Input high voltage		0.5 x VCC			V
I_{IL}	Input low current	V_{IN} = 0	-10		10	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
LOGIC-LEVEL OUTPUTS (FAULTn)						
V_{OL}	Output low voltage	V_{CC} = 5 V, I_{OL} = 4 mA(1)		0.5		V
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_{CC} = 5 V, I_O = 0.8 A, T_J = 125°C		340	450	mΩ
		V_{CC} = 5 V, I_O = 0.8 A, T_J = 25°C		250		
$R_{DS(ON)}$	LS FET on resistance	V_{CC} = 5 V, I_O = 0.8 A, T_J = 125°C		270	360	mΩ
		V_{CC} = 5 V, I_O = 0.8 A, T_J = 25°C		200		
I_{OFF}	Off-state leakage current		–20		20	µA
MOTOR DRIVER						
t_R	Rise time	V_{CC} = 3 V, load = 4 Ω	50		300	ns
t_F	Fall time	V_{CC} = 3 V, load = 4 Ω	50		300	ns
f_{SW}	Internal PWM frequency			44.5		kHz
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.3		3	A
t_{OCP}	OCP deglitch time			2		µs
T_{TSD}	Thermal shutdown temperature	Die temperature(1)	150	160	180	°C
VOLTAGE CONTROL						
V_{REF}	Reference output voltage		1.235	1.285	1.335	V
ΔV_{LINE}	Line regulation	V_{CC} = 3.3 V to 6 V, V_{OUT} = 3 V(1) I_{OUT} = 500 mA		±1		%
ΔV_{LOAD}	Load regulation	V_{CC} = 5 V, V_{OUT} = 3 V I_{OUT} = 200 mA to 800 mA(1)		±1		%
CURRENT LIMIT						
V_{ILIM}	Current limit sense voltage		160	200	240	mV
t_{ILIM}	Current limit fault deglitch time			275		ms
R_{ISEN}	Current limit set resistance (external resistor value)		0		1	Ω

(1) Not production tested.

TYPICAL PERFORMANCE GRAPHS

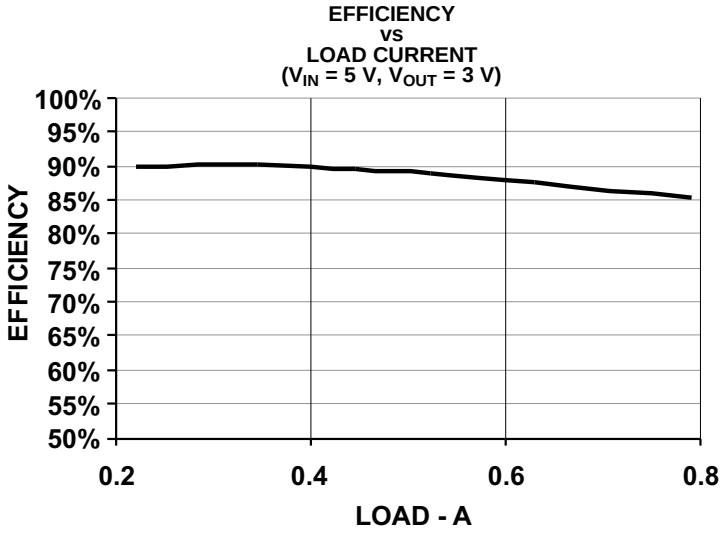


Figure 1.

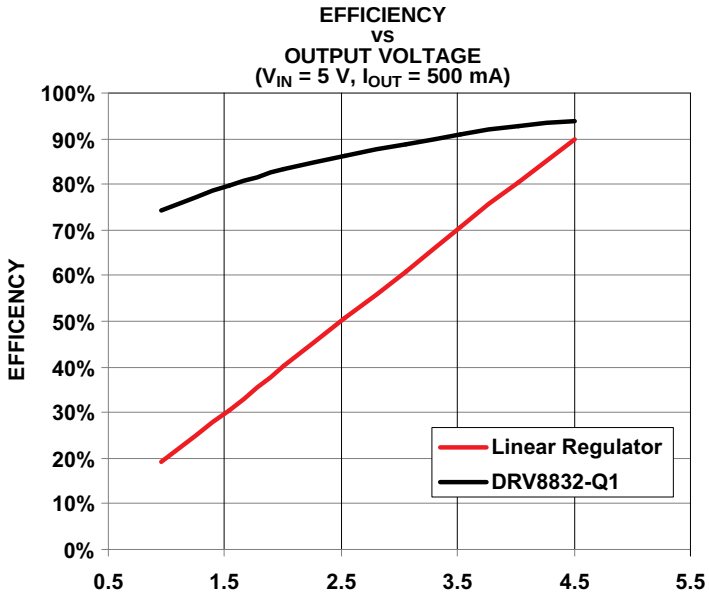


Figure 2.

FUNCTIONAL DESCRIPTION

Power Supervisor

The DRV8832 is capable of entering a low-power sleep mode by bringing both of the INx control inputs logic low. The outputs will be disabled Hi-Z.

In order to exit the sleep mode, bring either or both of the INx inputs logic high. This will enable the H-bridges. When exiting the sleep mode, the FAULTn pin will pulse low.

PWM Motor Driver

The DRV8832-Q1 contains an H-bridge motor driver with PWM voltage-control circuitry with current limit circuitry. A block diagram of the motor control circuitry is shown below.

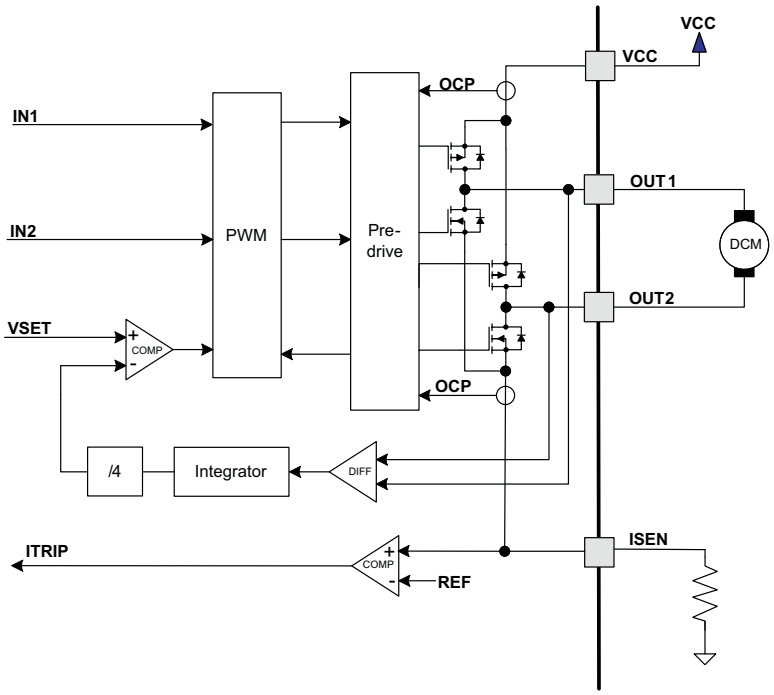


Figure 3. Motor Control Circuitry

Bridge Control

The IN1 and IN2 control pins enable the H-bridge outputs. The following table shows the logic:

Table 2. H-Bridge Logic

IN1	IN2	OUT1	OUT2	Function
0	0	Z	Z	Sleep/coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	H	H	Brake

When both bits are zero, the output drivers are disabled and the device is placed into a low-power sleep state. The current limit fault condition (if present) is also cleared. Note that when transitioning from either brake or sleep mode to forward or reverse, the voltage control PWM starts at zero duty cycle. The duty cycle slowly ramps up to the commanded voltage. This can take up to 12 ms to go from sleep to 100% duty cycle. Because of this, high-speed PWM signals cannot be applied to the IN1 and IN2 pins. To control motor speed, use the VSET pin as described below.

Because of the sleep mode functionality described previously, when applying an external PWM to the DRV8832-Q1, hold one input logic high while applying a PWM signal to the other. If the logic input is held low instead, then the device will cycle in and out of sleep mode, causing the FAULTn pin to pulse low on every sleep mode exit.

Voltage Regulation

The DRV8832-Q1 provides the ability to regulate the voltage applied to the motor winding. This feature allows constant motor speed to be maintained even when operating from a varying supply voltage such as a discharging battery.

The DRV8832-Q1 uses a pulse-width modulation (PWM) technique instead of a linear circuit to minimize current consumption and maximize battery life.

The circuit monitors the voltage difference between the output pins and integrates it, to get an average DC voltage value. This voltage is divided by 4 and compared to the VSET pin voltage. If the averaged output voltage (divided by 4) is lower than VSET, the duty cycle of the PWM output is increased; if the averaged output voltage (divided by 4) is higher than VSET, the duty cycle is decreased.

During PWM regulation, the H-bridge is enabled to drive current through the motor winding during the PWM on time. This is shown in the diagram below as case 1. The current flow direction shown indicates the state when IN1 is high and IN2 is low.

Note that if the programmed output voltage is greater than the supply voltage, the device will operate at 100% duty cycle and the voltage regulation feature will be disabled. In this mode the device behaves as a conventional H-bridge driver.

During the PWM off time, winding current is re-circulated by enabling both of the high-side FETs in the bridge. This is shown as case 2 below.

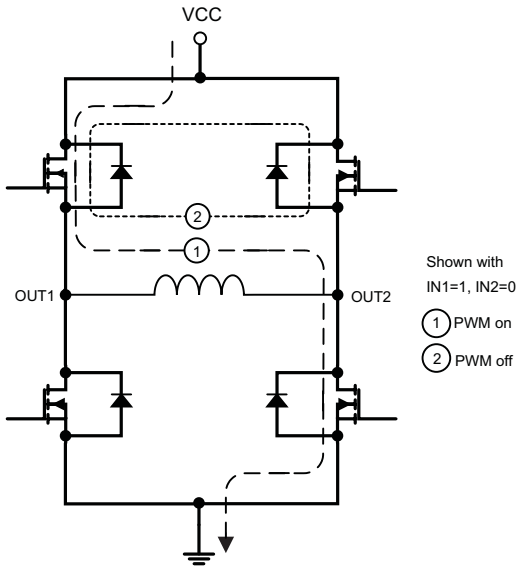


Figure 4. Voltage Regulation

Reference Output

The DRV8832-Q1 includes a reference voltage output that can be used to set the motor voltage. Typically for a constant-speed application, VSET is driven from VREF through a resistor divider to provide a voltage equal to 1/4 the desired motor drive voltage.

For example, if VREF is connected directly to VSET, the voltage will be regulated at 5.14 V. If the desired motor voltage is 3 V, VREF should be 0.75 V. This can be obtained with a voltage divider using 53 kΩ from VREF to VSET, and 75 kΩ from VSET to GND.

Current Limit

A current limit circuit is provided to protect the system in the event of an overcurrent condition, such as what would be encountered if driving a DC motor at start-up or with an abnormal mechanical load (stall condition).

The motor current is sensed by monitoring the voltage across an external sense resistor. When the voltage exceeds a reference voltage of 200 mV for more than approximately 3 µs, the PWM duty cycle is reduced to limit the current through the motor to this value. This current limit allows for starting the motor while controlling the current.

If the current limit condition persists for some time, it is likely that a fault condition has been encountered, such as the motor being run into a stop or a stalled condition. An overcurrent event must persist for approximately 275 ms before the fault is registered. After approximately 275 ms, a fault signaled to the host by driving the FAULTn signal low. Operation of the motor driver will continue.

The current limit fault condition is self-clearing and will be released when the abnormal load (stall condition) is removed.

The resistor used to set the current limit must be less than 1 Ω. Its value may be calculated as follows:

$$R_{ISENSE} = \frac{200\ mV}{I_{LIMIT}} \quad (1)$$

Where:

R_{ISENSE} is the current sense resistor value.

I_{LIMIT} is the desired current limit (in mA).

If the current limit feature is not needed, the ISENSE pin may be directly connected to ground.

Protection Circuits

The DRV8832-Q1 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled, and the FAULTn signal will be driven low. The device will remain disabled until VCC is removed and re-applied.

Overcurrent conditions are sensed independently on both high and low side devices. A short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that OCP is independent of the current limit function, which is typically set to engage at a lower current level; the OCP function is intended to prevent damage to the device under abnormal (e.g., short-circuit) conditions.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the FAULTn signal will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, the FAULTn signal will be driven low, and internal logic will be reset. Operation will resume when VCC rises above the UVLO threshold.

THERMAL INFORMATION

Thermal Protection

The DRV8832-Q1 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 160°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8832-Q1 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 2.

$$P_{TOT} = 2 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (2)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

修订历史记录

Changes from Revision A (August 2013) to Revision B **Page**

- Added Power Supervisor section 6
- Changed Bridge Control section 7
- Changed Current Limit section 9
- Changed Thermal Shutdown (TSD) section 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8832QDGQQ1	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	8832Q	Samples
DRV8832QDGQRQ1	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	8832Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

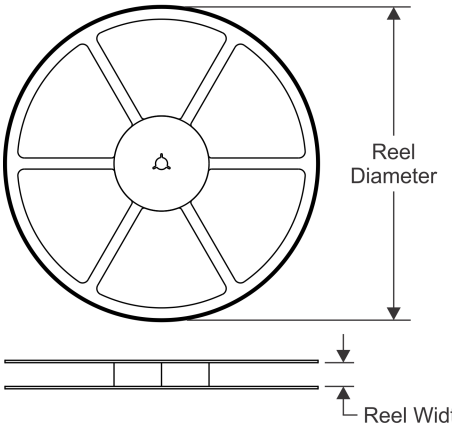
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

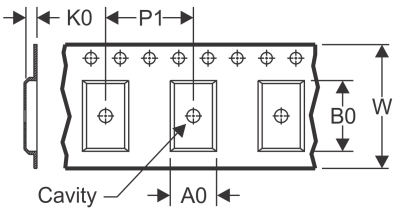
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

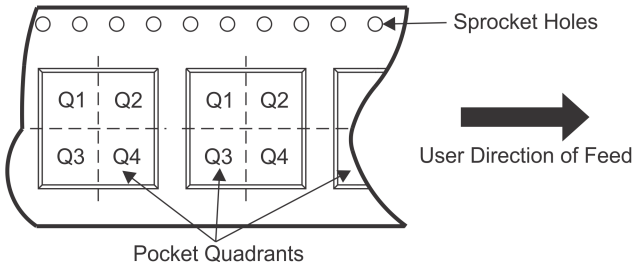


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

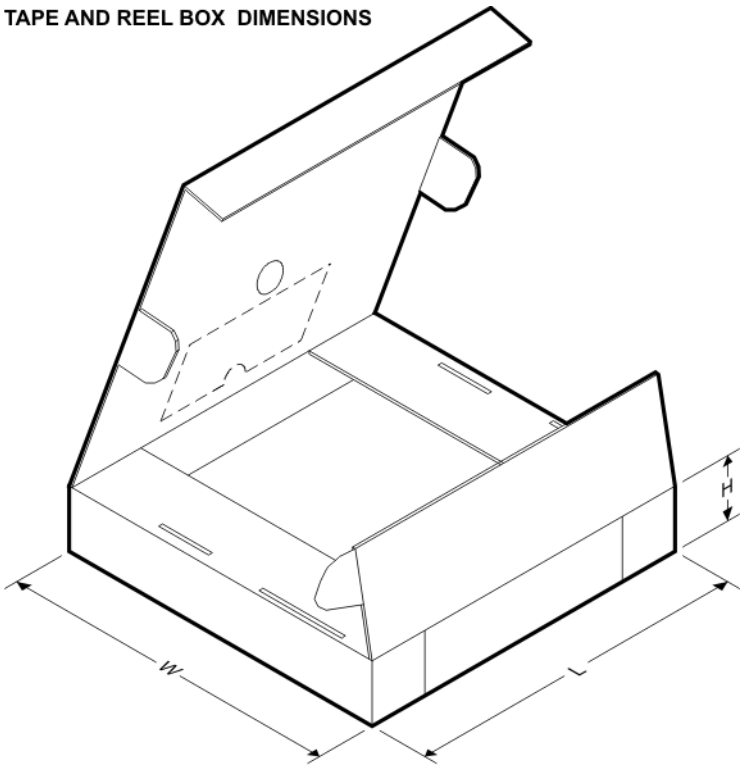
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8832QDGQRQ1	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8832QDGQRQ1	HVSSOP	DGQ	10	2500	853.0	449.0	35.0

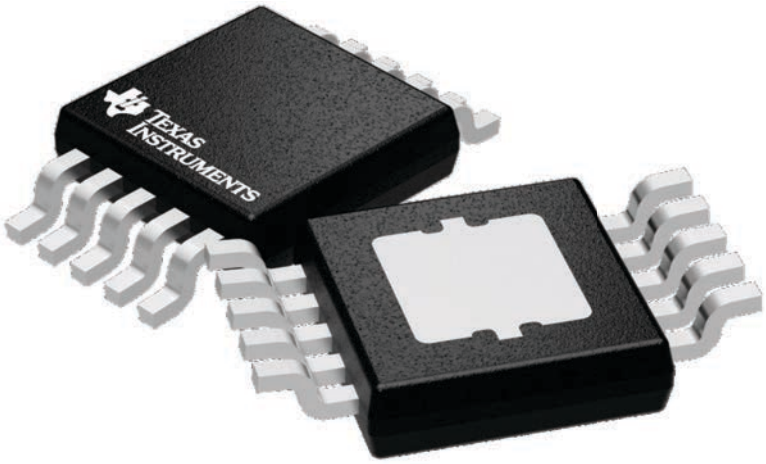
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

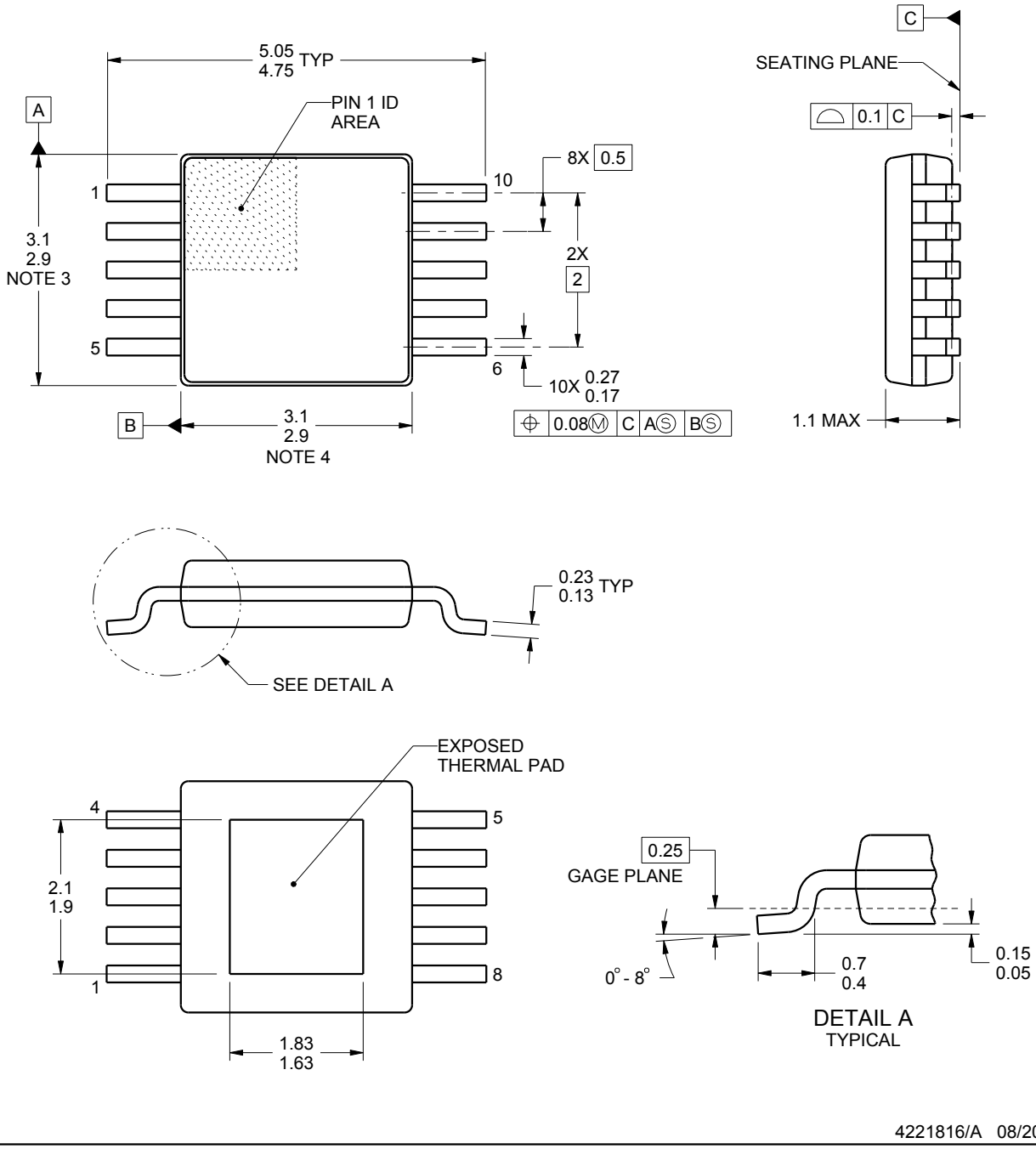
4224775/A

PACKAGE OUTLINE

DGQ0010E

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



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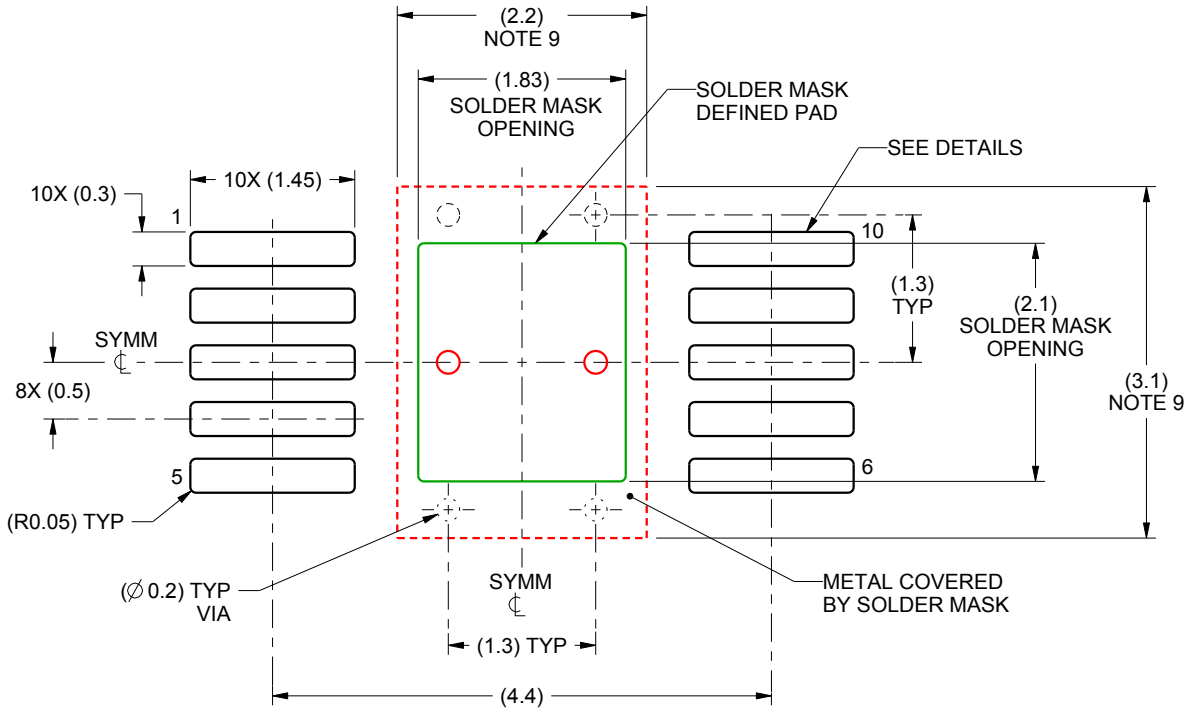
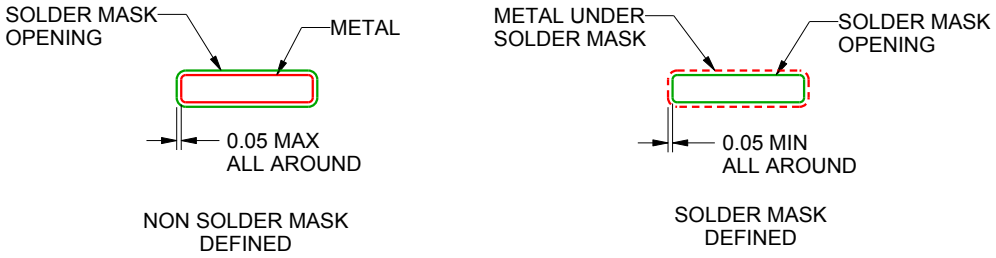
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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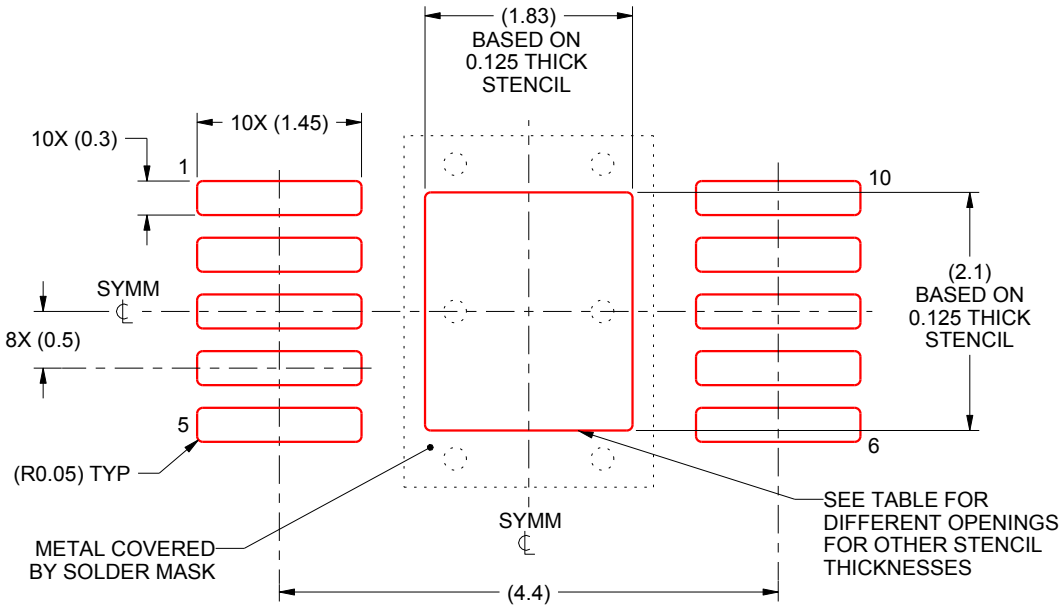
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.35
0.125	1.83 X 2.1 (SHOWN)
0.150	1.67 X 1.92
0.175	1.55 X 1.77

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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