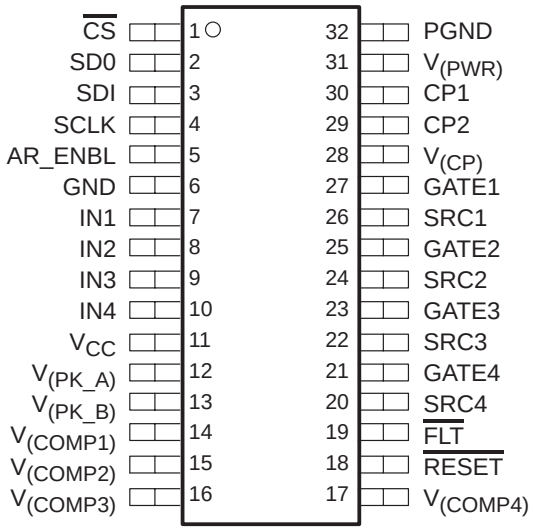
- **Serial or Parallel Control of Gate Outputs**
- **Sleep State for Low Quiescent Current**
- **Independent On-State Source Short-to-Ground (Shorted-Load) Detection/Protection**
- **Independent On-State Over-Current Detection/Protection With Dynamic Fault Threshold**
- **Independent Off-State Open-Load Detection**
- **Supply Over-Voltage Lockout Protection**
- **Asynchronous Open-Drain Fault Interrupt Terminal to Flag Fault Conditions. Output Can be OR'ed With Multiple Devices**
- **Encoded Fault Status Reporting Through Serial Output Terminal (2-Bits Per Channel)**
- **Programmable On-State Fault Deglitch Timers**
- **High Impedance CMOS Compatible Inputs With Hysteresis**
- **Fault Mode Selection: Outputs Latched Off or Switched at Low Duty Cycle**
- **Device Can be Cascaded With Serial Interface**

DA PACKAGE
(TOP VIEW)



description

The TPIC44H01 is a four channel high-side pre-FET driver which provides serial or parallel input interface to control four external NMOS power FETs. It is designed for use in low frequency switching applications for resistive or inductive loads, including solenoids and incandescent bulbs.

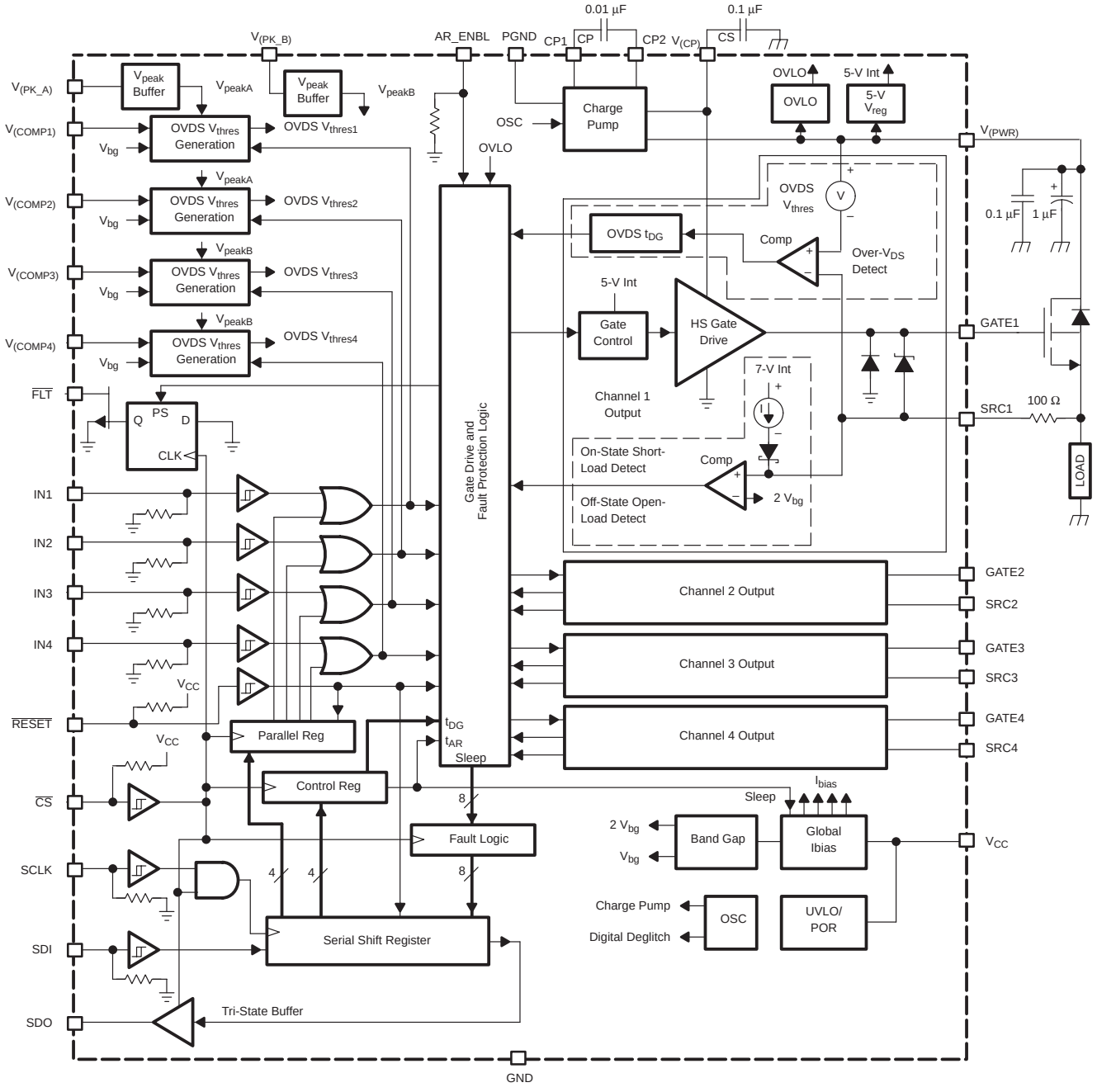
Each channel has over-current, short-to-ground, and open-load detection that is flagged through the $\overline{FLT}$ pin and distinguished through the serial interface. Over-current thresholds are set through the $V_{(PK\_X)}$ and $V_{(COMP1-4)}$ pins. Short-to-ground and open-load thresholds are set internally to approximately 2.5 V. The AR_ENBL pin is used to define the operation of the device during a fault condition, allowing the outputs to either latch off or to enter a low duty cycle, auto-retry mode. An over-voltage lockout circuit on $V_{(PWR)}$ protects the device and the external FETs. A low current sleep state mode is provided to allow the TPIC44H01 to be used in applications where $V_{(PWR)}$ is connected directly to the battery. An internal charge pump allows the use of N-channel FETs for high-side drive applications, while current-limit gate drive provides slope control for reduced RFI.

By having the unique ability to develop a dynamic over-current threshold, the TPIC44H01 can be used to drive incandescent bulbs with long inrush currents without falsely flagging a fault. Likewise, the user can select an internally set over-current threshold of ~1.25 V by pulling the respective $V_{(COMP1-4)}$ pin to V_{CC}.

description (continued)

The 8-bit serial peripheral interface (SPI) allows the user to command any of the four outputs on or off, to program one of eight possible open-load, over-current, and short-load fault deglitch timer settings, and to engage the sleep state. Data is clocked into the SDI pin on the rising edge of SCLK and clocked out of the SDO pin on the SCLK falling edge. The serial input bits are logic OR'ed with the IN1-IN4 parallel inputs pins. The serial interface is also used to read normal-load, open-load, over-current, and short-to-ground conditions for each channel. Over-voltage lockout can be detected when the $\overline{\text{FLT}}$ pin is low and no bits are set in the SDO register. Multiple TPIC44H01 devices may be cascaded together using the serial interface to further reduce I/O lines from the host controller.

schematic/block diagram



Terminal Functions

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	$\overline{CS}$	I	Chip Select. $\overline{CS}$ is an active low, logic level input with internal pullup. A logic level low on $\overline{CS}$ enables the serial interface and refreshes the fault interrupt ($\overline{FLT}$). A high on $\overline{CS}$ enables the serial register to serve as the fault data register.
2	SDO	O	Serial Data Output. SDO is a logic level, tri-state output that transfers fault data to the host controller. Serial input data passes to the next stage for cascade operation. SDO is forced into a high impendance state when $\overline{CS}$ terminal is in a high state. When $\overline{CS}$ is in a low state, data is clocked out on each falling edge of SCLK.
3	SDI	I	Serial Data Input. SDI is a logic level input with hysteresis and internal pulldown. Gate drive output control data is clocked into the serial register using SDI. A high SDI bit programs a particular gate output on, and a low turns it off, as long as the parallel input is off (OR function).
4	SCLK	I	Serial Clock. SCLK is a logic level input with hysteresis and internal pulldown. SCLK clocks data at the SDI terminal into the input serial shift register on each rising edge, and shifts out fault data (and serial input data for cascaded operation) to the SDO pin on each falling edge.
5	AR_ENBL	I	Auto-Retry Enable. AR_ENBL is a logic level input with hysteresis and internal pulldown. When AR_ENBL=0, an over-current/short-to-ground fault latches the channel off. When AR_ENBL = 1, an over-current/short-to-ground fault engages a low duty cycle operation.
6	GND	I	Analog ground and substrate connection
7–10	IN1-4	I	Parallel Inputs. IN1-4 are logic level inputs with hysteresis and internal pulldown. IN1–4 provide real-time control of gate pre-drive circuitry. A high on IN1-4 will turn on corresponding gate drive outputs (GATE1-4). Gate output status is a logic OR function of the parallel inputs and the serial input bits.
11	V_{CC}	I	5-V logic supply voltage
12	$V_{(PK\_A)}$	I	Dynamic over-current fault threshold peak voltage that is shared by channels 1 and 2
13	$V_{(PK\_B)}$	I	Dynamic over-current fault threshold peak voltage that is shared by channels 3 and 4
14–17	$V_{(COMP1-4)}$	I	Fault Reference Voltage. $V_{(COMP1–4)}$ are used to provide an external fault reference voltage for the over-current fault detection circuitry. It is also used to generate a dynamic threshold when used in conjunction with $V_{(PK\_x)}$. To guarantee $V_{(COMP)}$ stability, a minimum of 100 pF capacitance should be placed from $V_{(COMP)}$ to ground.
18	$\overline{RESET}$	I	Reset. $\overline{RESET}$ is an active low, logic level input with hysteresis and internal pullup. A low on $\overline{RESET}$ clears all registers and fault bits. All gate outputs are turned off and a latched $\overline{FLT}$ interrupt is cleared.
19	$\overline{FLT}$	O	Fault Interrupt. $\overline{FLT}$ is an active low, logic level, open-drain output providing real-time latched fault interrupts for fault detection. A latched $\overline{FLT}$ is cleared only by a low on $\overline{CS}$. The $\overline{FLT}$ terminal can be OR'ed with other devices for fault interrupt handling. An external pullup is required.
20, 22, 24, 26	SRC1-4	I	FET Source Inputs. These inputs are used for both open-load and over-current fault detection at the source of the external FETs.
21, 23, 25, 27	GATE1-4	O	Gate Drive Outputs. Output voltage is derived from $V_{(CP)}$ supply voltage. Internal clamps prevent the voltage on these nodes, with respect to SRC1-4, from exceeding the V_{GS} rating of most FETs.
28	$V_{(CP)}$	O	Charge pump voltage storage capacitor and supply pin to high-side gate drives
29	CP2	O	Charge pump capacitor terminal
30	CP1	O	Charge pump capacitor terminal
31	$V_{(PWR)}$	I	Power supply voltage input
32	PGND	I	Power ground for charge pump

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Logic supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 7 V
Power supply voltage range, $V_{(PWR)}$ (see Note 1) . . . . . –0.3 V to 40 V
Input voltage range, V_I (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, V_O (SDO and $\overline{FLT}$, see Note 1) . . . . . –0.3 V to 7 V
Source input voltage, $V_{I(SRCx)}$ (see Note 1) . . . . . –3 V to 40 V
Output voltage, $V_{O(GATEx)}$ (see Note 1) . . . . . –0.3 V to 45 V
Logic input current, I_I . . . . . ±25 µA
Operating case temperature range, T_C . . . . . –40°C to 125°C
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5	5.5	V
Power supply voltage, $V_{(PWR)}$	8		24	V
High level logic input voltage, V_{IH} (all logic inputs except $\overline{RESET}$)	$0.7\times V_{CC}$		V_{CC}	V
Low level logic input voltage, V_{IL} (all logic inputs except $\overline{RESET}$)	0		$0.3\times V_{CC}$	V
Setup time, SDI high before SCLK rising edge, t_{su} (see Figure 5)	10			ns
Hold time, SDI high after SCLK rising edge, t_h (see Figure 5)	10			ns
Operating case temperature, T_C	–40		125	°C

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Using JEDEC, low K, board configuration		86.04		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			7.32		°C/W

electrical characteristics over recommended operating case temperature and supply voltage range (unless otherwise noted)†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(PWR)}$	$V_{(PWR)}$ supply current	All outputs off, $V_{(PWR)}$ = 12 V	2	4	6	mA
I_{CCH}	5-V supply current	All outputs off, V_{CC} = 5.5 V	3	4	5	mA
$I_{(PWR\text{-}sleep)}$	Sleep state current (I_{PWR})	Sleep state (all outputs off), V_{CC} = 5.5 V, $V_{(PWR)}$ = 12 V, T_C = 25°C		15	40	µA
$I_{CCL(sleep)}$	Sleep state current (I_{CCL})	Sleep state (all outputs off), V_{CC} = 5.5 V, $V_{(PWR)}$ = 12 V, T_C = 25°C		30	40	µA
$V_{IT(POR)}$	Power-on reset threshold, V_{CC}	$V_{(PWR)}$ = 5.5 V, V_{CC} increasing	3.4	3.9	4.4	V
$V_{hys(POR)}$	Power-on reset threshold hysteresis, V_{CC}	$V_{(PWR)}$ = 5.5 V, V_{CC} decreasing	100	300	500	mV
$V_{(CP)}$	Charge pump voltage	$V_{(PWR)}$ > 24 V, CP = 0.01 µF, CS = 0.1 µF, $I_{(CP)}$ = –2 mA, See Figure 8		40	44	V
		$V_{(PWR)}$ = 24 V, CP = 0.01 µF, CS = 0.1 µF, $I_{(CP)}$ = –2 mA, See Figure 8	38	40	42	V
		$V_{(PWR)}$ = 8 V, CP = 0.01 µF, CS = 0.1 µF, $I_{(CP)}$ = –2 mA, See Figure 8	11.5	13.5		V
		$V_{(PWR)}$ = 5.5 V, CP = 0.01 µF, CS = 0.1 µF, $I_{(CP)}$ = –2 mA, See Figure 8	6.8	7.5		V
$V_{(OVLO)}$	Over-supply voltage lockout	Gate disabled, See Figure 10	27.5	30	32.5	V
$V_{hys(OV)}$	Over-supply voltage reset hysteresis	See Figure 10	0.5	1	2	V
V_G	Gate drive voltage	8 V < $V_{(PWR)}$ < 24 V, I_O = –100 µA, All channels on, See Note 2	$V_{(PWR)}$+4		$V_{(PWR)}$+18	V
		5.5 V < $V_{(PWR)}$ < 8 V, I_O = –100 µA, All channels on, See Note 2	$V_{(PWR)}$+1.5	$V_{(PWR)}$+3.5		V
$V_{G(sleep)}$	External gate sleep state voltage	I_O = 100 µA, $\overline{RESET}$ = $\overline{CS}$ = 0 V	0	100	300	mV
$V_{GS(clamp)}$	Gate-to-source clamp voltage	SRCx = 0 V, Output on	15	17	19.5	V
$V_{SG(clamp)}$	Source-to-gate clamp voltage	Output off, I_I = 100 µA	6.5	8	9.5	V
$I_{G(SRCx)}$	Gate drive source current	V_G = 0 V, $V_{(PWR)}$ = 12 V	–2.3	–3	–3.7	mA
		V_G = 10 V, $V_{(PWR)}$ = 12 V	–1.4	–2	–2.6	
$I_{G(SNKx)}$	Gate drive sink current	V_G = 2 V, $V_{(PWR)}$ = 12 V	1	1.5	2	mA
		V_G= $V_{(PWR)}$ = 12 V	2	2.6	3.2	
$V_{(open)}$	SRCx pin off-state open-load detection threshold	All outputs off, See Figure 11	1.9	2.4	2.6	V
$V_{hys(open)}$	Off-state open-load hysteresis	All outputs off	–50	–150	–300	mV

† Device will function with degraded performance for a power supply voltage between 5.5 V and 8 V.

NOTE 2: For characterization purposes only, not implemented in production testing.

electrical characteristics over recommended operating case temperature and supply voltage range (unless otherwise noted)† (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(open)}$	Off-state open-load detection current	All outputs off	–20	–50	–70	μA
$V_{(OVDS)}$	Drain-to-source over-voltage	$V_{(COMPx)} > V_{CC}$ – 250 mV	1	1.25	1.5	V
		0.1 V < $V_{(COMPx)}$ < 2.5 V, See Figures 12 and 13	$0.95\times V_{(COMPx)}-15$ mV		$1.05\times V_{(COMPx)}+15$ mV	V
$V_{(STG)}$	On-state short-to-ground detection voltage	See Figure 17	1.9	2.35	2.6	V
$V_{hys(STG)}$	On-state short-to-ground hysteresis		–50	–150	–300	mV
$I_{(pullup)}$	Logic input pullup current ($\overline{CS}$, $\overline{RESET}$)	V_{CC} = 5 V, V_{IN} = 0 V	–5	–20	–50	μA
$I_{(pulldown)}$	Logic input pulldown current (IN1–4, SCLK, SDI, AR_ENBL)	V_{CC} = 5 V, V_{IN} = 5 V	5	20	50	μA
V_{hys}	Logic input voltage hysteresis (IN1–4, SCLK, SDI, AR_ENBL, $\overline{CS}$)	V_{CC} = 5 V	0.5	0.8	1.2	V
V_{OH}	High level serial output voltage	I_O = –1 mA	$0.8\times V_{CC}$	4.96		V
V_{OL}	Low level serial output voltage	I_O = 1 mA	0	100	400	mV
I_{OZ}	Serial data output tri-state current	$V_{(SDO)}$ = 5.5 V to 0 V, V_{CC} = 5.5 V	–35	1	35	μA
$V_{OL(\overline{FLT})}$	$\overline{FLT}$ low level output voltage	I_O = 220 μA	0	30	350	mV
$I_{lkg(\overline{FLT})}$	$\overline{FLT}$ leakage current	$R_{(pullup)}$ = 25 K, V_{CC} = 5.5 V	0	1	20	μA
$V_{IH(\overline{RESET})}$	$\overline{RESET}$ high level logic input voltage		1.9	2.2	V_{CC}	V
$V_{IL(\overline{RESET})}$	$\overline{RESET}$ low level logic input voltage		0	1.2	1.4	V
$V_{hys(\overline{RESET})}$	Logic input voltage hysteresis ($\overline{RESET}$)	V_{CC} = 5 V	0.6	1	1.4	V

† Device will function with degraded performance for a power supply voltage between 5.5 V and 8 V.

switching characteristics, V_{CC} = 5 V, $V_{(PWR)}$ = 12 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(STG)}$	Short-to-ground deglitch time	SDI bits DG1–3 = 0 (default after POR), See Figures 11, 12, and 17 and Table 4		16		µs
$t_{(OC)}$	Over-current deglitch time			120		µs
$t_{(OL)}$	Open-load deglitch time			120		µs
$t_{(retry)}$	Auto-retry time			15		ms
t_{PLH}	Propagation turn-on delay, $\overline{CS}$ or IN1–4 to GATE1–4	C_G = 400 pF, See Figures 1 and 2		5		µs
t_{PHL}	Propagation turn-off delay, $\overline{CS}$ or IN1–4 to GATE1–4			5		µs
$f_{(SCLK)}$	Serial clock frequency	$t_{(WH)}$= $t_{(WL)}$ = 0.5/$f_{(SCLK)}$, See Figure 5		1	5	MHz
$t_{su(lead)}$	Setup from the falling edge of $\overline{CS}$ to the rising edge of SCLK	See Figure 5		100		ns
$t_{su(lag)}$	Setup from the falling edge of SCLK to rising edge of $\overline{CS}$			100		ns
$t_{pd(SDOEN)}$	Propagation delay from falling edge of $\overline{CS}$ to SDO valid	R_L = 10 kΩ, C_L = 200 pF, See Figure 5		50		ns
$t_{pd(valid)}$	Propagation delay from falling edge of SCLK to SDO valid			50		ns
$t_{pd(SDODIS)}$	Propagation delay from rising edge of $\overline{CS}$ to SDO Hi-Z state			150		ns
$t_{f(\overline{FLT})}$	Fall time of $\overline{FLT}$ output	R_L = 10 kΩ, C_L = 200 pF, See Figure 3		12		ns
$t_{(active)}$	POR-to-active status delay, sleep-to-active status delay	See Figure 4		512		µs

PARAMETER MEASUREMENT INFORMATION

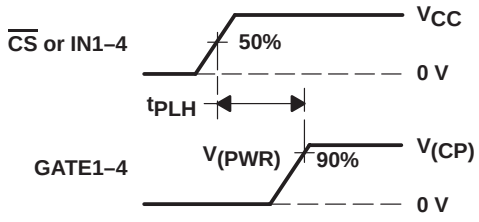


Figure 1. Gate Control Turn-On

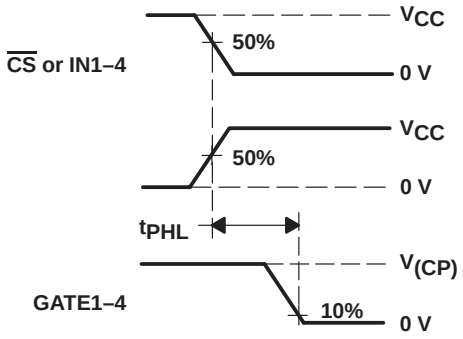


Figure 2. Gate Control Turn-Off

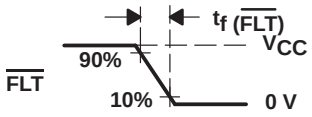


Figure 3. Fault Interrupt Fall Time

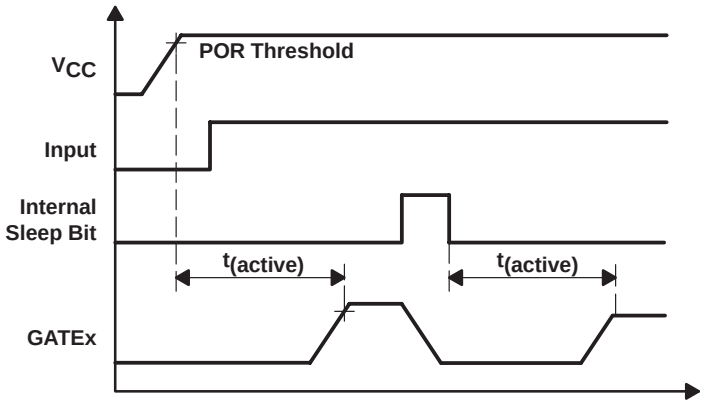
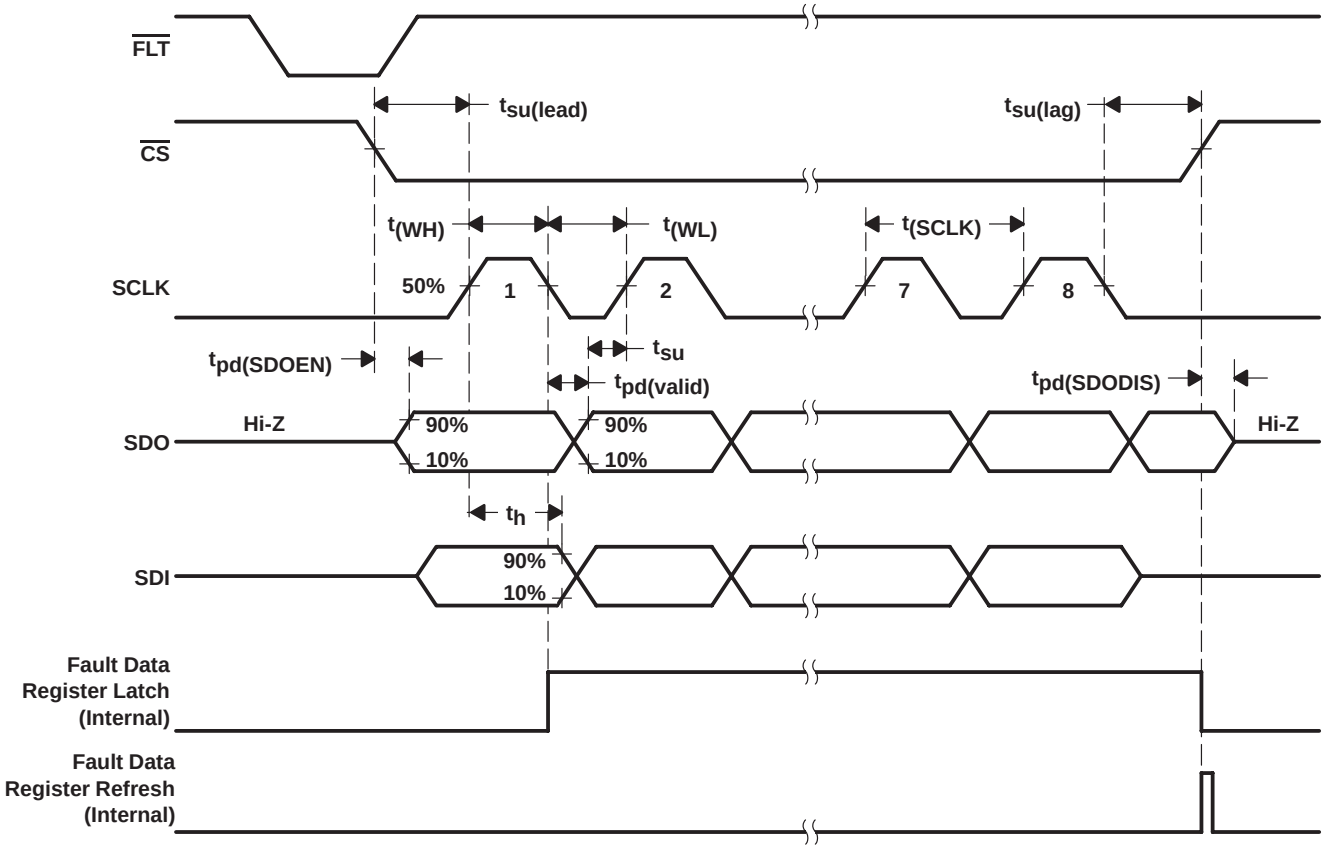
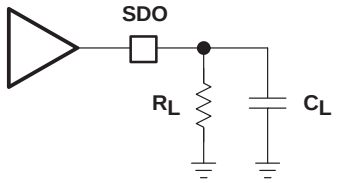


Figure 4. Power-Up Waveforms

PARAMETER MEASUREMENT INFORMATION





SDO Output Test Schematic

Figure 5. Serial Interface Timing Diagram

PRINCIPLES OF OPERATION

serial data operation

The TPIC44H01 offers a serial interface to a host microcontroller to receive control data and to return fault data to the host controller. For the serial interface operation, it is assumed that all parallel inputs, IN1–4, are low. The serial interface consists of:

SCLK	Serial clock
$\overline{CS}$	Chip select (active low)
SDI	Serial data input
SDO	Serial data output

After a $\overline{CS}$ transition from high to low, serial data at the SDI pin is shifted, MSB first, into the serial input shift register on the low-to-high transition of SCLK. Eight SCLK cycles are required (see Table 1) to shift the first data bit from LSB to MSB of the shift register. Eight SCLK cycles must occur before a transition from low to high on $\overline{CS}$ to insure proper control of the outputs. Less than eight clock cycles will result in fault data being latched into the output control buffer. Sixteen bits of data can be shifted into the device, but the first eight bits shifted out are always the fault data and the last eight bits shifted in are always the output control data. A low-to-high transition on $\overline{CS}$ will latch bits 1–4 of the serial shift register into the output control buffer, bits 5–7 into the deglitch timer control register, and bit 8 into the sleep state latch. A logic 0 in SDI bit1–4 will turn the corresponding gate drive output off (providing the parallel input for that channel is at a logic low state); likewise, a logic 1 will turn the output on. Functionality of bits 5–7 is detailed in Table 4. A logic 1 in SDI bit 8 will enable sleep state and a logic 0 will maintain normal operation.

Table 1. Serial Data Input Shift Register Bit Assignment

SDI, Normal Protocol (8–SCLKs)

	LSB (Last In)		Shift Direction →					MSB (First In)
SDI	B1	B2	B3	B4	B5	B6	B7	B8
→	IN1	IN2	IN3	IN4	DG1	DG2	DG3	SLEEP

Table 2. Serial Data Output Shift Register Bit Assignment

SDO, Fault Bit Protocol (8–SCLKs)

	MSB (First Out)		← Shift Direction					LSB (Last Out)
SDO	B8	B7	B6	B5	B4	B3	B2	B1
←	F4B	F4A	F3B	F3A	F2B	F2A	F1B	F1A

Table 3. Fault Bit Encoding

FAULT CONDITION	FxB	FxA	$\overline{FLT}$
Normal – no faults	X	X	1
Over-voltage	0	0	0
Open-load	0	1	0
Over-current	1	0	0
Short-to-ground	1	1	0

PRINCIPLES OF OPERATION

Table 4. Deglitch Time Encoding

DG1 SDI BIT5	DG2 SDI BIT6	DG3 SDI BIT7	SHORT-TO-GND DEGLITCH TIME, $t_{(STG)}$ (µs)	SHORT-TO-GND DUTY CYCLE WITH: AR_ENBL=1	OVER-CURRENT DEGLITCH TIME, $t_{(OC)}$ (µs)	OVER-CURRENT DUTY CYCLE WITH: AR_ENBL=1	AUTO-RETRY TIME, $t_{(retry)}$ (ms)	OPEN-LOAD DEGLITCH TIME, $t_{(OL)}$ (µs)
0	0	0	16†	0.1%†	120†	0.75%†	16†	120†
0	0	1	4	0.1%	30	0.75%	4	30
0	1	0	8	0.1%	60	0.75%	8	60
0	1	1	32	0.1%	240	0.75%	32	240
1	0	0	120	0.1%	120	0.75%	16	120
1	0	1	30	0.1%	30	0.75%	4	30
1	1	0	60	0.1%	60	0.75%	8	60
1	1	1	240	0.1%	240	0.75%	32	240

† Indicated default conditions after power up.

SDO MSB fault data is setup on the SDO pin by the high-to-low transition of $\overline{CS}$ prior to the first low-to-high transition of SCLK. Thus, there must be a lead time, $t_{su(lead)}$ (see Figure 5), in the host controller from $\overline{CS}$ high-to-low transition to the first rising edge of SCLK to allow the SDO tri-state output to enable and to setup the fault data MSB on the SDO pin. The remaining 7 bits of fault data are shifted out by the falling edge of the next 7 SCLK cycles. To prevent data from prematurely shifting out of SDO on a low transition of $\overline{CS}$ while SCLK is high, the device requires a low-to-high transition on SCLK after a low transition on $\overline{CS}$ before the second fault bit is shifted out. One SCLK cycle is required to clear the serial data register and latch in fault data. If a low transition on $\overline{CS}$ occurs without a low-to-high transition on SCLK, then fault data remains in the SDO register and the device will not latch data into the control register.

The serial register serves as the fault register while $\overline{CS}$ is high. Thus, a fault occurring any time after the end of the previous serial interface protocol (low-to-high transition of $\overline{CS}$) will be latched as a fault in the serial register and will be reported via SDO during the next serial protocol. The $\overline{FLT}$ interrupt will refresh on the high-to-low transition of $\overline{CS}$. The $\overline{CS}$ input must be driven to a high state after the last bit of serial data has been clocked into the device. The rising edge of $\overline{CS}$ will inhibit the SDI input port, put the SDO output port into a high impedance state, latch the 4 bits of SDI data into the output buffer, and clear/re-enable the serial fault registers (see Figure 6).

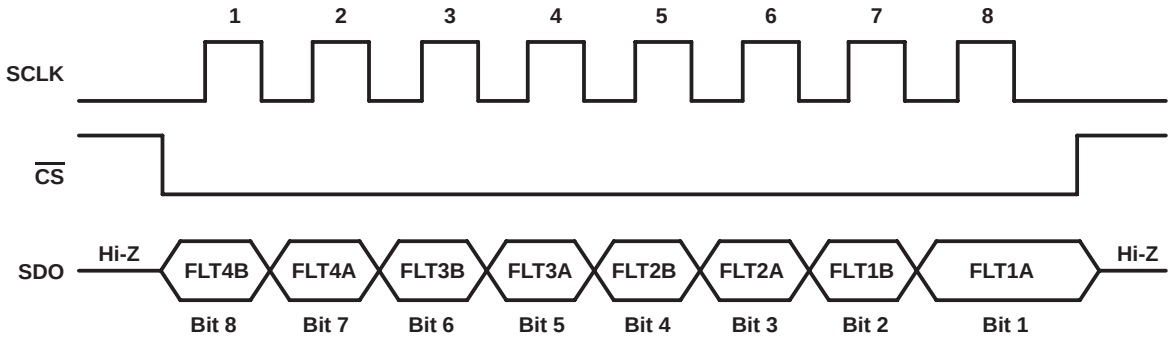


Figure 6. SDO Timing Diagram

The TPIC44H01 serial data interface allows multiple devices to be cascaded together to reduce I/O from the host controller by using a single $\overline{CS}$ line. In this configuration, 8 bits of data for every cascaded TPIC44H01 must be sent during the time that $\overline{CS}$ is low for proper operation (see Figure 7 for an example of two cascaded TPIC44H01s). If less than 8 bits of data per cascaded device is sent during the time $\overline{CS}$ is low, the wrong output may be enabled or disabled, and some fault data will be latched to the output(s) once $\overline{CS}$ returns high.

PRINCIPLES OF OPERATION

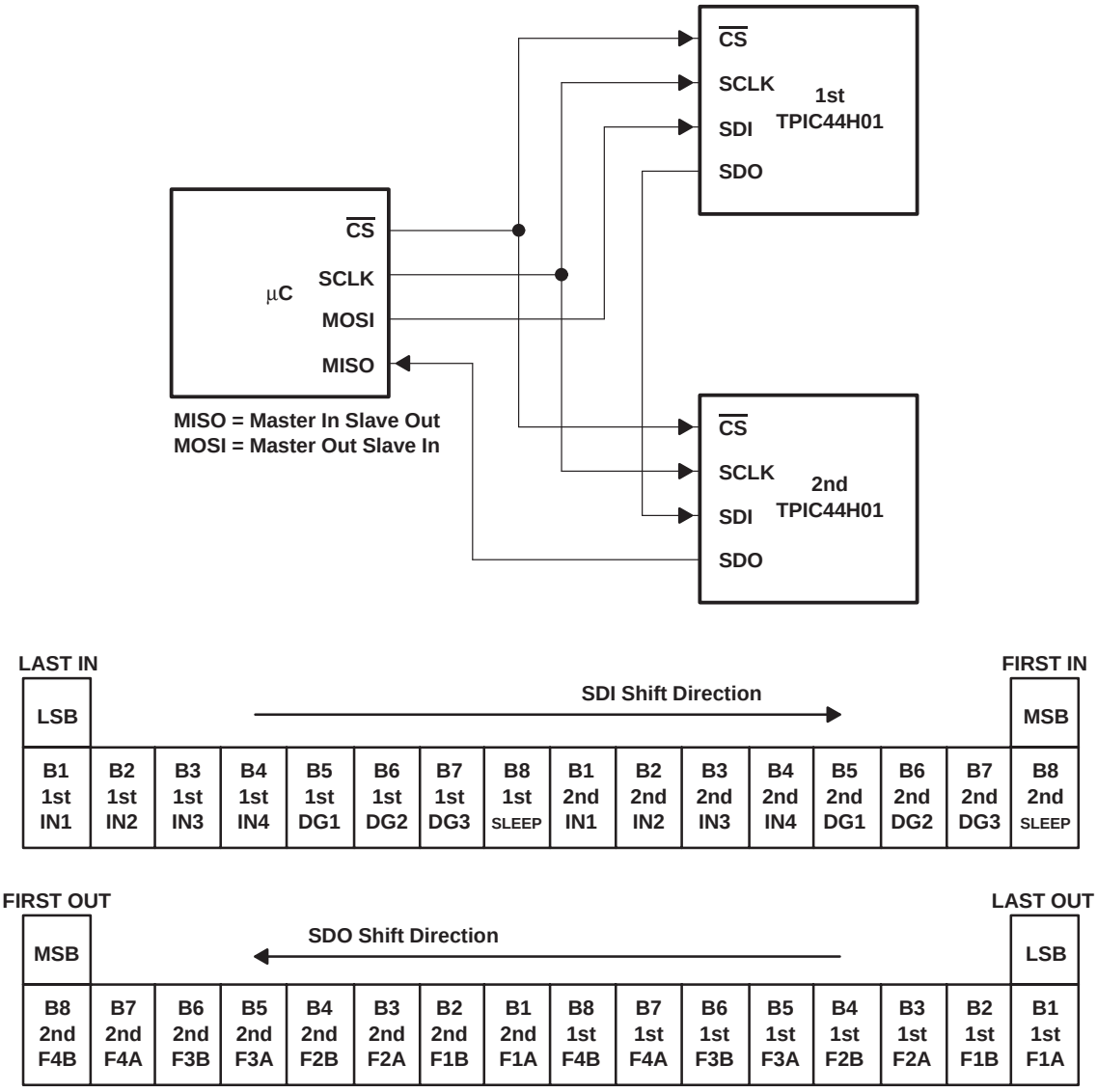


Figure 7. Cascading Multiple TIPC44H01s

PRINCIPLES OF OPERATION

parallel input data operation

In addition to the serial interface, the TPIC44H01 also provides a parallel interface to control gate drive outputs. Parallel input is OR'ed with the serial interface control bit. Thus, the parallel inputs provide direct, real-time control of the output drivers. SCLK and $\overline{CS}$ are not required to transfer parallel input data to the output buffer. Fault detection/protection is provided during parallel operation (see *performance under fault conditions* section).

With AR_ENBL pin low, detection of an over-current or short-to-ground fault condition will disabled the gate drive until the auto-retry timer clears and re-enables the output.

CAUTION:

If a parallel input is cycled low then high during auto-retry time, the timer is reset and the gate drive re-enable. The device will not prevent the user from switching at a higher duty cycle than the auto-retry function provides.

Serial fault data can be read over the serial data bus as described in the *serial data operation* section. If the $\overline{FLT}$ pin is latched low due to a fault detection, it cannot be cleared by cycling the parallel input. It can only be cleared by a low level on $\overline{CS}$.

In applications where the serial interface and $\overline{FLT}$ interrupt are unused, $\overline{CS}$ should be tied high to disable the serial interface.

In applications where the serial interface or $\overline{FLT}$ interrupt are used only to retrieve fault data, care should be taken to program the SDI input low to prevent accidental activation of a gate drive output using a serial input control bit.

charge pump operation

The TPIC44H01 provides a charge pump circuit to generate the high-side gate drive voltage. It is a doubler using external pump and storage capacitors, CP and CS respectively (refer to the schematic/block diagram). For $V_{(PWR)}$ voltage levels above 16 V, the charge pump voltage, $V_{(CP)}$, is internally regulated to approximately $V_{(PWR)}$ + 15 V. However, when $V_{(PWR)}$ voltage rises to higher than 27 V, $V_{(CP)}$ is limited to approximately 42 V from ground (see Figure 8).

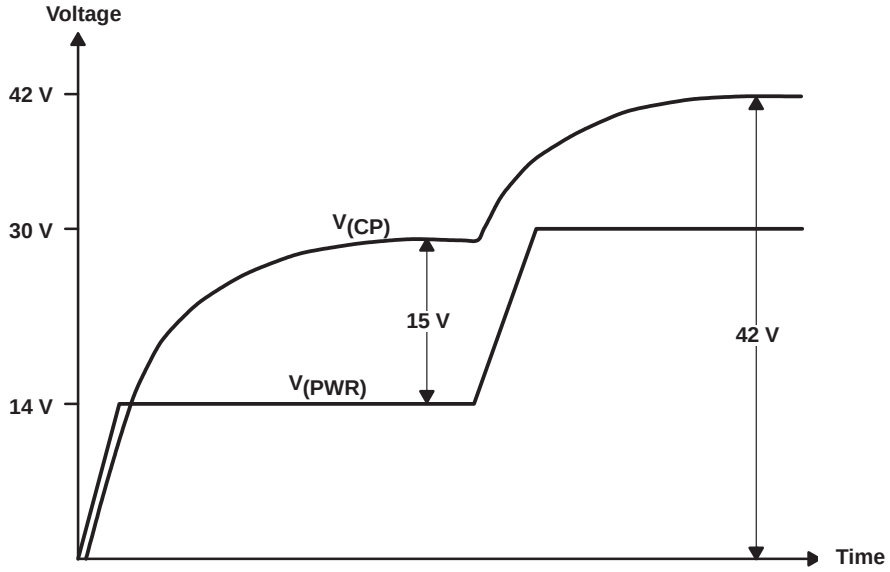


Figure 8. Charge Pump Voltage With Respect to $V_{(PWR)}$

PRINCIPLES OF OPERATION

gate drive operation

The TPIC44H01 uses a 2-mA source/sink method for external FET gate drive. This gate drive method limits the current drain from the charge pump so that when one channel is shorted to ground, the device will maintain sufficient gate drive for the remaining three channels. This benefit allows the user to add an external Miller capacitor between the FET's drain and gate pins to reduce the slew rate minimizing radiated emissions (see Figure 9).

In order to prevent the external FETs from turning on when V_{CC} is not applied to the TPIC44H01, an internal regulator powered from $V_{(PWR)}$ supplies voltage to the gate drive input control circuitry. This allows the device to be used in switched V_{CC} applications without the concern of one of the outputs turning on when V_{CC} is low.

An internal zener clamp (15 V – 17 V) from SRCx to GATEx protects the external FET from excessive V_{GS} voltages. During the flyback event when turning off an inductive load, the diode from GATEx to ground protects the TPIC44H01 and external FETs from overstress. The voltage at SRCx during flyback will be $V_{(GND)} – V_{(F)} – V_{GS}$, where $V_{(GND)}$ is ground potential, $V_{(F)}$ is the forward voltage drop of the internal diode from GATEx to ground, and V_{GS} is the voltage drop from gate to source of the external FET.

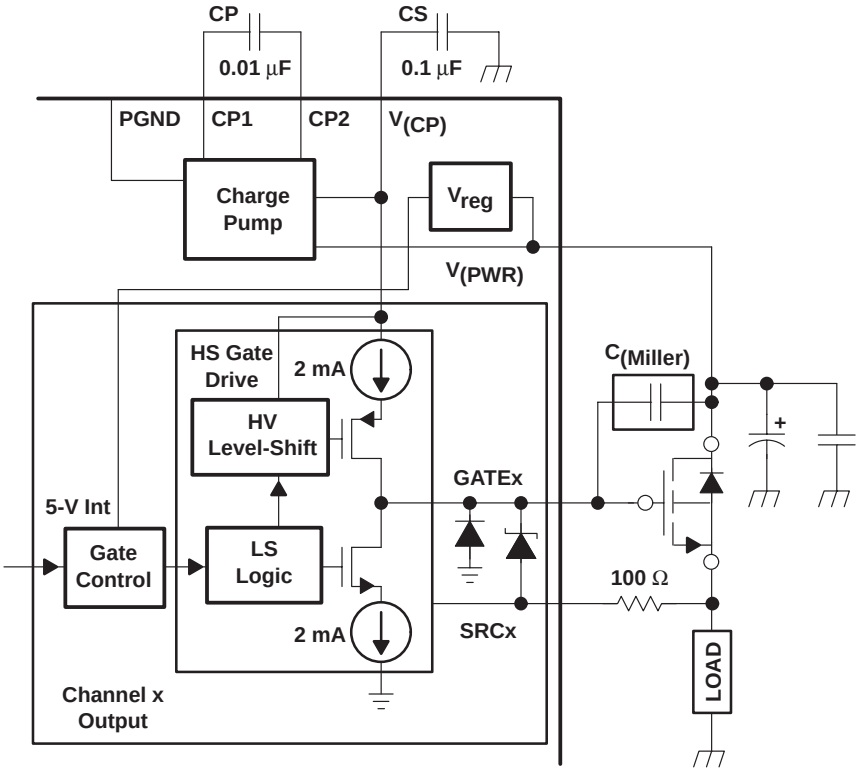


Figure 9. Gate Drive Block Diagram

PRINCIPLES OF OPERATION

performance under fault conditions

The TPIC44H01 is designed for normal operation over a supply voltage range of 8 V to 24 V with over-voltage fault detection typically at 30 V. The device offers on board fault detection to handle a variety of faults which may occur within a system. The primary function of the circuitry is to prevent damage to the load and the external power FETs in the event that a fault occurs, but off-state, open-load detection and reporting is also provided for diagnostics. Note that unused SRC1–4 inputs must be connected to their respective GATE1–4 pins to prevent false reporting of open-load fault conditions. Unused outputs with a SRC-to-GATE short should not be commanded on. For on-state faults, the circuitry detects the fault, shuts off the output to the FET, and reports the fault to the microcontroller. The primary faults monitored are:

1. $V_{(PWR)}$ over-voltage lockout (OVLO)
2. Open-load
3. Over-current
4. Short-to-ground

$\overline{\text{FLT}}$, fault interrupt operation

The $\overline{\text{FLT}}$ pin provides a real-time fault interrupt to signal a host controller that a fault has been detected. Any of the four fault conditions listed above causes the $\overline{\text{FLT}}$ pin to be latched low immediately upon fault detection.

NOTE:
Once $\overline{\text{FLT}}$ is latched low from a fault occurrence, it can only be cleared by a high-to-low transition on $\overline{\text{CS}}$.

$V_{(PWR)}$ over-voltage lockout

The TPIC44H01 monitors $V_{(PWR)}$ supply voltage and responds in the event of supply voltage exceeding OVLO. This condition may occur due to voltage transients resulting from a loose battery connection. If $V_{(PWR)}$ supply voltage is detected above 30 V, the device will turn off all gate drive outputs to prevent possible damage to the internal charge pump, the external FET, and the load. An OVLO fault will be flagged to the controller by $\overline{\text{FLT}}$ being latched low. The $\overline{\text{FLT}}$ interrupt will be reset by a high-to-low transition of $\overline{\text{CS}}$, provided that the OVLO condition is corrected, and no other faults have been detected with internal fault bits set. Thus, the user will detect an OVLO fault by a low transition on $\overline{\text{FLT}}$ with no fault bit read from SDO (see Table 3). The gate outputs will return to normal operation immediately after the OVLO condition is removed (the outputs are not latched off). Figure 10 illustrates the operation of the over-supply voltage detection circuit.

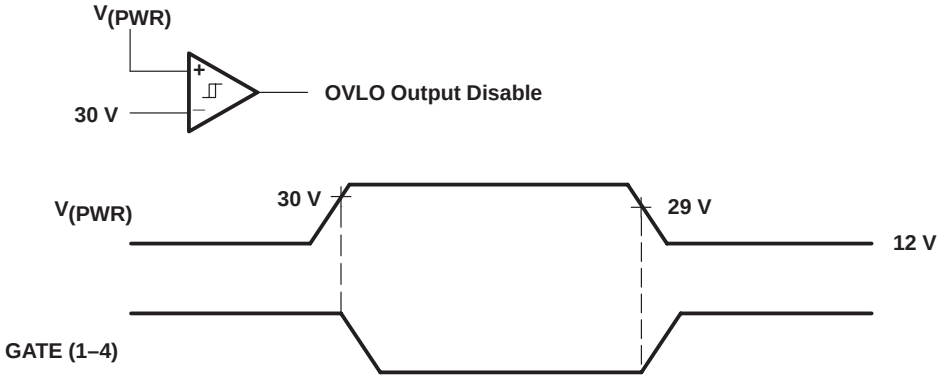


Figure 10. Over-Voltage Lockout Waveform

PRINCIPLES OF OPERATION

open load

An off-state, open-load condition is implemented in the TPIC44H01 by monitoring the SRCx terminal voltage when the FET is turned off by both the parallel input and the SDI bit being a logic 0. Figure 11 illustrates the operation of the open-load detection circuit. When the GATEx output is low, thus turning off the FET (see Figure 11), a 50-μA current is internally sourced from V_{CC} to pull up the SRCx pin for open-load fault detection.

If the load is open, or if the impedance is substantially high, the 50-μA current source will cause the SRCx pin to rise above the ~2.4 V reference threshold of the open-load comparator. Unused SRC1–4 inputs must be connected to their respective GATE1–4 pins to prevent false reporting of open-load fault conditions. An on board deglitch timer starts when the open-load comparator detects a SRCx voltage greater than ~2.4 V, providing time for the SRCx voltage to stabilize after the power FET has been turned off. The SRCx voltage must remain above the open-load detection threshold for the entire deglitch time, $t_{(OL)}$, (programmable, see Table 4) for the fault to be recognized as valid. If a valid fault is recognized, a real-time fault is flagged to the host controller by latching the $\overline{FLT}$ pin low, and the appropriate fault bit is set. The host controller can read the serial SDO bits to determine which channel reported the fault. Fault bits (1:8) distinguish faults for each of the output channels (see Table 2 and Table 3). This feature provides useful diagnostic information to the host controller to troubleshoot system failures and warn the operator that a problem exists.

If an open-load fault is detected by the TPIC44H01 while an output is off, the gate drive will be disabled the next time the output is commanded on either through the serial interface or the parallel inputs. In order to re-enable the gate drive, the load must return to a normal condition and the user must toggle the input to the previously faulted channel on then off then back on again.

NOTE:

If an open-load fault is detected by the TPIC44H01 while an output is off and AR_ENBL = 0, the gate drive will be disabled the next time the output is commanded on either through the serial interface or the parallel inputs. In order to re-enable the gate drive, the load must return to a normal condition and the user must toggle the input to the previously faulted channel on then off then back on again.

NOTE:

If an open-load fault is detected by the TPIC44H01 while an output is off and AR_ENBL = 1, the auto-retry timer will be initiated. This will cause the gate drive output to be delayed by $t_{(retry)}$ from the input signal. If more than one channel has detected an open-load fault, the delay from the input signal to the gate drive output signal will depend on which output detected the fault first. This happens because there is a single auto-retry timer used for all four channels. Normal operation will return once the fault condition is removed.

PRINCIPLES OF OPERATION

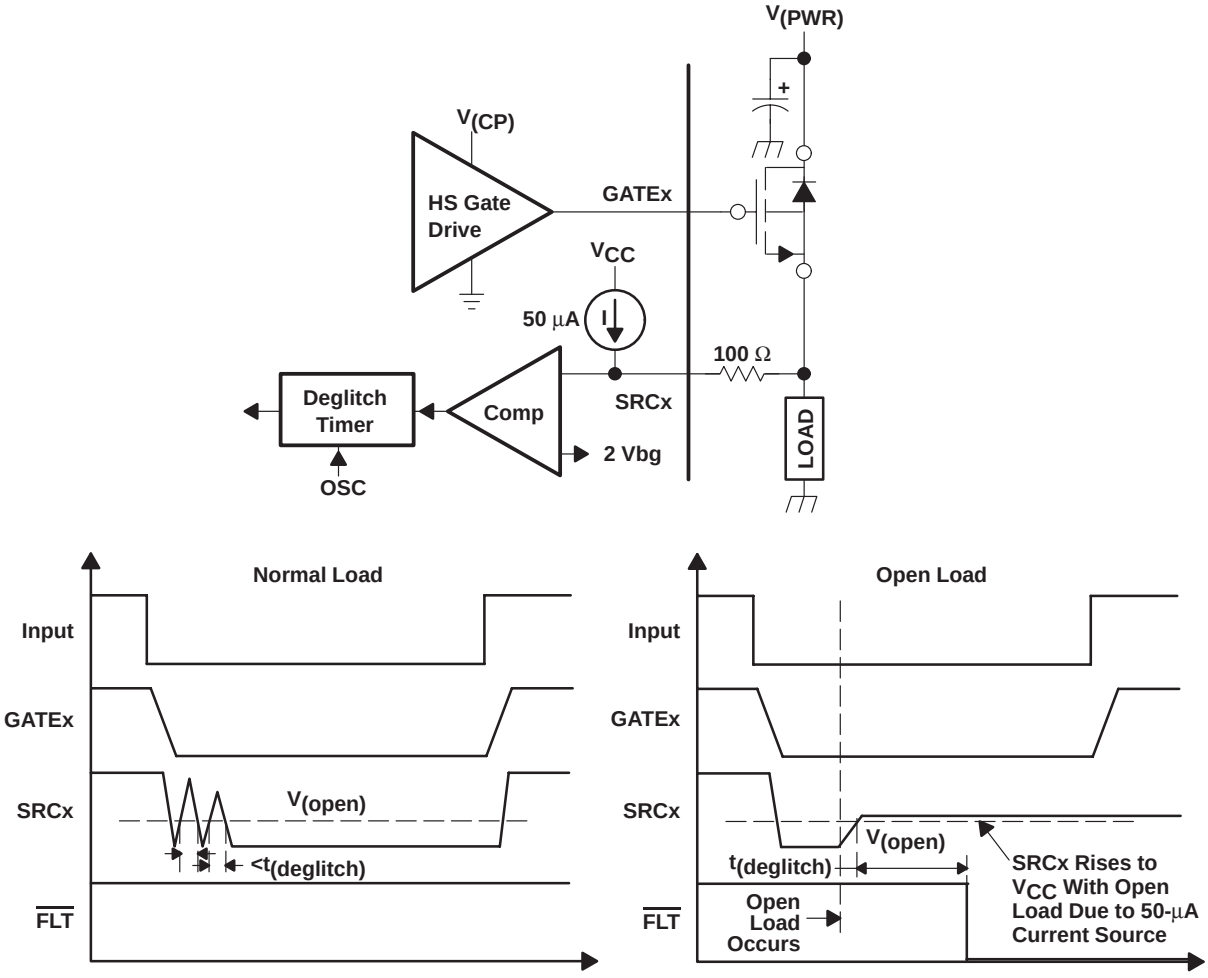


Figure 11. Open-Load Fault Detection

PRINCIPLES OF OPERATION

over-current detection/protection

On-state, over-current detection is implemented in TPIC44H01 by monitoring SRCx voltage with respect to $V_{(PWR)}$. Figure 12 shows the functionality of the over-current detection circuitry. When a channel is on (see Figure 12), the external FET V_{DS} is compared to the $V_{(OVDS)}$ fault threshold to detect an over-current condition. If the FET V_{DS} exceeds $V_{(OVDS)}$, the comparator detects an over-current event and a deglitch timer begins. The timer provides programmable deglitch time, t_{OC} (see Table 4), to allow V_{DS} voltage to stabilize after the FET is turned on. The deglitch timer starts only when $V_{DS} > V_{(OVDS)}$, and resets when $V_{DS} < V_{(OVDS)}$. If the $V_{(OVDS)}$ threshold is exceeded for the entire deglitch time, a valid over-current shutdown fault ($\overline{OCSD}$) is recognized.

If an over-current fault is detected with AR_ENBL = 0, a real-time fault condition is flagged to the host controller by latching $\overline{FLT}$ low, the appropriate internal fault bit is set, and the GATEx output is latched off. GATEx will remain off until the error condition has been corrected and the input bit or parallel input is cycled off then on. An over-heating condition of the FET can occur if the host controller continually re-enables the output under short-to-ground conditions.

If an over-current fault is detected with AR_ENBL = 1, $\overline{FLT}$ is latched low, the appropriate internal fault bit is set, and the gate output is disabled until an auto-retry timer re-enables it. If the over-current remains, auto-retry provides a low duty cycle PWM (≈ 0.75%) function to protect the FET from over heating. The PWM period is defined as $t_{(OC)} + t_{(retry)}$, while the duty cycle is defined as $t_{(OC)} / (t_{(OC)} + t_{(retry)})$. The auto-retry cycle is maintained until the fault has been eliminated and/or until the channel is turned off by both the INx parallel input and the serial control bit. The host controller can read the serial port of the device to determine which channel reported the fault condition. Fault bits (1:8) distinguish faults for each of the output channels (see Table 3).

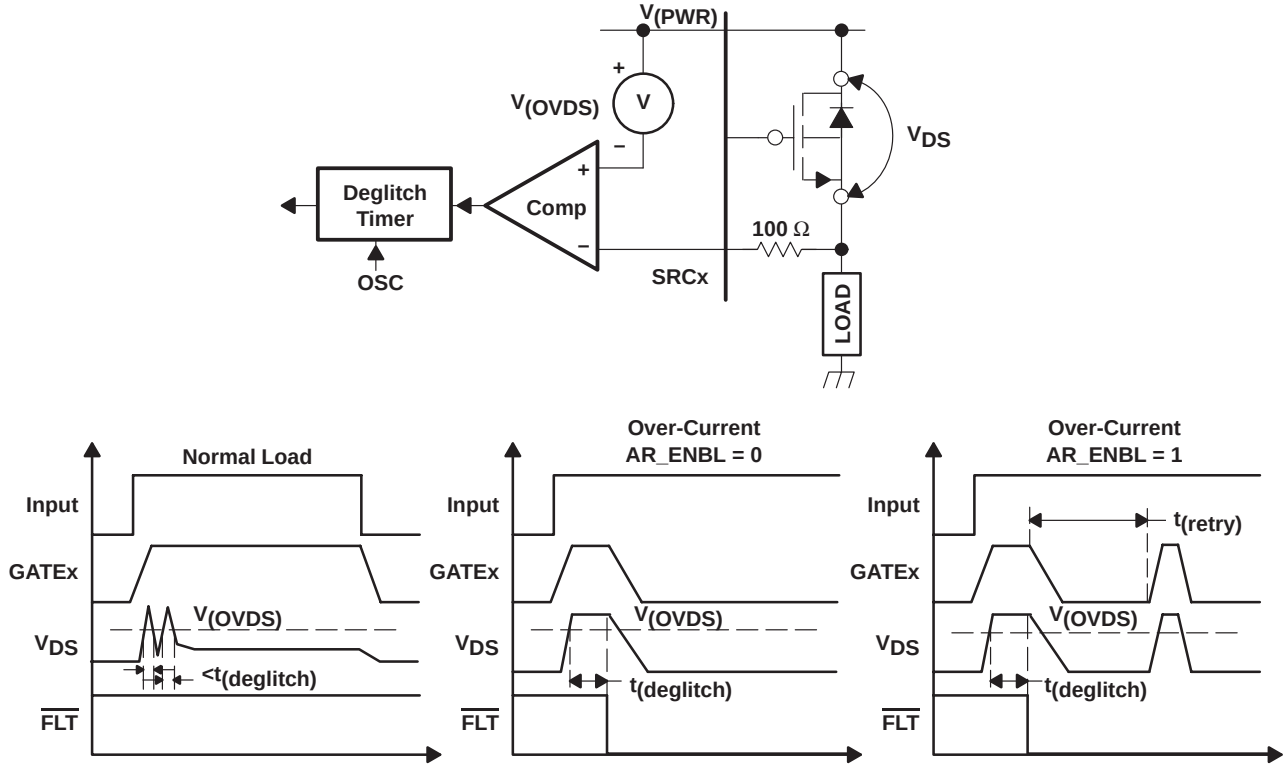


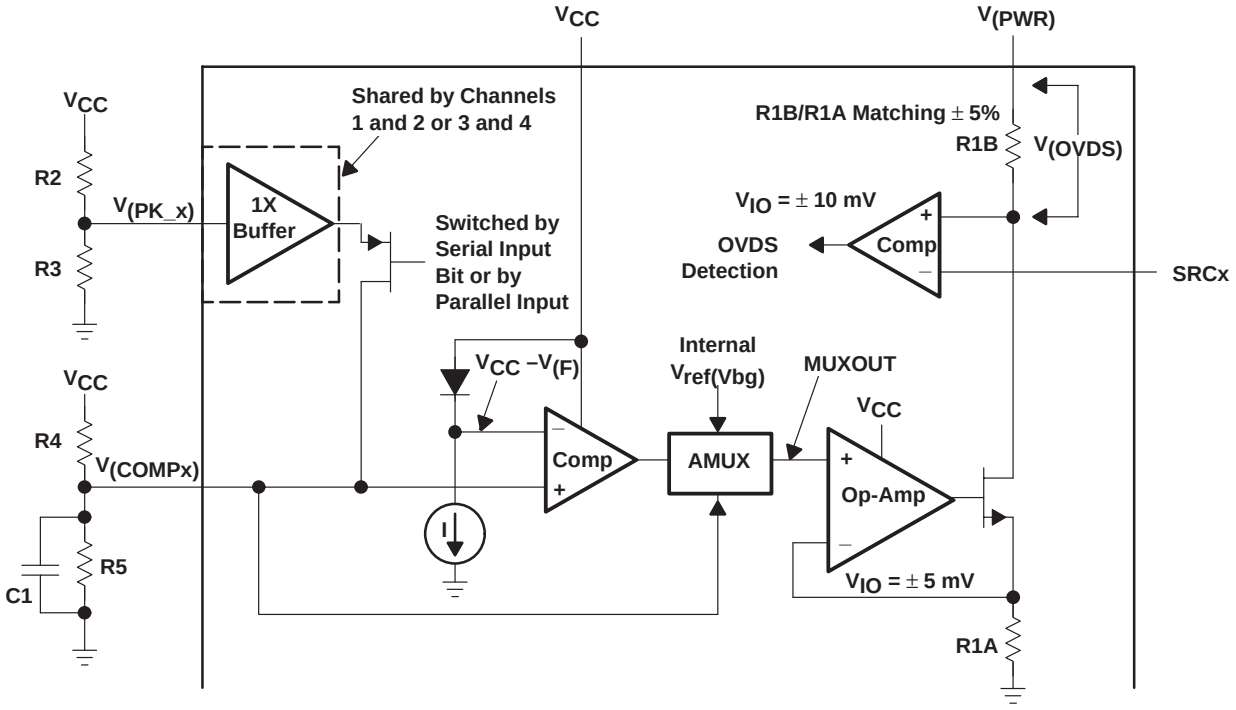
Figure 12. Over-Current Fault Detection

PRINCIPLES OF OPERATION

external over-current threshold generation

The TPIC44H01 device provides several means for setting $V_{(OVDS)}$, the threshold voltage used to detect over-current. Figure 13 shows operation of the $V_{(OVDS)}$ generation circuitry. Any voltage appearing at the MUXOUT node (see Figure 13) will be forced across R1A, setting up a current equal to $V_{(MUXOUT)}$/R1A. This current is passed through R1B, a resistor matched to R1A, thereby generating an IR drop, $V_{(OVDS)}$, down from $V_{(PWR)}$, which is identical to $V_{(MUXOUT)}$. The user can select either an internally generated ~1.25-V band-gap reference or can provide an external reference voltage using the $V_{(COMPx)}$ pin to control $V_{(OV)}$. The internal reference is selected by connecting the $V_{(COMPx)}$ pin to V_{CC}. This forces a comparator with a threshold of V_{CC} – $V_{(F)}$ to a state where it controls the analog AMUX block to connect MUXOUT to internal V_{ref}.

A user adjustable $V_{(OVDS)}$ threshold can be set by supplying a voltage to the $V_{(COMPx)}$ pin in the range of 0.1 to 2.5 V. With $V_{(COMPx)}$ voltage in this range, the comparator controlling AMUX is in the state where $V_{(COMPx)}$ voltage is connected to MUXOUT. Proper layout techniques should be used in the grounding network for the $V_{(COMP)}$ circuit on the TPIC44H01. Ground for the pre-driver and $V_{(COMPx)}$ network should be connected to a Kelvin ground, if available. Otherwise, there should be a single point contact back to PGND of the FET array. Improper grounding techniques may result in inaccurate fault detection.



NOTES: A. $V_{(COMPx)}$ should have at least 100 pF to ground to assure stability of the $V_{(COMPx)}$ amplifier.
B. Equation for dynamic fault threshold voltage at $V_{(COMP)}$:

$$V_{(COMPx)}(t) = V_{(PK\_x)}\left(e^{-(t/RC)}\right) + V_{(COMPx)}(0) \quad (1)$$

Where $V_{(COMPx)}(t)$ is the voltage at $V_{(COMPx)}$ at time t, $V_{(PK\_x)}$ is the voltage at $V_{(PK\_x)}$ set by the R2 and R3 resistor divider, C is the value of C1, R is the parallel combination of R4 and R5, and $V_{(COMPx)}(0)$ is the voltage set up by the R4 and R5 resistor divider.

Figure 13. Over-Current Fault Threshold Generation

PRINCIPLES OF OPERATION

dynamic over-current threshold generation

Figure 13 shows the internal circuitry associated with $V_{(PK\_x)}$ and the external resistor divider and capacitor connected to $V_{(COMPx)}$. The intent of this implementation is to allow a dynamic $V_{(COMPx)}$ voltage to be generated which begins at the voltage referenced to the $V_{(PK\_x)}$ pin and decays as an RC discharge to the resistor divider voltage setup by the network on the $V_{(COMPx)}$ pin. Figure 14 shows an example of the dynamic $V_{(COMPx)}$ voltage waveform. This waveform will be generated each time a channel is switched from off to on by either a serial bit or parallel input. The $V_{(OVDS)}$ threshold begins at a high value to allow the high in-rush current associated with cold lamp filament resistance and decays at an RC time constant to emulate the current decrease in the lamp as the filament warms up. The steady-state threshold after the RC decay provides protection against soft-short conditions that could cause the FET to over heat after a long period of time. Selection of $V_{(PK\_x)}$ voltage and $V_{(COMPx)}$ resistor divider and capacitor provides the user with the flexibility to accommodate a wide variety of lamp types. The TPIC44H01 thus provides a wide dynamic range of the over-current detection function, and a time-dependent variation in the threshold that are user adjustable by the selection of external components.

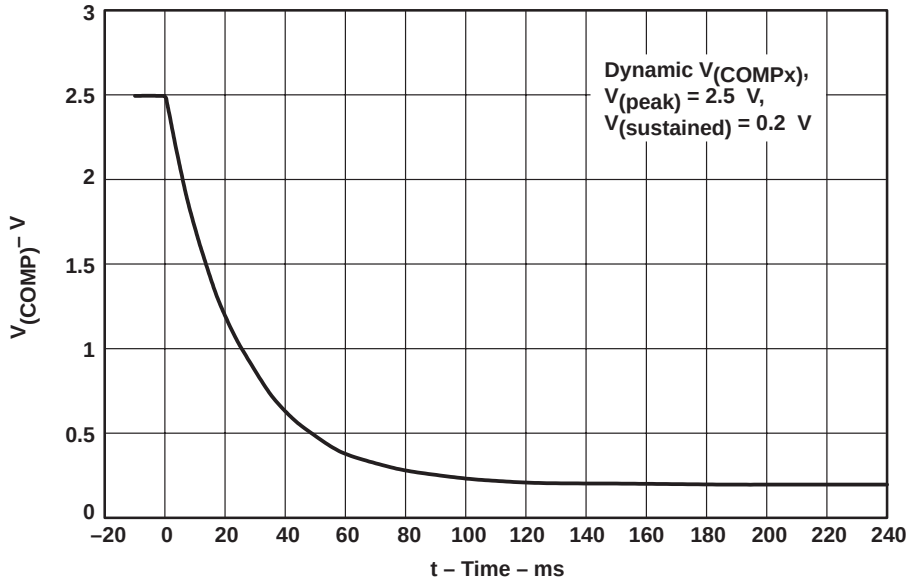


Figure 14. Dynamic Fault Threshold Voltage

PRINCIPLES OF OPERATION

To demonstrate how $V_{(COMPx)}$ voltage is reflected down from $V_{(PWR)}$ to establish the high-side $V_{(OVDS)}$ threshold, Figure 15 shows both waveforms. Figure 16 illustrates a typical $V_{(SRCx)}$ voltage waveform as compared to $V_{(OVDS)}$ during a normal turn-on transition.

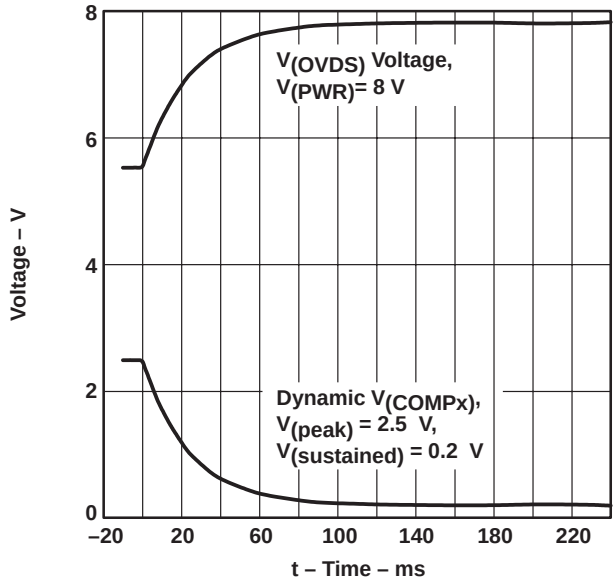


Figure 15. $V_{(COMPx)}$ Mirrored From $V_{(PWR)}$ to Generate $V_{(OVDS)}$ Threshold

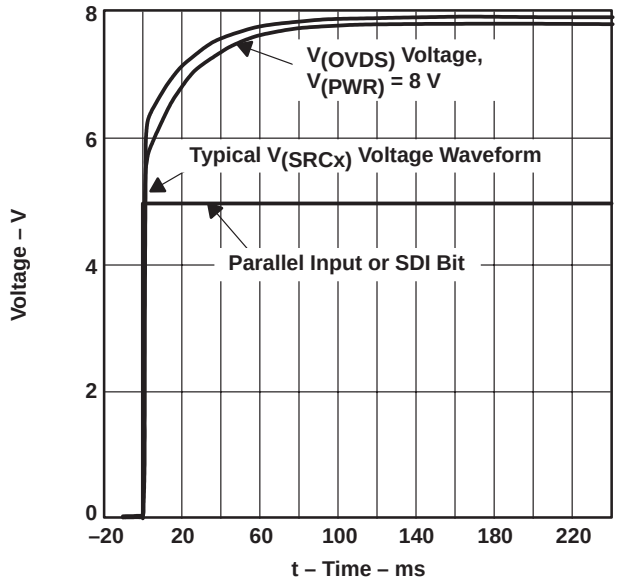


Figure 16. $V_{(OVDS)}$ Compared to $V_{(SRCx)}$

PRINCIPLES OF OPERATION

short-to-ground detection/protection

The TPIC44H01 provides short-to-ground detection to protect the external FET from a more severe condition than an over-current condition. This is accomplished by engaging a reduced deglitch time should a short-to-ground be detected, thereby turning off the FET faster than in an over-current condition. Figure 17 illustrates operation of the short-to-ground detection scheme. A short-to-ground is detected during on-state by monitoring the condition of the low-side comparator in addition to the $V_{(OVDS)}$ comparator. If the low-side comparator indicates SRCx voltage is below the $V_{(STG)}$ fault threshold voltage (2-V_{bg} referenced to ground), a short-to-ground condition is detected. Should this condition exist for the entire duration of $t_{(STG)}$, a valid fault is registered, causing the associated gate drive output to turn off, the $\overline{FLT}$ pin to latch low, and the appropriate serial data fault bits to be set. Deglitch of short-to-ground detection relies on the over-current deglitch timer, which begins if the FET V_{DS} exceeds $V_{(OVDS)}$ (that is over-current event). However, detection of short-to-ground reduces the deglitch time from $t_{(OC)}$ to $t_{(STG)}$, as shown in Table 4. The deglitch time allows $V_{(SRCx)}$ voltage to stabilize after the FET is turned on, and to distinguish between normal and shorted loads.

As shown in Figure 17, three short-to-ground cases can occur.

Case 1: SRCx is shorted to ground prior to gate drive turn on. GATEx is shut off when $t_{(STG)}$ is reached.

Case 2: SRCx is shorted to ground after gate drive is turned on and $V_{(SRCx)}$ falls beneath $V_{(STG)}$ before $t_{(STG)}$ is exceeded. Thus, $t_{(STG)}$ is initiated once $V_{(SRCx)}$ falls beneath $V_{(OVDS)}$ and GATEx is shut off when $t_{(STG)}$ is reached.

Case 3: After gate drive is turned on, SRCx is pulled beneath $V_{(OVDS)}$, then falls beneath $V_{(STG)}$ after $t_{(STG)}$ is reached. GATEx is not shut off when $t_{(STG)}$ is reached, but shuts off immediately when SRCx fall beneath $V_{(STG)}$.

PRINCIPLES OF OPERATION

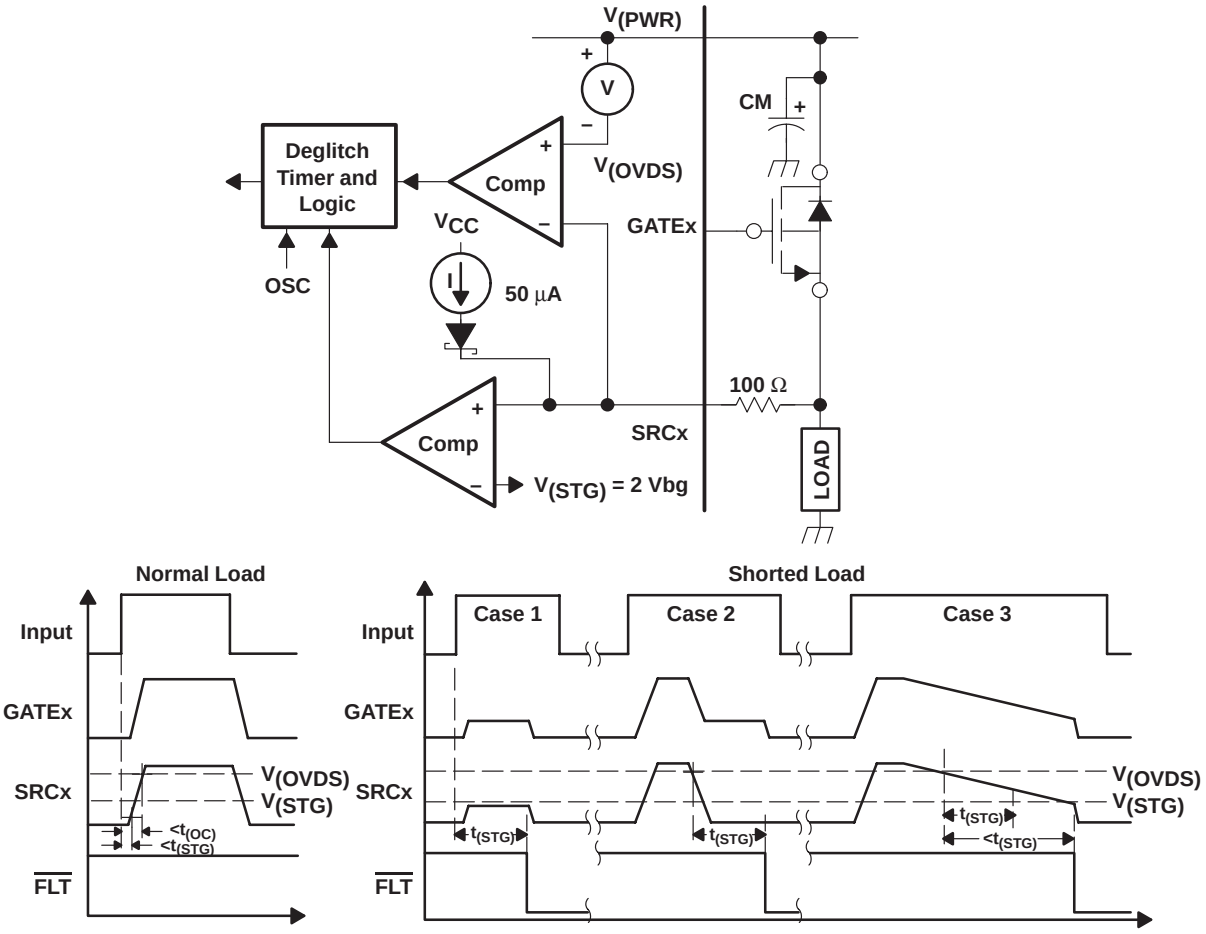


Figure 17. Short-to-Ground Fault Detection

PRINCIPLES OF OPERATION

sleep state

The TPIC44H01 provides a sleep state in which minimal current is drawn from V_{CC} and $V_{(PWR)}$. Sleep state can be engaged using the serial interface by programming the SDI MSB to a logic 1 and latching the sleep bit with a low-to-high transition of $\overline{CS}$. For parallel operation, sleep state can also be engaged immediately by simultaneously forcing a logic low on $\overline{CS}$ and $\overline{RESET}$. When sleep state is engaged, the charge pump is disabled, $I_{(bias)}$ to all analog circuits is disabled, all gate drive outputs are turned off, and all registers and deglitch timers are cleared.

Sleep state is terminated, returning the device to normal operation, by the next high-to-low transition of $\overline{CS}$, or by the next low-to-high transition of any parallel input, IN1–4 (providing all other non-transition INx inputs are held low). Since sleep state disables the charge pump shared by all high-side gate drives, a delay time, $t_{(active)}$, of approximately 512 μs is implemented after sleep state is terminated (see Figure 18) to allow sufficient time for $V_{(CP)}$ to charge and all analog circuits to power up and stabilized before any gate drive outputs can be re-engaged.

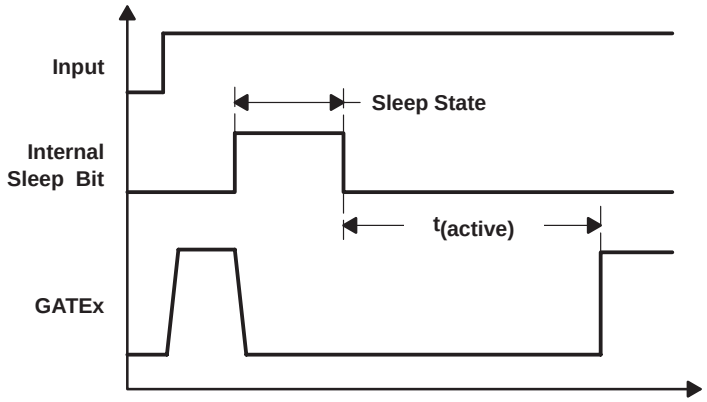


Figure 18. Sleep State Timing Diagram

gate drive control and sleep state

Refer to the schematic/block diagram and note the internal regulator block, 5-V Vreg, near $V_{(PWR)}$ pin. The internal regulator provides power to gate control input logic of gate drives any time an external voltage is applied to $V_{(PWR)}$ pin. Gate control block inputs have a passive pulldown which must be overcome with a high level from the core logic to turn on gate drives. This scheme ensures external FETs are actively held off when $V_{(PWR)}$ voltage is applied while sleep state is induced, and/or if voltage is not supplied to the V_{CC} pin while $V_{(PWR)}$ voltage is present. This eliminates the risk of external FET turn-on from drain-to-gate leakage current of the FET, allows the user to switch off V_{CC} as another option to disable the device and gate drives for system sleep state, and maintains voltage applied to the $V_{(PWR)}$ pin.

PRINCIPLES OF OPERATION

inductive voltage transients

A typical application for the TPIC44H01 is to switch inductive loads. Whenever an inductive load is switched off, the inductive flyback can cause a large voltage spike to occur at the FET source, or SRCx pin. These spikes can also capacitively couple to the FET gate. The voltages at the GATEx and SRCx pins must be limited from extending significantly below device ground to prevent potential internal latchup and to avoid damage to the FET by exceeding the maximum BV_{DSS}. To address this concern, the TPIC44H01 provides an internal diode connected between device GND and GATEx to limit the gate voltage from exceeding more than a diode drop negative below ground. If no additional external component is provided to limit $V_{(source)}$ and to recirculate the inductive energy, the FET source will fly negative due to the load inductive flyback during turn-off. The FET source will thus extend as negative as $V_G - V_{GS}$. Since the GATEx pin is clamped $V_{(diode)}$ beneath GND, $V_{(source)} = V_{(GND)} - V_{(diode)} - V_{GS}$. During this condition, the FET is operating in a high power dissipation region because V_{DS} is large while I_{DS} is flowing. Design of the FET thermal system must consider this power to avoid excessive junction temperature.

For high current applications where the FET power dissipation is a concern, an external recirculation diode connected between the source of the FET (diode cathode) and ground (diode anode) can be implemented to limit the source voltage to $-V_{(F)}$ of the diode. Damage to the device can occur if proper protection is not provided.

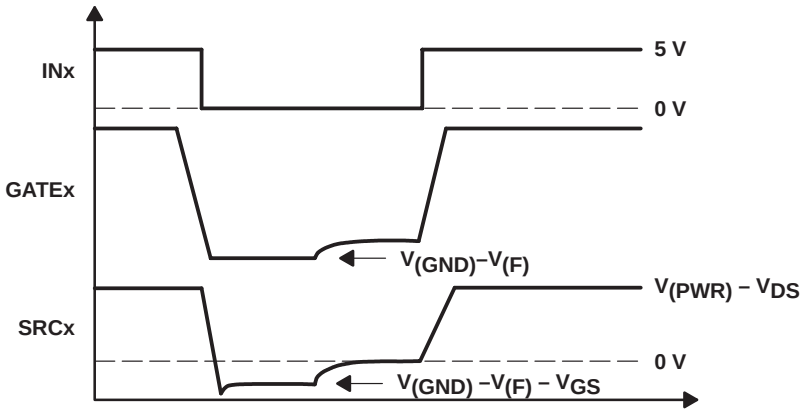


Figure 19. Inductive Load Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC44H01DA	ACTIVE	TSSOP	DA	32	46	RoHS & Green	NIPDAU	Level-1-220C-UNLIM	-40 to 125	TPIC44H01	Samples
TPIC44H01DAG4	ACTIVE	TSSOP	DA	32	46	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		TPIC44H01	Samples
TPIC44H01DAR	ACTIVE	TSSOP	DA	32	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC44H01	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

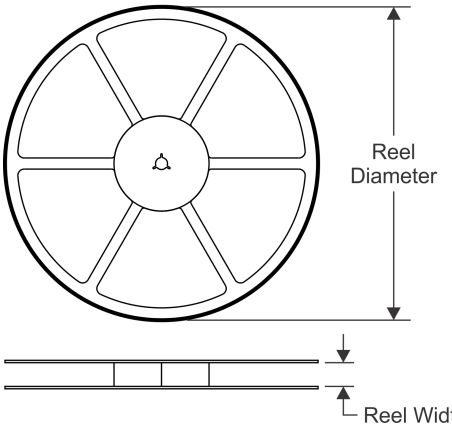
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

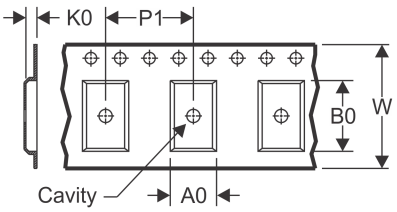
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

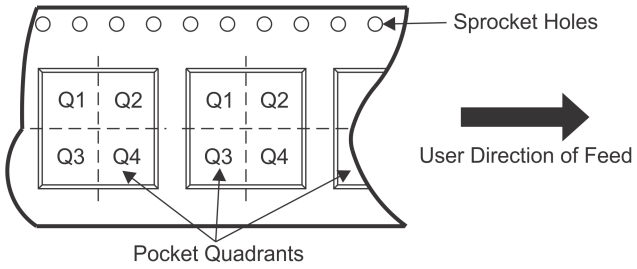


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

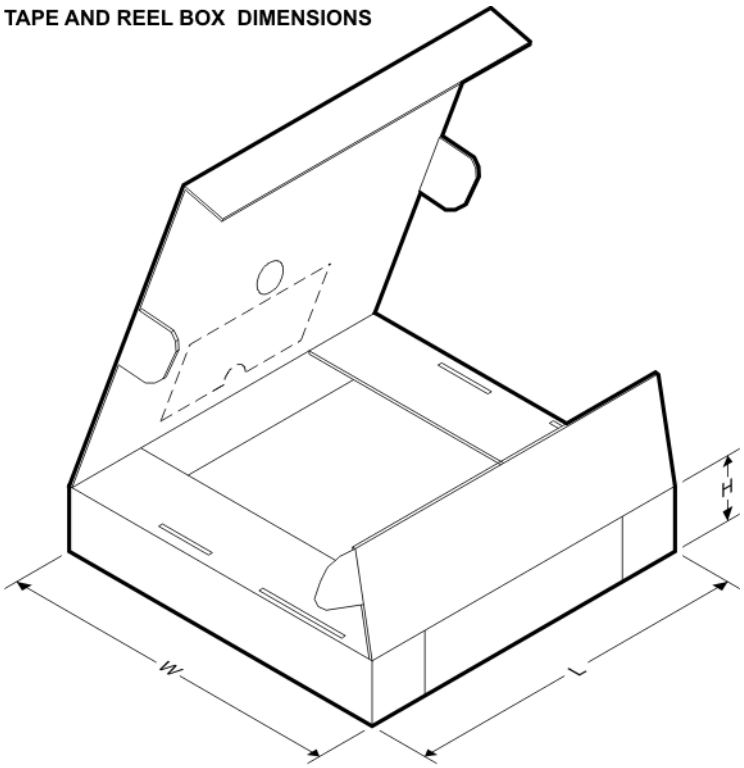
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC44H01DAR	TSSOP	DA	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

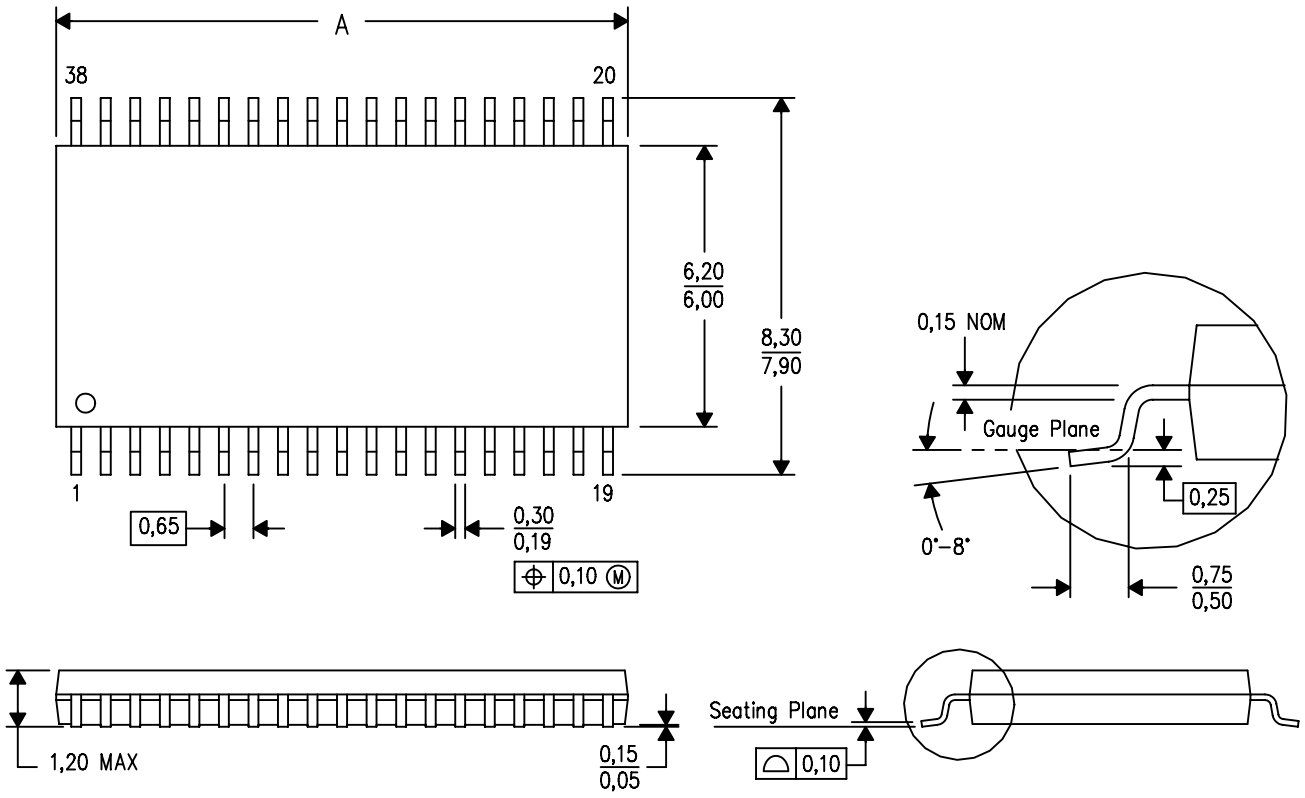


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC44H01DAR	TSSOP	DA	32	2000	350.0	350.0	43.0

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN



DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
△D MO–153 Variation	DB–1	DC	DD–1

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
△D Falls within JEDEC MO–153, except 30 pin body length.

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